

TDA2x ADAS Applications Processor

17mm Package (AAS Package)

Silicon Revision 2.0

1 Device Overview

1.1 Features

- Architecture Designed for ADAS Applications
- Video, Image, and Graphics Processing Support
 - Full-HD Video (1920 x 1080p, 60 fps)
 - Multiple Video Input and Video Output
- ARM® Cortex®-A15 Microprocessor Subsystem
- Up to 2 C66x Floating-Point VLIW DSP
 - Fully Object-Code Compatible With C67x and C64x+
 - Up to Thirty-two 16 x 16-Bit Fixed-Point Multiplies per Cycle
- Up to 2.5MB of On-Chip L3 RAM
- Level 3 (L3) and Level 4 (L4) Interconnects
- DDR2/DDR3/DDR3L Memory Interface (EMIF) Module
 - Supports up to DDR2-800 and DDR3-1066
 - Up to 2GB Supported
- Dual ARM® Cortex®-M4 Image Processing Units (IPU)
- Vision AccelerationPac
 - Up to Two Embedded Vision Engines (EVEs)
- IVA-HD Subsystem
- Display Subsystem
 - Display Controller With DMA Engine and Three Pipelines
 - HDMI™ Encoder: HDMI 1.4a and DVI 1.0 Compliant
- 2D-Graphics Accelerator (BB2D) Subsystem
 - Vivante™ GC320 Core
- Video Processing Engine (VPE)
- Dual-Core PowerVR® SGX544™ 3D GPU
- Two Video Input Port (VIP) Modules
 - Support for up to 7 Multiplexed Input Ports
- General-Purpose Memory Controller (GPMC)
- Enhanced Direct Memory Access (EDMA)
- Controller
 - 2-Port Gigabit Ethernet (GMAC)
 - Dual Controller Area Network (DCAN) Modules
 - CAN 2.0B Protocol
 - PCI-Express 3.0 Port With Integrated PHY
 - Single Port With 1 Lane at 5.0 Gbps
 - Sixteen 32-Bit General-Purpose Timers
 - 32-Bit MPU Watchdog Timer
 - Ten Configurable UART/IrDA/CIR Modules
 - Four Multichannel Serial Peripheral Interfaces (McSPI)
 - Quad SPI Interface (QSPI)
 - Five Inter-Integrated Circuit (I²C) Ports
 - Seven Multichannel Audio Serial Port (McASP) Modules
 - Three High-Speed USB 2.0 Dual-Role Devices
 - Three MultiMedia Card/Secure Digital/Secure Digital Input Output Interfaces (MMC™/SD®/SDIO)
 - Up to 247 General-Purpose I/O (GPIO) Pins
 - Real-Time Clock Subsystem (RTCSS)
 - Device security features
 - Hardware Crypto accelerators and DMA
 - Firewalls
 - JTAG® lock
 - Secure keys
 - Secure ROM and boot
 - Power, Reset, and Clock Management
 - On-Chip Debug With CTools Technology
 - Automotive AEC-Q100 Qualified
 - 28-nm CMOS Technology
 - 17 mm x 17 mm, 0.65-mm Pitch, 625-Pin BGA (AAS)



1.2 Applications

- Mono, Stereo or Tri-Optic Front Camera
 - Object Detection
 - Pedestrian Detection
 - Traffic Sign Recognition
 - Lane Detection and Departure Warning
 - Automatic Emergency Braking
 - Adaptive Cruise Control
 - Forward Collision Warning
 - High Beam Assist
- LVDS or Ethernet Surround View
 - 2D surround view
 - 3D surround view
 - Rear object detection
 - Parking assist
 - Pedestrian Detection
 - Lane tracking
 - Drive Recording
- Sensor Fusion – Vision, Radar, Ultrasonic, Lidar sensors
 - Object data fusion
 - Raw data fusion

1.3 Description

TI's new TDA2x System-on-Chip (SoC) is a highly optimized and scalable family of devices designed to meet the requirements of leading Advanced Driver Assistance Systems (ADAS). The TDA2x family enables broad ADAS applications in automobiles by integrating an optimal mix of performance, low power and ADAS vision analytics processing that aims to facilitate a more autonomous and collision-free driving experience.

The TDA2x SoC enables sophisticated embedded vision technology in automobiles by broadest range of ADAS applications including front camera, park assist, surround view and sensor fusion on a single architecture.

The TDA2x SoC incorporates a heterogeneous, scalable architecture that includes a mix of TI's fixed and floating-point TMS320C66x digital signal processor (DSP) generation cores, Vision AccelerationPac, ARM Cortex-A15 MPCore™ and dual-Cortex-M4 processors. The integration of a video accelerator for decoding multiple video streams over an Ethernet AVB network, along with graphics accelerators for rendering virtual views, enable a 3D viewing experience. And the TDA2x SoC also integrates a host of peripherals including multi-camera interfaces (both parallel and serial) for LVDS-based surround view systems, displays, CAN and GigB Ethernet AVB.

The Vision AccelerationPac for this family of products includes multiple embedded vision engines (EVEs) offloading the vision analytics functionality from the application processor while also reducing the power footprint. The Vision AccelerationPac is optimized for vision processing with a 32-bit RISC core for efficient program execution and a vector coprocessor for specialized vision processing.

Additionally, TI provides a complete set of development tools for the ARM, DSP, and EVE coprocessor, including C compilers, a DSP assembly optimizer to simplify programming and scheduling, and a debugging interface for visibility into source code execution.

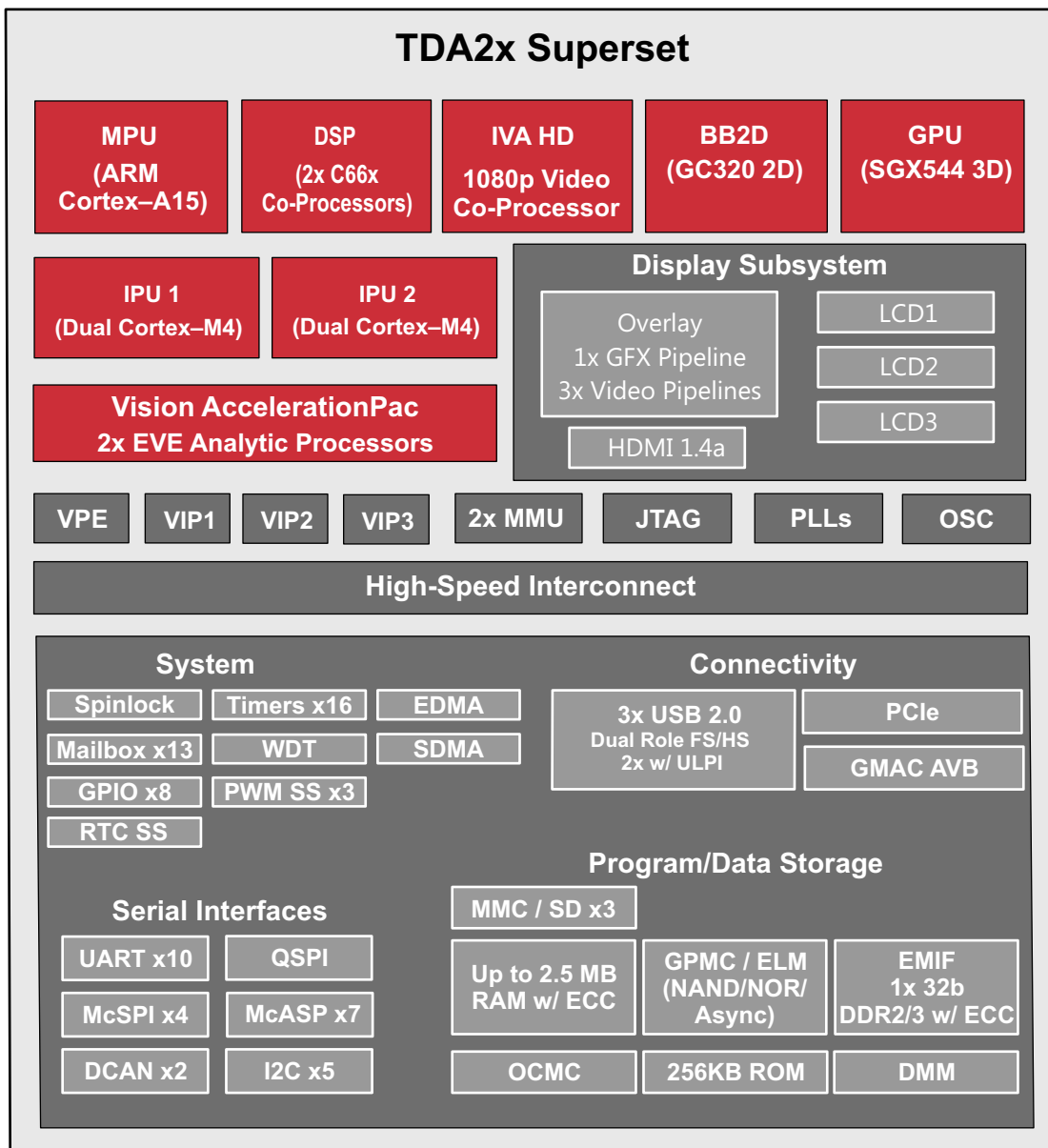
The TDA2x ADAS processor is qualified according to the AEC-Q100 standard.

Device Information

PART NUMBER	PACKAGE	BODY SIZE
TDA2x	FCBGA (625)	17.0 mm x 17.0 mm

1.4 Functional Block Diagram

Figure 1-1 is functional block diagram of the superset.



intro-001
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Figure 1-1. TDA2x Block Diagram

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2 Revision History

Changes from June 7, 2017 to January 31, 2018 (from C Revision (June 2017) to D Revision)	Page
• Added missing balls in Table 4-1	9
• Added clarification notes in Ball Characteristics Table	10
• Added missing PCIe buffer in Table 4-2	12
• Fixed typo in Table 4-21	108
• Removed signal names from Figure 5-1	146
• Updated DPLL type A CLKOUT output frequency in Table 6-13	167
• Updated McSPI and QSPI Timing figures	227
• Added CAN delay time receive and transmit parameters in relation to the shift registers	257
• Fixed typo in Table 8-49 and Table 8-50	368

3 Device Comparison

3.1 Device Comparison Table

Table 3-1 shows a comparison between devices, highlighting the differences.

Table 3-1. Device Comparison

Features		Device		
		TDA2HGx	TDA2Hx	
Features				
CTRL_WKUP_STD_FUSE_DIE_ID_2[31:24] Base PN register bitfield value ⁽²⁾		42 (0x2A)	37 (0x25)	
Processors/Accelerators				
Speed Grades		R, D	R, D	
Dual ARM Cortex-A15 Microprocessor Subsystem (MPU)	MPU core 0	Yes	Yes	
	MPU core 1	No	No	
C66x VLIW DSP	DSP1	Yes	Yes	
	DSP2	Yes	Yes	
BitBLT 2D Hardware Acceleration Engine (BB2D)	BB2B	Yes	No	
Display Subsystem	VOUT1	Yes	Yes	
	VOUT2	Yes	No	
	VOUT3	Yes	No	
	HDMI	Yes	Yes	
Embedded Vision Engine (EVE)	EVE1	Yes	Yes	
	EVE2	Yes	Yes	
	EVE3	No	No	
	EVE4	No	No	
Dual ARM Cortex-M4 Image Processing Unit (IPU)	IPU1	Yes	Yes	
	IPU2	Yes	Yes	
Image Video Accelerator (IVA)	IVA	Yes	No	
SGX544 Dual-Core 3D Graphics Processing Unit (GPU)	GPU	Yes	No	
Video Input Port (VIP)	VIP1	vin1a	Yes	Yes
		vin1b	Yes	Yes
		vin2a	Yes	No
		vin2b	Yes	Yes
	VIP2	vin3a	Yes	No
		vin3b	Yes	No
		vin4a	No	No
		vin4b	Yes	No
	VIP3	vin5a	No	No
		vin6a	No	No
Video Processing Engine (VPE)	VPE	Yes	Yes	
Program/Data Storage				
On-Chip Shared Memory (RAM)	OCMC_RAM1	512KB	512KB	
	OCMC_RAM2	1MB	1MB	
	OCMC_RAM3	1MB	1MB	
General-Purpose Memory Controller (GPMC)	GPMC	Yes	Yes	
DDR2/DDR3 Memory Controller	EMIF1 (with SECDEC)	up to 2GB	up to 2GB	
	EMIF2	No	No	

Table 3-1. Device Comparison (continued)

Features		Device	
		TDA2HGx	TDA2Hx
Dynamic Memory Manager (DMM)	DMM	Yes	Yes
Peripherals			
Dual Controller Area Network Interface (DCAN)	DCAN1	Yes	Yes
	DCAN2	Yes	Yes
Enhanced DMA	EDMA	Yes	Yes
System DMA	SDMA	Yes	Yes
Ethernet Subsystem (Ethernet SS)	GMAC_SW[0]	Yes	Yes
	GMAC_SW[1]	Yes	Yes
	Ethernet switch	Yes	Yes
General-Purpose I/O (GPIO)	GPIO	up to 247	up to 247
Inter-Integrated Circuit Interface (I ² C)	I2C	5	5
System Mailbox Module	MAILBOX	13	13
Multichannel Audio Serial Port (McASP)	McASP1	12 serializers	12 serializers
	McASP2	8 serializers	8 serializers
	McASP3	4 serializers	4 serializers
	McASP4	2 serializers	2 serializers
	McASP5	2 serializers	2 serializers
	McASP6	2 serializers	2 serializers
	McASP7	2 serializers	2 serializers
	McASP8	No	No
MultiMedia Card/Secure Digital/Secure Digital Input Output Interface (MMC/SD/SDIO)	MMC1	No	No
	MMC2 ⁽¹⁾	1x eMMC™ 8b	1x eMMC 8b
	MMC3	1x SDIO 8b	1x SDIO 8b
	MMC4	1x SDIO 4b	1x SDIO 4b
PCI Express 3.0 Port with Integrated PHY	PCIe_SS1	Yes	Yes
	PCIe_SS2	No	No
SATA Gen2 Interface	SATA	No	No
Real-Time Clock Subsystem	RTCSS	Yes	Yes
Multichannel Serial Peripheral Interface (McSPI)	McSPI	4	4
Quad SPI (QSPI)	QSPI	Yes	Yes
Spinlock Module	SPINLOCK	Yes	Yes
Timers, General-Purpose	TIMER	16	16
Timer, Watchdog	WATCHDOG TIMER	Yes	Yes
Pulse-Width Modulation Subsystem (PWMSS)	PWMSS1	Yes	Yes
	PWMSS2	Yes	Yes
	PWMSS3	Yes	Yes
Universal Asynchronous Receiver/Transmitter (UART)	UART	10	10
Universal Serial Bus (USB3.0)	USB1 (SuperSpeed, Dual-Role-Device [DRD])	Yes (USB2.0 mode only)	Yes (USB2.0 mode only)
Universal Serial Bus (USB2.0)	USB2 (HighSpeed, Dual-Role-Device [DRD], with embedded HS PHY)	No	No
	USB3 (HighSpeed, OTG2.0, with ULPI)	Yes	Yes
	USB4 (HighSpeed, OTG2.0, with ULPI)	Yes	Yes

- (1) MMC2 HS200 mode is NOT supported on this device.
- (2) For more details about the CTRL_WKUP_STD_FUSE_DIE_ID_2 register and Base PN bitfield, see the *TDA2x Technical Reference Manual*.

3.2 Related Products

Automotive Processors

TDAX ADAS SoCs TI's TDAx Driver Assistance System-on-Chip (SoC) family offers scalable and open solutions and a common hardware and software architecture for Advanced Driver Assistance Systems (ADAS) applications including camera-based front (mono and stereo), rear, surround view and night vision systems, and mid- and long-range radar and sensor fusion systems.

Companion Products for TDA2 Review products that are frequently purchased or used in conjunction with this product.

4 Terminal Configuration and Functions

4.1 Terminal Assignment

Figure 4-1 shows the ball locations for the 625-ball plastic ball grid array (PBGA) package and are used in conjunction with Table 4-2 through Table 4-28 to locate signal names and ball grid numbers.

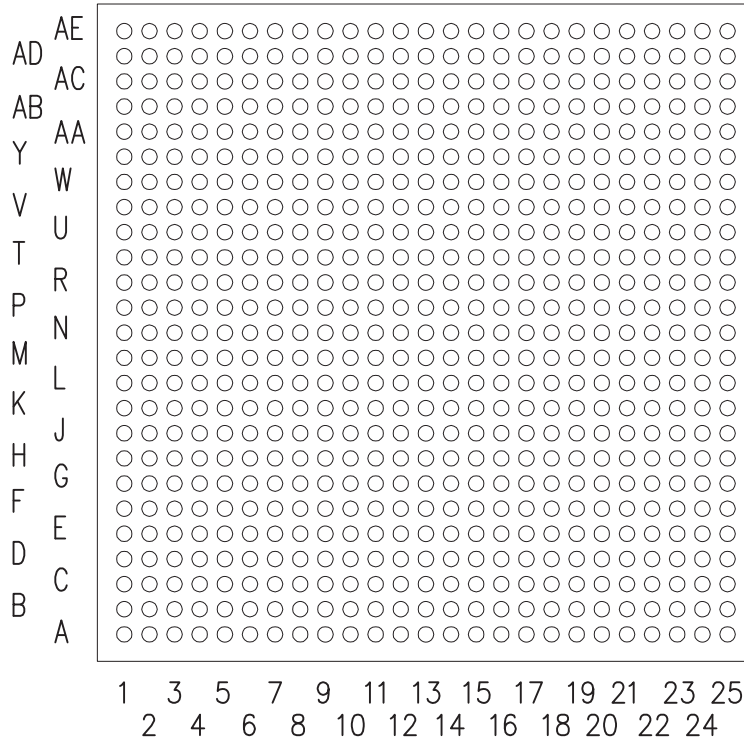


Figure 4-1. AAS S-PBGA-N625 Package (Bottom View)

4.1.1 Unused Balls Connection Requirements

This section describes the Unused/Reserved balls connection requirements.

NOTE

The following balls are reserved: Y7 / J21 / A24 / B25

These balls must be left unconnected.

NOTE

All unused power supply balls must be supplied with the voltages specified in the Section 5.4, *Recommended Operating Conditions*, unless alternative tie-off options are included in Section 4.4, *Signal Descriptions*.

Table 4-1. Unused Balls Specific Connection Requirements

Balls	Connection Requirements
AA13 / AA16 / AA17 / AB17 / AC13 / AC14 / AC17 / E17 / K25 / AA25 / V25 / U25 / P25	These balls must be connected to GND through an external pull resistor if unused
E18 / G22 / G24 / G25 / H21 / K24 / D18 / AA24 / V24 / U24 / P24 / F22 / F23	These balls must be connected to the corresponding power supply through an external pull resistor if unused

Table 4-1. Unused Balls Specific Connection Requirements (continued)

Balls	Connection Requirements
AA9 (rtc_iso)	This ball should be connected to the corresponding power supply through an external pull resistor if unused; or can be connected to F17 (porz) when RTC unused (level translation may be needed)
AA10 (rtc_porz)	This ball should be connected to VSS when RTC is unused; or can be connected to F17 (porz) when RTC unused (level translation may be needed)

NOTE

All other unused signal balls **with** a Pad Configuration Register can be left unconnected with their internal pullup or pulldown resistor enabled.

NOTE

All other unused signal balls **without** Pad Configuration Register can be left unconnected.

4.2 Ball Characteristics

Table 4-2 describes the terminal characteristics and the signals multiplexed on each ball. The following list describes the table column headers:

1. **BALL NUMBER:** Ball number(s) on the bottom side associated with each signal on the bottom.
2. **BALL NAME:** Mechanical name from package device (name is taken from muxmode 0).
3. **SIGNAL NAME:** Names of signals multiplexed on each ball (also notice that the name of the ball is the signal name in muxmode 0).

NOTE

Table 4-2 does not take into account the subsystem multiplexing signals. Subsystem multiplexing signals are described in Section 4.4, *Signal Descriptions*.

NOTE

In the Driver off mode, the buffer is configured in high-impedance.

4. **HGx/HAx:** This column shows if the functionality is applicable for **TDA2HGx / TDA2HAx** devices. Note that the ball characteristics table presents the functionality of Superset device.

HGx - TDA2HGx

HAx - TDA2HAx

5. **MUXMODE:** Multiplexing mode number:
 - a. MUXMODE 0 is the primary mode; this means that when MUXMODE=0, the function mapped on the pin corresponds to the name of the pin. The primary muxmode is not necessarily the default muxmode.

NOTE

The default muxmode is the muxmode at the release of the reset; also see the RESET REL. MUXMODE column.

- b. MUXMODE 1 through 15 are possible muxmodes for alternate functions. On each pin, some muxmodes are effectively used for alternate functions, while some muxmodes are not used. Only MUXMODE values which correspond to defined functions should be used.
- c. An empty box means Not Applicable.

6. **TYPE:** Signal type and direction:
 - I = Input
 - O = Output
 - IO = Input or Output
 - D = Open drain
 - DS = Differential Signaling
 - A = Analog
 - PWR = Power
 - GND = Ground
 - CAP = LDO Capacitor
7. **BALL RESET STATE:** The state of the terminal at power-on reset:
 - drive 0 (OFF): The buffer drives V_{OL} (pulldown or pullup resistor not activated)
 - drive 1 (OFF): The buffer drives V_{OH} (pulldown or pullup resistor not activated)
 - OFF: High-impedance
 - PD: High-impedance with an active pulldown resistor
 - PU: High-impedance with an active pullup resistor
 - An empty box means Not Applicable
8. **BALL RESET REL. STATE:** The state of the terminal at the deactivation of the rstoutn signal (also mapped to the PRCM SYS_WARM_OUT_RST signal)
 - drive 0 (OFF): The buffer drives V_{OL} (pulldown or pullup resistor not activated)
 - drive clk (OFF): The buffer drives a toggling clock (pulldown or pullup resistor not activated)
 - drive 1 (OFF): The buffer drives V_{OH} (pulldown or pullup resistor not activated)
 - OFF: High-impedance
 - PD: High-impedance with an active pulldown resistor
 - PU: High-impedance with an active pullup resistor
 - An empty box means Not Applicable

NOTE

For more information on the CORE_PWRON_RET_RST reset signal and its reset sources, see the Power Reset and Clock Management / PRCM Reset Management Functional Description section of the Device TRM.

9. **BALL RESET REL. MUXMODE:** This muxmode is automatically configured at the release of the rstoutn signal (also mapped to the PRCM SYS_WARM_OUT_RST signal).
An empty box means Not Applicable.
10. **IO VOLTAGE VALUE:** This column describes the IO voltage value (VDDS supply).
An empty box means Not Applicable.
11. **POWER:** The voltage supply that powers the terminal IO buffers.
An empty box means Not Applicable.
12. **HYS:** Indicates if the input buffer is with hysteresis:
 - Yes: With hysteresis
 - No: Without hysteresis
 - An empty box: Not Applicable

NOTE

For more information, see the hysteresis values in [Section 5.7](#), *DC Electrical Characteristics*.

13. **BUFFER TYPE:** Drive strength of the associated output buffer.
An empty box means Not Applicable.

NOTE

For programmable buffer strength:

- The default value is given in [Table 4-2](#).
- A note describes all possible values according to the selected muxmode.

14. **PULLUP / PULLDOWN TYPE:** Denotes the presence of an internal pullup or pulldown resistor. Pullup and pulldown resistors can be enabled or disabled via software.

- PU: Internal pullup
- PD: Internal pulldown
- PU/PD: Internal pullup and pulldown
- PUx/PDy: Programmable internal pullup and pulldown
- PDy: Programmable internal pulldown
- An empty box means No pull

15. **DSIS:** The deselected input state (DSIS) indicates the state driven on the peripheral input (logic "0" or logic "1") when the peripheral pin function is not selected by any of the PINCNLTx registers.

- 0: Logic 0 driven on the peripheral's input signal port.
- 1: Logic 1 driven on the peripheral's input signal port.
- blank: Pin state driven on the peripheral's input signal port.

NOTE

Configuring two pins to the same input signal is not supported as it can yield unexpected results. This can be easily prevented with the proper software configuration (Hi-Z mode is not an input signal).

NOTE

When a pad is set into a multiplexing mode which is not defined by pin multiplexing, that pad's behavior is undefined. This should be avoided.

CAUTION

Peripherals exposed in Ball Characteristics Table and Multiplexing Characteristics Table represent functionality of a superset device. Not all exposed peripherals are supported on ADAS devices. For peripherals supported on ADAS family of products please refer to [Table 3-1, Device Comparison](#).

NOTE

Some of the DDR1 signals have an additional state change at the release of porz. The state that the signals change to at the release of porz is as follows:

drive 0 (OFF) for: ddr1_csn0, ddr1_ck, ddr1_nck, ddr1_casn, ddr1_rasn, ddr1_wen, ddr1_ba[2:0], ddr1_a[15:0].

OFF for: ddr1_ecc_d[7:0], ddr1_dqm[3:0], ddr1_dqm_ecc, ddr1_dqs[3:0], ddr1_dqsn[3:0], ddr1_dqs_ecc, ddr1_dqsn_ecc, ddr1_d[31:0].

Table 4-2. Ball Characteristics(1)

BALL NUMBER [1]	BALL NAME [2]	SIGNAL NAME [3]	HGX/HAX [4]	MUXMODE [5]	TYPE [6]	BALL RESET STATE [7]	BALL RESET REL. STATE [8]	BALL RESET REL. MUXMODE [9]	I/O VOLTAGE VALUE [10]	POWER [11]	HYS [12]	BUFFER TYPE [13]	PULL UP/DOWN TYPE [14]	DSIS [15]
F11	cap_vbbldo_dspeve	cap_vbbldo_dspeve			CAP									
AA15	cap_vbbldo_gpu	cap_vbbldo_gpu			CAP									
P20	cap_vbbldo_iva	cap_vbbldo_iva			CAP									
F13	cap_vbbldo_mpu	cap_vbbldo_mpu			CAP									
J6	cap_vddram_core1	cap_vddram_core1			CAP									
F16	cap_vddram_core2	cap_vddram_core2			CAP									
N20	cap_vddram_core3	cap_vddram_core3			CAP									
T20	cap_vddram_core4	cap_vddram_core4			CAP									
Y14	cap_vddram_core5	cap_vddram_core5			CAP									
L6	cap_vddram_dspeve1	cap_vddram_dspeve1			CAP									
F9	cap_vddram_dspeve2	cap_vddram_dspeve2			CAP									
Y11	cap_vddram_gpu	cap_vddram_gpu			CAP									
R20	cap_vddram_iva	cap_vddram_iva			CAP									
F15	cap_vddram_mpu1	cap_vddram_mpu1			CAP									
F18	cap_vddram_mpu2	cap_vddram_mpu2			CAP									
E21	dcan1_rx	dcan1_rx		0	IO	PU	PU	15	1.8/3.3	vddshv3	Yes	Dual Voltage LVCMOS	PU/PD	1
		uart8_txd		2	O									
		mmc2_sdwp		3	I									
		hdmi1_cec		6	IO									
		gpio1_15		14	IO									
		Driver off		15	I									
E19	dcan1_tx	dcan1_tx		0	IO	PU	PU	15	1.8/3.3	vddshv3	Yes	Dual Voltage LVCMOS	PU/PD	1
		uart8_rxd		2	I									
		mmc2_sdc		3	I									
		hdmi1_hpd		6	I									
		gpio1_14		14	IO									
		Driver off		15	I									
AB18	ddr1_a0	ddr1_a0		0	O	PD	drive 1 (OFF)		1.35/1.5/1.8	vdds_ddr1	No	LVC MOS DDR	Pux/PDy	
AE20	ddr1_a1	ddr1_a1		0	O	PD	drive 1 (OFF)		1.35/1.5/1.8	vdds_ddr1	No	LVC MOS DDR	Pux/PDy	
AD24	ddr1_a2	ddr1_a2		0	O	PD	drive 1 (OFF)		1.35/1.5/1.8	vdds_ddr1	No	LVC MOS DDR	Pux/PDy	
AA18	ddr1_a3	ddr1_a3		0	O	PD	drive 1 (OFF)		1.35/1.5/1.8	vdds_ddr1	No	LVC MOS DDR	Pux/PDy	
AC21	ddr1_a4	ddr1_a4		0	O	PD	drive 1 (OFF)		1.35/1.5/1.8	vdds_ddr1	No	LVC MOS DDR	Pux/PDy	
AC20	ddr1_a5	ddr1_a5		0	O	PD	drive 1 (OFF)		1.35/1.5/1.8	vdds_ddr1	No	LVC MOS DDR	Pux/PDy	

Table 4-2. Ball Characteristics(1) (continued)

BALL NUMBER [1]	BALL NAME [2]	SIGNAL NAME [3]	HGX/HAX [4]	MUXMODE [5]	TYPE [6]	BALL RESET STATE [7]	BALL RESET REL. STATE [8]	BALL RESET REL. MUXMODE [9]	I/O VOLTAGE VALUE [10]	POWER [11]	HYS [12]	BUFFER TYPE [13]	PULL UP/DOWN TYPE [14]	DSIS [15]
AC23	ddr1_a6	ddr1_a6		0	O	PD	drive 1 (OFF)		1.35/1.5/1.8	vdds_ddr1	No	LVC MOS DDR	Pux/PDy	
AA19	ddr1_a7	ddr1_a7		0	O	PD	drive 1 (OFF)		1.35/1.5/1.8	vdds_ddr1	No	LVC MOS DDR	Pux/PDy	
AB20	ddr1_a8	ddr1_a8		0	O	PD	drive 1 (OFF)		1.35/1.5/1.8	vdds_ddr1	No	LVC MOS DDR	Pux/PDy	
AB23	ddr1_a9	ddr1_a9		0	O	PD	drive 1 (OFF)		1.35/1.5/1.8	vdds_ddr1	No	LVC MOS DDR	Pux/PDy	
AB22	ddr1_a10	ddr1_a10		0	O	PD	drive 1 (OFF)		1.35/1.5/1.8	vdds_ddr1	No	LVC MOS DDR	Pux/PDy	
AB25	ddr1_a11	ddr1_a11		0	O	PD	drive 1 (OFF)		1.35/1.5/1.8	vdds_ddr1	No	LVC MOS DDR	Pux/PDy	
AB24	ddr1_a12	ddr1_a12		0	O	PD	drive 1 (OFF)		1.35/1.5/1.8	vdds_ddr1	No	LVC MOS DDR	Pux/PDy	
AD17	ddr1_a13	ddr1_a13		0	O	PD	drive 1 (OFF)		1.35/1.5/1.8	vdds_ddr1	No	LVC MOS DDR	Pux/PDy	
AE17	ddr1_a14	ddr1_a14		0	O	PD	drive 1 (OFF)		1.35/1.5/1.8	vdds_ddr1	No	LVC MOS DDR	Pux/PDy	
AD18	ddr1_a15	ddr1_a15		0	O	PD	drive 1 (OFF)		1.35/1.5/1.8	vdds_ddr1	No	LVC MOS DDR	Pux/PDy	
AE18	ddr1_ba0	ddr1_ba0		0	O	PD	drive 1 (OFF)		1.35/1.5/1.8	vdds_ddr1	No	LVC MOS DDR	Pux/PDy	
AE21	ddr1_ba1	ddr1_ba1		0	O	PD	drive 1 (OFF)		1.35/1.5/1.8	vdds_ddr1	No	LVC MOS DDR	Pux/PDy	
AE23	ddr1_ba2	ddr1_ba2		0	O	PD	drive 1 (OFF)		1.35/1.5/1.8	vdds_ddr1	No	LVC MOS DDR	Pux/PDy	
AC18	ddr1_casn	ddr1_casn		0	O	PD	drive 1 (OFF)		1.35/1.5/1.8	vdds_ddr1	No	LVC MOS DDR	Pux/PDy	
AC25	ddr1_ck	ddr1_ck		0	O	PD	drive clk (OFF)		1.35/1.5/1.8	vdds_ddr1	No	LVC MOS DDR	Pux/PDy	
AB19	ddr1_cke	ddr1_cke		0	O	PD	drive 0 (OFF)		1.35/1.5/1.8	vdds_ddr1	No	LVC MOS DDR	Pux/PDy	
AC22	ddr1_csn0	ddr1_csn0		0	O	PD	drive 1 (OFF)		1.35/1.5/1.8	vdds_ddr1	No	LVC MOS DDR	Pux/PDy	
Y21	ddr1_d0	ddr1_d0		0	IO	PD	PD		1.35/1.5/1.8	vdds_ddr1	No	LVC MOS DDR	Pux/PDy	
Y24	ddr1_d1	ddr1_d1		0	IO	PD	PD		1.35/1.5/1.8	vdds_ddr1	No	LVC MOS DDR	Pux/PDy	
W24	ddr1_d2	ddr1_d2		0	IO	PD	PD		1.35/1.5/1.8	vdds_ddr1	No	LVC MOS DDR	Pux/PDy	
Y22	ddr1_d3	ddr1_d3		0	IO	PD	PD		1.35/1.5/1.8	vdds_ddr1	No	LVC MOS DDR	Pux/PDy	
W25	ddr1_d4	ddr1_d4		0	IO	PD	PD		1.35/1.5/1.8	vdds_ddr1	No	LVC MOS DDR	Pux/PDy	
Y25	ddr1_d5	ddr1_d5		0	IO	PD	PD		1.35/1.5/1.8	vdds_ddr1	No	LVC MOS DDR	Pux/PDy	

Table 4-2. Ball Characteristics(1) (continued)

BALL NUMBER [1]	BALL NAME [2]	SIGNAL NAME [3]	HGx/HAx [4]	MUXMODE [5]	TYPE [6]	BALL RESET STATE [7]	BALL RESET REL. STATE [8]	BALL RESET REL. MUXMODE [9]	I/O VOLTAGE VALUE [10]	POWER [11]	HYS [12]	BUFFER TYPE [13]	PULL UP/DOWN TYPE [14]	DSIS [15]
AA22	ddr1_d6	ddr1_d6		0	IO	PD	PD		1.35/1.5/1.8	vdds_ddr1	No	LVC MOS DDR	Pux/PDy	
AA21	ddr1_d7	ddr1_d7		0	IO	PD	PD		1.35/1.5/1.8	vdds_ddr1	No	LVC MOS DDR	Pux/PDy	
W21	ddr1_d8	ddr1_d8		0	IO	PD	PD		1.35/1.5/1.8	vdds_ddr1	No	LVC MOS DDR	Pux/PDy	
W22	ddr1_d9	ddr1_d9		0	IO	PD	PD		1.35/1.5/1.8	vdds_ddr1	No	LVC MOS DDR	Pux/PDy	
W23	ddr1_d10	ddr1_d10		0	IO	PD	PD		1.35/1.5/1.8	vdds_ddr1	No	LVC MOS DDR	Pux/PDy	
V23	ddr1_d11	ddr1_d11		0	IO	PD	PD		1.35/1.5/1.8	vdds_ddr1	No	LVC MOS DDR	Pux/PDy	
V22	ddr1_d12	ddr1_d12		0	IO	PD	PD		1.35/1.5/1.8	vdds_ddr1	No	LVC MOS DDR	Pux/PDy	
V21	ddr1_d13	ddr1_d13		0	IO	PD	PD		1.35/1.5/1.8	vdds_ddr1	No	LVC MOS DDR	Pux/PDy	
U23	ddr1_d14	ddr1_d14		0	IO	PD	PD		1.35/1.5/1.8	vdds_ddr1	No	LVC MOS DDR	Pux/PDy	
U22	ddr1_d15	ddr1_d15		0	IO	PD	PD		1.35/1.5/1.8	vdds_ddr1	No	LVC MOS DDR	Pux/PDy	
R22	ddr1_d16	ddr1_d16		0	IO	PD	PD		1.35/1.5/1.8	vdds_ddr1	No	LVC MOS DDR	Pux/PDy	
P23	ddr1_d17	ddr1_d17		0	IO	PD	PD		1.35/1.5/1.8	vdds_ddr1	No	LVC MOS DDR	Pux/PDy	
T21	ddr1_d18	ddr1_d18		0	IO	PD	PD		1.35/1.5/1.8	vdds_ddr1	No	LVC MOS DDR	Pux/PDy	
R25	ddr1_d19	ddr1_d19		0	IO	PD	PD		1.35/1.5/1.8	vdds_ddr1	No	LVC MOS DDR	Pux/PDy	
R24	ddr1_d20	ddr1_d20		0	IO	PD	PD		1.35/1.5/1.8	vdds_ddr1	No	LVC MOS DDR	Pux/PDy	
R21	ddr1_d21	ddr1_d21		0	IO	PD	PD		1.35/1.5/1.8	vdds_ddr1	No	LVC MOS DDR	Pux/PDy	
T22	ddr1_d22	ddr1_d22		0	IO	PD	PD		1.35/1.5/1.8	vdds_ddr1	No	LVC MOS DDR	Pux/PDy	
T25	ddr1_d23	ddr1_d23		0	IO	PD	PD		1.35/1.5/1.8	vdds_ddr1	No	LVC MOS DDR	Pux/PDy	
N21	ddr1_d24	ddr1_d24		0	IO	PD	PD		1.35/1.5/1.8	vdds_ddr1	No	LVC MOS DDR	Pux/PDy	
N25	ddr1_d25	ddr1_d25		0	IO	PD	PD		1.35/1.5/1.8	vdds_ddr1	No	LVC MOS DDR	Pux/PDy	
N24	ddr1_d26	ddr1_d26		0	IO	PD	PD		1.35/1.5/1.8	vdds_ddr1	No	LVC MOS DDR	Pux/PDy	
M22	ddr1_d27	ddr1_d27		0	IO	PD	PD		1.35/1.5/1.8	vdds_ddr1	No	LVC MOS DDR	Pux/PDy	
N23	ddr1_d28	ddr1_d28		0	IO	PD	PD		1.35/1.5/1.8	vdds_ddr1	No	LVC MOS DDR	Pux/PDy	

Table 4-2. Ball Characteristics(1) (continued)

BALL NUMBER [1]	BALL NAME [2]	SIGNAL NAME [3]	HGX/HAX [4]	MUXMODE [5]	TYPE [6]	BALL RESET STATE [7]	BALL RESET REL. STATE [8]	BALL RESET REL. MUXMODE [9]	I/O VOLTAGE VALUE [10]	POWER [11]	HYS [12]	BUFFER TYPE [13]	PULL UP/DOWN TYPE [14]	DSIS [15]
P22	ddr1_d29	ddr1_d29		0	IO	PD	PD		1.35/1.5/1.8	vdds_ddr1	No	LVC MOS DDR	Pux/PDy	
M21	ddr1_d30	ddr1_d30		0	IO	PD	PD		1.35/1.5/1.8	vdds_ddr1	No	LVC MOS DDR	Pux/PDy	
N22	ddr1_d31	ddr1_d31		0	IO	PD	PD		1.35/1.5/1.8	vdds_ddr1	No	LVC MOS DDR	Pux/PDy	
AA20	ddr1_dqm0	ddr1_dqm0		0	O	PD	PD		1.35/1.5/1.8	vdds_ddr1	No	LVC MOS DDR	Pux/PDy	
U21	ddr1_dqm1	ddr1_dqm1		0	O	PD	PD		1.35/1.5/1.8	vdds_ddr1	No	LVC MOS DDR	Pux/PDy	
T24	ddr1_dqm2	ddr1_dqm2		0	O	PD	PD		1.35/1.5/1.8	vdds_ddr1	No	LVC MOS DDR	Pux/PDy	
P21	ddr1_dqm3	ddr1_dqm3		0	O	PD	PD		1.35/1.5/1.8	vdds_ddr1	No	LVC MOS DDR	Pux/PDy	
K22	ddr1_dqm_ecc	ddr1_dqm_ecc		0	O	PD	PD		1.35/1.5/1.8	vdds_ddr1	No	LVC MOS DDR	Pux/PDy	
AA25	ddr1_dqs0	ddr1_dqs0		0	IO	PD	PD		1.35/1.5/1.8	vdds_ddr1		LVC MOS DDR	Pux/PDy	
V25	ddr1_dqs1	ddr1_dqs1		0	IO	PD	PD		1.35/1.5/1.8	vdds_ddr1		LVC MOS DDR	Pux/PDy	
U25	ddr1_dqs2	ddr1_dqs2		0	IO	PD	PD		1.35/1.5/1.8	vdds_ddr1		LVC MOS DDR	Pux/PDy	
P25	ddr1_dqs3	ddr1_dqs3		0	IO	PD	PD		1.35/1.5/1.8	vdds_ddr1		LVC MOS DDR	Pux/PDy	
AA24	ddr1_dqsn0	ddr1_dqsn0		0	IO	PU	PU		1.35/1.5/1.8	vdds_ddr1		LVC MOS DDR	Pux/PDy	
V24	ddr1_dqsn1	ddr1_dqsn1		0	IO	PU	PU		1.35/1.5/1.8	vdds_ddr1		LVC MOS DDR	Pux/PDy	
U24	ddr1_dqsn2	ddr1_dqsn2		0	IO	PU	PU		1.35/1.5/1.8	vdds_ddr1		LVC MOS DDR	Pux/PDy	
P24	ddr1_dqsn3	ddr1_dqsn3		0	IO	PU	PU		1.35/1.5/1.8	vdds_ddr1		LVC MOS DDR	Pux/PDy	
K24	ddr1_dqsn_ecc	ddr1_dqsn_ecc		0	IO	PU	PU		1.35/1.5/1.8	vdds_ddr1		LVC MOS DDR	Pux/PDy	
K25	ddr1_dqs_ecc	ddr1_dqs_ecc		0	IO	PD	PD		1.35/1.5/1.8	vdds_ddr1		LVC MOS DDR	Pux/PDy	
M25	ddr1_ecc_d0	ddr1_ecc_d0		0	IO	PD	PD		1.35/1.5/1.8	vdds_ddr1	No	LVC MOS DDR	Pux/PDy	
M24	ddr1_ecc_d1	ddr1_ecc_d1		0	IO	PD	PD		1.35/1.5/1.8	vdds_ddr1	No	LVC MOS DDR	Pux/PDy	
J23	ddr1_ecc_d2	ddr1_ecc_d2		0	IO	PD	PD		1.35/1.5/1.8	vdds_ddr1	No	LVC MOS DDR	Pux/PDy	
L22	ddr1_ecc_d3	ddr1_ecc_d3		0	IO	PD	PD		1.35/1.5/1.8	vdds_ddr1	No	LVC MOS DDR	Pux/PDy	
K23	ddr1_ecc_d4	ddr1_ecc_d4		0	IO	PD	PD		1.35/1.5/1.8	vdds_ddr1	No	LVC MOS DDR	Pux/PDy	

Table 4-2. Ball Characteristics(1) (continued)

BALL NUMBER [1]	BALL NAME [2]	SIGNAL NAME [3]	HGx/HAx [4]	MUXMODE [5]	TYPE [6]	BALL RESET STATE [7]	BALL RESET REL. STATE [8]	BALL RESET REL. MUXMODE [9]	I/O VOLTAGE VALUE [10]	POWER [11]	HYS [12]	BUFFER TYPE [13]	PULL UP/DOWN TYPE [14]	DSIS [15]
L24	ddr1_ecc_d5	ddr1_ecc_d5		0	IO	PD	PD		1.35/1.5/1.8	vdds_dds1	No	LVC MOS DDR	Pux/PDy	
L25	ddr1_ecc_d6	ddr1_ecc_d6		0	IO	PD	PD		1.35/1.5/1.8	vdds_dds1	No	LVC MOS DDR	Pux/PDy	
L21	ddr1_ecc_d7	ddr1_ecc_d7		0	IO	PD	PD		1.35/1.5/1.8	vdds_dds1	No	LVC MOS DDR	Pux/PDy	
AC24	ddr1_nck	ddr1_nck		0	O	PD	drive clk (OFF)		1.35/1.5/1.8	vdds_dds1	No	LVC MOS DDR	Pux/PDy	
AD23	ddr1_odt0	ddr1_odt0		0	O	PD	drive 0 (OFF)		1.35/1.5/1.8	vdds_dds1	No	LVC MOS DDR	Pux/PDy	
AE19	ddr1_rasn	ddr1_rasn		0	O	PD	drive 1 (OFF)		1.35/1.5/1.8	vdds_dds1	No	LVC MOS DDR	Pux/PDy	
AD20	ddr1_rst	ddr1_rst		0	O	PD	drive 0 (OFF)		1.35/1.5/1.8	vdds_dds1	No	LVC MOS DDR	Pux/PDy	
AB21	ddr1_vref0	ddr1_vref0		0	PWR	OFF	OFF		1.35/1.5/1.8	vdds_dds1	No	LVC MOS DDR		
AD21	ddr1_wen	ddr1_wen		0	O	PD	drive 1 (OFF)		1.35/1.5/1.8	vdds_dds1	No	LVC MOS DDR	Pux/PDy	
E20	emu0	emu0		0	IO	PU	PU	0	1.8/3.3	vddshv3	Yes	Dual Voltage LVC MOS	PU/PD	
		gpio8_30		14	IO									
D21	emu1	emu1		0	IO	PU	PU	0	1.8/3.3	vddshv3	Yes	Dual Voltage LVC MOS	PU/PD	
		gpio8_31		14	IO									
Y1	gpio6_10	gpio6_10		0	IO	PU	PU	15	1.8/3.3	vddshv7	Yes	Dual Voltage LVC MOS	PU/PD	
		mdio_mclk		1	O									1
		i2c3_sda		2	IO									1
		usb3_ulpi_d7		3	IO									0
		vin2b_hsync1		4	I									
		ehrpwm2A		10	O									
		gpio6_10		14	IO									
		Driver off		15	I									
W1	gpio6_11	gpio6_11		0	IO	PU	PU	15	1.8/3.3	vddshv7	Yes	Dual Voltage LVC MOS	PU/PD	
		mdio_d		1	IO									1
		i2c3_scl		2	IO									1
		usb3_ulpi_d6		3	IO									0
		vin2b_vsync1		4	I									
		ehrpwm2B		10	O									
		gpio6_11		14	IO									
		Driver off		15	I									

Table 4-2. Ball Characteristics(1) (continued)

BALL NUMBER [1]	BALL NAME [2]	SIGNAL NAME [3]	HGx/HAx [4]	MUXMODE [5]	TYPE [6]	BALL RESET STATE [7]	BALL RESET REL. STATE [8]	BALL RESET REL. MUXMODE [9]	I/O VOLTAGE VALUE [10]	POWER [11]	HYS [12]	BUFFER TYPE [13]	PULL UP/DOWN TYPE [14]	DSIS [15]
N3	gpmc_a0	gpmc_a0		0	O	PD	PD	15	1.8/3.3	vddshv10	Yes	Dual Voltage LVCMOS	PU/PD	
		vin3a_d16	Yes / No	2	I									0
		vout3_d16	Yes / No	3	O									
		vin4b_d0	Yes / No	6	I									0
		i2c4_scl		7	IO									1
		uart5_rxd		8	I									1
		gpio7_3		14	IO									
		Driver off		15	I									
P3	gpmc_a1	gpmc_a1		0	O	PD	PD	15	1.8/3.3	vddshv10	Yes	Dual Voltage LVCMOS	PU/PD	
		vin3a_d17	Yes / No	2	I									0
		vout3_d17	Yes / No	3	O									
		vin4b_d1	Yes / No	6	I									0
		i2c4_sda		7	IO									1
		uart5_txd		8	O									
		gpio7_4		14	IO									
		Driver off		15	I									
P1	gpmc_a2	gpmc_a2		0	O	PD	PD	15	1.8/3.3	vddshv10	Yes	Dual Voltage LVCMOS	PU/PD	
		vin3a_d18	Yes / No	2	I									0
		vout3_d18	Yes / No	3	O									
		vin4b_d2	Yes / No	6	I									0
		uart7_rxd		7	I									1
		uart5_ctsn		8	I									1
		gpio7_5		14	IO									
		Driver off		15	I									
P2	gpmc_a3	gpmc_a3		0	O	PD	PD	15	1.8/3.3	vddshv10	Yes	Dual Voltage LVCMOS	PU/PD	
		qspi1_cs2		1	O									1
		vin3a_d19	Yes / No	2	I									0
		vout3_d19	Yes / No	3	O									
		vin4b_d3	Yes / No	6	I									0
		uart7_txd		7	O									
		uart5_rtsn		8	O									
		gpio7_6		14	IO									
		Driver off		15	I									

Table 4-2. Ball Characteristics(1) (continued)

BALL NUMBER [1]	BALL NAME [2]	SIGNAL NAME [3]	HGx/HAx [4]	MUXMODE [5]	TYPE [6]	BALL RESET STATE [7]	BALL RESET REL. STATE [8]	BALL RESET REL. MUXMODE [9]	I/O VOLTAGE VALUE [10]	POWER [11]	HYS [12]	BUFFER TYPE [13]	PULL UP/DOWN TYPE [14]	DSIS [15]
N2	gpmc_a4	gpmc_a4		0	O	PD	PD	15	1.8/3.3	vddshv10	Yes	Dual Voltage LVCMOS	PU/PD	
		qspi1_cs3		1	O									1
		vin3a_d20	Yes / No	2	I									0
		vout3_d20	Yes / No	3	O									
		vin4b_d4	Yes / No	6	I									0
		i2c5_scl		7	IO									1
		uart6_rxd		8	I									1
		gpio1_26		14	IO									
Driver off		15	I											
N1	gpmc_a5	gpmc_a5		0	O	PD	PD	15	1.8/3.3	vddshv10	Yes	Dual Voltage LVCMOS	PU/PD	
		vin3a_d21	Yes / No	2	I									0
		vout3_d21	Yes / No	3	O									
		vin4b_d5	Yes / No	6	I									0
		i2c5_sda		7	IO									1
		uart6_txd		8	O									
		gpio1_27		14	IO									
Driver off		15	I											
M5	gpmc_a6	gpmc_a6		0	O	PD	PD	15	1.8/3.3	vddshv10	Yes	Dual Voltage LVCMOS	PU/PD	
		vin3a_d22	Yes / No	2	I									0
		vout3_d22	Yes / No	3	O									
		vin4b_d6	Yes / No	6	I									0
		uart8_rxd		7	I									1
		uart6_ctsn		8	I									1
		gpio1_28		14	IO									
Driver off		15	I											
M4	gpmc_a7	gpmc_a7		0	O	PD	PD	15	1.8/3.3	vddshv10	Yes	Dual Voltage LVCMOS	PU/PD	
		vin3a_d23	Yes / No	2	I									0
		vout3_d23	Yes / No	3	O									
		vin4b_d7	Yes / No	6	I									0
		uart8_txd		7	O									
		uart6_rtsn		8	O									
		gpio1_29		14	IO									
Driver off		15	I											

Table 4-2. Ball Characteristics(1) (continued)

BALL NUMBER [1]	BALL NAME [2]	SIGNAL NAME [3]	HGx/HAx [4]	MUXMODE [5]	TYPE [6]	BALL RESET STATE [7]	BALL RESET REL. STATE [8]	BALL RESET REL. MUXMODE [9]	I/O VOLTAGE VALUE [10]	POWER [11]	HYS [12]	BUFFER TYPE [13]	PULL UP/DOWN TYPE [14]	DSIS [15]
M1	gpmc_a8	gpmc_a8		0	O	PD	PD	15	1.8/3.3	vddshv10	Yes	Dual Voltage LVCMOS	PU/PD	
		vin3a_hsync0	Yes / No	2	I									0
		vout3_hsync	Yes / No	3	O									
		vin4b_hsync1	Yes / No	6	I									0
		timer12		7	IO									
		spl4_sclk		8	IO									0
		gpio1_30		14	IO									
		Driver off		15	I									
M3	gpmc_a9	gpmc_a9		0	O	PD	PD	15	1.8/3.3	vddshv10	Yes	Dual Voltage LVCMOS	PU/PD	
		vin3a_vsync0	Yes / No	2	I									0
		vout3_vsync	Yes / No	3	O									
		vin4b_vsync1	Yes / No	6	I									0
		timer11		7	IO									
		spl4_d1		8	IO									0
		gpio1_31		14	IO									
		Driver off		15	I									
M6	gpmc_a10	gpmc_a10		0	O	PD	PD	15	1.8/3.3	vddshv10	Yes	Dual Voltage LVCMOS	PU/PD	
		vin3a_de0	Yes / No	2	I									0
		vout3_de	Yes / No	3	O									
		vin4b_clk1	Yes / No	6	I									0
		timer10		7	IO									
		spl4_d0		8	IO									0
		gpio2_0		14	IO									
		Driver off		15	I									
N5	gpmc_a11	gpmc_a11		0	O	PD	PD	15	1.8/3.3	vddshv10	Yes	Dual Voltage LVCMOS	PU/PD	
		vin3a_fld0	Yes / No	2	I									0
		vout3_fld	Yes / No	3	O									
		vin4b_de1	Yes / No	6	I									0
		timer9		7	IO									
		spl4_cs0		8	IO									1
		gpio2_1		14	IO									
		Driver off		15	I									

Table 4-2. Ball Characteristics(1) (continued)

BALL NUMBER [1]	BALL NAME [2]	SIGNAL NAME [3]	HGx/HAx [4]	MUXMODE [5]	TYPE [6]	BALL RESET STATE [7]	BALL RESET REL. STATE [8]	BALL RESET REL. MUXMODE [9]	I/O VOLTAGE VALUE [10]	POWER [11]	HYS [12]	BUFFER TYPE [13]	PULL UP/DOWN TYPE [14]	DSIS [15]	
L5	gpmc_a12	gpmc_a12		0	O	PD	PD	15	1.8/3.3	vddshv10	Yes	Dual Voltage LVCMOS	PU/PD		
		gpmc_a0		5	O										
		vin4b_fld1	Yes / No	6	I										0
		timer8		7	IO										
		spi4_cs1		8	IO										1
		dma_evt1		9	I										0
		gpio2_2		14	IO										
Driver off		15	I												
L4	gpmc_a13	gpmc_a13		0	O	PD	PD	15	1.8/3.3	vddshv10	Yes	Dual Voltage LVCMOS	PU/PD		
		qspi1_rtclk		1	I										0
		timer7		7	IO										
		spi4_cs2		8	IO										1
		dma_evt2		9	I										0
		gpio2_3		14	IO										
Driver off		15	I												
L3	gpmc_a14	gpmc_a14		0	O	PD	PD	15	1.8/3.3	vddshv10	Yes	Dual Voltage LVCMOS	PU/PD		
		qspi1_d3		1	I										0
		timer6		7	IO										
		spi4_cs3		8	IO										1
		gpio2_4		14	IO										
		Driver off		15	I										
L2	gpmc_a15	gpmc_a15		0	O	PD	PD	15	1.8/3.3	vddshv10	Yes	Dual Voltage LVCMOS	PU/PD		
		qspi1_d2		1	I										0
		timer5		7	IO										
		gpio2_5		14	IO										
		Driver off		15	I										
L1	gpmc_a16	gpmc_a16		0	O	PD	PD	15	1.8/3.3	vddshv10	Yes	Dual Voltage LVCMOS	PU/PD		
		qspi1_d0		1	IO										0
		gpio2_6		14	IO										
		Driver off		15	I										
K6	gpmc_a17	gpmc_a17		0	O	PD	PD	15	1.8/3.3	vddshv10	Yes	Dual Voltage LVCMOS	PU/PD		
		qspi1_d1		1	I										0
		gpio2_7		14	IO										
		Driver off		15	I										

Table 4-2. Ball Characteristics(1) (continued)

BALL NUMBER [1]	BALL NAME [2]	SIGNAL NAME [3]	HGx/HAx [4]	MUXMODE [5]	TYPE [6]	BALL RESET STATE [7]	BALL RESET REL. STATE [8]	BALL RESET REL. MUXMODE [9]	I/O VOLTAGE VALUE [10]	POWER [11]	HYS [12]	BUFFER TYPE [13]	PULL UP/DOWN TYPE [14]	DSIS [15]
K5	gpmc_a18	gpmc_a18		0	O	PD	PD	15	1.8/3.3	vddshv10	Yes	Dual Voltage LVCMOS	PU/PD	
		qspi1_sclk		1	O									
		gpio2_8		14	IO									
		Driver off		15	I									
C2 ⁽⁹⁾	gpmc_a19	gpmc_a19		0	O	PD	PD	15	1.8/3.3	vddshv11	Yes	Dual Voltage LVCMOS	PU/PD	
		mmc2_dat4		1	IO									1
		gpmc_a13		2	O									
		vin3b_d0	Yes / No	6	I									0
		gpio2_9		14	IO									
		Driver off		15	I									
D3 ⁽⁹⁾	gpmc_a20	gpmc_a20		0	O	PD	PD	15	1.8/3.3	vddshv11	Yes	Dual Voltage LVCMOS	PU/PD	
		mmc2_dat5		1	IO									1
		gpmc_a14		2	O									
		vin3b_d1	Yes / No	6	I									0
		gpio2_10		14	IO									
		Driver off		15	I									
D2 ⁽⁹⁾	gpmc_a21	gpmc_a21		0	O	PD	PD	15	1.8/3.3	vddshv11	Yes	Dual Voltage LVCMOS	PU/PD	
		mmc2_dat6		1	IO									1
		gpmc_a15		2	O									
		vin3b_d2	Yes / No	6	I									0
		gpio2_11		14	IO									
		Driver off		15	I									
D1 ⁽⁹⁾	gpmc_a22	gpmc_a22		0	O	PD	PD	15	1.8/3.3	vddshv11	Yes	Dual Voltage LVCMOS	PU/PD	
		mmc2_dat7		1	IO									1
		gpmc_a16		2	O									
		vin3b_d3	Yes / No	6	I									0
		gpio2_12		14	IO									
		Driver off		15	I									
E1	gpmc_a23	gpmc_a23		0	O	PD	PD	15	1.8/3.3	vddshv11	Yes	Dual Voltage LVCMOS	PU/PD	
		mmc2_clk		1	IO									1
		gpmc_a17		2	O									
		vin3b_d4	Yes / No	6	I									0
		gpio2_13		14	IO									
		Driver off		15	I									

Table 4-2. Ball Characteristics(1) (continued)

BALL NUMBER [1]	BALL NAME [2]	SIGNAL NAME [3]	HGx/HAx [4]	MUXMODE [5]	TYPE [6]	BALL RESET STATE [7]	BALL RESET REL. STATE [8]	BALL RESET REL. MUXMODE [9]	I/O VOLTAGE VALUE [10]	POWER [11]	HYS [12]	BUFFER TYPE [13]	PULL UP/DOWN TYPE [14]	DSIS [15]
E2 (9)	gpmc_a24	gpmc_a24		0	O	PD	PD	15	1.8/3.3	vddshv11	Yes	Dual Voltage LVCMOS	PU/PD	
		mmc2_dat0		1	IO									1
		gpmc_a18		2	O									
		vin3b_d5	Yes / No	6	I									0
		gpio2_14		14	IO									
		Driver off		15	I									
E3 (9)	gpmc_a25	gpmc_a25		0	O	PD	PD	15	1.8/3.3	vddshv11	Yes	Dual Voltage LVCMOS	PU/PD	
		mmc2_dat1		1	IO									1
		gpmc_a19		2	O									
		vin3b_d6	Yes / No	6	I									0
		gpio2_15		14	IO									
		Driver off		15	I									
E4 (9)	gpmc_a26	gpmc_a26		0	O	PD	PD	15	1.8/3.3	vddshv11	Yes	Dual Voltage LVCMOS	PU/PD	
		mmc2_dat2		1	IO									1
		gpmc_a20		2	O									
		vin3b_d7	Yes / No	6	I									0
		gpio2_16		14	IO									
		Driver off		15	I									
F3 (9)	gpmc_a27	gpmc_a27		0	O	PD	PD	15	1.8/3.3	vddshv11	Yes	Dual Voltage LVCMOS	PU/PD	
		mmc2_dat3		1	IO									1
		gpmc_a21		2	O									
		vin3b_hsync1	Yes / No	6	I									0
		gpio2_17		14	IO									
		Driver off		15	I									
J4	gpmc_ad0	gpmc_ad0		0	IO	OFF	OFF	15	1.8/3.3	vddshv10	Yes	Dual Voltage LVCMOS	PU/PD	0
		vin3a_d0	Yes / No	2	I									0
		vout3_d0	Yes / No	3	O									
		gpio1_6		14	IO									
		sysboot0		15	I									
H6	gpmc_ad1	gpmc_ad1		0	IO	OFF	OFF	15	1.8/3.3	vddshv10	Yes	Dual Voltage LVCMOS	PU/PD	0
		vin3a_d1	Yes / No	2	I									0
		vout3_d1	Yes / No	3	O									
		gpio1_7		14	IO									
		sysboot1		15	I									

Table 4-2. Ball Characteristics(1) (continued)

BALL NUMBER [1]	BALL NAME [2]	SIGNAL NAME [3]	HGx/HAx [4]	MUXMODE [5]	TYPE [6]	BALL RESET STATE [7]	BALL RESET REL. STATE [8]	BALL RESET REL. MUXMODE [9]	I/O VOLTAGE VALUE [10]	POWER [11]	HYS [12]	BUFFER TYPE [13]	PULL UP/DOWN TYPE [14]	DSIS [15]
G1	gpmc_ad2	gpmc_ad2		0	IO	OFF	OFF	15	1.8/3.3	vddshv10	Yes	Dual Voltage LVCMOS	PU/PD	0
		vin3a_d2	Yes / No	2	I									0
		vout3_d2	Yes / No	3	O									
		gpio1_8		14	IO									
		sysboot2		15	I									
H2	gpmc_ad3	gpmc_ad3		0	IO	OFF	OFF	15	1.8/3.3	vddshv10	Yes	Dual Voltage LVCMOS	PU/PD	0
		vin3a_d3	Yes / No	2	I									0
		vout3_d3	Yes / No	3	O									
		gpio1_9		14	IO									
		sysboot3		15	I									
H3	gpmc_ad4	gpmc_ad4		0	IO	OFF	OFF	15	1.8/3.3	vddshv10	Yes	Dual Voltage LVCMOS	PU/PD	0
		vin3a_d4	Yes / No	2	I									0
		vout3_d4	Yes / No	3	O									
		gpio1_10		14	IO									
		sysboot4		15	I									
H4	gpmc_ad5	gpmc_ad5		0	IO	OFF	OFF	15	1.8/3.3	vddshv10	Yes	Dual Voltage LVCMOS	PU/PD	0
		vin3a_d5	Yes / No	2	I									0
		vout3_d5	Yes / No	3	O									
		gpio1_11		14	IO									
		sysboot5		15	I									
H5	gpmc_ad6	gpmc_ad6		0	IO	OFF	OFF	15	1.8/3.3	vddshv10	Yes	Dual Voltage LVCMOS	PU/PD	0
		vin3a_d6	Yes / No	2	I									0
		vout3_d6	Yes / No	3	O									
		gpio1_12		14	IO									
		sysboot6		15	I									
F1	gpmc_ad7	gpmc_ad7		0	IO	OFF	OFF	15	1.8/3.3	vddshv10	Yes	Dual Voltage LVCMOS	PU/PD	0
		vin3a_d7	Yes / No	2	I									0
		vout3_d7	Yes / No	3	O									
		gpio1_13		14	IO									
		sysboot7		15	I									
G2	gpmc_ad8	gpmc_ad8		0	IO	OFF	OFF	15	1.8/3.3	vddshv10	Yes	Dual Voltage LVCMOS	PU/PD	0
		vin3a_d8	Yes / No	2	I									0
		vout3_d8	Yes / No	3	O									
		gpio7_18		14	IO									
		sysboot8		15	I									

Table 4-2. Ball Characteristics(1) (continued)

BALL NUMBER [1]	BALL NAME [2]	SIGNAL NAME [3]	HGx/HAx [4]	MUXMODE [5]	TYPE [6]	BALL RESET STATE [7]	BALL RESET REL. STATE [8]	BALL RESET REL. MUXMODE [9]	I/O VOLTAGE VALUE [10]	POWER [11]	HYS [12]	BUFFER TYPE [13]	PULL UP/DOWN TYPE [14]	DSIS [15]
G3	gpmc_ad9	gpmc_ad9		0	IO	OFF	OFF	15	1.8/3.3	vddshv10	Yes	Dual Voltage LVCMOS	PU/PD	0
		vin3a_d9	Yes / No	2	I									0
		vout3_d9	Yes / No	3	O									
		gpio7_19		14	IO									
		sysboot9		15	I									
G4	gpmc_ad10	gpmc_ad10		0	IO	OFF	OFF	15	1.8/3.3	vddshv10	Yes	Dual Voltage LVCMOS	PU/PD	0
		vin3a_d10	Yes / No	2	I									0
		vout3_d10	Yes / No	3	O									
		gpio7_28		14	IO									
		sysboot10		15	I									
G5	gpmc_ad11	gpmc_ad11		0	IO	OFF	OFF	15	1.8/3.3	vddshv10	Yes	Dual Voltage LVCMOS	PU/PD	0
		vin3a_d11	Yes / No	2	I									0
		vout3_d11	Yes / No	3	O									
		gpio7_29		14	IO									
		sysboot11		15	I									
G6	gpmc_ad12	gpmc_ad12		0	IO	OFF	OFF	15	1.8/3.3	vddshv10	Yes	Dual Voltage LVCMOS	PU/PD	0
		vin3a_d12	Yes / No	2	I									0
		vout3_d12	Yes / No	3	O									
		gpio1_18		14	IO									
		sysboot12		15	I									
F5	gpmc_ad13	gpmc_ad13		0	IO	OFF	OFF	15	1.8/3.3	vddshv10	Yes	Dual Voltage LVCMOS	PU/PD	0
		vin3a_d13	Yes / No	2	I									0
		vout3_d13	Yes / No	3	O									
		gpio1_19		14	IO									
		sysboot13		15	I									
E5	gpmc_ad14	gpmc_ad14		0	IO	OFF	OFF	15	1.8/3.3	vddshv10	Yes	Dual Voltage LVCMOS	PU/PD	0
		vin3a_d14	Yes / No	2	I									0
		vout3_d14	Yes / No	3	O									
		gpio1_20		14	IO									
		sysboot14		15	I									
F4	gpmc_ad15	gpmc_ad15		0	IO	OFF	OFF	15	1.8/3.3	vddshv10	Yes	Dual Voltage LVCMOS	PU/PD	0
		vin3a_d15	Yes / No	2	I									0
		vout3_d15	Yes / No	3	O									
		gpio1_21		14	IO									
		sysboot15		15	I									

Table 4-2. Ball Characteristics(1) (continued)

BALL NUMBER [1]	BALL NAME [2]	SIGNAL NAME [3]	HGX/HAX [4]	MUXMODE [5]	TYPE [6]	BALL RESET STATE [7]	BALL RESET REL. STATE [8]	BALL RESET REL. MUXMODE [9]	I/O VOLTAGE VALUE [10]	POWER [11]	HYS [12]	BUFFER TYPE [13]	PULL UP/DOWN TYPE [14]	DSIS [15]
J5	gpmc_advn_ale	gpmc_advn_ale		0	O	PU	PU	15	1.8/3.3	vddshv10	Yes	Dual Voltage LVCMOS	PU/PD	
		gpmc_cs6		1	O									
		clkout2		2	O									
		gpmc_wait1		3	I									1
		gpmc_a2		5	O									
		gpmc_a23		6	O									
		timer3		7	IO									
		i2c3_sda		8	IO									1
		dma_evt2		9	I									0
		gpio2_23		14	IO									
		Driver off		15	I									
M2	gpmc_ben0	gpmc_ben0		0	O	PU	PU	15	1.8/3.3	vddshv10	Yes	Dual Voltage LVCMOS	PU/PD	
		gpmc_cs4		1	O									
		vin1b_hsync1		3	I									0
		vin3b_de1	Yes / No	6	I									0
		timer2		7	IO									
		dma_evt3		9	I									0
		gpio2_26		14	IO									
		Driver off		15	I									
J3	gpmc_ben1	gpmc_ben1		0	O	PU	PU	15	1.8/3.3	vddshv10	Yes	Dual Voltage LVCMOS	PU/PD	
		gpmc_cs5		1	O									
		vin1b_de1		3	I									0
		vin3b_clk1	Yes / No	4	I									0
		gpmc_a3		5	O									
		vin3b fld1	Yes / No	6	I									0
		timer1		7	IO									
		dma_evt4		9	I									0
		gpio2_27		14	IO									
Driver off		15	I											

Table 4-2. Ball Characteristics(1) (continued)

BALL NUMBER [1]	BALL NAME [2]	SIGNAL NAME [3]	HGx/HAx [4]	MUXMODE [5]	TYPE [6]	BALL RESET STATE [7]	BALL RESET REL. STATE [8]	BALL RESET REL. MUXMODE [9]	I/O VOLTAGE VALUE [10]	POWER [11]	HYS [12]	BUFFER TYPE [13]	PULL UP/DOWN TYPE [14]	DSIS [15]
N6	gpmc_clk	gpmc_clk		0	IO	PU	PU	15	1.8/3.3	vddshv10	Yes	Dual Voltage LVCMOS	PU/PD	0
		gpmc_cs7		1	O									
		clkout1		2	O									
		gpmc_wait1		3	I									
		vin3b_clk1	Yes / No	6	I									
		timer4		7	IO									
		i2c3_scl		8	IO									
		dma_evt1		9	I									
		gpio2_22		14	IO									
Driver off		15	I											
K4	gpmc_cs0	gpmc_cs0		0	O	PU	PU	15	1.8/3.3	vddshv10	Yes	Dual Voltage LVCMOS	PU/PD	
		gpio2_19		14	IO									
		Driver off		15	I									
C1	gpmc_cs1	gpmc_cs1		0	O	PU	PU	15	1.8/3.3	vddshv11	Yes	Dual Voltage LVCMOS	PU/PD	
		mmc2_cmd		1	IO									
		gpmc_a22		2	O									
		vin3b_vsync1	Yes / No	6	I									
		gpio2_18		14	IO									
Driver off		15	I											
K3	gpmc_cs2	gpmc_cs2		0	O	PU	PU	15	1.8/3.3	vddshv10	Yes	Dual Voltage LVCMOS	PU/PD	
		qspi1_cs0		1	O									
		gpio2_20		14	IO									
		Driver off		15	I									
K2	gpmc_cs3	gpmc_cs3		0	O	PU	PU	15	1.8/3.3	vddshv10	Yes	Dual Voltage LVCMOS	PU/PD	
		qspi1_cs1		1	O									
		vin3a_clk0	Yes / No	2	I									
		vout3_clk	Yes / No	3	O									
		gpmc_a1		5	O									
		gpio2_21		14	IO									
Driver off		15	I											
H1	gpmc_oen_ren	gpmc_oen_ren		0	O	PU	PU	15	1.8/3.3	vddshv10	Yes	Dual Voltage LVCMOS	PU/PD	
		gpio2_24		14	IO									
		Driver off		15	I									
K1	gpmc_wait0	gpmc_wait0		0	I	PU	PU	15	1.8/3.3	vddshv10	Yes	Dual Voltage LVCMOS	PU/PD	1
		gpio2_28		14	IO									
		Driver off		15	I									

Table 4-2. Ball Characteristics(1) (continued)

BALL NUMBER [1]	BALL NAME [2]	SIGNAL NAME [3]	HGX/HAX [4]	MUXMODE [5]	TYPE [6]	BALL RESET STATE [7]	BALL RESET REL. STATE [8]	BALL RESET REL. MUXMODE [9]	I/O VOLTAGE VALUE [10]	POWER [11]	HYS [12]	BUFFER TYPE [13]	PULL UP/DOWN TYPE [14]	DSIS [15]
F2	gpmc_wen	gpmc_wen		0	O	PU	PU	15	1.8/3.3	vddshv10	Yes	Dual Voltage LVCMOS	PU/PD	
		gpio2_25		14	IO									
		Driver off		15	I									
AD13	hdmi1_clockx	hdmi1_clockx		0	O				1.8	vdda_hdmi		HDMIPHY	PDy	
AE13	hdmi1_clocky	hdmi1_clocky		0	O				1.8	vdda_hdmi		HDMIPHY	PDy	
AD14	hdmi1_data0x	hdmi1_data0x		0	O				1.8	vdda_hdmi		HDMIPHY	PDy	
AE14	hdmi1_data0y	hdmi1_data0y		0	O				1.8	vdda_hdmi		HDMIPHY	PDy	
AD15	hdmi1_data1x	hdmi1_data1x		0	O				1.8	vdda_hdmi		HDMIPHY	PDy	
AE15	hdmi1_data1y	hdmi1_data1y		0	O				1.8	vdda_hdmi		HDMIPHY	PDy	
AD16	hdmi1_data2x	hdmi1_data2x		0	O				1.8	vdda_hdmi		HDMIPHY	PDy	
AE16	hdmi1_data2y	hdmi1_data2y		0	O				1.8	vdda_hdmi		HDMIPHY	PDy	
G24	i2c1_scl	i2c1_scl		0	IO	OFF	OFF		1.8/3.3	vddshv3	Yes	Dual Voltage LVCMOS I2C	PU/PD	
G25	i2c1_sda	i2c1_sda		0	IO	OFF	OFF		1.8/3.3	vddshv3	Yes	Dual Voltage LVCMOS I2C	PU/PD	
F23	i2c2_scl	i2c2_scl		0	IO	OFF	OFF	15	1.8/3.3	vddshv3	Yes	Dual Voltage LVCMOS I2C	PU/PD	1
		hdmi1_ddc_sda		1	IO									
		Driver off		15	I									
F22	i2c2_sda	i2c2_sda		0	IO	OFF	OFF	15	1.8/3.3	vddshv3	Yes	Dual Voltage LVCMOS I2C	PU/PD	1
		hdmi1_ddc_scl		1	IO									
		Driver off		15	I									
AD12	ljcb_clkn	ljcb_clkn		0	IO				1.8	vdda_pcie		LJCB		
AE12	ljcb_clkp	ljcb_clkp		0	IO				1.8	vdda_pcie		LJCB		
C25	mcaspl1_aclkx	mcasp1_aclkx		0	IO	PD	PD	15	1.8/3.3	vddshv3	Yes	Dual Voltage LVCMOS	PU/PD	0
		i2c3_sda		10	IO									1
		gpio7_31		14	IO									
		Driver off		15	I									
B15	mcaspl1_axr0	mcasp1_axr0		0	IO	PD	PD	15	1.8/3.3	vddshv3	Yes	Dual Voltage LVCMOS	PU/PD	0
		uart6_rxd		3	I									1
		i2c5_sda		10	IO									1
		gpio5_2		14	IO									
		Driver off		15	I									

Table 4-2. Ball Characteristics(1) (continued)

BALL NUMBER [1]	BALL NAME [2]	SIGNAL NAME [3]	HGX/HAX [4]	MUXMODE [5]	TYPE [6]	BALL RESET STATE [7]	BALL RESET REL. STATE [8]	BALL RESET REL. MUXMODE [9]	I/O VOLTAGE VALUE [10]	POWER [11]	HYS [12]	BUFFER TYPE [13]	PULL UP/DOWN TYPE [14]	DSIS [15]
A15	mcasep1_axr1	mcasep1_axr1		0	IO	PD	PD	15	1.8/3.3	vddshv3	Yes	Dual Voltage LVCMOS	PU/PD	0
		uart6_txd		3	O									
		i2c5_scl		10	IO									1
		gpio5_3		14	IO									
		Driver off		15	I									
A16	mcasep1_axr8	mcasep1_axr8		0	IO	PD	PD	15	1.8/3.3	vddshv3	Yes	Dual Voltage LVCMOS	PU/PD	0
		mcasep6_axr0		1	IO									0
		spi3_sclk		3	IO									0
		timer5		10	IO									
		gpio5_10		14	IO									
		Driver off		15	I									
		A17	mcasep1_axr9	mcasep1_axr9										0
mcasep6_axr1				1	IO	0								
spi3_d1				3	IO	0								
timer6				10	IO									
gpio5_11				14	IO									
Driver off				15	I									
A19	mcasep1_axr10	mcasep1_axr10		0	IO	PD	PD	15	1.8/3.3	vddshv3	Yes	Dual Voltage LVCMOS	PU/PD	0
		mcasep6_aclkx		1	IO									0
		mcasep6_aclkr		2	IO									
		spi3_d0		3	IO									0
		timer7		10	IO									
		gpio5_12		14	IO									
		Driver off		15	I									
A20	mcasep1_axr11	mcasep1_axr11		0	IO	PD	PD	15	1.8/3.3	vddshv3	Yes	Dual Voltage LVCMOS	PU/PD	0
		mcasep6_fsx		1	IO									0
		mcasep6_fsr		2	IO									
		spi3_cs0		3	IO									1
		timer8		10	IO									
		gpio4_17		14	IO									
		Driver off		15	I									
A21	mcasep1_axr12	mcasep1_axr12		0	IO	PD	PD	15	1.8/3.3	vddshv3	Yes	Dual Voltage LVCMOS	PU/PD	0
		mcasep7_axr0		1	IO									0
		spi3_cs1		3	IO									1
		timer9		10	IO									
		gpio4_18		14	IO									
		Driver off		15	I									

Table 4-2. Ball Characteristics(1) (continued)

BALL NUMBER [1]	BALL NAME [2]	SIGNAL NAME [3]	HGX/HAX [4]	MUXMODE [5]	TYPE [6]	BALL RESET STATE [7]	BALL RESET REL. STATE [8]	BALL RESET REL. MUXMODE [9]	I/O VOLTAGE VALUE [10]	POWER [11]	HYS [12]	BUFFER TYPE [13]	PULL UP/DOWN TYPE [14]	DSIS [15]
A23	mcasep1_axr13	mcasep1_axr13		0	IO	PD	PD	15	1.8/3.3	vddshv3	Yes	Dual Voltage LVCMOS	PU/PD	0
		mcasep7_axr1		1	IO									0
		timer10		10	IO									
		gpio6_4		14	IO									
		Driver off		15	I									
C15	mcasep1_axr14	mcasep1_axr14		0	IO	PD	PD	15	1.8/3.3	vddshv3	Yes	Dual Voltage LVCMOS	PU/PD	0
		mcasep7_aclkx		1	IO									0
		mcasep7_aclkr		2	IO									
		timer11		10	IO									
		gpio6_5		14	IO									
		Driver off		15	I									
B16	mcasep1_axr15	mcasep1_axr15		0	IO	PD	PD	15	1.8/3.3	vddshv3	Yes	Dual Voltage LVCMOS	PU/PD	0
		mcasep7_fsx		1	IO									0
		mcasep7_fsr		2	IO									
		timer12		10	IO									
		gpio6_6		14	IO									
		Driver off		15	I									
B24	mcasep1_fsx	mcasep1_fsx		0	IO	PD	PD	15	1.8/3.3	vddshv3	Yes	Dual Voltage LVCMOS	PU/PD	0
		i2c3_scl		10	IO									1
		gpio7_30		14	IO									
		Driver off		15	I									
B21	mcasep2_aclkx	mcasep2_aclkx		0	IO	PD	PD	15	1.8/3.3	vddshv3	Yes	Dual Voltage LVCMOS	PU/PD	0
		Driver off		15	I									
B23	mcasep2_axr2	mcasep2_axr2		0	IO	PD	PD	15	1.8/3.3	vddshv3	Yes	Dual Voltage LVCMOS	PU/PD	0
		mcasep3_axr2		1	IO									0
		gpio6_8		14	IO									
		Driver off		15	I									
B17	mcasep2_axr3	mcasep2_axr3		0	IO	PD	PD	15	1.8/3.3	vddshv3	Yes	Dual Voltage LVCMOS	PU/PD	0
		mcasep3_axr3		1	IO									0
		gpio6_9		14	IO									
		Driver off		15	I									
B20	mcasep2_fsx	mcasep2_fsx		0	IO	PD	PD	15	1.8/3.3	vddshv3	Yes	Dual Voltage LVCMOS	PU/PD	0
		Driver off		15	I									

Table 4-2. Ball Characteristics(1) (continued)

BALL NUMBER [1]	BALL NAME [2]	SIGNAL NAME [3]	HGx/HAx [4]	MUXMODE [5]	TYPE [6]	BALL RESET STATE [7]	BALL RESET REL. STATE [8]	BALL RESET REL. MUXMODE [9]	I/O VOLTAGE VALUE [10]	POWER [11]	HYS [12]	BUFFER TYPE [13]	PULL UP/DOWN TYPE [14]	DSIS [15]
B19	mcasep3_aclkx	mcasep3_aclkx		0	IO	PD	PD	15	1.8/3.3	vddshv3	Yes	Dual Voltage LVCMOS	PU/PD	0
		mcasep3_aclkr		1	IO									
		mcasep2_axr12		2	IO									0
		uart7_rxd		3	I									1
		gpio5_13		14	IO									
		Driver off		15	I									
C17	mcasep3_axr0	mcasep3_axr0		0	IO	PD	PD	15	1.8/3.3	vddshv3	Yes	Dual Voltage LVCMOS	PU/PD	0
		mcasep2_axr14		2	IO									0
		uart7_ctsn		3	I									1
		uart5_rxd		4	I									1
		Driver off		15	I									
		C20	mcasep3_axr1	mcasep3_axr1										0
mcasep2_axr15				2	IO	0								
uart7_rtsn				3	O									
uart5_txd				4	O									
Driver off				15	I									
C16	mcasep3_fsx			mcasep3_fsx		0	IO	PD	PD	15	1.8/3.3	vddshv3	Yes	Dual Voltage LVCMOS
		mcasep3_fsr		1	IO									
		mcasep2_axr13		2	IO	0								
		uart7_txd		3	O									
		gpio5_14		14	IO									
		Driver off		15	I									
E24	mcasep4_aclkx	mcasep4_aclkx		0	IO	PD	PD	15	1.8/3.3	vddshv3	Yes	Dual Voltage LVCMOS	PU/PD	0
		mcasep4_aclkr		1	IO									
		spi3_sclk		2	IO									0
		uart8_rxd		3	I									1
		i2c4_sda		4	IO									1
		vout2_d16	Yes / No	6	O									
		Driver off		15	I									
		E25	mcasep4_axr0	mcasep4_axr0										0
spi3_d0				2	IO	0								
uart8_ctsn				3	I	1								
uart4_rxd				4	I	1								
vout2_d18	Yes / No			6	O									
Driver off				15	I									

Table 4-2. Ball Characteristics(1) (continued)

BALL NUMBER [1]	BALL NAME [2]	SIGNAL NAME [3]	HGX/HAx [4]	MUXMODE [5]	TYPE [6]	BALL RESET STATE [7]	BALL RESET REL. STATE [8]	BALL RESET REL. MUXMODE [9]	I/O VOLTAGE VALUE [10]	POWER [11]	HYS [12]	BUFFER TYPE [13]	PULL UP/DOWN TYPE [14]	DSIS [15]
E23	mcasep4_axr1	mcasep4_axr1		0	IO	PD	PD	15	1.8/3.3	vddshv3	Yes	Dual Voltage LVCMOS	PU/PD	0
		spi3_cs0		2	IO									1
		uart8_rtsn		3	O									
		uart4_txd		4	O									
		vout2_d19	Yes / No	6	O									
		Driver off		15	I									
D23	mcasep4_fsx	mcasep4_fsx		0	IO	PD	PD	15	1.8/3.3	vddshv3	Yes	Dual Voltage LVCMOS	PU/PD	0
		mcasep4_fsr		1	IO									
		spi3_d1		2	IO									0
		uart8_txd		3	O									
		i2c4_scl		4	IO									1
		vout2_d17	Yes / No	6	O									
Driver off		15	I											
V1	mcasep5_aclkx	mcasep5_aclkx		0	IO	PD	PD	15	1.8/3.3	vddshv7	Yes	Dual Voltage LVCMOS	PU/PD	0
		mcasep5_aclkr		1	IO									
		spi4_sclk		2	IO									0
		uart9_rxd		3	I									1
		i2c5_sda		4	IO									1
		vout2_d20	Yes / No	6	O									
Driver off		15	I											
V2	mcasep5_axr0	mcasep5_axr0		0	IO	PD	PD	15	1.8/3.3	vddshv7	Yes	Dual Voltage LVCMOS	PU/PD	0
		spi4_d0		2	IO									0
		uart9_ctsn		3	I									1
		uart3_rxd		4	I									1
		vout2_d22	Yes / No	6	O									
		Driver off		15	I									
U1	mcasep5_axr1	mcasep5_axr1		0	IO	PD	PD	15	1.8/3.3	vddshv7	Yes	Dual Voltage LVCMOS	PU/PD	0
		spi4_cs0		2	IO									1
		uart9_rtsn		3	O									
		uart3_txd		4	O									
		vout2_d23	Yes / No	6	O									
		Driver off		15	I									

Table 4-2. Ball Characteristics(1) (continued)

BALL NUMBER [1]	BALL NAME [2]	SIGNAL NAME [3]	HGx/HAx [4]	MUXMODE [5]	TYPE [6]	BALL RESET STATE [7]	BALL RESET REL. STATE [8]	BALL RESET REL. MUXMODE [9]	I/O VOLTAGE VALUE [10]	POWER [11]	HYS [12]	BUFFER TYPE [13]	PULL UP/DOWN TYPE [14]	DSIS [15]			
W2	mcasep5_fsx	mcasep5_fsx		0	IO	PD	PD	15	1.8/3.3	vddshv7	Yes	Dual Voltage LVCMOS	PU/PD	0			
		mcasep5_fsr		1	IO												
		spi4_d1		2	IO											0	
		uart9_txd		3	O												
		i2c5_scl		4	IO												1
		vout2_d21	Yes / No	6	O												
		Driver off		15	I												
T1	mdio_d	mdio_d		0	IO	PU	PU	15	1.8/3.3	vddshv9	Yes	Dual Voltage LVCMOS	PU/PD	1			
		uart3_ctsn		1	I											1	
		mii0_txer		3	O											0	
		vin2a_d0	Yes / No	4	I											0	
		vin4b_d0	Yes / No	5	I											0	
		gpio5_16		14	IO												
		Driver off		15	I												
R3	mdio_mclk	mdio_mclk		0	O	PU	PU	15	1.8/3.3	vddshv9	Yes	Dual Voltage LVCMOS	PU/PD	1			
		uart3_rtsn		1	O												
		mii0_col		3	I											0	
		vin2a_clk0	Yes / No	4	I												
		vin4b_clk1	Yes / No	5	I												0
		gpio5_15		14	IO												
		Driver off		15	I												
W5	mmc3_clk	mmc3_clk		0	IO	PU	PU	15	1.8/3.3	vddshv7	Yes	Dual Voltage LVCMOS	PU/PD	1			
		usb3_ulpi_d5		3	IO											0	
		vin2b_d7		4	I											0	
		ehrpwm2_tripzone_input		10	IO											0	
		gpio6_29		14	IO												
		Driver off		15	I												
		W4	mmc3_cmd	mmc3_cmd		0	IO	PU	PU	15	1.8/3.3			vddshv7	Yes	Dual Voltage LVCMOS	PU/PD
spi3_sclk				1	IO									0			
usb3_ulpi_d4				3	IO									0			
vin2b_d6				4	I									0			
eCAP2_in_PWM2_out				10	IO									0			
gpio6_30				14	IO												
Driver off				15	I												

Table 4-2. Ball Characteristics(1) (continued)

BALL NUMBER [1]	BALL NAME [2]	SIGNAL NAME [3]	HGx/HAx [4]	MUXMODE [5]	TYPE [6]	BALL RESET STATE [7]	BALL RESET REL. STATE [8]	BALL RESET REL. MUXMODE [9]	I/O VOLTAGE VALUE [10]	POWER [11]	HYS [12]	BUFFER TYPE [13]	PULL UP/DOWN TYPE [14]	DSIS [15]
U6	mmc3_dat0	mmc3_dat0		0	IO	PU	PU	15	1.8/3.3	vddshv7	Yes	Dual Voltage LVCMOS	PU/PD	1
		spi3_d1		1	IO									0
		uart5_rxd		2	I									1
		usb3_ulpi_d3		3	IO									0
		vin2b_d5		4	I									0
		eQEP3A_in		10	I									0
		gpio6_31		14	IO									
		Driver off		15	I									
V6	mmc3_dat1	mmc3_dat1		0	IO	PU	PU	15	1.8/3.3	vddshv7	Yes	Dual Voltage LVCMOS	PU/PD	1
		spi3_d0		1	IO									0
		uart5_txd		2	O									
		usb3_ulpi_d2		3	IO									0
		vin2b_d4		4	I									0
		eQEP3B_in		10	I									0
		gpio7_0		14	IO									
		Driver off		15	I									
U5	mmc3_dat2	mmc3_dat2		0	IO	PU	PU	15	1.8/3.3	vddshv7	Yes	Dual Voltage LVCMOS	PU/PD	1
		spi3_cs0		1	IO									1
		uart5_ctsn		2	I									1
		usb3_ulpi_d1		3	IO									0
		vin2b_d3		4	I									0
		eQEP3_index		10	IO									0
		gpio7_1		14	IO									
		Driver off		15	I									
V3	mmc3_dat3	mmc3_dat3		0	IO	PU	PU	15	1.8/3.3	vddshv7	Yes	Dual Voltage LVCMOS	PU/PD	1
		spi3_cs1		1	IO									1
		uart5_rtsn		2	O									
		usb3_ulpi_d0		3	IO									0
		vin2b_d2		4	I									0
		eQEP3_strobe		10	IO									0
		gpio7_2		14	IO									
		Driver off		15	I									

Table 4-2. Ball Characteristics(1) (continued)

BALL NUMBER [1]	BALL NAME [2]	SIGNAL NAME [3]	HGx/HAx [4]	MUXMODE [5]	TYPE [6]	BALL RESET STATE [7]	BALL RESET REL. STATE [8]	BALL RESET REL. MUXMODE [9]	I/O VOLTAGE VALUE [10]	POWER [11]	HYS [12]	BUFFER TYPE [13]	PULL UP/DOWN TYPE [14]	DSIS [15]
V5	mmc3_dat4	mmc3_dat4		0	IO	PU	PU	15	1.8/3.3	vddshv7	Yes	Dual Voltage LVCMOS	PU/PD	1
		spi4_sclk		1	IO									0
		uart10_rxd		2	I									1
		usb3_ulpi_nxt		3	I									0
		vin2b_d1		4	I									0
		ehrpwm3A		10	O									
		gpio1_22		14	IO									
		Driver off		15	I									
W6	mmc3_dat5	mmc3_dat5		0	IO	PU	PU	15	1.8/3.3	vddshv7	Yes	Dual Voltage LVCMOS	PU/PD	1
		spi4_d1		1	IO									0
		uart10_txd		2	O									
		usb3_ulpi_dir		3	I									0
		vin2b_d0		4	I									0
		ehrpwm3B		10	O									
		gpio1_23		14	IO									
		Driver off		15	I									
W3	mmc3_dat6	mmc3_dat6		0	IO	PU	PU	15	1.8/3.3	vddshv7	Yes	Dual Voltage LVCMOS	PU/PD	1
		spi4_d0		1	IO									0
		uart10_ctsn		2	I									1
		usb3_ulpi_stp		3	O									
		vin2b_de1		4	I									
		ehrpwm3_tripzone_input		10	IO									0
		gpio1_24		14	IO									
		Driver off		15	I									
V4	mmc3_dat7	mmc3_dat7		0	IO	PU	PU	15	1.8/3.3	vddshv7	Yes	Dual Voltage LVCMOS	PU/PD	1
		spi4_cs0		1	IO									1
		uart10_rtsn		2	O									
		usb3_ulpi_clk		3	I									0
		vin2b_clk1		4	I									
		eCAP3_in_PWM3_out		10	IO									0
		gpio1_25		14	IO									
		Driver off		15	I									
G22	nmin_dsp	nmin_dsp		0	I	PD	PD		1.8/3.3	vddshv3	Yes	Dual Voltage LVCMOS	PU/PD	
AA11	on_off	on_off		0	O	PU	drive 1 (OFF)		1.8/3.3	vddshv5	Yes	BC1833IH HV	PU/PD	
AD10	pcie_rxn0	pcie_rxn0		0	I	OFF	OFF		1.8	vdda_pcie0		SERDES		

Table 4-2. Ball Characteristics(1) (continued)

BALL NUMBER [1]	BALL NAME [2]	SIGNAL NAME [3]	HGx/HAx [4]	MUXMODE [5]	TYPE [6]	BALL RESET STATE [7]	BALL RESET REL. STATE [8]	BALL RESET REL. MUXMODE [9]	I/O VOLTAGE VALUE [10]	POWER [11]	HYS [12]	BUFFER TYPE [13]	PULL UP/DOWN TYPE [14]	DSIS [15]
AE10	pcie_rxp0	pcie_rxp0		0	I	OFF	OFF		1.8	vdda_pcie0		SERDES		
AD11	pcie_txn0	pcie_txn0		0	O				1.8	vdda_pcie0		SERDES		
AE11	pcie_txp0	pcie_txp0		0	O				1.8	vdda_pcie0		SERDES		
F17	porz	porz		0	I				1.8/3.3	vddshv3	Yes	IHHV1833	PU/PD	
H21	resetrn	resetrn		0	I	PU	PU		1.8/3.3	vddshv3	Yes	Dual Voltage LVCMOS	PU/PD	
U2	rgmii0_rxc	rgmii0_rxc		0	I	PD	PD	15	1.8/3.3	vddshv9	Yes	Dual Voltage LVCMOS	PU/PD	0
		rmii1_txen		2	O									0
		mii0_txcclk		3	I									0
		vin2a_d5	Yes / No	4	I									0
		vin4b_d5	Yes / No	5	I									0
		usb4_ulpi_d2		6	IO									0
		gpio5_26		14	IO									
Driver off		15	I											
U3	rgmii0_rxctl	rgmii0_rxctl		0	I	PD	PD	15	1.8/3.3	vddshv9	Yes	Dual Voltage LVCMOS	PU/PD	0
		rmii1_txd1		2	O									
		mii0_txd3		3	O									
		vin2a_d6	Yes / No	4	I									0
		vin4b_d6	Yes / No	5	I									0
		usb4_ulpi_d3		6	IO									0
		gpio5_27		14	IO									
Driver off		15	I											
R4	rgmii0_rxd0	rgmii0_rxd0		0	I	PD	PD	15	1.8/3.3	vddshv9	Yes	Dual Voltage LVCMOS	PU/PD	0
		rmii0_txd0		1	O									
		mii0_txd0		3	O									
		vin2a_fld0	Yes / No	4	I									
		vin4b_fld1	Yes / No	5	I									0
		usb4_ulpi_d7		6	IO									0
		gpio5_31		14	IO									
Driver off		15	I											
T3	rgmii0_rxd1	rgmii0_rxd1		0	I	PD	PD	15	1.8/3.3	vddshv9	Yes	Dual Voltage LVCMOS	PU/PD	0
		rmii0_txd1		1	O									
		mii0_txd1		3	O									
		vin2a_d9	Yes / No	4	I									0
		usb4_ulpi_d6		6	IO									0
		gpio5_30		14	IO									
		Driver off		15	I									

Table 4-2. Ball Characteristics(1) (continued)

BALL NUMBER [1]	BALL NAME [2]	SIGNAL NAME [3]	HGx/HAx [4]	MUXMODE [5]	TYPE [6]	BALL RESET STATE [7]	BALL RESET REL. STATE [8]	BALL RESET REL. MUXMODE [9]	I/O VOLTAGE VALUE [10]	POWER [11]	HYS [12]	BUFFER TYPE [13]	PULL UP/DOWN TYPE [14]	DSIS [15]			
U4	rgmii0_rxd2	rgmii0_rxd2		0	I	PD	PD	15	1.8/3.3	vddshv9	Yes	Dual Voltage LVCMOS	PU/PD	0			
		rmii0_txen		1	O												
		mii0_txen		3	O												
		vin2a_d8	Yes / No	4	I											0	
		usb4_ulpi_d5		6	IO												0
		gpio5_29		14	IO												
		Driver off		15	I												
P5	rgmii0_rxd3	rgmii0_rxd3		0	I	PD	PD	15	1.8/3.3	vddshv9	Yes	Dual Voltage LVCMOS	PU/PD	0			
		rmii1_txd0		2	O												
		mii0_txd2		3	O												
		vin2a_d7	Yes / No	4	I											0	
		vin4b_d7	Yes / No	5	I												0
		usb4_ulpi_d4		6	IO												0
		gpio5_28		14	IO												
Driver off		15	I														
R6	rgmii0_txc	rgmii0_txc		0	O	PD	PD	15	1.8/3.3	vddshv9	Yes	Dual Voltage LVCMOS	PU/PD				
		uart3_ctsn		1	I											1	
		rmii1_rxd1		2	I											0	
		mii0_rxd3		3	I											0	
		vin2a_d3	Yes / No	4	I												0
		vin4b_d3	Yes / No	5	I												0
		usb4_ulpi_clk		6	I												0
		spi3_d0		7	IO												0
		spi4_cs2		8	IO												1
		gpio5_20		14	IO												
		Driver off		15	I												
P6	rgmii0_txctl	rgmii0_txctl		0	O	PD	PD	15	1.8/3.3	vddshv9	Yes	Dual Voltage LVCMOS	PU/PD				
		uart3_rtsn		1	O												
		rmii1_rxd0		2	I											0	
		mii0_rxd2		3	I											0	
		vin2a_d4	Yes / No	4	I												0
		vin4b_d4	Yes / No	5	I												0
		usb4_ulpi_stp		6	O												
		spi3_cs0		7	IO												1
		spi4_cs3		8	IO												1
		gpio5_21		14	IO												
		Driver off		15	I												

Table 4-2. Ball Characteristics(1) (continued)

BALL NUMBER [1]	BALL NAME [2]	SIGNAL NAME [3]	HGx/HAx [4]	MUXMODE [5]	TYPE [6]	BALL RESET STATE [7]	BALL RESET REL. STATE [8]	BALL RESET REL. MUXMODE [9]	I/O VOLTAGE VALUE [10]	POWER [11]	HYS [12]	BUFFER TYPE [13]	PULL UP/DOWN TYPE [14]	DSIS [15]
R5	rgmii0_txd0	rgmii0_txd0		0	O	PD	PD	15	1.8/3.3	vddshv9	Yes	Dual Voltage LVCMOS	PU/PD	
		rmii0_rxd0		1	I									0
		mii0_rxd0		3	I									0
		vin2a_d10	Yes / No	4	I									0
		usb4_ulpi_d1		6	IO									0
		spi4_cs0		7	IO									1
		uart4_rtsn		8	O									
		gpio5_25		14	IO									
		Driver off		15	I									
T4	rgmii0_txd1	rgmii0_txd1		0	O	PD	PD	15	1.8/3.3	vddshv9	Yes	Dual Voltage LVCMOS	PU/PD	
		rmii0_rxd1		1	I									0
		mii0_rxd1		3	I									0
		vin2a_vsync0	Yes / No	4	I									
		vin4b_vsync1	Yes / No	5	I									0
		usb4_ulpi_d0		6	IO									0
		spi4_d0		7	IO									0
		uart4_ctsn		8	IO									1
		gpio5_24		14	IO									
Driver off		15	I											
T6	rgmii0_txd2	rgmii0_txd2		0	O	PD	PD	15	1.8/3.3	vddshv9	Yes	Dual Voltage LVCMOS	PU/PD	
		rmii0_rxer		1	I									0
		mii0_rxer		3	I									0
		vin2a_hsync0	Yes / No	4	I									
		vin4b_hsync1	Yes / No	5	I									0
		usb4_ulpi_nxt		6	I									0
		spi4_d1		7	IO									0
		uart4_txd		8	O									
		gpio5_23		14	IO									
Driver off		15	I											

Table 4-2. Ball Characteristics(1) (continued)

BALL NUMBER [1]	BALL NAME [2]	SIGNAL NAME [3]	HGx/HAx [4]	MUXMODE [5]	TYPE [6]	BALL RESET STATE [7]	BALL RESET REL. STATE [8]	BALL RESET REL. MUXMODE [9]	I/O VOLTAGE VALUE [10]	POWER [11]	HYS [12]	BUFFER TYPE [13]	PULL UP/DOWN TYPE [14]	DSIS [15]
T5	rgmii0_txd3	rgmii0_txd3		0	O	PD	PD	15	1.8/3.3	vddshv9	Yes	Dual Voltage LVCMOS	PU/PD	
		rmii0_crs		1	I									0
		mii0_crs		3	I									0
		vin2a_de0	Yes / No	4	I									0
		vin4b_de1	Yes / No	5	I									0
		usb4_ulpi_dir		6	I									0
		spl4_sclk		7	IO									0
		uart4_rxd		8	I									1
		gpio5_22		14	IO									
	Driver off			15	I									
R2	RMII_MHZ_50_CLK	RMII_MHZ_50_CLK		0	IO	PD	PD	15	1.8/3.3	vddshv9	Yes	Dual Voltage LVCMOS	PU/PD	0
		vin2a_d11	Yes / No	4	I									0
		gpio5_17		14	IO									
		Driver off		15	I									
G21	rstoutn	rstoutn		0	O	PD	drive 1 (OFF)		1.8/3.3	vddshv3	Yes	Dual Voltage LVCMOS	PU/PD	
D19	rtck	rtck		0	O	PU	drive clk (OFF)	0	1.8/3.3	vddshv3	Yes	Dual Voltage LVCMOS	PU/PD	
		gpio8_29		14	IO									
AA9	rtc_iso	rtc_iso		0	I				1.8/3.3	vddshv5	Yes	IHHV1833	PU/PD	
AA13	rtc_osc_xi_clkin32	rtc_osc_xi_clkin32		0	I				1.8	vdda_rtc	No	LVCMOS OSC		
AA12	rtc_osc_xo	rtc_osc_xo		0	O				1.8	vdda_rtc	No	LVCMOS OSC		
AA10	rtc_porz	rtc_porz		0	I				1.8/3.3	vddshv5	Yes	IHHV1833	PU/PD	
D22	spi1_cs0	spi1_cs0		0	IO	PU	PU	15	1.8/3.3	vddshv3	Yes	Dual Voltage LVCMOS	PU/PD	1
		gpio7_10		14	IO									
		Driver off		15	I									
D16	spi1_cs1	spi1_cs1		0	IO	PU	PU	15	1.8/3.3	vddshv3	Yes	Dual Voltage LVCMOS	PU/PD	1
		spi2_cs1		3	IO									1
		gpio7_11		14	IO									
		Driver off		15	I									

Table 4-2. Ball Characteristics(1) (continued)

BALL NUMBER [1]	BALL NAME [2]	SIGNAL NAME [3]	HGX/HAX [4]	MUXMODE [5]	TYPE [6]	BALL RESET STATE [7]	BALL RESET REL. STATE [8]	BALL RESET REL. MUXMODE [9]	I/O VOLTAGE VALUE [10]	POWER [11]	HYS [12]	BUFFER TYPE [13]	PULL UP/DOWN TYPE [14]	DSIS [15]
C19	spi1_cs2	spi1_cs2		0	IO	PU	PU	15	1.8/3.3	vddshv3	Yes	Dual Voltage LVCMOS	PU/PD	1
		uart4_rxd		1	I									1
		mmc3_sdcd		2	I									1
		spi2_cs2		3	IO									1
		dcan2_tx		4	IO									1
		mdio_mclk		5	O									1
		hdmi1_hpd		6	I									
		gpio7_12		14	IO									
	Driver off		15	I										
C24	spi1_cs3	spi1_cs3		0	IO	PU	PU	15	1.8/3.3	vddshv3	Yes	Dual Voltage LVCMOS	PU/PD	1
		uart4_txd		1	O									
		mmc3_sdwp		2	I									0
		spi2_cs3		3	IO									1
		dcan2_rx		4	IO									1
		mdio_d		5	IO									1
		hdmi1_cec		6	IO									
		gpio7_13		14	IO									
	Driver off		15	I										
E22	spi1_d0	spi1_d0		0	IO	PD	PD	15	1.8/3.3	vddshv3	Yes	Dual Voltage LVCMOS	PU/PD	0
		gpio7_9		14	IO									
		Driver off		15	I									
C21	spi1_d1	spi1_d1		0	IO	PD	PD	15	1.8/3.3	vddshv3	Yes	Dual Voltage LVCMOS	PU/PD	0
		gpio7_8		14	IO									
		Driver off		15	I									
C18	spi1_sclk	spi1_sclk		0	IO	PD	PD	15	1.8/3.3	vddshv3	Yes	Dual Voltage LVCMOS	PU/PD	0
		gpio7_7		14	IO									
		Driver off		15	I									
D17	spi2_cs0	spi2_cs0		0	IO	PU	PU	15	1.8/3.3	vddshv3	Yes	Dual Voltage LVCMOS	PU/PD	1
		uart3_rtsn		1	O									
		uart5_txd		2	O									
		gpio7_17		14	IO									
		Driver off		15	I									
E16	spi2_d0	spi2_d0		0	IO	PD	PD	15	1.8/3.3	vddshv3	Yes	Dual Voltage LVCMOS	PU/PD	0
		uart3_ctsn		1	I									1
		uart5_rxd		2	I									1
		gpio7_16		14	IO									
		Driver off		15	I									

Table 4-2. Ball Characteristics(1) (continued)

BALL NUMBER [1]	BALL NAME [2]	SIGNAL NAME [3]	HGx/HAx [4]	MUXMODE [5]	TYPE [6]	BALL RESET STATE [7]	BALL RESET REL. STATE [8]	BALL RESET REL. MUXMODE [9]	I/O VOLTAGE VALUE [10]	POWER [11]	HYS [12]	BUFFER TYPE [13]	PULL UP/DOWN TYPE [14]	DSIS [15]						
F25	spi2_d1	spi2_d1		0	IO	PD	PD	15	1.8/3.3	vddshv3	Yes	Dual Voltage LVCMOS	PU/PD	0						
		uart3_txd		1	O															
		gpio7_15		14	IO															
		Driver off		15	I															
F24	spi2_sclk	spi2_sclk		0	IO	PD	PD	15	1.8/3.3	vddshv3	Yes	Dual Voltage LVCMOS	PU/PD	0						
		uart3_rxd		1	I										1					
		gpio7_14		14	IO															
		Driver off		15	I															
E18	tclk	tclk		0	I	PU	PU	0	1.8/3.3	vddshv3	Yes	IQ1833	PU/PD							
D20	tdi	tdi		0	I	PU	PU	0	1.8/3.3	vddshv3	Yes	Dual Voltage LVCMOS	PU/PD							
		gpio8_27		14	I															
F21	tdo	tdo		0	O	PU	PU	0	1.8/3.3	vddshv3	Yes	Dual Voltage LVCMOS	PU/PD							
		gpio8_28		14	IO															
D18	tms	tms		0	IO	OFF	OFF	0	1.8/3.3	vddshv3	Yes	Dual Voltage LVCMOS	PU/PD							
E17	trstn	trstn		0	I	PD	PD		1.8/3.3	vddshv3	Yes	Dual Voltage LVCMOS	PU/PD							
H25	uart1_ctsn	uart1_ctsn		0	I	PU	PU	15	1.8/3.3	vddshv4	Yes	Dual Voltage LVCMOS	PU/PD	1						
		uart9_rxd		2	I															1
		mmc4_clk		3	IO															1
		gpio7_24		14	IO															
		Driver off		15	I															
H24	uart1_rtsn	uart1_rtsn		0	O	PU	PU	15	1.8/3.3	vddshv4	Yes	Dual Voltage LVCMOS	PU/PD							
		uart9_txd		2	O															
		mmc4_cmd		3	IO															1
		gpio7_25		14	IO															
		Driver off		15	I															
G23	uart1_rxd	uart1_rxd		0	I	PU	PU	15	1.8/3.3	vddshv4	Yes	Dual Voltage LVCMOS	PU/PD	1						
		mmc4_sdcd		3	I															1
		gpio7_22		14	IO															
		Driver off		15	I															
H22	uart1_txd	uart1_txd		0	O	PU	PU	15	1.8/3.3	vddshv4	Yes	Dual Voltage LVCMOS	PU/PD							
		mmc4_sdwp		3	I															0
		gpio7_23		14	IO															
		Driver off		15	I															

Table 4-2. Ball Characteristics(1) (continued)

BALL NUMBER [1]	BALL NAME [2]	SIGNAL NAME [3]	HGx/HAx [4]	MUXMODE [5]	TYPE [6]	BALL RESET STATE [7]	BALL RESET REL. STATE [8]	BALL RESET REL. MUXMODE [9]	I/O VOLTAGE VALUE [10]	POWER [11]	HYS [12]	BUFFER TYPE [13]	PULL UP/DOWN TYPE [14]	DSIS [15]
J22	uart2_ctsn	uart2_ctsn		0	I	PU	PU	15	1.8/3.3	vddshv4	Yes	Dual Voltage LVCMOS	PU/PD	1
		uart3_rxd		2	I									1
		mmc4_dat2		3	IO									1
		uart10_rxd		4	I									1
		uart1_dtrn		5	O									
		gpio1_16		14	IO									
		Driver off		15	I									
J24	uart2_rtsn	uart2_rtsn		0	O	PU	PU	15	1.8/3.3	vddshv4	Yes	Dual Voltage LVCMOS	PU/PD	
		uart3_txd		1	O									
		uart3_irtx		2	O									
		mmc4_dat3		3	IO									1
		uart10_txd		4	O									
		uart1_rin		5	I									1
		gpio1_17		14	IO									
Driver off		15	I											
H23	uart2_rxd	uart3_ctsn		1	I	PU	PU	15	1.8/3.3	vddshv4	Yes	Dual Voltage LVCMOS	PU/PD	1
		uart3_rctx		2	O									
		mmc4_dat0		3	IO									1
		uart2_rxd		4	I									1
		uart1_dcdn		5	I									1
		gpio7_26		14	IO									
		Driver off		15	I									
J25	uart2_txd	uart2_txd		0	O	PU	PU	15	1.8/3.3	vddshv4	Yes	Dual Voltage LVCMOS	PU/PD	
		uart3_rtsn		1	O									
		uart3_sd		2	O									
		mmc4_dat1		3	IO									1
		uart2_txd		4	O									
		uart1_dsrn		5	I									0
		gpio7_27		14	IO									
Driver off		15	I											

Table 4-2. Ball Characteristics(1) (continued)

BALL NUMBER [1]	BALL NAME [2]	SIGNAL NAME [3]	HGx/HAx [4]	MUXMODE [5]	TYPE [6]	BALL RESET STATE [7]	BALL RESET REL. STATE [8]	BALL RESET REL. MUXMODE [9]	I/O VOLTAGE VALUE [10]	POWER [11]	HYS [12]	BUFFER TYPE [13]	PULL UP/DOWN TYPE [14]	DSIS [15]
R1	uart3_rxd	uart3_rxd		0	I	PD	PD	15	1.8/3.3	vddshv9	Yes	Dual Voltage LVCMOS	PU/PD	1
		rmii1_crs		2	I									0
		mii0_rxdv		3	I									0
		vin2a_d1	Yes / No	4	I									0
		vin4b_d1	Yes / No	5	I									0
		spi3_sclk		7	IO									0
		gpio5_18		14	IO									
		Driver off		15	I									
T2	uart3_txd	uart3_txd		0	O	PD	PD	15	1.8/3.3	vddshv9	Yes	Dual Voltage LVCMOS	PU/PD	
		rmii1_rxer		2	I									0
		mii0_rxclk		3	I									0
		vin2a_d2	Yes / No	4	I									0
		vin4b_d2	Yes / No	5	I									0
		spi3_d1		7	IO									0
		spi4_cs1		8	IO									1
		gpio5_19		14	IO									
Driver off		15	I											
AD8	usb1_dm	usb1_dm		0	IO	OFF	OFF		3.3	vdda33v_usb1		USB3PHY		
AE8	usb1_dp	usb1_dp		0	IO	OFF	OFF		3.3	vdda33v_usb1		USB3PHY		
AE6	usb1_drvvbus	usb1_drvvbus		0	O	PD	PD	15	1.8/3.3	vddshv6	Yes	Dual Voltage LVCMOS	PU/PD	
		timer16		7	IO									
		gpio6_12		14	IO									
		Driver off		15	I									
AE9	usb_rxn0	usb_rxn0		0	I	OFF	OFF		1.8	vdda_usb1				
AD9	usb_rxp0	usb_rxp0		0	I	OFF	OFF		1.8	vdda_usb1				
AE7	usb_txn0	usb_txn0		0	O				1.8	vdda_usb1				
AD7	usb_txp0	usb_txp0		0	O				1.8	vdda_usb1				
H10, H13, H14, H9, J19, K19, M12, M13, M14, M9, N12, N13, N14, N15, N9, P10, P12, P15, P16, P9, R10, R12, R15, R16, R8, T11, T12, T13, T15, V18, W14, W15, W16, W18	vdd	vdd												
AB8	vdda33v_usb1	vdda33v_usb1												
L14	vdda_abe_per	vdda_abe_per												

Table 4-2. Ball Characteristics(1) (continued)

BALL NUMBER [1]	BALL NAME [2]	SIGNAL NAME [3]	HGX/HAX [4]	MUXMODE [5]	TYPE [6]	BALL RESET STATE [7]	BALL RESET REL. STATE [8]	BALL RESET REL. MUXMODE [9]	I/O VOLTAGE VALUE [10]	POWER [11]	HYS [12]	BUFFER TYPE [13]	PULL UP/DOWN TYPE [14]	DSIS [15]
P18	vdda_dds	vdda_dds			PWR									
M8	vdda_debug	vdda_debug			PWR									
F12	vdda_dsp_eve	vdda_dsp_eve			PWR									
P14	vdda_gmac_core	vdda_gmac_core			PWR									
Y12	vdda_gpu	vdda_gpu			PWR									
AB16	vdda_hdmi	vdda_hdmi			PWR									
Y15	vdda_iva	vdda_iva			PWR									
N18	vdda_mpu	vdda_mpu			PWR									
AC15	vdda_osc	vdda_osc			PWR									
AC10	vdda_pcie0	vdda_pcie0			PWR									
AC12	vdda_pcie	vdda_pcie			PWR									
AA14	vdda_rtc	vdda_rtc			PWR									
AB10	vdda_usb1	vdda_usb1			PWR									
AB9	vdda_usb3	vdda_usb3			PWR									
P11	vdda_video	vdda_video			PWR									
G10, G11, G17, G18, K8, L8, R18, R19, V8, W8, Y16, Y17, Y8	vdds18v	vdds18v			PWR									
M20, N19, U20, W20	vdds18v_dds1	vdds18v_dds1			PWR									
A2, B1, F7, H8, J2	vddshv1	vddshv1			PWR									
D12, G12, G13, G8, G9	vddshv2	vddshv2			PWR									
B18, B22, D24, F20, G14, G15, G16, G19	vddshv3	vddshv3			PWR									
H20	vddshv4	vddshv4			PWR									
AA8	vddshv5	vddshv5			PWR									
AC4, AD1, AE2, Y9	vddshv6	vddshv6			PWR									
V7, W7	vddshv7	vddshv7			PWR									
N4, R7, T7	vddshv9	vddshv9			PWR									
J7, K7, L7, M7, N7, P7	vddshv10	vddshv10			PWR									
G7, H7	vddshv11	vddshv11			PWR									
AD19, AD22, AD25, AE24, K21, L20, L23, P19, R23, V19, V20, W19, Y18, Y20, Y23	vdds_dds1	vdds_dds1			PWR									

Table 4-2. Ball Characteristics(1) (continued)

BALL NUMBER [1]	BALL NAME [2]	SIGNAL NAME [3]	HGx/HAx [4]	MUXMODE [5]	TYPE [6]	BALL RESET STATE [7]	BALL RESET REL. STATE [8]	BALL RESET REL. MUXMODE [9]	I/O VOLTAGE VALUE [10]	POWER [11]	HYS [12]	BUFFER TYPE [13]	PULL UP/DOWN TYPE [14]	DSIS [15]
H12, J10, J12, J13, J8, J9, K10, K12, K13, K9, L9	vdd_dspeve	vdd_dspeve			PWR									
U10, U11, U12, U8, U9, V10, V11, V12, V13, V9, W11, W12, W9	vdd_gpu	vdd_gpu			PWR									
T17, T18, U17, U18, U19	vdd_iva	vdd_iva			PWR									
H15, H16, H17, H18, H19, J15, J18, K15, K16, K17, K18, L16, L17, L18, L19, M16, M17, M18	vdd_mpu	vdd_mpu			PWR									
Y13	vdd_rtc	vdd_rtc			PWR									
AB6	vin1a_clk0	vin1a_clk0		0	I	PD	PD	15	1.8/3.3	vddshv6	Yes	Dual Voltage LVCMOS	PU/PD	0
		vout3_d16 ⁽⁸⁾	Yes / No	3	O									
		vout3_fld ⁽⁸⁾	Yes / No	4	O									
		gpio2_30		14	IO									
		Driver off		15	I									
AD5	vin1a_d0	vin1a_d0		0	I	PD	PD	15	1.8/3.3	vddshv6	Yes	Dual Voltage LVCMOS	PU/PD	0
		vout3_d7 ⁽⁸⁾	Yes / No	3	O									
		vout3_d23 ⁽⁸⁾	Yes / No	4	O									
		uart8_rxd		5	I									1
		ehrpwm1A		10	O									
		gpio3_4		14	IO									
		Driver off		15	I									
AE5	vin1a_d1	vin1a_d1		0	I	PD	PD	15	1.8/3.3	vddshv6	Yes	Dual Voltage LVCMOS	PU/PD	0
		vout3_d6 ⁽⁸⁾	Yes / No	3	O									
		vout3_d22 ⁽⁸⁾	Yes / No	4	O									
		uart8_txd		5	O									
		ehrpwm1B		10	O									
		gpio3_5		14	IO									
		Driver off		15	I									

Table 4-2. Ball Characteristics(1) (continued)

BALL NUMBER [1]	BALL NAME [2]	SIGNAL NAME [3]	HGx/HAx [4]	MUXMODE [5]	TYPE [6]	BALL RESET STATE [7]	BALL RESET REL. STATE [8]	BALL RESET REL. MUXMODE [9]	I/O VOLTAGE VALUE [10]	POWER [11]	HYS [12]	BUFFER TYPE [13]	PULL UP/DOWN TYPE [14]	DSIS [15]		
AA5	vin1a_d2	vin1a_d2		0	I	PD	PD	15	1.8/3.3	vddshv6	Yes	Dual Voltage LVCMOS	PU/PD	0		
		vout3_d5 ⁽⁶⁾	Yes / No	3	O											
		vout3_d21 ⁽⁶⁾	Yes / No	4	O											
		uart8_ctsn		5	I											1
		ehrpwm1_tripzone_input		10	IO											0
		gpio3_6		14	IO											
		Driver off		15	I											
Y5	vin1a_d3	vin1a_d3		0	I	PD	PD	15	1.8/3.3	vddshv6	Yes	Dual Voltage LVCMOS	PU/PD	0		
		vout3_d4 ⁽⁶⁾	Yes / No	3	O											
		vout3_d20 ⁽⁶⁾	Yes / No	4	O											
		uart8_rtsn		5	O											
		eCAP1_in_PWM1_out		10	IO											0
		gpio3_7		14	IO											
		Driver off		15	I											
AB7	vin1a_d4	vin1a_d4		0	I	PD	PD	15	1.8/3.3	vddshv6	Yes	Dual Voltage LVCMOS	PU/PD	0		
		vout3_d3 ⁽⁶⁾	Yes / No	3	O											
		vout3_d19 ⁽⁶⁾	Yes / No	4	O											
		ehrpwm1_synci		10	I											0
		gpio3_8		14	IO											
		Driver off		15	I											
AE4	vin1a_d5	vin1a_d5		0	I	PD	PD	15	1.8/3.3	vddshv6	Yes	Dual Voltage LVCMOS	PU/PD	0		
		vout3_d2 ⁽⁶⁾	Yes / No	3	O											
		vout3_d18 ⁽⁶⁾	Yes / No	4	O											
		ehrpwm1_synco		10	O											
		gpio3_9		14	IO											
		Driver off		15	I											
AB5	vin1a_d6	vin1a_d6		0	I	PD	PD	15	1.8/3.3	vddshv6	Yes	Dual Voltage LVCMOS	PU/PD	0		
		vout3_d1 ⁽⁶⁾	Yes / No	3	O											
		vout3_d17 ⁽⁶⁾	Yes / No	4	O											
		eQEP2A_in		10	I											0
		gpio3_10		14	IO											
		Driver off		15	I											

Table 4-2. Ball Characteristics(1) (continued)

BALL NUMBER [1]	BALL NAME [2]	SIGNAL NAME [3]	HGx/HAx [4]	MUXMODE [5]	TYPE [6]	BALL RESET STATE [7]	BALL RESET REL. STATE [8]	BALL RESET REL. MUXMODE [9]	I/O VOLTAGE VALUE [10]	POWER [11]	HYS [12]	BUFFER TYPE [13]	PULL UP/DOWN TYPE [14]	DSIS [15]	
AD4	vin1a_d7	vin1a_d7		0	I	PD	PD	15	1.8/3.3	vddshv6	Yes	Dual Voltage LVCMOS	PU/PD	0	
		vout3_d0 ⁽⁶⁾	Yes / No	3	O										
		vout3_d16 ⁽⁶⁾	Yes / No	4	O										
		eQEP2B_in		10	I										0
		gpio3_11		14	IO										
		Driver off		15	I										
AA3	vin1a_d8	vin1a_d8		0	I	PD	PD	15	1.8/3.3	vddshv6	Yes	Dual Voltage LVCMOS	PU/PD	0	
		vin1b_d7		1	I										0
		vout3_d15 ⁽⁶⁾	Yes / No	4	O										
		eQEP2_index		10	IO										0
		gpio3_12		14	IO										
		Driver off		15	I										
Y4	vin1a_d9	vin1a_d9		0	I	PD	PD	15	1.8/3.3	vddshv6	Yes	Dual Voltage LVCMOS	PU/PD	0	
		vin1b_d6		1	I										0
		vout3_d14 ⁽⁶⁾	Yes / No	4	O										
		eQEP2_strobe		10	IO										0
		gpio3_13		14	IO										
		Driver off		15	I										
AE3	vin1a_d10	vin1a_d10		0	I	PD	PD	15	1.8/3.3	vddshv6	Yes	Dual Voltage LVCMOS	PU/PD	0	
		vin1b_d5		1	I										0
		vout3_d13 ⁽⁶⁾	Yes / No	4	O										
		gpio3_14		14	IO										
		Driver off		15	I										
AA4	vin1a_d11	vin1a_d11		0	I	PD	PD	15	1.8/3.3	vddshv6	Yes	Dual Voltage LVCMOS	PU/PD	0	
		vin1b_d4		1	I										0
		vout3_d12 ⁽⁶⁾	Yes / No	4	O										
		gpmc_a23		5	O										
		gpio3_15		14	IO										
		Driver off		15	I										
AD3	vin1a_d12	vin1a_d12		0	I	PD	PD	15	1.8/3.3	vddshv6	Yes	Dual Voltage LVCMOS	PU/PD	0	
		vin1b_d3		1	I										0
		usb3_ulpi_d7		2	IO										0
		vout3_d11 ⁽⁶⁾	Yes / No	4	O										
		gpmc_a24		5	O										
		gpio3_16		14	IO										
		Driver off		15	I										

Table 4-2. Ball Characteristics(1) (continued)

BALL NUMBER [1]	BALL NAME [2]	SIGNAL NAME [3]	HGx/HAx [4]	MUXMODE [5]	TYPE [6]	BALL RESET STATE [7]	BALL RESET REL. STATE [8]	BALL RESET REL. MUXMODE [9]	I/O VOLTAGE VALUE [10]	POWER [11]	HYS [12]	BUFFER TYPE [13]	PULL UP/DOWN TYPE [14]	DSIS [15]
AC3	vin1a_d13	vin1a_d13		0	I	PD	PD	15	1.8/3.3	vddshv6	Yes	Dual Voltage LVCMOS	PU/PD	0
		vin1b_d2		1	I									0
		usb3_ulpi_d6		2	IO									0
		vout3_d10 (6)	Yes / No	4	O									
		gpmc_a25		5	O									
		gpio3_17		14	IO									
		Driver off		15	I									
AD2	vin1a_d14	vin1a_d14		0	I	PD	PD	15	1.8/3.3	vddshv6	Yes	Dual Voltage LVCMOS	PU/PD	0
		vin1b_d1		1	I									0
		usb3_ulpi_d5		2	IO									0
		vout3_d9 (6)	Yes / No	4	O									
		gpmc_a26		5	O									
		gpio3_18		14	IO									
		Driver off		15	I									
AB3	vin1a_d15	vin1a_d15		0	I	PD	PD	15	1.8/3.3	vddshv6	Yes	Dual Voltage LVCMOS	PU/PD	0
		vin1b_d0		1	I									0
		usb3_ulpi_d4		2	IO									0
		vout3_d8 (6)	Yes / No	4	O									
		gpmc_a27		5	O									
		gpio3_19		14	IO									
		Driver off		15	I									
AA2	vin1a_d16	vin1a_d16		0	I	PD	PD	15	1.8/3.3	vddshv6	Yes	Dual Voltage LVCMOS	PU/PD	0
		vin1b_d7		1	I									0
		usb3_ulpi_d3		2	IO									0
		vout3_d7 (6)	Yes / No	4	O									
		vin3a_d0	Yes / No	6	I									0
		gpio3_20		14	IO									
		Driver off		15	I									
AC2	vin1a_d17	vin1a_d17		0	I	PD	PD	15	1.8/3.3	vddshv6	Yes	Dual Voltage LVCMOS	PU/PD	0
		vin1b_d6		1	I									0
		usb3_ulpi_d2		2	IO									0
		vout3_d6 (6)	Yes / No	4	O									
		vin3a_d1	Yes / No	6	I									0
		gpio3_21		14	IO									
		Driver off		15	I									

Table 4-2. Ball Characteristics(1) (continued)

BALL NUMBER [1]	BALL NAME [2]	SIGNAL NAME [3]	HGx/HAx [4]	MUXMODE [5]	TYPE [6]	BALL RESET STATE [7]	BALL RESET REL. STATE [8]	BALL RESET REL. MUXMODE [9]	I/O VOLTAGE VALUE [10]	POWER [11]	HYS [12]	BUFFER TYPE [13]	PULL UP/DOWN TYPE [14]	DSIS [15]
Y3	vin1a_d18	vin1a_d18		0	I	PD	PD	15	1.8/3.3	vddshv6	Yes	Dual Voltage LVCMOS	PU/PD	0
		vin1b_d5		1	I									0
		usb3_ulpi_d1		2	IO									0
		vout3_d5 (6)	Yes / No	4	O									
		vin3a_d2	Yes / No	6	I									0
		gpio3_22		14	IO									
		Driver off		15	I									
AB2	vin1a_d19	vin1a_d19		0	I	PD	PD	15	1.8/3.3	vddshv6	Yes	Dual Voltage LVCMOS	PU/PD	0
		vin1b_d4		1	I									0
		usb3_ulpi_d0		2	IO									0
		vout3_d4 (6)	Yes / No	4	O									
		vin3a_d3	Yes / No	6	I									0
		gpio3_23		14	IO									
		Driver off		15	I									
AB1	vin1a_d20	vin1a_d20		0	I	PD	PD	15	1.8/3.3	vddshv6	Yes	Dual Voltage LVCMOS	PU/PD	0
		vin1b_d3		1	I									0
		usb3_ulpi_nxt		2	I									0
		vout3_d3 (6)	Yes / No	4	O									
		vin3a_d4	Yes / No	6	I									0
		gpio3_24		14	IO									
		Driver off		15	I									
AC1	vin1a_d21	vin1a_d21		0	I	PD	PD	15	1.8/3.3	vddshv6	Yes	Dual Voltage LVCMOS	PU/PD	0
		vin1b_d2		1	I									0
		usb3_ulpi_dir		2	I									0
		vout3_d2 (6)	Yes / No	4	O									
		vin3a_d5	Yes / No	6	I									0
		gpio3_25		14	IO									
		Driver off		15	I									
AA1	vin1a_d22	vin1a_d22		0	I	PD	PD	15	1.8/3.3	vddshv6	Yes	Dual Voltage LVCMOS	PU/PD	0
		vin1b_d1		1	I									0
		usb3_ulpi_stp		2	O									
		vout3_d1 (6)	Yes / No	4	O									
		vin3a_d6	Yes / No	6	I									0
		gpio3_26		14	IO									
		Driver off		15	I									

Table 4-2. Ball Characteristics(1) (continued)

BALL NUMBER [1]	BALL NAME [2]	SIGNAL NAME [3]	HGx/HAx [4]	MUXMODE [5]	TYPE [6]	BALL RESET STATE [7]	BALL RESET REL. STATE [8]	BALL RESET REL. MUXMODE [9]	I/O VOLTAGE VALUE [10]	POWER [11]	HYS [12]	BUFFER TYPE [13]	PULL UP/DOWN TYPE [14]	DSIS [15]
Y2	vin1a_d23	vin1a_d23		0	I	PD	PD	15	1.8/3.3	vddshv6	Yes	Dual Voltage LVCMOS	PU/PD	0
		vin1b_d0		1	I									0
		usb3_ulpi_clk		2	I									0
		vout3_d0 (6)	Yes / No	4	O									
		vin3a_d7	Yes / No	6	I									0
		gpio3_27		14	IO									
		Driver off		15	I									
AA7	vin1a_de0	vin1a_de0		0	I	PD	PD	15	1.8/3.3	vddshv6	Yes	Dual Voltage LVCMOS	PU/PD	0
		vin1b_hsync1		1	I									0
		vout3_d17 (6)	Yes / No	3	O									
		vout3_de (8)	Yes / No	4	O									
		uart7_rxd		5	I									1
		timer16		7	IO									
		spi3_sclk		8	IO									0
		eQEP1A_in		10	I									0
		gpio3_0		14	IO									
		Driver off		15	I									
AD6	vin1a_fld0	vin1a_fld0		0	I	PD	PD	15	1.8/3.3	vddshv6	Yes	Dual Voltage LVCMOS	PU/PD	0
		vin1b_vsync1		1	I									0
		vout3_clk (6)	Yes / No	4	O									
		uart7_txd		5	O									
		timer15		7	IO									
		spi3_d1		8	IO									0
		eQEP1B_in		10	I									0
		gpio3_1		14	IO									
		Driver off		15	I									
AC6	vin1a_hsync0	vin1a_hsync0		0	I	PD	PD	15	1.8/3.3	vddshv6	Yes	Dual Voltage LVCMOS	PU/PD	0
		vin1b_fld1		1	I									0
		vout3_hsync (6)	Yes / No	4	O									
		uart7_ctsn		5	I									1
		timer14		7	IO									
		spi3_d0		8	IO									0
		eQEP1_index		10	IO									0
		gpio3_2		14	IO									
		Driver off		15	I									

Table 4-2. Ball Characteristics(1) (continued)

BALL NUMBER [1]	BALL NAME [2]	SIGNAL NAME [3]	HGx/HAx [4]	MUXMODE [5]	TYPE [6]	BALL RESET STATE [7]	BALL RESET REL. STATE [8]	BALL RESET REL. MUXMODE [9]	I/O VOLTAGE VALUE [10]	POWER [11]	HYS [12]	BUFFER TYPE [13]	PULL UP/DOWN TYPE [14]	DSIS [15]
AC5	vin1a_vsync0	vin1a_vsync0		0	I	PD	PD	15	1.8/3.3	vddshv6	Yes	Dual Voltage LVCMOS	PU/PD	0
		vin1b_de1		1	I									0
		vout3_vsync ⁽⁶⁾	Yes / No	4	O									
		uart7_rtsn		5	O									
		timer13		7	IO									
		spi3_cs0		8	IO									1
		eQEP1_strobe		10	IO									0
		gpio3_3		14	IO									
	Driver off		15	I										
AA6	vin1b_clk1	vin1b_clk1		0	I	PD	PD	15	1.8/3.3	vddshv6	Yes	Dual Voltage LVCMOS	PU/PD	0
		vin3a_clk0	Yes / No	6	I									0
		gpio2_31		14	IO									
			Driver off		15	I								
D4	vin2a_clk0	vin2a_clk0	Yes / No	0	I	PD	PD	15	1.8/3.3	vddshv1	Yes	Dual Voltage LVCMOS	PU/PD	
		vout2_fld	Yes / No	4	O									
		emu5		5	O									
		eQEP1A_in		10	I									0
		gpio3_28		14	IO									
	Driver off		15	I										
C3	vin2a_d0	vin2a_d0	Yes / No	0	I	PD	PD	15	1.8/3.3	vddshv1	Yes	Dual Voltage LVCMOS	PU/PD	0
		vout2_d23	Yes / No	4	O									
		emu10		5	O									
		uart9_ctsn		7	I									1
		spi4_d0		8	IO									0
		ehrpwm1B		10	O									
		gpio4_1		14	IO									
	Driver off		15	I										
B2	vin2a_d1	vin2a_d1	Yes / No	0	I	PD	PD	15	1.8/3.3	vddshv1	Yes	Dual Voltage LVCMOS	PU/PD	0
		vout2_d22	Yes / No	4	O									
		emu11		5	O									
		uart9_rtsn		7	O									
		spi4_cs0		8	IO									1
		ehrpwm1_tripzone_input		10	IO									0
		gpio4_2		14	IO									
	Driver off		15	I										

Table 4-2. Ball Characteristics(1) (continued)

BALL NUMBER [1]	BALL NAME [2]	SIGNAL NAME [3]	HGx/HAx [4]	MUXMODE [5]	TYPE [6]	BALL RESET STATE [7]	BALL RESET REL. STATE [8]	BALL RESET REL. MUXMODE [9]	I/O VOLTAGE VALUE [10]	POWER [11]	HYS [12]	BUFFER TYPE [13]	PULL UP/DOWN TYPE [14]	DSIS [15]			
E7	vin2a_d2	vin2a_d2	Yes / No	0	I	PD	PD	15	1.8/3.3	vddshv1	Yes	Dual Voltage LVCMOS	PU/PD	0			
		vout2_d21	Yes / No	4	O												
		emu12		5	O												
		uart10_rxd		8	I											1	
		eCAP1_in_PWM1_out		10	IO												0
		gpio4_3		14	IO												
		Driver off		15	I												
B3	vin2a_d3	vin2a_d3	Yes / No	0	I	PD	PD	15	1.8/3.3	vddshv1	Yes	Dual Voltage LVCMOS	PU/PD	0			
		vout2_d20	Yes / No	4	O												
		emu13		5	O												
		uart10_txd		8	O												
		ehrpwm1_synci		10	I												0
		gpio4_4		14	IO												
		Driver off		15	I												
A3	vin2a_d4	vin2a_d4	Yes / No	0	I	PD	PD	15	1.8/3.3	vddshv1	Yes	Dual Voltage LVCMOS	PU/PD	0			
		vout2_d19	Yes / No	4	O												
		emu14		5	O												
		uart10_ctsn		8	I												1
		ehrpwm1_synco		10	O												
		gpio4_5		14	IO												
		Driver off		15	I												
C6	vin2a_d5	vin2a_d5	Yes / No	0	I	PD	PD	15	1.8/3.3	vddshv1	Yes	Dual Voltage LVCMOS	PU/PD	0			
		vout2_d18	Yes / No	4	O												
		emu15		5	O												
		uart10_rtsn		8	O												
		eQEP2A_in		10	I												0
		gpio4_6		14	IO												
		Driver off		15	I												
A4	vin2a_d6	vin2a_d6	Yes / No	0	I	PD	PD	15	1.8/3.3	vddshv1	Yes	Dual Voltage LVCMOS	PU/PD	0			
		vout2_d17	Yes / No	4	O												
		emu16		5	O												
		mii1_rxd1		8	I												0
		eQEP2B_in		10	I												0
		gpio4_7		14	IO												
		Driver off		15	I												

Table 4-2. Ball Characteristics(1) (continued)

BALL NUMBER [1]	BALL NAME [2]	SIGNAL NAME [3]	HGx/HAx [4]	MUXMODE [5]	TYPE [6]	BALL RESET STATE [7]	BALL RESET REL. STATE [8]	BALL RESET REL. MUXMODE [9]	I/O VOLTAGE VALUE [10]	POWER [11]	HYS [12]	BUFFER TYPE [13]	PULL UP/DOWN TYPE [14]	DSIS [15]			
B5	vin2a_d7	vin2a_d7	Yes / No	0	I	PD	PD	15	1.8/3.3	vddshv1	Yes	Dual Voltage LVCMOS	PU/PD	0			
		vout2_d16	Yes / No	4	O												
		emu17		5	O												
		mii1_rxd2		8	I											0	
		eQEP2_index		10	IO												0
		gpio4_8		14	IO												
		Driver off		15	I												
C5	vin2a_d8	vin2a_d8	Yes / No	0	I	PD	PD	15	1.8/3.3	vddshv1	Yes	Dual Voltage LVCMOS	PU/PD	0			
		vout2_d15	Yes / No	4	O												
		emu18		5	O												
		mii1_rxd3		8	I											0	
		eQEP2_strobe		10	IO												0
		gpio4_9		14	IO												
		Driver off		15	I												
A7	vin2a_d9	vin2a_d9	Yes / No	0	I	PD	PD	15	1.8/3.3	vddshv1	Yes	Dual Voltage LVCMOS	PU/PD	0			
		vout2_d14	Yes / No	4	O												
		emu19		5	O												
		mii1_rxd0		8	I											0	
		ehrpwm2A		10	O												
		gpio4_10		14	IO												
		Driver off		15	I												
A5	vin2a_d10	vin2a_d10	Yes / No	0	I	PD	PD	15	1.8/3.3	vddshv1	Yes	Dual Voltage LVCMOS	PU/PD	0			
		mdio_mclk		3	O												
		vout2_d13	Yes / No	4	O												
		ehrpwm2B		10	O												
		gpio4_11		14	IO												
		Driver off		15	I												
B6	vin2a_d11	vin2a_d11	Yes / No	0	I	PD	PD	15	1.8/3.3	vddshv1	Yes	Dual Voltage LVCMOS	PU/PD	0			
		mdio_d		3	IO												
		vout2_d12	Yes / No	4	O												
		ehrpwm2_tripzone_input		10	IO												
		gpio4_12		14	IO												
		Driver off		15	I												

Table 4-2. Ball Characteristics(1) (continued)

BALL NUMBER [1]	BALL NAME [2]	SIGNAL NAME [3]	HGx/HAx [4]	MUXMODE [5]	TYPE [6]	BALL RESET STATE [7]	BALL RESET REL. STATE [8]	BALL RESET REL. MUXMODE [9]	I/O VOLTAGE VALUE [10]	POWER [11]	HYS [12]	BUFFER TYPE [13]	PULL UP/DOWN TYPE [14]	DSIS [15]
E8	vin2a_d12	vin2a_d12	Yes / No	0	I	PD	PD	15	1.8/3.3	vddshv1	Yes	Dual Voltage LVCMOS	PU/PD	0
		rgmii1_txc		3	O									
		vout2_d11	Yes / No	4	O									
		mii1_rxc		8	I									0
		eCAP2_in_PWM2_out		10	IO									0
		gpio4_13		14	IO									
		Driver off		15	I									
A6	vin2a_d13	vin2a_d13	Yes / No	0	I	PD	PD	15	1.8/3.3	vddshv1	Yes	Dual Voltage LVCMOS	PU/PD	0
		rgmii1_txc		3	O									
		vout2_d10	Yes / No	4	O									
		mii1_rxd		8	I									0
		eQEP3A_in		10	I									0
		gpio4_14		14	IO									
		Driver off		15	I									
C7	vin2a_d14	vin2a_d14	Yes / No	0	I	PD	PD	15	1.8/3.3	vddshv1	Yes	Dual Voltage LVCMOS	PU/PD	0
		rgmii1_txc		3	O									
		vout2_d9	Yes / No	4	O									
		mii1_txc		8	I									0
		eQEP3B_in		10	I									0
		gpio4_15		14	IO									
		Driver off		15	I									
D6	vin2a_d15	vin2a_d15	Yes / No	0	I	PD	PD	15	1.8/3.3	vddshv1	Yes	Dual Voltage LVCMOS	PU/PD	0
		rgmii1_txc		3	O									
		vout2_d8	Yes / No	4	O									
		mii1_txd		8	O									
		eQEP3_index		10	IO									0
		gpio4_16		14	IO									
		Driver off		15	I									
B7	vin2a_d16	vin2a_d16	Yes / No	0	I	PD	PD	15	1.8/3.3	vddshv1	Yes	Dual Voltage LVCMOS	PU/PD	0
		vin2b_d7		2	I									0
		rgmii1_txc		3	O									
		vout2_d7	Yes / No	4	O									
		vin3a_d8	Yes / No	6	I									0
		mii1_txd		8	O									
		eQEP3_strobe		10	IO									0
		gpio4_24		14	IO									
		Driver off		15	I									

Table 4-2. Ball Characteristics(1) (continued)

BALL NUMBER [1]	BALL NAME [2]	SIGNAL NAME [3]	HGx/HAx [4]	MUXMODE [5]	TYPE [6]	BALL RESET STATE [7]	BALL RESET REL. STATE [8]	BALL RESET REL. MUXMODE [9]	I/O VOLTAGE VALUE [10]	POWER [11]	HYS [12]	BUFFER TYPE [13]	PULL UP/DOWN TYPE [14]	DSIS [15]
B8	vin2a_d17	vin2a_d17	Yes / No	0	I	PD	PD	15	1.8/3.3	vddshv1	Yes	Dual Voltage LVCMOS	PU/PD	0
		vin2b_d6		2	I									0
		rgmii1_txd0		3	O									
		vout2_d6	Yes / No	4	O									
		vin3a_d9	Yes / No	6	I									0
		mii1_txd2		8	O									
		ehrpwm3A		10	O									
		gpio4_25		14	IO									
	Driver off			15	I									
A8	vin2a_d18	vin2a_d18	Yes / No	0	I	PD	PD	15	1.8/3.3	vddshv1	Yes	Dual Voltage LVCMOS	PU/PD	0
		vin2b_d5		2	I									0
		rgmii1_rxc		3	I									0
		vout2_d5	Yes / No	4	O									
		vin3a_d10	Yes / No	6	I									0
		mii1_txd3		8	O									
		ehrpwm3B		10	O									
		gpio4_26		14	IO									
	Driver off			15	I									
D7	vin2a_d19	vin2a_d19	Yes / No	0	I	PD	PD	15	1.8/3.3	vddshv1	Yes	Dual Voltage LVCMOS	PU/PD	0
		vin2b_d4		2	I									0
		rgmii1_rxtl		3	I									0
		vout2_d4	Yes / No	4	O									
		vin3a_d11	Yes / No	6	I									0
		mii1_txer		8	O									0
		ehrpwm3_tripzone_input		10	IO									0
		gpio4_27		14	IO									
	Driver off			15	I									
C8	vin2a_d20	vin2a_d20	Yes / No	0	I	PD	PD	15	1.8/3.3	vddshv1	Yes	Dual Voltage LVCMOS	PU/PD	0
		vin2b_d3		2	I									0
		rgmii1_rxd3		3	I									0
		vout2_d3	Yes / No	4	O									
		vin3a_de0	Yes / No	5	I									0
		vin3a_d12	Yes / No	6	I									0
		mii1_rxer		8	I									0
		eCAP3_in_PWM3_out		10	IO									0
gpio4_28		14	IO											
	Driver off			15	I									

Table 4-2. Ball Characteristics(1) (continued)

BALL NUMBER [1]	BALL NAME [2]	SIGNAL NAME [3]	HGx/HAx [4]	MUXMODE [5]	TYPE [6]	BALL RESET STATE [7]	BALL RESET REL. STATE [8]	BALL RESET REL. MUXMODE [9]	I/O VOLTAGE VALUE [10]	POWER [11]	HYS [12]	BUFFER TYPE [13]	PULL UP/DOWN TYPE [14]	DSIS [15]		
D8	vin2a_d21	vin2a_d21	Yes / No	0	I	PD	PD	15	1.8/3.3	vddshv1	Yes	Dual Voltage LVCMOS	PU/PD	0		
		vin2b_d2		2	I									0		
		rgmii1_rxd2		3	I									0		
		vout2_d2	Yes / No	4	O											
		vin3a_fld0	Yes / No	5	I										0	
		vin3a_d13	Yes / No	6	I										0	
		mii1_col		8	I										0	
		gpio4_29		14	IO											
		Driver off		15	I											
F8	vin2a_d22	vin2a_d22	Yes / No	0	I	PD	PD	15	1.8/3.3	vddshv1	Yes	Dual Voltage LVCMOS	PU/PD	0		
		vin2b_d1		2	I										0	
		rgmii1_rxd1		3	I										0	
		vout2_d1	Yes / No	4	O											
		vin3a_hsync0	Yes / No	5	I											0
		vin3a_d14	Yes / No	6	I											0
		mii1_crs		8	I											0
		gpio4_30		14	IO											
		Driver off		15	I											
E9	vin2a_d23	vin2a_d23	Yes / No	0	I	PD	PD	15	1.8/3.3	vddshv1	Yes	Dual Voltage LVCMOS	PU/PD	0		
		vin2b_d0		2	I										0	
		rgmii1_rxd0		3	I										0	
		vout2_d0	Yes / No	4	O											
		vin3a_vsync0	Yes / No	5	I											0
		vin3a_d15	Yes / No	6	I											0
		mii1_txen		8	O											
		gpio4_31		14	IO											
		Driver off		15	I											
B4	vin2a_de0	vin2a_de0	Yes / No	0	I	PD	PD	15	1.8/3.3	vddshv1	Yes	Dual Voltage LVCMOS	PU/PD			
		vin2a_fld0	Yes / No	1	I											
		vin2b_fld1		2	I											
		vin2b_de1		3	I											
		vout2_de	Yes / No	4	O											
		emu6		5	O											
		eQEP1B_in		10	I											0
		gpio3_29		14	IO											
		Driver off		15	I											

Table 4-2. Ball Characteristics(1) (continued)

BALL NUMBER [1]	BALL NAME [2]	SIGNAL NAME [3]	HGx/HAx [4]	MUXMODE [5]	TYPE [6]	BALL RESET STATE [7]	BALL RESET REL. STATE [8]	BALL RESET REL. MUXMODE [9]	I/O VOLTAGE VALUE [10]	POWER [11]	HYS [12]	BUFFER TYPE [13]	PULL UP/DOWN TYPE [14]	DSIS [15]
E6	vin2a_fld0	vin2a_fld0	Yes / No	0	I	PD	PD	15	1.8/3.3	vddshv1	Yes	Dual Voltage LVCMOS	PU/PD	
		vin2b_clk1		2	I									
		vout2_clk	Yes / No	4	O									
		emu7		5	O									
		eQEP1_index		10	IO									0
		gpio3_30		14	IO									
		Driver off		15	I									
D5	vin2a_hsync0	vin2a_hsync0	Yes / No	0	I	PD	PD	15	1.8/3.3	vddshv1	Yes	Dual Voltage LVCMOS	PU/PD	
		vin2b_hsync1		3	I									
		vout2_hsync	Yes / No	4	O									
		emu8		5	O									
		uart9_rxd		7	I									1
		spi4_sclk		8	IO									0
		eQEP1_strobe		10	IO									0
		gpio3_31		14	IO									
Driver off		15	I											
C4	vin2a_vsync0	vin2a_vsync0	Yes / No	0	I	PD	PD	15	1.8/3.3	vddshv1	Yes	Dual Voltage LVCMOS	PU/PD	
		vin2b_vsync1		3	I									
		vout2_vsync	Yes / No	4	O									
		emu9		5	O									
		uart9_txd		7	O									
		spi4_d1		8	IO									0
		ehrpwm1A		10	O									
		gpio4_0		14	IO									
Driver off		15	I											
D10	vout1_clk	vout1_clk		0	O	PD	PD	15	1.8/3.3	vddshv2	Yes	Dual Voltage LVCMOS	PU/PD	
		vin3a_fld0	Yes / No	4	I									0
		spi3_cs0		8	IO									1
		gpio4_19		14	IO									
		Driver off		15	I									
B9	vout1_d0	vout1_d0		0	O	PD	PD	15	1.8/3.3	vddshv2	Yes	Dual Voltage LVCMOS	PU/PD	
		uart5_rxd		2	I									1
		vin3a_d16	Yes / No	4	I									0
		spi3_cs2		8	IO									1
		gpio8_0		14	IO									
		Driver off		15	I									

Table 4-2. Ball Characteristics(1) (continued)

BALL NUMBER [1]	BALL NAME [2]	SIGNAL NAME [3]	HGx/HAx [4]	MUXMODE [5]	TYPE [6]	BALL RESET STATE [7]	BALL RESET REL. STATE [8]	BALL RESET REL. MUXMODE [9]	I/O VOLTAGE VALUE [10]	POWER [11]	HYS [12]	BUFFER TYPE [13]	PULL UP/DOWN TYPE [14]	DSIS [15]	
A9	vout1_d1	vout1_d1		0	O	PD	PD	15	1.8/3.3	vddshv2	Yes	Dual Voltage LVCMOS	PU/PD		
		uart5_txd		2	O										
		vin3a_d17	Yes / No	4	I										0
		gpio8_1		14	IO										
		Driver off		15	I										
A11	vout1_d2	vout1_d2		0	O	PD	PD	15	1.8/3.3	vddshv2	Yes	Dual Voltage LVCMOS	PU/PD		
		emu2		2	O										
		vin3a_d18	Yes / No	4	I										0
		obs0		5	O										
		obs16		6	O										
		obs_irq1		7	O										
		gpio8_2		14	IO										
Driver off		15	I												
C9	vout1_d3	vout1_d3		0	O	PD	PD	15	1.8/3.3	vddshv2	Yes	Dual Voltage LVCMOS	PU/PD		
		emu5		2	O										
		vin3a_d19	Yes / No	4	I										0
		obs1		5	O										
		obs17		6	O										
		obs_dmarq1		7	O										
		gpio8_3		14	IO										
Driver off		15	I												
A13	vout1_d4	vout1_d4		0	O	PD	PD	15	1.8/3.3	vddshv2	Yes	Dual Voltage LVCMOS	PU/PD		
		emu6		2	O										
		vin3a_d20	Yes / No	4	I										0
		obs2		5	O										
		obs18		6	O										
		gpio8_4		14	IO										
Driver off		15	I												
A12	vout1_d5	vout1_d5		0	O	PD	PD	15	1.8/3.3	vddshv2	Yes	Dual Voltage LVCMOS	PU/PD		
		emu7		2	O										
		vin3a_d21	Yes / No	4	I										0
		obs3		5	O										
		obs19		6	O										
		gpio8_5		14	IO										
Driver off		15	I												

Table 4-2. Ball Characteristics(1) (continued)

BALL NUMBER [1]	BALL NAME [2]	SIGNAL NAME [3]	HGx/HAx [4]	MUXMODE [5]	TYPE [6]	BALL RESET STATE [7]	BALL RESET REL. STATE [8]	BALL RESET REL. MUXMODE [9]	I/O VOLTAGE VALUE [10]	POWER [11]	HYS [12]	BUFFER TYPE [13]	PULL UP/DOWN TYPE [14]	DSIS [15]
B14	vout1_d6	vout1_d6		0	O	PD	PD	15	1.8/3.3	vddshv2	Yes	Dual Voltage LVCMOS	PU/PD	
		emu8		2	O									
		vin3a_d22	Yes / No	4	I									0
		obs4		5	O									
		obs20		6	O									
		gpio8_6		14	IO									
		Driver off		15	I									
B13	vout1_d7	vout1_d7		0	O	PD	PD	15	1.8/3.3	vddshv2	Yes	Dual Voltage LVCMOS	PU/PD	
		emu9		2	O									
		vin3a_d23	Yes / No	4	I									0
		gpio8_7		14	IO									
		Driver off		15	I									
A14	vout1_d8	vout1_d8		0	O	PD	PD	15	1.8/3.3	vddshv2	Yes	Dual Voltage LVCMOS	PU/PD	
		uart6_rxd		2	I									1
		vin3a_d8	Yes / No	4	I									0
		gpio8_8		14	IO									
		Driver off		15	I									
B11	vout1_d9	vout1_d9		0	O	PD	PD	15	1.8/3.3	vddshv2	Yes	Dual Voltage LVCMOS	PU/PD	
		uart6_txd		2	O									
		vin3a_d9	Yes / No	4	I									0
		gpio8_9		14	IO									
		Driver off		15	I									
B12	vout1_d10	vout1_d10		0	O	PD	PD	15	1.8/3.3	vddshv2	Yes	Dual Voltage LVCMOS	PU/PD	
		emu3		2	O									
		vin3a_d10	Yes / No	4	I									0
		obs5		5	O									
		obs21		6	O									
		obs_irq2		7	O									
		gpio8_10		14	IO									
		Driver off		15	I									

Table 4-2. Ball Characteristics(1) (continued)

BALL NUMBER [1]	BALL NAME [2]	SIGNAL NAME [3]	HGx/HAx [4]	MUXMODE [5]	TYPE [6]	BALL RESET STATE [7]	BALL RESET REL. STATE [8]	BALL RESET REL. MUXMODE [9]	I/O VOLTAGE VALUE [10]	POWER [11]	HYS [12]	BUFFER TYPE [13]	PULL UP/DOWN TYPE [14]	DSIS [15]
B10	vout1_d11	vout1_d11		0	O	PD	PD	15	1.8/3.3	vddshv2	Yes	Dual Voltage LVCMOS	PU/PD	
		emu10		2	O									
		vin3a_d11	Yes / No	4	I									0
		obs6		5	O									
		obs22		6	O									
		obs_dmarq2		7	O									
		gpio8_11		14	IO									
		Driver off		15	I									
C14	vout1_d12	vout1_d12		0	O	PD	PD	15	1.8/3.3	vddshv2	Yes	Dual Voltage LVCMOS	PU/PD	
		emu11		2	O									
		vin3a_d12	Yes / No	4	I									0
		obs7		5	O									
		obs23		6	O									
		gpio8_12		14	IO									
		Driver off		15	I									
		C10	vout1_d13	vout1_d13		0	O	PD	PD	15	1.8/3.3			vddshv2
emu12				2	O									
vin3a_d13	Yes / No			4	I							0		
obs8				5	O									
obs24				6	O									
gpio8_13				14	IO									
Driver off				15	I									
A10	vout1_d14			vout1_d14		0	O	PD	PD	15	1.8/3.3	vddshv2	Yes	Dual Voltage LVCMOS
		emu13		2	O									
		vin3a_d14	Yes / No	4	I							0		
		obs9		5	O									
		obs25		6	O									
		gpio8_14		14	IO									
		Driver off		15	I									
		C13	vout1_d15	vout1_d15		0	O	PD	PD	15	1.8/3.3	vddshv2	Yes	
emu14				2	O									
vin3a_d15	Yes / No			4	I							0		
obs10				5	O									
obs26				6	O									
gpio8_15				14	IO									
Driver off				15	I									

Table 4-2. Ball Characteristics(1) (continued)

BALL NUMBER [1]	BALL NAME [2]	SIGNAL NAME [3]	HGx/HAx [4]	MUXMODE [5]	TYPE [6]	BALL RESET STATE [7]	BALL RESET REL. STATE [8]	BALL RESET REL. MUXMODE [9]	I/O VOLTAGE VALUE [10]	POWER [11]	HYS [12]	BUFFER TYPE [13]	PULL UP/DOWN TYPE [14]	DSIS [15]
C11	vout1_d16	vout1_d16		0	O	PD	PD	15	1.8/3.3	vddshv2	Yes	Dual Voltage LVCMOS	PU/PD	
		uart7_rxd		2	I									1
		vin3a_d0	Yes / No	4	I									0
		gpio8_16		14	IO									
		Driver off		15	I									
E10	vout1_d17	vout1_d17		0	O	PD	PD	15	1.8/3.3	vddshv2	Yes	Dual Voltage LVCMOS	PU/PD	
		uart7_txd		2	O									
		vin3a_d1	Yes / No	4	I									0
		gpio8_17		14	IO									
		Driver off		15	I									
D15	vout1_d18	vout1_d18		0	O	PD	PD	15	1.8/3.3	vddshv2	Yes	Dual Voltage LVCMOS	PU/PD	
		emu4		2	O									
		vin3a_d2	Yes / No	4	I									0
		obs11		5	O									
		obs27		6	O									
		gpio8_18		14	IO									
E15	vout1_d19	vout1_d19		0	O	PD	PD	15	1.8/3.3	vddshv2	Yes	Dual Voltage LVCMOS	PU/PD	
		emu15		2	O									
		vin3a_d3	Yes / No	4	I									0
		obs12		5	O									
		obs28		6	O									
		gpio8_19		14	IO									
		Driver off		15	I									
D9	vout1_d20	vout1_d20		0	O	PD	PD	15	1.8/3.3	vddshv2	Yes	Dual Voltage LVCMOS	PU/PD	
		emu16		2	O									
		vin3a_d4	Yes / No	4	I									0
		obs13		5	O									
		obs29		6	O									
		gpio8_20		14	IO									
		Driver off		15	I									

Table 4-2. Ball Characteristics(1) (continued)

BALL NUMBER [1]	BALL NAME [2]	SIGNAL NAME [3]	HGX/HAX [4]	MUXMODE [5]	TYPE [6]	BALL RESET STATE [7]	BALL RESET REL. STATE [8]	BALL RESET REL. MUXMODE [9]	I/O VOLTAGE VALUE [10]	POWER [11]	HYS [12]	BUFFER TYPE [13]	PULL UP/DOWN TYPE [14]	DSIS [15]
E14	vout1_d21	vout1_d21		0	O	PD	PD	15	1.8/3.3	vddshv2	Yes	Dual Voltage LVCMOS	PU/PD	
		emu17		2	O									
		vin3a_d5	Yes / No	4	I									0
		obs14		5	O									
		obs30		6	O									
		gpio8_21		14	IO									
		Driver off		15	I									
D14	vout1_d22	vout1_d22		0	O	PD	PD	15	1.8/3.3	vddshv2	Yes	Dual Voltage LVCMOS	PU/PD	
		emu18		2	O									
		vin3a_d6	Yes / No	4	I									0
		obs15		5	O									
		obs31		6	O									
		gpio8_22		14	IO									
		Driver off		15	I									
D11	vout1_d23	vout1_d23		0	O	PD	PD	15	1.8/3.3	vddshv2	Yes	Dual Voltage LVCMOS	PU/PD	
		emu19		2	O									
		vin3a_d7	Yes / No	4	I									0
		spi3_cs3		8	IO									1
		gpio8_23		14	IO									
		Driver off		15	I									
D13	vout1_de	vout1_de		0	O	PD	PD	15	1.8/3.3	vddshv2	Yes	Dual Voltage LVCMOS	PU/PD	
		vin3a_de0	Yes / No	4	I									0
		spi3_d1		8	IO									0
		gpio4_20		14	IO									
		Driver off		15	I									
E11	vout1_fld	vout1_fld		0	O	PD	PD	15	1.8/3.3	vddshv2	Yes	Dual Voltage LVCMOS	PU/PD	
		vin3a_clk0	Yes / No	4	I									0
		spi3_cs1		8	IO									1
		gpio4_21		14	IO									
		Driver off		15	I									
E12	vout1_hsync	vout1_hsync		0	O	PD	PD	15	1.8/3.3	vddshv2	Yes	Dual Voltage LVCMOS	PU/PD	
		vin3a_hsync0	Yes / No	4	I									0
		spi3_d0		8	IO									0
		gpio4_22		14	IO									
		Driver off		15	I									

Table 4-2. Ball Characteristics(1) (continued)

BALL NUMBER [1]	BALL NAME [2]	SIGNAL NAME [3]	HGx/HAx [4]	MUXMODE [5]	TYPE [6]	BALL RESET STATE [7]	BALL RESET REL. STATE [8]	BALL RESET REL. MUXMODE [9]	I/O VOLTAGE VALUE [10]	POWER [11]	HYS [12]	BUFFER TYPE [13]	PULL UP/DOWN TYPE [14]	DSIS [15]
E13	vout1_vsync	vout1_vsync		0	O	PD	PD	15	1.8/3.3	vddshv2	Yes	Dual Voltage LVCMOS	PU/PD	
		vin3a_vsync0	Yes / No	4	I									0
		spi3_sclk		8	IO									0
		gpio4_23		14	IO									
		Driver off		15	I									
A1, A18, A22, A25, AA23, AB4, AC19, AC8, AE1, AE22, AE25, C12, D25, F10, F14, F19, F6, G20, H11, J1, J11, J14, J16, J17, J20, K11, K14, K20, L10, L11, L12, L13, L15, M10, M11, M15, M19, M23, N10, N11, N16, N17, N8, P13, P17, P4, P8, R11, R14, R17, R9, T10, T14, T16, T19, T23, T8, T9, U13, U14, U15, U16, U7, V14, V15, V16, V17, W10, W13, W17, Y10, Y19, Y6	vss	vss			GND									
AC16	vssa_hdmi	vssa_hdmi			GND									
AB15	vssa_osc0	vssa_osc0			GND									
AB12	vssa_osc1	vssa_osc1			GND									
AB11, AC11	vssa_pcie	vssa_pcie			GND									
AC7	vssa_usb	vssa_usb			GND									
AC9	vssa_usb3	vssa_usb3			GND									
R13	vssa_video	vssa_video			GND									
AA16	Wakeup0	Wakeup0		0	I	OFF	OFF	15	1.8/3.3	vddshv5	Yes	IHHV1833	PU/PD	
		dcan1_rx		1	I									1
		gpio1_0		14	I									
		Driver off		15	I									
AA17	Wakeup1	Wakeup1		0	I	OFF	OFF	15	1.8/3.3	vddshv5	Yes	IHHV1833	PU/PD	
		dcan2_rx		1	I									1
		gpio1_1		14	I									
		Driver off		15	I									
AB17	Wakeup2	Wakeup2		0	I	OFF	OFF	15	1.8/3.3	vddshv5	Yes	IHHV1833	PU/PD	
		sys_nirq2		1	I									
		gpio1_2		14	I									
		Driver off		15	I									

Table 4-2. Ball Characteristics(1) (continued)

BALL NUMBER [1]	BALL NAME [2]	SIGNAL NAME [3]	HGX/HAX [4]	MUXMODE [5]	TYPE [6]	BALL RESET STATE [7]	BALL RESET REL. STATE [8]	BALL RESET REL. MUXMODE [9]	I/O VOLTAGE VALUE [10]	POWER [11]	HYS [12]	BUFFER TYPE [13]	PULL UP/DOWN TYPE [14]	DSIS [15]
AC17	Wakeup3	Wakeup3		0	I	OFF	OFF	15	1.8/3.3	vddshv5	Yes	IHHV1833	PU/PD	
		sys_nirq1		1	I									
		gpio1_3		14	I									
		Driver off		15	I									
AC14	xi_osc0	xi_osc0		0	I				1.8	vdda_osc	No	LVC MOS Analog		
AC13	xi_osc1	xi_osc1		0	I				1.8	vdda_osc	No	LVC MOS Analog		
AB14	xo_osc0	xo_osc0		0	O				1.8	vdda_osc	No	LVC MOS Analog		
AB13	xo_osc1	xo_osc1		0	A				1.8	vdda_osc	No	LVC MOS Analog		
C23	xref_clk0	xref_clk0		0	I	PD	PD	15	1.8/3.3	vddshv3	Yes	Dual Voltage LVC MOS	PU/PD	
		mcasp2_axr8		1	IO									0
		mcasp1_axr4		2	IO									0
		mcasp1_ahclkx		3	O									
		mcasp5_ahclkx		4	O									
		clkout2		9	O									
		timer13		10	IO									
		gpio6_17		14	IO									
		Driver off		15	I									
C22	xref_clk1	xref_clk1		0	I	PD	PD	15	1.8/3.3	vddshv3	Yes	Dual Voltage LVC MOS	PU/PD	
		mcasp2_axr9		1	IO									0
		mcasp1_axr5		2	IO									0
		mcasp2_ahclkx		3	O									
		mcasp6_ahclkx		4	O									
		timer14		10	IO									
		gpio6_18		14	IO									
		Driver off		15	I									

(1) NA in this table stands for Not Applicable.

(2) For more information on recommended operating conditions, see [Table 5-4, Recommended Operating Conditions](#).

(3) The pullup or pulldown block strength is equal to: minimum = 50 μ A, typical = 100 μ A, maximum = 250 μ A.

(4) The output impedance settings of this IO cell are programmable; by default, the value is DS[1:0] = 10, this means 40 Ω . For more information on DS[1:0] register configuration, see the Device TRM.

(5) IO drive strength for usb1_dp, usb1_dm, usb2_dp and usb2_dm: minimum 18.3 mA, maximum 89 mA (for a power supply vdda33v_usb1 = 3.46 V).

(6) Minimum PU = 900 Ω , maximum PU = 3.090 k Ω and minimum PD = 14.25 k Ω , maximum PD = 24.8 k Ω .
For more information, see chapter 7 of the USB2.0 specification, in particular section Signaling / Device Speed Identification.

(7) In PUx / PDy, x and y = 60 to 200 μ A.

The output impedance settings (or drive strengths) of this IO are programmable (34 Ω, 40 Ω, 48 Ω, 60 Ω, 80 Ω) depending on the values of the I[2:0] registers.

- (8) The VOUT3 interface when multiplexed onto balls mapped to the VDDSHV6 supply rail is restricted to operating in 1.8V mode only (i.e., VDDSHV6 must be supplied with 1.8V). 3.3V mode is not supported. This must be considered in the pin mux programming and VDDSHVx supply connections.
- (9) The internal pull resistors for balls C2, D3, D2, D1, E2, E3, E4, F3 are permanently disabled when sysboot15 is set to 1 as described in the section *Sysboot Configuration* of the Device TRM. If internal pull-up/down resistors are desired on these balls then sysboot15 should be set to 0. If gpmc boot mode is used with SYSBOOT15=1 (not recommended) then external pull-downs should be implemented to keep the address bus at logic-0 value during boot since the gpmc ms-address bits are high-z during boot.

4.3 Multiplexing Characteristics

Table 4-3 describes the device multiplexing (no characteristics are available in this table).

NOTE

This table doesn't take into account subsystem multiplexing signals. Subsystem multiplexing signals are described in [Section 4.4, Signal Descriptions](#).

NOTE

For more information, see the Control Module / Control Module Functional Description / PAD Functional Multiplexing and Configuration section of the Device TRM.

NOTE

Configuring two pins to the same input signal is not supported as it can yield unexpected results. This can be easily prevented with the proper software configuration (Hi-Z mode is not an input signal).

NOTE

When a pad is set into a multiplexing mode which is not defined by pin multiplexing, that pad's behavior is undefined. This should be avoided.

CAUTION

The I/O timings provided in [Section 7 Timing Requirements and Switching Characteristics](#) are valid only if signals within a single IOSET are used. The IOSETs are defined in the corresponding tables.

Table 4-3. Multiplexing Characteristics

ADDRESS	REGISTER NAME	BALL NUMBER	MUXMODE FIELD SETTINGS (CTRL_CORE_PAD_ *[3:0])												
			0	1	2	3	4	5	6	7	8	9	10	14	15
		P25	ddr1_dqs3												
		P21	ddr1_dqm3												
		AE15	hdmi1_data1y												
		AE7	usb_txn0												
		U25	ddr1_dqs2												
		AA20	ddr1_dqm0												
		V25	ddr1_dqs1												
		T25	ddr1_d23												
		N21	ddr1_d24												
		AB25	ddr1_a11												
		AE9	usb_rxn0												
		W23	ddr1_d10												
		AC24	ddr1_nck												
		AD16	hdmi1_data2x												
		F17	porz												
		AD18	ddr1_a15												
		AE19	ddr1_rasn												
		AC20	ddr1_a5												
		U21	ddr1_dqm1												
		AA24	ddr1_dqs0												
		K25	ddr1_dqs_ecc												
		R21	ddr1_d21												
		L24	ddr1_ecc_d5												
		L22	ddr1_ecc_d3												
		AD8	usb1_dm												
		AB21	ddr1_vref0												
		K22	ddr1_dqm_ecc												
		AC14	xi_osc0												
		V22	ddr1_d12												
		AA9	rtc_iso												
		AA12	rtc_osc_xo												
		AC18	ddr1_casn												
		AE11	pcie_txp0												
		R25	ddr1_d19												
		Y24	ddr1_d1												
		Y21	ddr1_d0												
		W21	ddr1_d8												

Table 4-3. Multiplexing Characteristics (continued)

ADDRESS	REGISTER NAME	BALL NUMBER	MUXMODE FIELD SETTINGS (CTRL_CORE_PAD_*[3:0])														
			0	1	2	3	4	5	6	7	8	9	10	14	15		
		AA25	ddr1_dqs0														
		AD20	ddr1_rst														
		AB20	ddr1_a8														
		N25	ddr1_d25														
		AD13	hdmi1_clockx														
		AD14	hdmi1_data0x														
		AC25	ddr1_ck														
		AB23	ddr1_a9														
		U22	ddr1_d15														
		AB24	ddr1_a12														
		AE16	hdmi1_data2y														
		L21	ddr1_ecc_d7														
		T22	ddr1_d22														
		T21	ddr1_d18														
		V21	ddr1_d13														
		AA19	ddr1_a7														
		AB19	ddr1_cke														
		AE10	pcie_rxp0														
		AC21	ddr1_a4														
		M24	ddr1_ecc_d1														
		AD17	ddr1_a13														
		N24	ddr1_d26														
		AD23	ddr1_odt0														
		AD9	usb_rxp0														
		V24	ddr1_dqs1														
		K23	ddr1_ecc_d4														
		M21	ddr1_d30														
		AB14	xo_osc0														
		U23	ddr1_d14														
		AD24	ddr1_a2														
		AC22	ddr1_csn0														
		AE21	ddr1_ba1														
		AD7	usb_txp0														
		AE23	ddr1_ba2														
		AD21	ddr1_wen														
		Y25	ddr1_d5														
		AE17	ddr1_a14														
		W22	ddr1_d9														
		V23	ddr1_d11														

Table 4-3. Multiplexing Characteristics (continued)

ADDRESS	REGISTER NAME	BALL NUMBER	MUXMODE FIELD SETTINGS (CTRL_CORE_PAD_*[3:0])														
			0	1	2	3	4	5	6	7	8	9	10	14	15		
		AE14	hdmi1_data0y														
		AE12	ljcb_clkp														
		AB18	ddr1_a0														
		M25	ddr1_ecc_d0														
		AD11	pcie_txn0														
		AE8	usb1_dp														
		AA21	ddr1_d7														
		N23	ddr1_d28														
		M22	ddr1_d27														
		K24	ddr1_dqsn_ecc														
		W25	ddr1_d4														
		P24	ddr1_dqsn3														
		R22	ddr1_d16														
		U24	ddr1_dqsn2														
		P22	ddr1_d29														
		AE18	ddr1_ba0														
		N22	ddr1_d31														
		AE20	ddr1_a1														
		AB13	xo_osc1														
		W24	ddr1_d2														
		AB22	ddr1_a10														
		T24	ddr1_dqm2														
		R24	ddr1_d20														
		AD15	hdmi1_data1x														
		AA18	ddr1_a3														
		AC13	xi_osc1														
		J23	ddr1_ecc_d2														
		AD12	ljcb_clkn														
		Y22	ddr1_d3														
		AD10	pcie_rxn0														
		AE13	hdmi1_clocky														
		AA13	rtc_osc_xi_clk_in32														
		P23	ddr1_d17														
		AA22	ddr1_d6														
		AC23	ddr1_a6														
		L25	ddr1_ecc_d6														
0x1400	CTRL_CORE_PAD_GPMC_AD0	J4	gpmc_ad0		vin3a_d0	vout3_d0										gpio1_6	sysboot0

Table 4-3. Multiplexing Characteristics (continued)

ADDRESS	REGISTER NAME	BALL NUMBER	MUXMODE FIELD SETTINGS (CTRL_CORE_PAD_*[3:0])													
			0	1	2	3	4	5	6	7	8	9	10	14	15	
0x1404	CTRL_CORE_PAD_GPMC_AD1	H6	gpmc_ad1		vin3a_d1	vout3_d1									gpio1_7	sysboot1
0x1408	CTRL_CORE_PAD_GPMC_AD2	G1	gpmc_ad2		vin3a_d2	vout3_d2									gpio1_8	sysboot2
0x140C	CTRL_CORE_PAD_GPMC_AD3	H2	gpmc_ad3		vin3a_d3	vout3_d3									gpio1_9	sysboot3
0x1410	CTRL_CORE_PAD_GPMC_AD4	H3	gpmc_ad4		vin3a_d4	vout3_d4									gpio1_10	sysboot4
0x1414	CTRL_CORE_PAD_GPMC_AD5	H4	gpmc_ad5		vin3a_d5	vout3_d5									gpio1_11	sysboot5
0x1418	CTRL_CORE_PAD_GPMC_AD6	H5	gpmc_ad6		vin3a_d6	vout3_d6									gpio1_12	sysboot6
0x141C	CTRL_CORE_PAD_GPMC_AD7	F1	gpmc_ad7		vin3a_d7	vout3_d7									gpio1_13	sysboot7
0x1420	CTRL_CORE_PAD_GPMC_AD8	G2	gpmc_ad8		vin3a_d8	vout3_d8									gpio7_18	sysboot8
0x1424	CTRL_CORE_PAD_GPMC_AD9	G3	gpmc_ad9		vin3a_d9	vout3_d9									gpio7_19	sysboot9
0x1428	CTRL_CORE_PAD_GPMC_AD10	G4	gpmc_ad10		vin3a_d10	vout3_d10									gpio7_28	sysboot10
0x142C	CTRL_CORE_PAD_GPMC_AD11	G5	gpmc_ad11		vin3a_d11	vout3_d11									gpio7_29	sysboot11
0x1430	CTRL_CORE_PAD_GPMC_AD12	G6	gpmc_ad12		vin3a_d12	vout3_d12									gpio1_18	sysboot12
0x1434	CTRL_CORE_PAD_GPMC_AD13	F5	gpmc_ad13		vin3a_d13	vout3_d13									gpio1_19	sysboot13
0x1438	CTRL_CORE_PAD_GPMC_AD14	E5	gpmc_ad14		vin3a_d14	vout3_d14									gpio1_20	sysboot14
0x143C	CTRL_CORE_PAD_GPMC_AD15	F4	gpmc_ad15		vin3a_d15	vout3_d15									gpio1_21	sysboot15
0x1440	CTRL_CORE_PAD_GPMC_A0	N3	gpmc_a0		vin3a_d16	vout3_d16			vin4b_d0	i2c4_scl	uart5_rxd				gpio7_3	Driver off
0x1444	CTRL_CORE_PAD_GPMC_A1	P3	gpmc_a1		vin3a_d17	vout3_d17			vin4b_d1	i2c4_sda	uart5_txd				gpio7_4	Driver off
0x1448	CTRL_CORE_PAD_GPMC_A2	P1	gpmc_a2		vin3a_d18	vout3_d18			vin4b_d2	uart7_rxd	uart5_ctsn				gpio7_5	Driver off
0x144C	CTRL_CORE_PAD_GPMC_A3	P2	gpmc_a3	qspi1_cs2	vin3a_d19	vout3_d19			vin4b_d3	uart7_txd	uart5_rtsn				gpio7_6	Driver off
0x1450	CTRL_CORE_PAD_GPMC_A4	N2	gpmc_a4	qspi1_cs3	vin3a_d20	vout3_d20			vin4b_d4	i2c5_scl	uart6_rxd				gpio1_26	Driver off
0x1454	CTRL_CORE_PAD_GPMC_A5	N1	gpmc_a5		vin3a_d21	vout3_d21			vin4b_d5	i2c5_sda	uart6_txd				gpio1_27	Driver off
0x1458	CTRL_CORE_PAD_GPMC_A6	M5	gpmc_a6		vin3a_d22	vout3_d22			vin4b_d6	uart8_rxd	uart6_ctsn				gpio1_28	Driver off
0x145C	CTRL_CORE_PAD_GPMC_A7	M4	gpmc_a7		vin3a_d23	vout3_d23			vin4b_d7	uart8_txd	uart6_rtsn				gpio1_29	Driver off
0x1460	CTRL_CORE_PAD_GPMC_A8	M1	gpmc_a8		vin3a_hsync0	vout3_hsync			vin4b_hsync1	timer12	spi4_sclk				gpio1_30	Driver off

Table 4-3. Multiplexing Characteristics (continued)

ADDRESS	REGISTER NAME	BALL NUMBER	MUXMODE FIELD SETTINGS (CTRL_CORE_PAD_*[3:0])													
			0	1	2	3	4	5	6	7	8	9	10	14	15	
0x1464	CTRL_CORE_PAD_GPMC_A9	M3	gpmc_a9		vin3a_vsync0	vout3_vsync				vin4b_vsync1	timer11	spi4_d1			gpio1_31	Driver off
0x1468	CTRL_CORE_PAD_GPMC_A10	M6	gpmc_a10		vin3a_de0	vout3_de				vin4b_clk1	timer10	spi4_d0			gpio2_0	Driver off
0x146C	CTRL_CORE_PAD_GPMC_A11	N5	gpmc_a11		vin3a_fld0	vout3_fld				vin4b_de1	timer9	spi4_cs0			gpio2_1	Driver off
0x1470	CTRL_CORE_PAD_GPMC_A12	L5	gpmc_a12						gpmc_a0	vin4b_fld1	timer8	spi4_cs1	dma_evt1		gpio2_2	Driver off
0x1474	CTRL_CORE_PAD_GPMC_A13	L4	gpmc_a13	qspi1_rtclk							timer7	spi4_cs2	dma_evt2		gpio2_3	Driver off
0x1478	CTRL_CORE_PAD_GPMC_A14	L3	gpmc_a14	qspi1_d3							timer6	spi4_cs3			gpio2_4	Driver off
0x147C	CTRL_CORE_PAD_GPMC_A15	L2	gpmc_a15	qspi1_d2							timer5				gpio2_5	Driver off
0x1480	CTRL_CORE_PAD_GPMC_A16	L1	gpmc_a16	qspi1_d0											gpio2_6	Driver off
0x1484	CTRL_CORE_PAD_GPMC_A17	K6	gpmc_a17	qspi1_d1											gpio2_7	Driver off
0x1488	CTRL_CORE_PAD_GPMC_A18	K5	gpmc_a18	qspi1_sclk											gpio2_8	Driver off
0x148C	CTRL_CORE_PAD_GPMC_A19	C2	gpmc_a19	mmc2_dat4	gpmc_a13					vin3b_d0					gpio2_9	Driver off
0x1490	CTRL_CORE_PAD_GPMC_A20	D3	gpmc_a20	mmc2_dat5	gpmc_a14					vin3b_d1					gpio2_10	Driver off
0x1494	CTRL_CORE_PAD_GPMC_A21	D2	gpmc_a21	mmc2_dat6	gpmc_a15					vin3b_d2					gpio2_11	Driver off
0x1498	CTRL_CORE_PAD_GPMC_A22	D1	gpmc_a22	mmc2_dat7	gpmc_a16					vin3b_d3					gpio2_12	Driver off
0x149C	CTRL_CORE_PAD_GPMC_A23	E1	gpmc_a23	mmc2_clk	gpmc_a17					vin3b_d4					gpio2_13	Driver off
0x14A0	CTRL_CORE_PAD_GPMC_A24	E2	gpmc_a24	mmc2_dat0	gpmc_a18					vin3b_d5					gpio2_14	Driver off
0x14A4	CTRL_CORE_PAD_GPMC_A25	E3	gpmc_a25	mmc2_dat1	gpmc_a19					vin3b_d6					gpio2_15	Driver off
0x14A8	CTRL_CORE_PAD_GPMC_A26	E4	gpmc_a26	mmc2_dat2	gpmc_a20					vin3b_d7					gpio2_16	Driver off
0x14AC	CTRL_CORE_PAD_GPMC_A27	F3	gpmc_a27	mmc2_dat3	gpmc_a21					vin3b_hsync1					gpio2_17	Driver off
0x14B0	CTRL_CORE_PAD_GPMC_CS1	C1	gpmc_cs1	mmc2_cmd	gpmc_a22					vin3b_vsync1					gpio2_18	Driver off
0x14B4	CTRL_CORE_PAD_GPMC_CS0	K4	gpmc_cs0												gpio2_19	Driver off
0x14B8	CTRL_CORE_PAD_GPMC_CS2	K3	gpmc_cs2	qspi1_cs0											gpio2_20	Driver off
0x14BC	CTRL_CORE_PAD_GPMC_CS3	K2	gpmc_cs3	qspi1_cs1	vin3a_clk0	vout3_clk			gpmc_a1						gpio2_21	Driver off
0x14C0	CTRL_CORE_PAD_GPMC_CLK	N6	gpmc_clk	gpmc_cs7	clkout1	gpmc_wait1				vin3b_clk1	timer4	i2c3_scl	dma_evt1		gpio2_22	Driver off

Table 4-3. Multiplexing Characteristics (continued)

ADDRESS	REGISTER NAME	BALL NUMBER	MUXMODE FIELD SETTINGS (CTRL_CORE_PAD_*[3:0])													
			0	1	2	3	4	5	6	7	8	9	10	14	15	
0x14C4	CTRL_CORE_PAD_GPMC_ADV_N_ALE	J5	gpmc_adv_n_ale	gpmc_cs6	clkout2	gpmc_wait1			gpmc_a2	gpmc_a23	timer3	i2c3_sda	dma_evt2		gpio2_23	Driver off
0x14C8	CTRL_CORE_PAD_GPMC_OEN_REN	H1	gpmc_oen_ren												gpio2_24	Driver off
0x14CC	CTRL_CORE_PAD_GPMC_WEN	F2	gpmc_wen												gpio2_25	Driver off
0x14D0	CTRL_CORE_PAD_GPMC_BEN0	M2	gpmc_ben0	gpmc_cs4		vin1b_hsync1				vin3b_de1	timer2		dma_evt3		gpio2_26	Driver off
0x14D4	CTRL_CORE_PAD_GPMC_BEN1	J3	gpmc_ben1	gpmc_cs5		vin1b_de1	vin3b_clk1	gpmc_a3	vin3b_fld1	timer1		dma_evt4			gpio2_27	Driver off
0x14D8	CTRL_CORE_PAD_GPMC_WAIT0	K1	gpmc_wait0												gpio2_28	Driver off
0x14DC	CTRL_CORE_PAD_VIN1A_CLK0	AB6	vin1a_clk0			vout3_d16	vout3_fld								gpio2_30	Driver off
0x14E0	CTRL_CORE_PAD_VIN1B_CLK1	AA6	vin1b_clk1						vin3a_clk0						gpio2_31	Driver off
0x14E4	CTRL_CORE_PAD_VIN1A_DE0	AA7	vin1a_de0	vin1b_hsync1		vout3_d17	vout3_de	uart7_rxd		timer16	spi3_sclk		eQEP1A_in	gpio3_0	Driver off	
0x14E8	CTRL_CORE_PAD_VIN1A_FLD0	AD6	vin1a_fld0	vin1b_vsync1			vout3_clk	uart7_txd		timer15	spi3_d1		eQEP1B_in	gpio3_1	Driver off	
0x14EC	CTRL_CORE_PAD_VIN1A_HSYNCO	AC6	vin1a_hsync0	vin1b_fld1			vout3_hsync	uart7_ctsn		timer14	spi3_d0		eQEP1_index	gpio3_2	Driver off	
0x14F0	CTRL_CORE_PAD_VIN1A_VSYNCO	AC5	vin1a_vsync0	vin1b_de1			vout3_vsync	uart7_rtsn		timer13	spi3_cs0		eQEP1_strobe	gpio3_3	Driver off	
0x14F4	CTRL_CORE_PAD_VIN1A_D0	AD5	vin1a_d0			vout3_d7	vout3_d23	uart8_rxd					ehrpwm1A	gpio3_4	Driver off	
0x14F8	CTRL_CORE_PAD_VIN1A_D1	AE5	vin1a_d1			vout3_d6	vout3_d22	uart8_txd					ehrpwm1B	gpio3_5	Driver off	
0x14FC	CTRL_CORE_PAD_VIN1A_D2	AA5	vin1a_d2			vout3_d5	vout3_d21	uart8_ctsn					ehrpwm1_tripzone_input	gpio3_6	Driver off	
0x1500	CTRL_CORE_PAD_VIN1A_D3	Y5	vin1a_d3			vout3_d4	vout3_d20	uart8_rtsn					eCAP1_in_PWM1_out	gpio3_7	Driver off	
0x1504	CTRL_CORE_PAD_VIN1A_D4	AB7	vin1a_d4			vout3_d3	vout3_d19						ehrpwm1_syn ci	gpio3_8	Driver off	
0x1508	CTRL_CORE_PAD_VIN1A_D5	AE4	vin1a_d5			vout3_d2	vout3_d18						ehrpwm1_syn co	gpio3_9	Driver off	
0x150C	CTRL_CORE_PAD_VIN1A_D6	AB5	vin1a_d6			vout3_d1	vout3_d17						eQEP2A_in	gpio3_10	Driver off	
0x1510	CTRL_CORE_PAD_VIN1A_D7	AD4	vin1a_d7			vout3_d0	vout3_d16						eQEP2B_in	gpio3_11	Driver off	
0x1514	CTRL_CORE_PAD_VIN1A_D8	AA3	vin1a_d8	vin1b_d7			vout3_d15						eQEP2_index	gpio3_12	Driver off	
0x1518	CTRL_CORE_PAD_VIN1A_D9	Y4	vin1a_d9	vin1b_d6			vout3_d14						eQEP2_strobe	gpio3_13	Driver off	
0x151C	CTRL_CORE_PAD_VIN1A_D10	AE3	vin1a_d10	vin1b_d5			vout3_d13							gpio3_14	Driver off	
0x1520	CTRL_CORE_PAD_VIN1A_D11	AA4	vin1a_d11	vin1b_d4			vout3_d12	gpmc_a23						gpio3_15	Driver off	

Table 4-3. Multiplexing Characteristics (continued)

ADDRESS	REGISTER NAME	BALL NUMBER	MUXMODE FIELD SETTINGS (CTRL_CORE_PAD_*[3:0])												
			0	1	2	3	4	5	6	7	8	9	10	14	15
0x1524	CTRL_CORE_PAD_VIN1A_D12	AD3	vin1a_d12	vin1b_d3	usb3_ulpi_d7		vout3_d11	gpmc_a24						gpio3_16	Driver off
0x1528	CTRL_CORE_PAD_VIN1A_D13	AC3	vin1a_d13	vin1b_d2	usb3_ulpi_d6		vout3_d10	gpmc_a25						gpio3_17	Driver off
0x152C	CTRL_CORE_PAD_VIN1A_D14	AD2	vin1a_d14	vin1b_d1	usb3_ulpi_d5		vout3_d9	gpmc_a26						gpio3_18	Driver off
0x1530	CTRL_CORE_PAD_VIN1A_D15	AB3	vin1a_d15	vin1b_d0	usb3_ulpi_d4		vout3_d8	gpmc_a27						gpio3_19	Driver off
0x1534	CTRL_CORE_PAD_VIN1A_D16	AA2	vin1a_d16	vin1b_d7	usb3_ulpi_d3		vout3_d7		vin3a_d0					gpio3_20	Driver off
0x1538	CTRL_CORE_PAD_VIN1A_D17	AC2	vin1a_d17	vin1b_d6	usb3_ulpi_d2		vout3_d6		vin3a_d1					gpio3_21	Driver off
0x153C	CTRL_CORE_PAD_VIN1A_D18	Y3	vin1a_d18	vin1b_d5	usb3_ulpi_d1		vout3_d5		vin3a_d2					gpio3_22	Driver off
0x1540	CTRL_CORE_PAD_VIN1A_D19	AB2	vin1a_d19	vin1b_d4	usb3_ulpi_d0		vout3_d4		vin3a_d3					gpio3_23	Driver off
0x1544	CTRL_CORE_PAD_VIN1A_D20	AB1	vin1a_d20	vin1b_d3	usb3_ulpi_nxt		vout3_d3		vin3a_d4					gpio3_24	Driver off
0x1548	CTRL_CORE_PAD_VIN1A_D21	AC1	vin1a_d21	vin1b_d2	usb3_ulpi_dir		vout3_d2		vin3a_d5					gpio3_25	Driver off
0x154C	CTRL_CORE_PAD_VIN1A_D22	AA1	vin1a_d22	vin1b_d1	usb3_ulpi_stp		vout3_d1		vin3a_d6					gpio3_26	Driver off
0x1550	CTRL_CORE_PAD_VIN1A_D23	Y2	vin1a_d23	vin1b_d0	usb3_ulpi_clk		vout3_d0		vin3a_d7					gpio3_27	Driver off
0x1554	CTRL_CORE_PAD_VIN2A_CLK0	D4	vin2a_clk0				vout2_fld	emu5					eQEP1A_in	gpio3_28	Driver off
0x1558	CTRL_CORE_PAD_VIN2A_DE0	B4	vin2a_de0	vin2a_fld0	vin2b_fld1	vin2b_de1	vout2_de	emu6					eQEP1B_in	gpio3_29	Driver off
0x155C	CTRL_CORE_PAD_VIN2A_FLD0	E6	vin2a_fld0		vin2b_clk1		vout2_clk	emu7					eQEP1_index	gpio3_30	Driver off
0x1560	CTRL_CORE_PAD_VIN2A_HSYNC0	D5	vin2a_hsync0			vin2b_hsync1	vout2_hsync	emu8		uart9_rxd	spi4_sclk		eQEP1_strobe	gpio3_31	Driver off
0x1564	CTRL_CORE_PAD_VIN2A_VSYNC0	C4	vin2a_vsync0			vin2b_vsync1	vout2_vsync	emu9		uart9_txd	spi4_d1		ehrpwm1A	gpio4_0	Driver off
0x1568	CTRL_CORE_PAD_VIN2A_D0	C3	vin2a_d0				vout2_d23	emu10		uart9_ctsn	spi4_d0		ehrpwm1B	gpio4_1	Driver off
0x156C	CTRL_CORE_PAD_VIN2A_D1	B2	vin2a_d1				vout2_d22	emu11		uart9_rtsn	spi4_cs0		ehrpwm1_tripzone_input	gpio4_2	Driver off
0x1570	CTRL_CORE_PAD_VIN2A_D2	E7	vin2a_d2				vout2_d21	emu12			uart10_rxd		eCAP1_in_PWM1_out	gpio4_3	Driver off
0x1574	CTRL_CORE_PAD_VIN2A_D3	B3	vin2a_d3				vout2_d20	emu13			uart10_txd		ehrpwm1_syn ci	gpio4_4	Driver off
0x1578	CTRL_CORE_PAD_VIN2A_D4	A3	vin2a_d4				vout2_d19	emu14			uart10_ctsn		ehrpwm1_syn co	gpio4_5	Driver off
0x157C	CTRL_CORE_PAD_VIN2A_D5	C6	vin2a_d5				vout2_d18	emu15			uart10_rtsn		eQEP2A_in	gpio4_6	Driver off
0x1580	CTRL_CORE_PAD_VIN2A_D6	A4	vin2a_d6				vout2_d17	emu16			mii1_rxd1		eQEP2B_in	gpio4_7	Driver off

Table 4-3. Multiplexing Characteristics (continued)

ADDRESS	REGISTER NAME	BALL NUMBER	MUXMODE FIELD SETTINGS (CTRL_CORE_PAD_*(3:0))														
			0	1	2	3	4	5	6	7	8	9	10	14	15		
0x1584	CTRL_CORE_PAD_VIN2A_D7	B5	vin2a_d7					vout2_d16	emu17				mii1_rxd2		eQEP2_index	gpio4_8	Driver off
0x1588	CTRL_CORE_PAD_VIN2A_D8	C5	vin2a_d8					vout2_d15	emu18				mii1_rxd3		eQEP2_strobe	gpio4_9	Driver off
0x158C	CTRL_CORE_PAD_VIN2A_D9	A7	vin2a_d9					vout2_d14	emu19				mii1_rxd0		ehrpwm2A	gpio4_10	Driver off
0x1590	CTRL_CORE_PAD_VIN2A_D10	A5	vin2a_d10				mdio_mclk	vout2_d13							ehrpwm2B	gpio4_11	Driver off
0x1594	CTRL_CORE_PAD_VIN2A_D11	B6	vin2a_d11				mdio_d	vout2_d12							ehrpwm2_tripzone_input	gpio4_12	Driver off
0x1598	CTRL_CORE_PAD_VIN2A_D12	E8	vin2a_d12				rgmii1_txc	vout2_d11					mii1_rxclk		eCAP2_in_PWM2_out	gpio4_13	Driver off
0x159C	CTRL_CORE_PAD_VIN2A_D13	A6	vin2a_d13				rgmii1_txctl	vout2_d10					mii1_rxdv		eQEP3A_in	gpio4_14	Driver off
0x15A0	CTRL_CORE_PAD_VIN2A_D14	C7	vin2a_d14				rgmii1_txd3	vout2_d9					mii1_txclk		eQEP3B_in	gpio4_15	Driver off
0x15A4	CTRL_CORE_PAD_VIN2A_D15	D6	vin2a_d15				rgmii1_txd2	vout2_d8					mii1_txd0		eQEP3_index	gpio4_16	Driver off
0x15A8	CTRL_CORE_PAD_VIN2A_D16	B7	vin2a_d16		vin2b_d7		rgmii1_txd1	vout2_d7			vin3a_d8		mii1_txd1		eQEP3_strobe	gpio4_24	Driver off
0x15AC	CTRL_CORE_PAD_VIN2A_D17	B8	vin2a_d17		vin2b_d6		rgmii1_txd0	vout2_d6			vin3a_d9		mii1_txd2		ehrpwm3A	gpio4_25	Driver off
0x15B0	CTRL_CORE_PAD_VIN2A_D18	A8	vin2a_d18		vin2b_d5		rgmii1_rxc	vout2_d5			vin3a_d10		mii1_txd3		ehrpwm3B	gpio4_26	Driver off
0x15B4	CTRL_CORE_PAD_VIN2A_D19	D7	vin2a_d19		vin2b_d4		rgmii1_rxctl	vout2_d4			vin3a_d11		mii1_txer		ehrpwm3_tripzone_input	gpio4_27	Driver off
0x15B8	CTRL_CORE_PAD_VIN2A_D20	C8	vin2a_d20		vin2b_d3		rgmii1_rxd3	vout2_d3	vin3a_de0	vin3a_d12			mii1_rxer		eCAP3_in_PWM3_out	gpio4_28	Driver off
0x15BC	CTRL_CORE_PAD_VIN2A_D21	D8	vin2a_d21		vin2b_d2		rgmii1_rxd2	vout2_d2	vin3a_fld0	vin3a_d13			mii1_col			gpio4_29	Driver off
0x15C0	CTRL_CORE_PAD_VIN2A_D22	F8	vin2a_d22		vin2b_d1		rgmii1_rxd1	vout2_d1	vin3a_hsync0	vin3a_d14			mii1_crs			gpio4_30	Driver off
0x15C4	CTRL_CORE_PAD_VIN2A_D23	E9	vin2a_d23		vin2b_d0		rgmii1_rxd0	vout2_d0	vin3a_vsync0	vin3a_d15			mii1_txen			gpio4_31	Driver off
0x15C8	CTRL_CORE_PAD_VOUT1_CLK	D10	vout1_clk						vin3a_fld0				spi3_cs0			gpio4_19	Driver off
0x15CC	CTRL_CORE_PAD_VOUT1_DE	D13	vout1_de						vin3a_de0				spi3_d1			gpio4_20	Driver off
0x15D0	CTRL_CORE_PAD_VOUT1_FLD	E11	vout1_fld						vin3a_clk0				spi3_cs1			gpio4_21	Driver off
0x15D4	CTRL_CORE_PAD_VOUT1_HSYNC	E12	vout1_hsync						vin3a_hsync0				spi3_d0			gpio4_22	Driver off
0x15D8	CTRL_CORE_PAD_VOUT1_VSYNC	E13	vout1_vsync						vin3a_vsync0				spi3_sclk			gpio4_23	Driver off
0x15DC	CTRL_CORE_PAD_VOUT1_D0	B9	vout1_d0		uart5_rxd				vin3a_d16				spi3_cs2			gpio8_0	Driver off
0x15E0	CTRL_CORE_PAD_VOUT1_D1	A9	vout1_d1		uart5_txd				vin3a_d17							gpio8_1	Driver off

Table 4-3. Multiplexing Characteristics (continued)

ADDRESS	REGISTER NAME	BALL NUMBER	MUXMODE FIELD SETTINGS (CTRL_CORE_PAD_*[3:0])													
			0	1	2	3	4	5	6	7	8	9	10	14	15	
0x15E4	CTRL_CORE_PAD_V_OUT1_D2	A11	vout1_d2		emu2			vin3a_d18	obs0	obs16	obs_irq1				gpio8_2	Driver off
0x15E8	CTRL_CORE_PAD_V_OUT1_D3	C9	vout1_d3		emu5			vin3a_d19	obs1	obs17	obs_dmarq1				gpio8_3	Driver off
0x15EC	CTRL_CORE_PAD_V_OUT1_D4	A13	vout1_d4		emu6			vin3a_d20	obs2	obs18					gpio8_4	Driver off
0x15F0	CTRL_CORE_PAD_V_OUT1_D5	A12	vout1_d5		emu7			vin3a_d21	obs3	obs19					gpio8_5	Driver off
0x15F4	CTRL_CORE_PAD_V_OUT1_D6	B14	vout1_d6		emu8			vin3a_d22	obs4	obs20					gpio8_6	Driver off
0x15F8	CTRL_CORE_PAD_V_OUT1_D7	B13	vout1_d7		emu9			vin3a_d23							gpio8_7	Driver off
0x15FC	CTRL_CORE_PAD_V_OUT1_D8	A14	vout1_d8		uart6_rxd			vin3a_d8							gpio8_8	Driver off
0x1600	CTRL_CORE_PAD_V_OUT1_D9	B11	vout1_d9		uart6_txd			vin3a_d9							gpio8_9	Driver off
0x1604	CTRL_CORE_PAD_V_OUT1_D10	B12	vout1_d10		emu3			vin3a_d10	obs5	obs21	obs_irq2				gpio8_10	Driver off
0x1608	CTRL_CORE_PAD_V_OUT1_D11	B10	vout1_d11		emu10			vin3a_d11	obs6	obs22	obs_dmarq2				gpio8_11	Driver off
0x160C	CTRL_CORE_PAD_V_OUT1_D12	C14	vout1_d12		emu11			vin3a_d12	obs7	obs23					gpio8_12	Driver off
0x1610	CTRL_CORE_PAD_V_OUT1_D13	C10	vout1_d13		emu12			vin3a_d13	obs8	obs24					gpio8_13	Driver off
0x1614	CTRL_CORE_PAD_V_OUT1_D14	A10	vout1_d14		emu13			vin3a_d14	obs9	obs25					gpio8_14	Driver off
0x1618	CTRL_CORE_PAD_V_OUT1_D15	C13	vout1_d15		emu14			vin3a_d15	obs10	obs26					gpio8_15	Driver off
0x161C	CTRL_CORE_PAD_V_OUT1_D16	C11	vout1_d16		uart7_rxd			vin3a_d0							gpio8_16	Driver off
0x1620	CTRL_CORE_PAD_V_OUT1_D17	E10	vout1_d17		uart7_txd			vin3a_d1							gpio8_17	Driver off
0x1624	CTRL_CORE_PAD_V_OUT1_D18	D15	vout1_d18		emu4			vin3a_d2	obs11	obs27					gpio8_18	Driver off
0x1628	CTRL_CORE_PAD_V_OUT1_D19	E15	vout1_d19		emu15			vin3a_d3	obs12	obs28					gpio8_19	Driver off
0x162C	CTRL_CORE_PAD_V_OUT1_D20	D9	vout1_d20		emu16			vin3a_d4	obs13	obs29					gpio8_20	Driver off
0x1630	CTRL_CORE_PAD_V_OUT1_D21	E14	vout1_d21		emu17			vin3a_d5	obs14	obs30					gpio8_21	Driver off
0x1634	CTRL_CORE_PAD_V_OUT1_D22	D14	vout1_d22		emu18			vin3a_d6	obs15	obs31					gpio8_22	Driver off
0x1638	CTRL_CORE_PAD_V_OUT1_D23	D11	vout1_d23		emu19			vin3a_d7					spi3_cs3		gpio8_23	Driver off
0x163C	CTRL_CORE_PAD_MDIO_MCLK	R3	mdio_mclk	uart3_rtsn		mii0_col	vin2a_clk0	vin4b_clk1							gpio5_15	Driver off
0x1640	CTRL_CORE_PAD_MDIO_D	T1	mdio_d	uart3_ctsn		mii0_txer	vin2a_d0	vin4b_d0							gpio5_16	Driver off

Table 4-3. Multiplexing Characteristics (continued)

ADDRESS	REGISTER NAME	BALL NUMBER	MUXMODE FIELD SETTINGS (CTRL_CORE_PAD_*[3:0])														
			0	1	2	3	4	5	6	7	8	9	10	14	15		
0x1644	CTRL_CORE_PAD_R_MII_MHZ_50_CLK	R2	RMII_MHZ_50_CLK					vin2a_d11								gpio5_17	Driver off
0x1648	CTRL_CORE_PAD_U_ART3_RXD	R1	uart3_rxd		rmii1_crs	mii0_rxdv		vin2a_d1	vin4b_d1			spi3_sclk				gpio5_18	Driver off
0x164C	CTRL_CORE_PAD_U_ART3_TXD	T2	uart3_txd		rmii1_rxr	mii0_rxclk		vin2a_d2	vin4b_d2			spi3_d1	spi4_cs1			gpio5_19	Driver off
0x1650	CTRL_CORE_PAD_R_GMII0_TXC	R6	rgmii0_txc	uart3_ctsn	rmii1_rxd1	mii0_rxd3		vin2a_d3	vin4b_d3	usb4_ulpi_clk	spi3_d0	spi4_cs2				gpio5_20	Driver off
0x1654	CTRL_CORE_PAD_R_GMII0_TXCTL	P6	rgmii0_txctl	uart3_rtsn	rmii1_rxd0	mii0_rxd2		vin2a_d4	vin4b_d4	usb4_ulpi_stp	spi3_cs0	spi4_cs3				gpio5_21	Driver off
0x1658	CTRL_CORE_PAD_R_GMII0_TXD3	T5	rgmii0_txd3	rmii0_crs		mii0_crs		vin2a_de0	vin4b_de1	usb4_ulpi_dir	spi4_sclk	uart4_rxd				gpio5_22	Driver off
0x165C	CTRL_CORE_PAD_R_GMII0_TXD2	T6	rgmii0_txd2	rmii0_rxr		mii0_rxr		vin2a_hsync0	vin4b_hsync1	usb4_ulpi_nxt	spi4_d1	uart4_txd				gpio5_23	Driver off
0x1660	CTRL_CORE_PAD_R_GMII0_TXD1	T4	rgmii0_txd1	rmii0_rxd1		mii0_rxd1		vin2a_vsync0	vin4b_vsync1	usb4_ulpi_d0	spi4_d0	uart4_ctsn				gpio5_24	Driver off
0x1664	CTRL_CORE_PAD_R_GMII0_TXD0	R5	rgmii0_txd0	rmii0_rxd0		mii0_rxd0		vin2a_d10		usb4_ulpi_d1	spi4_cs0	uart4_rtsn				gpio5_25	Driver off
0x1668	CTRL_CORE_PAD_R_GMII0_RXC	U2	rgmii0_rxc		rmii1_txen	mii0_txclk		vin2a_d5	vin4b_d5	usb4_ulpi_d2						gpio5_26	Driver off
0x166C	CTRL_CORE_PAD_R_GMII0_RXCTL	U3	rgmii0_rxctl		rmii1_txd1	mii0_txd3		vin2a_d6	vin4b_d6	usb4_ulpi_d3						gpio5_27	Driver off
0x1670	CTRL_CORE_PAD_R_GMII0_RXD3	P5	rgmii0_rxd3		rmii1_txd0	mii0_txd2		vin2a_d7	vin4b_d7	usb4_ulpi_d4						gpio5_28	Driver off
0x1674	CTRL_CORE_PAD_R_GMII0_RXD2	U4	rgmii0_rxd2	rmii0_txen		mii0_txen		vin2a_d8		usb4_ulpi_d5						gpio5_29	Driver off
0x1678	CTRL_CORE_PAD_R_GMII0_RXD1	T3	rgmii0_rxd1	rmii0_txd1		mii0_txd1		vin2a_d9		usb4_ulpi_d6						gpio5_30	Driver off
0x167C	CTRL_CORE_PAD_R_GMII0_RXD0	R4	rgmii0_rxd0	rmii0_txd0		mii0_txd0		vin2a_fld0	vin4b_fld1	usb4_ulpi_d7						gpio5_31	Driver off
0x1680	CTRL_CORE_PAD_U_SB1_DRVVBUS	AE6	usb1_drvvbus								timer16					gpio6_12	Driver off
0x1694	CTRL_CORE_PAD_X_REF_CLK0	C23	xref_clk0	mcasp2_axr8	mcasp1_axr4	mcasp1_ahclkx	mcasp5_ahclkx					clkout2	timer13			gpio6_17	Driver off
0x1698	CTRL_CORE_PAD_X_REF_CLK1	C22	xref_clk1	mcasp2_axr9	mcasp1_axr5	mcasp2_ahclkx	mcasp6_ahclkx						timer14			gpio6_18	Driver off
0x16A4	CTRL_CORE_PAD_MCASP1_ACLKX	C25	mcasp1_aclkx										i2c3_sda			gpio7_31	Driver off
0x16A8	CTRL_CORE_PAD_MCASP1_FSX	B24	mcasp1_fsx										i2c3_scl			gpio7_30	Driver off
0x16B4	CTRL_CORE_PAD_MCASP1_AXR0	B15	mcasp1_axr0			uart6_rxd							i2c5_sda			gpio5_2	Driver off
0x16B8	CTRL_CORE_PAD_MCASP1_AXR1	A15	mcasp1_axr1			uart6_txd							i2c5_scl			gpio5_3	Driver off
0x16D4	CTRL_CORE_PAD_MCASP1_AXR8	A16	mcasp1_axr8	mcasp6_axr0		spi3_sclk							timer5			gpio5_10	Driver off
0x16D8	CTRL_CORE_PAD_MCASP1_AXR9	A17	mcasp1_axr9	mcasp6_axr1		spi3_d1							timer6			gpio5_11	Driver off

Table 4-3. Multiplexing Characteristics (continued)

ADDRESS	REGISTER NAME	BALL NUMBER	MUXMODE FIELD SETTINGS (CTRL_CORE_PAD_*[3:0])													
			0	1	2	3	4	5	6	7	8	9	10	14	15	
0x16DC	CTRL_CORE_PAD_MCASP1_AXR10	A19	mcasp1_axr10	mcasp6_aclkx	mcasp6_aclkr	spi3_d0								timer7	gpio5_12	Driver off
0x16E0	CTRL_CORE_PAD_MCASP1_AXR11	A20	mcasp1_axr11	mcasp6_fsx	mcasp6_fsr	spi3_cs0								timer8	gpio4_17	Driver off
0x16E4	CTRL_CORE_PAD_MCASP1_AXR12	A21	mcasp1_axr12	mcasp7_axr0		spi3_cs1								timer9	gpio4_18	Driver off
0x16E8	CTRL_CORE_PAD_MCASP1_AXR13	A23	mcasp1_axr13	mcasp7_axr1										timer10	gpio6_4	Driver off
0x16EC	CTRL_CORE_PAD_MCASP1_AXR14	C15	mcasp1_axr14	mcasp7_aclkx	mcasp7_aclkr									timer11	gpio6_5	Driver off
0x16F0	CTRL_CORE_PAD_MCASP1_AXR15	B16	mcasp1_axr15	mcasp7_fsx	mcasp7_fsr									timer12	gpio6_6	Driver off
0x16F4	CTRL_CORE_PAD_MCASP2_ACLKX	B21	mcasp2_aclkx													Driver off
0x16F8	CTRL_CORE_PAD_MCASP2_FSX	B20	mcasp2_fsx													Driver off
0x170C	CTRL_CORE_PAD_MCASP2_AXR2	B23	mcasp2_axr2	mcasp3_axr2											gpio6_8	Driver off
0x1710	CTRL_CORE_PAD_MCASP2_AXR3	B17	mcasp2_axr3	mcasp3_axr3											gpio6_9	Driver off
0x1724	CTRL_CORE_PAD_MCASP3_ACLKX	B19	mcasp3_aclkx	mcasp3_aclkr	mcasp2_axr12	uart7_rxd									gpio5_13	Driver off
0x1728	CTRL_CORE_PAD_MCASP3_FSX	C16	mcasp3_fsx	mcasp3_fsr	mcasp2_axr13	uart7_txd									gpio5_14	Driver off
0x172C	CTRL_CORE_PAD_MCASP3_AXR0	C17	mcasp3_axr0		mcasp2_axr14	uart7_ctsn	uart5_rxd									Driver off
0x1730	CTRL_CORE_PAD_MCASP3_AXR1	C20	mcasp3_axr1		mcasp2_axr15	uart7_rtsn	uart5_txd									Driver off
0x1734	CTRL_CORE_PAD_MCASP4_ACLKX	E24	mcasp4_aclkx	mcasp4_aclkr	spi3_sclk	uart8_rxd	i2c4_sda			vout2_d16						Driver off
0x1738	CTRL_CORE_PAD_MCASP4_FSX	D23	mcasp4_fsx	mcasp4_fsr	spi3_d1	uart8_txd	i2c4_scl			vout2_d17						Driver off
0x173C	CTRL_CORE_PAD_MCASP4_AXR0	E25	mcasp4_axr0		spi3_d0	uart8_ctsn	uart4_rxd			vout2_d18						Driver off
0x1740	CTRL_CORE_PAD_MCASP4_AXR1	E23	mcasp4_axr1		spi3_cs0	uart8_rtsn	uart4_txd			vout2_d19						Driver off
0x1744	CTRL_CORE_PAD_MCASP5_ACLKX	V1	mcasp5_aclkx	mcasp5_aclkr	spi4_sclk	uart9_rxd	i2c5_sda			vout2_d20						Driver off
0x1748	CTRL_CORE_PAD_MCASP5_FSX	W2	mcasp5_fsx	mcasp5_fsr	spi4_d1	uart9_txd	i2c5_scl			vout2_d21						Driver off
0x174C	CTRL_CORE_PAD_MCASP5_AXR0	V2	mcasp5_axr0		spi4_d0	uart9_ctsn	uart3_rxd			vout2_d22						Driver off
0x1750	CTRL_CORE_PAD_MCASP5_AXR1	U1	mcasp5_axr1		spi4_cs0	uart9_rtsn	uart3_txd			vout2_d23						Driver off
0x1774	CTRL_CORE_PAD_GPIO6_10	Y1	gpio6_10	mdio_mclk	i2c3_sda	usb3_ulpi_d7	vin2b_hsync1							ehrpwm2A	gpio6_10	Driver off
0x1778	CTRL_CORE_PAD_GPIO6_11	W1	gpio6_11	mdio_d	i2c3_scl	usb3_ulpi_d6	vin2b_vsync1							ehrpwm2B	gpio6_11	Driver off

Table 4-3. Multiplexing Characteristics (continued)

ADDRESS	REGISTER NAME	BALL NUMBER	MUXMODE FIELD SETTINGS (CTRL_CORE_PAD_*[3:0])													
			0	1	2	3	4	5	6	7	8	9	10	14	15	
0x177C	CTRL_CORE_PAD_MMC3_CLK	W5	mmc3_clk			usb3_ulpi_d5	vin2b_d7							ehrpwm2_tripzone_input	gpio6_29	Driver off
0x1780	CTRL_CORE_PAD_MMC3_CMD	W4	mmc3_cmd	spi3_sclk		usb3_ulpi_d4	vin2b_d6							eCAP2_in_PWM2_out	gpio6_30	Driver off
0x1784	CTRL_CORE_PAD_MMC3_DAT0	U6	mmc3_dat0	spi3_d1	uart5_rxd	usb3_ulpi_d3	vin2b_d5							eQEP3A_in	gpio6_31	Driver off
0x1788	CTRL_CORE_PAD_MMC3_DAT1	V6	mmc3_dat1	spi3_d0	uart5_txd	usb3_ulpi_d2	vin2b_d4							eQEP3B_in	gpio7_0	Driver off
0x178C	CTRL_CORE_PAD_MMC3_DAT2	U5	mmc3_dat2	spi3_cs0	uart5_ctsn	usb3_ulpi_d1	vin2b_d3							eQEP3_index	gpio7_1	Driver off
0x1790	CTRL_CORE_PAD_MMC3_DAT3	V3	mmc3_dat3	spi3_cs1	uart5_rtsn	usb3_ulpi_d0	vin2b_d2							eQEP3_strobe	gpio7_2	Driver off
0x1794	CTRL_CORE_PAD_MMC3_DAT4	V5	mmc3_dat4	spi4_sclk	uart10_rxd	usb3_ulpi_nxt	vin2b_d1							ehrpwm3A	gpio1_22	Driver off
0x1798	CTRL_CORE_PAD_MMC3_DAT5	W6	mmc3_dat5	spi4_d1	uart10_txd	usb3_ulpi_dir	vin2b_d0							ehrpwm3B	gpio1_23	Driver off
0x179C	CTRL_CORE_PAD_MMC3_DAT6	W3	mmc3_dat6	spi4_d0	uart10_ctsn	usb3_ulpi_stp	vin2b_de1							ehrpwm3_tripzone_input	gpio1_24	Driver off
0x17A0	CTRL_CORE_PAD_MMC3_DAT7	V4	mmc3_dat7	spi4_cs0	uart10_rtsn	usb3_ulpi_clk	vin2b_clk1							eCAP3_in_PWM3_out	gpio1_25	Driver off
0x17A4	CTRL_CORE_PAD_SPI1_SCLK	C18	spi1_sclk												gpio7_7	Driver off
0x17A8	CTRL_CORE_PAD_SPI1_D1	C21	spi1_d1												gpio7_8	Driver off
0x17AC	CTRL_CORE_PAD_SPI1_D0	E22	spi1_d0												gpio7_9	Driver off
0x17B0	CTRL_CORE_PAD_SPI1_CS0	D22	spi1_cs0												gpio7_10	Driver off
0x17B4	CTRL_CORE_PAD_SPI1_CS1	D16	spi1_cs1			spi2_cs1									gpio7_11	Driver off
0x17B8	CTRL_CORE_PAD_SPI1_CS2	C19	spi1_cs2	uart4_rxd	mmc3_sdcd	spi2_cs2	dcan2_tx	mdio_mclk	hdmi1_hpd						gpio7_12	Driver off
0x17BC	CTRL_CORE_PAD_SPI1_CS3	C24	spi1_cs3	uart4_txd	mmc3_sdwp	spi2_cs3	dcan2_rx	mdio_d	hdmi1_cec						gpio7_13	Driver off
0x17C0	CTRL_CORE_PAD_SPI2_SCLK	F24	spi2_sclk	uart3_rxd											gpio7_14	Driver off
0x17C4	CTRL_CORE_PAD_SPI2_D1	F25	spi2_d1	uart3_txd											gpio7_15	Driver off
0x17C8	CTRL_CORE_PAD_SPI2_D0	E16	spi2_d0	uart3_ctsn	uart5_rxd										gpio7_16	Driver off
0x17CC	CTRL_CORE_PAD_SPI2_CS0	D17	spi2_cs0	uart3_rtsn	uart5_txd										gpio7_17	Driver off
0x17D0	CTRL_CORE_PAD_DCAN1_TX	E19	dcan1_tx		uart8_rxd	mmc2_sdcd				hdmi1_hpd					gpio1_14	Driver off
0x17D4	CTRL_CORE_PAD_DCAN1_RX	E21	dcan1_rx		uart8_txd	mmc2_sdwp				hdmi1_cec					gpio1_15	Driver off
0x17E0	CTRL_CORE_PAD_UART1_RXD	G23	uart1_rxd			mmc4_sdcd									gpio7_22	Driver off

Table 4-3. Multiplexing Characteristics (continued)

ADDRESS	REGISTER NAME	BALL NUMBER	MUXMODE FIELD SETTINGS (CTRL_CORE_PAD_*[3:0])													
			0	1	2	3	4	5	6	7	8	9	10	14	15	
0x17E4	CTRL_CORE_PAD_UART1_TXD	H22	uart1_txd			mmc4_sdwp									gpio7_23	Driver off
0x17E8	CTRL_CORE_PAD_UART1_CTSN	H25	uart1_ctsn		uart9_rxd	mmc4_clk									gpio7_24	Driver off
0x17EC	CTRL_CORE_PAD_UART1_RTSN	H24	uart1_rtsn		uart9_txd	mmc4_cmd									gpio7_25	Driver off
0x17F0	CTRL_CORE_PAD_UART2_RXD	H23		uart3_ctsn	uart3_rctx	mmc4_dat0	uart2_rxd	uart1_dcdn							gpio7_26	Driver off
0x17F4	CTRL_CORE_PAD_UART2_TXD	J25	uart2_txd	uart3_rtsn	uart3_sd	mmc4_dat1	uart2_txd	uart1_dsrn							gpio7_27	Driver off
0x17F8	CTRL_CORE_PAD_UART2_CTSN	J22	uart2_ctsn		uart3_rxd	mmc4_dat2	uart10_rxd	uart1_dtrn							gpio1_16	Driver off
0x17FC	CTRL_CORE_PAD_UART2_RTSN	J24	uart2_rtsn	uart3_txd	uart3_irtx	mmc4_dat3	uart10_txd	uart1_rin							gpio1_17	Driver off
0x1800	CTRL_CORE_PAD_I2C1_SDA	G25	i2c1_sda													
0x1804	CTRL_CORE_PAD_I2C1_SCL	G24	i2c1_scl													
0x1808	CTRL_CORE_PAD_I2C2_SDA	F22	i2c2_sda	hdmi1_ddc_scl												Driver off
0x180C	CTRL_CORE_PAD_I2C2_SCL	F23	i2c2_scl	hdmi1_ddc_sda												Driver off
0x1818	CTRL_CORE_PAD_WAKEUP0	AA16	Wakeup0	dcan1_rx											gpio1_0	Driver off
0x181C	CTRL_CORE_PAD_WAKEUP1	AA17	Wakeup1	dcan2_rx											gpio1_1	Driver off
0x1820	CTRL_CORE_PAD_WAKEUP2	AB17	Wakeup2	sys_nirq2											gpio1_2	Driver off
0x1824	CTRL_CORE_PAD_WAKEUP3	AC17	Wakeup3	sys_nirq1											gpio1_3	Driver off
0x1828	CTRL_CORE_PAD_ON_OFF	AA11	on_off													
0x182C	CTRL_CORE_PAD_RTC_PORZ	AA10	rtc_porz													
0x1830	CTRL_CORE_PAD_TMS	D18	tms													
0x1834	CTRL_CORE_PAD_TDI	D20	tdi												gpio8_27	
0x1838	CTRL_CORE_PAD_TDO	F21	tdo												gpio8_28	
0x183C	CTRL_CORE_PAD_TCLK	E18	tclk													
0x1840	CTRL_CORE_PAD_TRSTN	E17	trstn													
0x1844	CTRL_CORE_PAD_RTCK	D19	rtck												gpio8_29	
0x1848	CTRL_CORE_PAD_EMU0	E20	emu0												gpio8_30	

Table 4-3. Multiplexing Characteristics (continued)

ADDRESS	REGISTER NAME	BALL NUMBER	MUXMODE FIELD SETTINGS (CTRL_CORE_PAD_*[3:0])														
			0	1	2	3	4	5	6	7	8	9	10	14	15		
0x184C	CTRL_CORE_PAD_EMU1	D21	emu1													gpio8_31	
0x185C	CTRL_CORE_PAD_RESETN	H21	resetn														
0x1860	CTRL_CORE_PAD_NMIN_DSP	G22	nmin_dsp														
0x1864	CTRL_CORE_PAD_RSTOUTN	G21	rstoutn														

1. NA in table stands for Not Applicable.

4.4 Signal Descriptions

Many signals are available on multiple pins, according to the software configuration of the pin multiplexing options.

1. **SIGNAL NAME:** The name of the signal passing through the pin.

NOTE

The subsystem multiplexing signals are not described in [Table 4-2](#) and [Table 4-3](#).

2. **DESCRIPTION:** Description of the signal
3. **TYPE:** Signal direction and type:
 - I = Input
 - O = Output
 - IO = Input or output
 - D = Open Drain
 - DS = Differential Signaling
 - A = Analog
 - PWR = Power
 - GND = Ground
4. **BALL:** Associated ball(s) number

NOTE

For more information, see the Control Module / Control Module Register Manual section of the device TRM.

4.4.1 Video Input Ports (VIP)

NOTE

For more information, see the Video Input Port (VIP) section of the device TRM.

CAUTION

The I/O timings provided in [Section 7 Timing Requirements and Switching Characteristics](#) are applicable for all combinations of signals for vin1. However, the timings are valid only for vin2, vin3, and vin4 if signals within a single IOSET are used. The IOSETs are defined in [Table 7-4](#), [Table 7-5](#) and [Table 7-6](#).

Table 4-4. VIP Signal Descriptions

SIGNAL NAME	DESCRIPTION	TYPE	BALL
Video Input 1 (VIP1)			
vin1a_clk0	Video Input 1 Port A Clock input. Input clock for 8-bit 16-bit or 24-bit Port A video capture. Input data is sampled on the CLK0 edge.	I	AB6
vin1a_de0	Video Input 1 Data Enable input	I	AA7
vin1a_fld0	Video Input 1 Port A Data Enable input	I	AD6
vin1a_hsync0	Video Input 1 Port A Horizontal Sync input	I	AC6
vin1a_vsync0	Video Input 1 Port A Vertical Sync input	I	AC5
vin1a_d0	Video Input 1 Port A Data input	I	AD5
vin1a_d1	Video Input 1 Port A Data input	I	AE5
vin1a_d2	Video Input 1 Port A Data input	I	AA5

Table 4-4. VIP Signal Descriptions (continued)

SIGNAL NAME	DESCRIPTION	TYPE	BALL
vin1a_d3	Video Input 1 Port A Data input	I	Y5
vin1a_d4	Video Input 1 Port A Data input	I	AB7
vin1a_d5	Video Input 1 Port A Data input	I	AE4
vin1a_d6	Video Input 1 Port A Data input	I	AB5
vin1a_d7	Video Input 1 Port A Data input	I	AD4
vin1a_d8	Video Input 1 Port A Data input	I	AA3
vin1a_d9	Video Input 1 Port A Data input	I	Y4
vin1a_d10	Video Input 1 Port A Data input	I	AE3
vin1a_d11	Video Input 1 Port A Data input	I	AA4
vin1a_d12	Video Input 1 Port A Data input	I	AD3
vin1a_d13	Video Input 1 Port A Data input	I	AC3
vin1a_d14	Video Input 1 Port A Data input	I	AD2
vin1a_d15	Video Input 1 Port A Data input	I	AB3
vin1a_d16	Video Input 1 Port A Data input	I	AA2
vin1a_d17	Video Input 1 Port A Data input	I	AC2
vin1a_d18	Video Input 1 Port A Data input	I	Y3
vin1a_d19	Video Input 1 Port A Data input	I	AB2
vin1a_d20	Video Input 1 Port A Data input	I	AB1
vin1a_d21	Video Input 1 Port A Data input	I	AC1
vin1a_d22	Video Input 1 Port A Data input	I	AA1
vin1a_d23	Video Input 1 Port A Data input	I	Y2
vin1b_hsync1	Video Input 1 Port B Horizontal Sync input	I	AA7/ M2
vin1b_vsync1	Video Input 1 Port B Vertical Sync input	I	AD6
vin1b fld1	Video Input 1 Port B Field ID input	I	AC6
vin1b_de1	Video Input 1 Port B Data Enable input	I	AC5/ J3
vin1b_clk1	Video Input 1 Port B Clock input	I	AA6
vin1b_d0	Video Input 1 Port B Data input	I	AB3/ Y2
vin1b_d1	Video Input 1 Port B Data input	I	AA1/ AD2
vin1b_d2	Video Input 1 Port B Data input	I	AC1/ AC3
vin1b_d3	Video Input 1 Port B Data input	I	AB1/ AD3
vin1b_d4	Video Input 1 Port B Data input	I	AA4/ AB2
vin1b_d5	Video Input 1 Port B Data input	I	AE3/ Y3
vin1b_d6	Video Input 1 Port B Data input	I	AC2/ Y4
vin1b_d7	Video Input 1 Port B Data input	I	AA2/ AA3
Video Input 2 (VIP1)			
vin2a_clk0	Video Input 2 Port A Clock input.	I	D4/ R3
vin2a_de0	Video Input 2 Port A Data Enable input	I	B4/ T5
vin2a fld0	Video Input 2 Port A Field ID input	I	B4/ E6/ R4
vin2b fld1	Video Input 2 Port B Field ID input	I	B4
vin2a_hsync0	Video Input 2 Port A Horizontal Sync input	I	D5/ T6
vin2a_vsync0	Video Input 2 Port A Vertical Sync input	I	C4/ T4
vin2a_d0	Video Input 2 Port A Data input	I	C3/ T1
vin2a_d1	Video Input 2 Port A Data input	I	B2/ R1
vin2a_d2	Video Input 2 Port A Data input	I	E7/ T2
vin2a_d3	Video Input 2 Port A Data input	I	B3/ R6
vin2a_d4	Video Input 2 Port A Data input	I	A3/ P6
vin2a_d5	Video Input 2 Port A Data input	I	C6/ U2

Table 4-4. VIP Signal Descriptions (continued)

SIGNAL NAME	DESCRIPTION	TYPE	BALL
vin2a_d6	Video Input 2 Port A Data input	I	A4/ U3
vin2a_d7	Video Input 2 Port A Data input	I	B5/ P5
vin2a_d8	Video Input 2 Port A Data input	I	C5/ U4
vin2a_d9	Video Input 2 Port A Data input	I	A7/ T3
vin2a_d10	Video Input 2 Port A Data input	I	A5/ R5
vin2a_d11	Video Input 2 Port A Data input	I	B6/ R2
vin2a_d12	Video Input 2 Port A Data input	I	E8
vin2a_d13	Video Input 2 Port A Data input	I	A6
vin2a_d14	Video Input 2 Port A Data input	I	C7
vin2a_d15	Video Input 2 Port A Data input	I	D6
vin2a_d16	Video Input 2 Port A Data input	I	B7
vin2a_d17	Video Input 2 Port A Data input	I	B8
vin2a_d18	Video Input 2 Port A Data input	I	A8
vin2a_d19	Video Input 2 Port A Data input	I	D7
vin2a_d20	Video Input 2 Port A Data input	I	C8
vin2a_d21	Video Input 2 Port A Data input	I	D8
vin2a_d22	Video Input 2 Port A Data input	I	F8
vin2a_d23	Video Input 2 Port A Data input	I	E9
vin2b_clk1	Video Input 2 Port B Clock input	I	E6/ V4
vin2b_de1	Video Input 2 Port B Data Enable input	I	B4/ W3
vin2b_hsync1	Video Input 2 Port B Horizontal Sync input	I	D5/ Y1
vin2b_vsync1	Video Input 2 Port B Vertical Sync input	I	C4/ W1
vin2b_d0	Video Input 2 Port B Data input	I	E9/ W6
vin2b_d1	Video Input 2 Port B Data input	I	F8/ V5
vin2b_d2	Video Input 2 Port B Data input	I	D8/ V3
vin2b_d3	Video Input 2 Port B Data input	I	C8/ U5
vin2b_d4	Video Input 2 Port B Data input	I	D7/ V6
vin2b_d5	Video Input 2 Port B Data input	I	A8/ U6
vin2b_d6	Video Input 2 Port B Data input	I	B8/ W4
vin2b_d7	Video Input 2 Port B Data input	I	B7/ W5
Video Input 3 (VIP2)			
vin3a_clk0	Video Input 3 Port A Clock input	I	AA6/ E11/ K2
vin3a_de0	Video Input 3 Port A Data Enable input	I	C8/ D13/ M6
vin3a fld0	Video Input 3 Port A Field ID input	I	D10/ D8/ N5
vin3a_hsync0	Video Input 3 Port A Horizontal Sync input	I	E12/ F8/ M1
vin3a_vsync0	Video Input 3 Port A Vertical Sync input	I	E13/ E9/ M3
vin3a_d0	Video Input 3 Port A Data input	I	AA2/ C11/ J4
vin3a_d1	Video Input 3 Port A Data input	I	AC2/ E10/ H6
vin3a_d2	Video Input 3 Port A Data input	I	D15/ G1/ Y3
vin3a_d3	Video Input 3 Port A Data input	I	AB2/ E15/ H2
vin3a_d4	Video Input 3 Port A Data input	I	AB1/ D9/ H3
vin3a_d5	Video Input 3 Port A Data input	I	AC1/ E14/ H4
vin3a_d6	Video Input 3 Port A Data input	I	AA1/ D14/ H5
vin3a_d7	Video Input 3 Port A Data input	I	D11/ F1/ Y2
vin3a_d8	Video Input 3 Port A Data input	I	A14/ B7/ G2
vin3a_d9	Video Input 3 Port A Data input	I	B11/ B8/ G3
vin3a_d10	Video Input 3 Port A Data input	I	A8/ B12/ G4

Table 4-4. VIP Signal Descriptions (continued)

SIGNAL NAME	DESCRIPTION	TYPE	BALL
vin3a_d11	Video Input 3 Port A Data input	I	B10/ D7/ G5
vin3a_d12	Video Input 3 Port A Data input	I	C14/ C8/ G6
vin3a_d13	Video Input 3 Port A Data input	I	C10/ D8/ F5
vin3a_d14	Video Input 3 Port A Data input	I	A10/ E5/ F8
vin3a_d15	Video Input 3 Port A Data input	I	C13/ E9/ F4
vin3a_d16	Video Input 3 Port A Data input	I	B9/ N3
vin3a_d17	Video Input 3 Port A Data input	I	A9/ P3
vin3a_d18	Video Input 3 Port A Data input	I	A11/ P1
vin3a_d19	Video Input 3 Port A Data input	I	C9/ P2
vin3a_d20	Video Input 3 Port A Data input	I	A13/ N2
vin3a_d21	Video Input 3 Port A Data input	I	A12/ N1
vin3a_d22	Video Input 3 Port A Data input	I	B14/ M5
vin3a_d23	Video Input 3 Port A Data input	I	B13/ M4
vin3b_clk1	Video Input 3 Port B Clock input	I	J3/ N6
vin3b_de1	Video Input 3 Port B Data Enable input	I	M2
vin3b fld1	Video Input 3 Port A Field ID input	I	J3
vin3b_hsync1	Video Input 3 Port A Horizontal Sync input	I	F3
vin3b_vsync1	Video Input 3 Port A Vertical Sync input	I	C1
vin3b_d0	Video Input 3 Port B Data input	I	C2
vin3b_d1	Video Input 3 Port B Data input	I	D3
vin3b_d2	Video Input 3 Port B Data input	I	D2
vin3b_d3	Video Input 3 Port B Data input	I	D1
vin3b_d4	Video Input 3 Port B Data input	I	E1
vin3b_d5	Video Input 3 Port B Data input	I	E2
vin3b_d6	Video Input 3 Port B Data input	I	E3
vin3b_d7	Video Input 3 Port B Data input	I	E4
Video Input 4 (VIP2)			
vin4b_clk1	Video Input 4 Port B Clock input	I	M6/ R3
vin4b_de1	Video Input 4 Port B Data Enable input	I	N5/ T5
vin4b fld1	Video Input 4 Port B Field ID input	I	L5/ R4
vin4b_hsync1	Video Input 4 Port B Horizontal Sync input	I	M1/ T6
vin4b_vsync1	Video Input 4 Port B Vertical Sync input	I	M3/ T4
vin4b_d0	Video Input 4 Port B Data input	I	N3/ T1
vin4b_d1	Video Input 4 Port B Data input	I	P3/ R1
vin4b_d2	Video Input 4 Port B Data input	I	P1/ T2
vin4b_d3	Video Input 4 Port B Data input	I	P2/ R6
vin4b_d4	Video Input 4 Port B Data input	I	N2/ P6
vin4b_d5	Video Input 4 Port B Data input	I	N1/ U2
vin4b_d6	Video Input 4 Port B Data input	I	M5/ U3
vin4b_d7	Video Input 4 Port B Data input	I	M4/ P5

NOTE**Support per device:**

- Vision Super: VIP1 + VIP2 + VIP3 : Full support
- Vision High: VIP1 + (VIN3a+VIN3b+VIN4b)
- Vision Mid: VIN1a+VIN1b+VIN2b

For more details on the device differentiation, refer to the [Table 3-1, Device Comparison](#).

4.4.2 Display Subsystem – Video Output Ports**CAUTION**

The I/O timings provided in [Section 7 Timing Requirements and Switching Characteristics](#) are valid only if signals within a single IOSET are used. The IOSETs are defined in the [Table 7-16](#) and [Table 7-17](#).

Table 4-5. DSS Signal Descriptions

SIGNAL NAME	DESCRIPTION	TYPE	BALL
DPI Video Output 1			
vout1_clk	Video Output 1 Clock output	O	D10
vout1_de	Video Output 1 Data Enable output	O	D13
vout1 fld	Video Output 1 Field ID output. This signal is not used for embedded sync modes.	O	E11
vout1_hsync	Video Output 1 Horizontal Sync output. This signal is not used for embedded sync modes.	O	E12
vout1_vsync	Video Output 1 Vertical Sync output. This signal is not used for embedded sync modes.	O	E13
vout1_d0	Video Output 1 Data output	O	B9
vout1_d1	Video Output 1 Data output	O	A9
vout1_d2	Video Output 1 Data output	O	A11
vout1_d3	Video Output 1 Data output	O	C9
vout1_d4	Video Output 1 Data output	O	A13
vout1_d5	Video Output 1 Data output	O	A12
vout1_d6	Video Output 1 Data output	O	B14
vout1_d7	Video Output 1 Data output	O	B13
vout1_d8	Video Output 1 Data output	O	A14
vout1_d9	Video Output 1 Data output	O	B11
vout1_d10	Video Output 1 Data output	O	B12
vout1_d11	Video Output 1 Data output	O	B10
vout1_d12	Video Output 1 Data output	O	C14
vout1_d13	Video Output 1 Data output	O	C10
vout1_d14	Video Output 1 Data output	O	A10
vout1_d15	Video Output 1 Data output	O	C13
vout1_d16	Video Output 1 Data output	O	C11
vout1_d17	Video Output 1 Data output	O	E10
vout1_d18	Video Output 1 Data output	O	D15
vout1_d19	Video Output 1 Data output	O	E15
vout1_d20	Video Output 1 Data output	O	D9

Table 4-5. DSS Signal Descriptions (continued)

SIGNAL NAME	DESCRIPTION	TYPE	BALL
vout1_d21	Video Output 1 Data output	O	E14
vout1_d22	Video Output 1 Data output	O	D14
vout1_d23	Video Output 1 Data output	O	D11
DPI Video Output 2			
vout2_clk	Video Output 2 Clock output	O	E6
vout2_d0	Video Output 2 Data output	O	E9
vout2_d1	Video Output 2 Data output	O	F8
vout2_d2	Video Output 2 Data output	O	D8
vout2_d3	Video Output 2 Data output	O	C8
vout2_d4	Video Output 2 Data output	O	D7
vout2_d5	Video Output 2 Data output	O	A8
vout2_d6	Video Output 2 Data output	O	B8
vout2_d7	Video Output 2 Data output	O	B7
vout2_d8	Video Output 2 Data output	O	D6
vout2_d9	Video Output 2 Data output	O	C7
vout2_d10	Video Output 2 Data output	O	A6
vout2_d11	Video Output 2 Data output	O	E8
vout2_d12	Video Output 2 Data output	O	B6
vout2_d13	Video Output 2 Data output	O	A5
vout2_d14	Video Output 2 Data output	O	A7
vout2_d15	Video Output 2 Data output	O	C5
vout2_d16	Video Output 2 Data output	O	B5, E24
vout2_d17	Video Output 2 Data output	O	A4, D23
vout2_d18	Video Output 2 Data output	O	C6, E25
vout2_d19	Video Output 2 Data output	O	A3, E23
vout2_d20	Video Output 2 Data output	O	B3, V1
vout2_d21	Video Output 2 Data output	O	E7, W2
vout2_d22	Video Output 2 Data output	O	B2, V2
vout2_d23	Video Output 2 Data output	O	C3, U1
vout2_de	Video Output 2 Data Enable output	O	B4
vout2_fid	Video Output 2 Field ID output. This signal is not used for embedded sync modes.	O	D4
vout2_hsync	Video Output 2 Horizontal Sync output. This signal is not used for embedded sync modes.	O	D5
vout2_vsync	Video Output 2 Vertical Sync output. This signal is not used for embedded sync modes.	O	C4
DPI Video Output 3			
vout3_clk	Video Output 3 Clock output	O	AD6 ⁽¹⁾ , K2
vout3_d0	Video Output 3 Data output	O	AD4 ⁽¹⁾ , J4, Y2 ⁽¹⁾
vout3_d1	Video Output 3 Data output	O	AA1 ⁽¹⁾ , AB5 ⁽¹⁾ , H6
vout3_d2	Video Output 3 Data output	O	AC1 ⁽¹⁾ , AE4 ⁽¹⁾ , G1
vout3_d3	Video Output 3 Data output	O	AB1 ⁽¹⁾ , AB7 ⁽¹⁾ , H2
vout3_d4	Video Output 3 Data output	O	AB2 ⁽¹⁾ , H3, Y5 ⁽¹⁾
vout3_d5	Video Output 3 Data output	O	AA5 ⁽¹⁾ , H4, Y3 ⁽¹⁾
vout3_d6	Video Output 3 Data output	O	AC2 ⁽¹⁾ , AE5 ⁽¹⁾ , H5
vout3_d7	Video Output 3 Data output	O	AA2 ⁽¹⁾ , AD5 ⁽¹⁾ , F1
vout3_d8	Video Output 3 Data output	O	AB3 ⁽¹⁾ , G2

Table 4-5. DSS Signal Descriptions (continued)

SIGNAL NAME	DESCRIPTION	TYPE	BALL
vout3_d9	Video Output 3 Data output	O	AD2 ⁽¹⁾ , G3
vout3_d10	Video Output 3 Data output	O	AC3 ⁽¹⁾ , G4
vout3_d11	Video Output 3 Data output	O	AD3 ⁽¹⁾ , G5
vout3_d12	Video Output 3 Data output	O	AA4 ⁽¹⁾ , G6
vout3_d13	Video Output 3 Data output	O	AE3 ⁽¹⁾ , F5
vout3_d14	Video Output 3 Data output	O	E5, Y4 ⁽¹⁾
vout3_d15	Video Output 3 Data output	O	AA3 ⁽¹⁾ , F4
vout3_d16	Video Output 3 Data output	O	AB6 ⁽¹⁾ , AD4 ⁽¹⁾ , N3
vout3_d17	Video Output 3 Data output	O	AA7 ⁽¹⁾ , AB5 ⁽¹⁾ , P3
vout3_d18	Video Output 3 Data output	O	AE4 ⁽¹⁾ , P1
vout3_d19	Video Output 3 Data output	O	AB7 ⁽¹⁾ , P2
vout3_d20	Video Output 3 Data output	O	N2, Y5 ⁽¹⁾
vout3_d21	Video Output 3 Data output	O	AA5 ⁽¹⁾ , N1
vout3_d22	Video Output 3 Data output	O	AE5 ⁽¹⁾ , M5
vout3_d23	Video Output 3 Data output	O	AD5 ⁽¹⁾ , M4
vout3_de	Video Output 3 Data Enable output	O	AA7 ⁽¹⁾ , M6
vout3_fid	Video Output 3 Field ID output. This signal is not used for embedded sync modes.	O	AB6 ⁽¹⁾ , N5
vout3_hsync	Video Output 3 Horizontal Sync output. This signal is not used for embedded sync modes.	O	AC6 ⁽¹⁾ , M1
vout3_vsync	Video Output 3 Vertical Sync output. This signal is not used for embedded sync modes.	O	AC5 ⁽¹⁾ , M3

(1) The VOUT3 interface when multiplexed onto balls mapped to the VDDSHV6 supply rail is restricted to operating in 1.8V mode only (i.e., VDDSHV6 must be supplied with 1.8V). 3.3V mode is not supported. This must be considered in the pin mux programming and VDDSHVx supply connections.

4.4.3 Display Subsystem – High-Definition Multimedia Interface (HDMI)

NOTE

For more information, see the Display Subsystem section of the device TRM.

Table 4-6. HDMI Signal Descriptions

SIGNAL NAME	DESCRIPTION	TYPE	BALL
hdmi1_cec	HDMI consumer electronic control	IOD	C24/ E21
hdmi1_hpd	HDMI display hot plug detect	I	C19/ E19
hdmi1_ddc_scl	HDMI display data channel clock	IOD	F22
hdmi1_ddc_sda	HDMI display data channel data	IOD	F23
hdmi1_clockx	HDMI clock differential positive or negative	ODS	AD13
hdmi1_clocky	HDMI clock differential positive or negative	ODS	AE13
hdmi1_data2x	HDMI data 2 differential positive or negative	ODS	AD16
hdmi1_data2y	HDMI data 2 differential positive or negative	ODS	AE16
hdmi1_data1x	HDMI data 1 differential positive or negative	ODS	AD15
hdmi1_data1y	HDMI data 1 differential positive or negative	ODS	AE15
hdmi1_data0x	HDMI data 0 differential positive or negative	ODS	AD14
hdmi1_data0y	HDMI data 0 differential positive or negative	ODS	AE14

4.4.4 External Memory Interface (EMIF)

NOTE

For more information, see the Memory Subsystem, EMIF Controller section of the device TRM.

Table 4-7. EMIF Signal Descriptions

SIGNAL NAME	DESCRIPTION	TYPE	BALL
ddr1_csn0	EMIF1 Chip Select 0	O	AC22
ddr1_cke	EMIF1 Clock Enable	O	AB19
ddr1_ck	EMIF1 Clock	O	AC25
ddr1_nck	EMIF1 Negative Clock	O	AC24
ddr1_odt0	EMIF1 On-Die Termination for Chip Select 0	O	AD23
ddr1_casn	EMIF1 Column Address Strobe	O	AC18
ddr1_rasn	EMIF1 Row Address Strobe	O	AE19
ddr1_wen	EMIF1 Write Enable	O	AD21
ddr1_rst	EMIF1 Reset output (DDR3-SDRAM only)	O	AD20
ddr1_ba0	EMIF1 Bank Address	O	AE18
ddr1_ba1	EMIF1 Bank Address	O	AE21
ddr1_ba2	EMIF1 Bank Address	O	AE23
ddr1_a0	EMIF1 Address Bus	O	AB18
ddr1_a1	EMIF1 Address Bus	O	AE20
ddr1_a2	EMIF1 Address Bus	O	AD24
ddr1_a3	EMIF1 Address Bus	O	AA18
ddr1_a4	EMIF1 Address Bus	O	AC21
ddr1_a5	EMIF1 Address Bus	O	AC20
ddr1_a6	EMIF1 Address Bus	O	AC23
ddr1_a7	EMIF1 Address Bus	O	AA19
ddr1_a8	EMIF1 Address Bus	O	AB20
ddr1_a9	EMIF1 Address Bus	O	AB23
ddr1_a10	EMIF1 Address Bus	O	AB22
ddr1_a11	EMIF1 Address Bus	O	AB25
ddr1_a12	EMIF1 Address Bus	O	AB24
ddr1_a13	EMIF1 Address Bus	O	AD17
ddr1_a14	EMIF1 Address Bus	O	AE17
ddr1_a15	EMIF1 Address Bus	O	AD18
ddr1_d0	EMIF1 Data Bus	IO	Y21
ddr1_d1	EMIF1 Data Bus	IO	Y24
ddr1_d2	EMIF1 Data Bus	IO	W24
ddr1_d3	EMIF1 Data Bus	IO	Y22
ddr1_d4	EMIF1 Data Bus	IO	W25
ddr1_d5	EMIF1 Data Bus	IO	Y25
ddr1_d6	EMIF1 Data Bus	IO	AA22
ddr1_d7	EMIF1 Data Bus	IO	AA21
ddr1_d8	EMIF1 Data Bus	IO	W21
ddr1_d9	EMIF1 Data Bus	IO	W22
ddr1_d10	EMIF1 Data Bus	IO	W23
ddr1_d11	EMIF1 Data Bus	IO	V23
ddr1_d12	EMIF1 Data Bus	IO	V22

Table 4-7. EMIF Signal Descriptions (continued)

SIGNAL NAME	DESCRIPTION	TYPE	BALL
ddr1_d13	EMIF1 Data Bus	IO	V21
ddr1_d14	EMIF1 Data Bus	IO	U23
ddr1_d15	EMIF1 Data Bus	IO	U22
ddr1_d16	EMIF1 Data Bus	IO	R22
ddr1_d17	EMIF1 Data Bus	IO	P23
ddr1_d18	EMIF1 Data Bus	IO	T21
ddr1_d19	EMIF1 Data Bus	IO	R25
ddr1_d20	EMIF1 Data Bus	IO	R24
ddr1_d21	EMIF1 Data Bus	IO	R21
ddr1_d22	EMIF1 Data Bus	IO	T22
ddr1_d23	EMIF1 Data Bus	IO	T25
ddr1_d24	EMIF1 Data Bus	IO	N21
ddr1_d25	EMIF1 Data Bus	IO	N25
ddr1_d26	EMIF1 Data Bus	IO	N24
ddr1_d27	EMIF1 Data Bus	IO	M22
ddr1_d28	EMIF1 Data Bus	IO	N23
ddr1_d29	EMIF1 Data Bus	IO	P22
ddr1_d30	EMIF1 Data Bus	IO	M21
ddr1_d31	EMIF1 Data Bus	IO	N22
ddr1_ecc_d0	EMIF1 ECC Data Bus	IO	M25
ddr1_ecc_d1	EMIF1 ECC Data Bus	IO	M24
ddr1_ecc_d2	EMIF1 ECC Data Bus	IO	J23
ddr1_ecc_d3	EMIF1 ECC Data Bus	IO	L22
ddr1_ecc_d4	EMIF1 ECC Data Bus	IO	K23
ddr1_ecc_d5	EMIF1 ECC Data Bus	IO	L24
ddr1_ecc_d6	EMIF1 ECC Data Bus	IO	L25
ddr1_ecc_d7	EMIF1 ECC Data Bus	IO	L21
ddr1_dqm0	EMIF1 Data Mask	O	AA20
ddr1_dqm1	EMIF1 Data Mask	O	U21
ddr1_dqm2	EMIF1 Data Mask	O	T24
ddr1_dqm3	EMIF1 Data Mask	O	P21
ddr1_dqm_ecc	EMIF1 ECC Data Mask	O	K22
ddr1_dqs0	Data strobe 0 input/output for byte 0 of the 32-bit data bus. This signal is output to the EMIF1 memory when writing and input when reading.	IO	AA25
ddr1_dqsn0	Data strobe 0 invert	IO	AA24
ddr1_dqs1	Data strobe 1 input/output for byte 1 of the 32-bit data bus. This signal is output to the EMIF1 memory when writing and input when reading.	IO	V25
ddr1_dqsn1	Data strobe 1 invert	IO	V24
ddr1_dqs2	Data strobe 2 input/output for byte 2 of the 32-bit data bus. This signal is output to the EMIF1 memory when writing and input when reading.	IO	U25
ddr1_dqsn2	Data strobe 2 invert	IO	U24
ddr1_dqs3	Data strobe 3 input/output for byte 3 of the 32-bit data bus. This signal is output to the EMIF1 memory when writing and input when reading.	IO	P25
ddr1_dqsn3	Data strobe 3 invert	IO	P24
ddr1_dqs_ecc	EMIF1 ECC Data strobe input/output. This signal is output to the EMIF1 memory when writing and input when reading.	IO	K25
ddr1_dqsn_ecc	EMIF1 ECC Complementary Data strobe	IO	K24
ddr1_vref0	Reference Power Supply EMIF1	A	AB21

NOTE

For more details on the device differentiation, refer to the [Table 3-1, Device Comparison](#).

NOTE

The index number 1 which is part of the EMIF1 signal prefix (ddr1_*) listed in [Figure 4-1, DDR2/DDR3/DDR3L SDRAM Signal Descriptions](#), column "SIGNAL NAME" not to be confused with DDR1 type of SDRAM memories.

4.4.5 General-Purpose Memory Controller (GPMC)

NOTE

For more information, see the Memory Subsystem, General-Purpose Memory Controller section of the device TRM.

Table 4-8. GPMC Signal Descriptions

SIGNAL NAME	DESCRIPTION	TYPE	BALL
gpmc_ad0	GPMC Data 0 in A/D nonmultiplexed mode and additionally Address 1 in A/D multiplexed mode	IO	J4
gpmc_ad1	GPMC Data 1 in A/D nonmultiplexed mode and additionally Address 2 in A/D multiplexed mode	IO	H6
gpmc_ad2	GPMC Data 2 in A/D nonmultiplexed mode and additionally Address 3 in A/D multiplexed mode	IO	G1
gpmc_ad3	GPMC Data 3 in A/D nonmultiplexed mode and additionally Address 4 in A/D multiplexed mode	IO	H2
gpmc_ad4	GPMC Data 4 in A/D nonmultiplexed mode and additionally Address 5 in A/D multiplexed mode	IO	H3
gpmc_ad5	GPMC Data 5 in A/D nonmultiplexed mode and additionally Address 6 in A/D multiplexed mode	IO	H4
gpmc_ad6	GPMC Data 6 in A/D nonmultiplexed mode and additionally Address 7 in A/D multiplexed mode	IO	H5
gpmc_ad7	GPMC Data 7 in A/D nonmultiplexed mode and additionally Address 8 in A/D multiplexed mode	IO	F1
gpmc_ad8	GPMC Data 8 in A/D nonmultiplexed mode and additionally Address 9 in A/D multiplexed mode	IO	G2
gpmc_ad9	GPMC Data 9 in A/D nonmultiplexed mode and additionally Address 10 in A/D multiplexed mode	IO	G3
gpmc_ad10	GPMC Data 10 in A/D nonmultiplexed mode and additionally Address 11 in A/D multiplexed mode	IO	G4
gpmc_ad11	GPMC Data 11 in A/D nonmultiplexed mode and additionally Address 12 in A/D multiplexed mode	IO	G5
gpmc_ad12	GPMC Data 12 in A/D nonmultiplexed mode and additionally Address 13 in A/D multiplexed mode	IO	G6
gpmc_ad13	GPMC Data 13 in A/D nonmultiplexed mode and additionally Address 14 in A/D multiplexed mode	IO	F5
gpmc_ad14	GPMC Data 14 in A/D nonmultiplexed mode and additionally Address 15 in A/D multiplexed mode	IO	E5
gpmc_ad15	GPMC Data 15 in A/D nonmultiplexed mode and additionally Address 16 in A/D multiplexed mode	IO	F4
gpmc_a0	GPMC Address 0. Only used to effectively address 8-bit data nonmultiplexed memories	O	L5/ N3
gpmc_a1	GPMC address 1 in A/D nonmultiplexed mode and Address 17 in A/D multiplexed mode	O	K2/ P3
gpmc_a2	GPMC address 2 in A/D nonmultiplexed mode and Address 18 in A/D multiplexed mode	O	J5/ P1
gpmc_a3	GPMC address 3 in A/D nonmultiplexed mode and Address 19 in A/D multiplexed mode	O	J3/ P2
gpmc_a4	GPMC address 4 in A/D nonmultiplexed mode and Address 20 in A/D multiplexed mode	O	N2
gpmc_a5	GPMC address 5 in A/D nonmultiplexed mode and Address 21 in A/D multiplexed mode	O	N1
gpmc_a6	GPMC address 6 in A/D nonmultiplexed mode and Address 22 in A/D multiplexed mode	O	M5
gpmc_a7	GPMC address 7 in A/D nonmultiplexed mode and Address 23 in A/D multiplexed mode	O	M4

Table 4-8. GPMC Signal Descriptions (continued)

SIGNAL NAME	DESCRIPTION	TYPE	BALL
gpmc_a8	GPMC address 8 in A/D nonmultiplexed mode and Address 24 in A/D multiplexed mode	O	M1
gpmc_a9	GPMC address 9 in A/D nonmultiplexed mode and Address 25 in A/D multiplexed mode	O	M3
gpmc_a10	GPMC address 10 in A/D nonmultiplexed mode and Address 26 in A/D multiplexed mode	O	M6
gpmc_a11	GPMC address 11 in A/D nonmultiplexed mode and unused in A/D multiplexed mode	O	N5
gpmc_a12	GPMC address 12 in A/D nonmultiplexed mode and unused in A/D multiplexed mode	O	L5
gpmc_a13	GPMC address 13 in A/D nonmultiplexed mode and unused in A/D multiplexed mode	O	C2/ L4
gpmc_a14	GPMC address 14 in A/D nonmultiplexed mode and unused in A/D multiplexed mode	O	D3/ L3
gpmc_a15	GPMC address 15 in A/D nonmultiplexed mode and unused in A/D multiplexed mode	O	D2/ L2
gpmc_a16	GPMC address 16 in A/D nonmultiplexed mode and unused in A/D multiplexed mode	O	D1/ L1
gpmc_a17	GPMC address 17 in A/D nonmultiplexed mode and unused in A/D multiplexed mode	O	E1/ K6
gpmc_a18	GPMC address 18 in A/D nonmultiplexed mode and unused in A/D multiplexed mode	O	E2/ K5
gpmc_a19	GPMC address 19 in A/D nonmultiplexed mode and unused in A/D multiplexed mode	O	C2 ⁽³⁾ / E3
gpmc_a20	GPMC address 20 in A/D nonmultiplexed mode and unused in A/D multiplexed mode	O	D3 ⁽³⁾ / E4
gpmc_a21	GPMC address 21 in A/D nonmultiplexed mode and unused in A/D multiplexed mode	O	D2 ⁽³⁾ / F3
gpmc_a22	GPMC address 22 in A/D nonmultiplexed mode and unused in A/D multiplexed mode	O	C1 / D1 ⁽³⁾
gpmc_a23	GPMC address 23 in A/D nonmultiplexed mode and unused in A/D multiplexed mode	O	AA4/ E1/ J5
gpmc_a24	GPMC address 24 in A/D nonmultiplexed mode and unused in A/D multiplexed mode	O	AD3 / E2 ⁽³⁾
gpmc_a25	GPMC address 25 in A/D nonmultiplexed mode and unused in A/D multiplexed mode	O	AC3 / E3 ⁽³⁾
gpmc_a26	GPMC address 26 in A/D nonmultiplexed mode and unused in A/D multiplexed mode	O	AD2 / E4 ⁽³⁾
gpmc_a27	GPMC address 27 in A/D nonmultiplexed mode and Address 27 in A/D multiplexed mode	O	AB3 / F3 ⁽³⁾
gpmc_cs0	GPMC Chip Select 0 (active low)	O	K4
gpmc_cs1	GPMC Chip Select 1 (active low)	O	C1
gpmc_cs2	GPMC Chip Select 2 (active low)	O	K3
gpmc_cs3	GPMC Chip Select 3 (active low)	O	K2
gpmc_cs4	GPMC Chip Select 4 (active low)	O	M2
gpmc_cs5	GPMC Chip Select 5 (active low)	O	J3
gpmc_cs6	GPMC Chip Select 6 (active low)	O	J5
gpmc_cs7	GPMC Chip Select 7 (active low)	O	N6
gpmc_clk ⁽¹⁾⁽²⁾	GPMC Clock output	IO	N6
gpmc_advn_ale	GPMC address valid active low or address latch enable	O	J5
gpmc_oen_ren	GPMC output enable active low or read enable	O	H1
gpmc_wen	GPMC write enable active low	O	F2
gpmc_ben0	GPMC lower-byte enable active low	O	M2
gpmc_ben1	GPMC upper-byte enable active low	O	J3

Table 4-8. GPMC Signal Descriptions (continued)

SIGNAL NAME	DESCRIPTION	TYPE	BALL
gpmc_wait0	GPMC external indication of wait 0	I	K1
gpmc_wait1	GPMC external indication of wait 1	I	J5/ N6

- (1) This clock signal is implemented as 'pad loopback' inside the device - the output signal is looped back through the input buffer to serve as the internal reference signal. Series termination is recommended (as close to device pin as possible) to improve signal integrity of the clock input. Any nonmonotonicity in voltage that occurs at the pad loopback clock pin between V_{IH} and V_{IL} must be less than V_{HYS} .
- (2) The gpio6_16.clkout1 signal can be used as an "always-on" alternative to gpmc_clk provided that the external device can support the associated timing. See [Table 7-22 GPMC/NOR Flash Interface Switching Characteristics - Synchronous Mode - Default](#) and [Table 7-24 GPMC/NOR Flash Interface Switching Characteristics - Synchronous Mode - Alternate](#) for timing information.
- (3) The internal pull resistors for balls C2, D3, D2, D1, E2, E3, E4, F3 are permanently disabled when sysboot15 is set to 1 as described in the section *Sysboot Configuration* of the Device TRM. If internal pull-up/down resistors are desired on these balls then sysboot15 should be set to 0. If gpmc boot mode is used with SYSBOOT15=1 (not recommended) then external pull-downs should be implemented to keep the address bus at logic-0 value during boot since the gpmc ms-address bits are high-z during boot.

4.4.6 Timers

NOTE

For more information, see the Timers section of the device TRM.

Table 4-9. Timers Signal Descriptions

SIGNAL NAME	DESCRIPTION	TYPE	BALL
timer1	PWM output/event trigger input	IO	J3
timer2	PWM output/event trigger input	IO	M2
timer3	PWM output/event trigger input	IO	J5
timer4	PWM output/event trigger input	IO	N6
timer5	PWM output/event trigger input	IO	L2/ A16
timer6	PWM output/event trigger input	IO	L3/ A17
timer7	PWM output/event trigger input	IO	L4/ A19
timer8	PWM output/event trigger input	IO	L5/ A20
timer9	PWM output/event trigger input	IO	N5/ A21
timer10	PWM output/event trigger input	IO	M6/ A23
timer11	PWM output/event trigger input	IO	M3/ C15
timer12	PWM output/event trigger input	IO	M1/ B16
timer13	PWM output/event trigger input	IO	AC5/ C23
timer14	PWM output/event trigger input	IO	AC6/ C22
timer15	PWM output/event trigger input	IO	AD6
timer16	PWM output/event trigger input	IO	AA7/ AE6

4.4.7 Inter-Integrated Circuit Interface (I2C)

NOTE

For more information, see the Serial Communication Interface, I2C section of the device TRM.

NOTE

I2C1 and I2C2 do not support HS Mode.

Table 4-10. I²C Signal Descriptions

SIGNAL NAME	DESCRIPTION	TYPE	BALL
Inter-Integrated Circuit Interface (I2C1)			
i2c1_scl	I2C1 Clock	IOD	G24
i2c1_sda	I2C1 Data	IOD	G25
Inter-Integrated Circuit Interface (I2C2)			
i2c2_scl	I2C2 Clock	IOD	F23
i2c2_sda	I2C2 Data	IOD	F22
Inter-Integrated Circuit Interface (I2C3)			
i2c3_scl	I2C3 Clock	IOD	B24/ N6/ W1
i2c3_sda	I2C3 Data	IOD	C25/ J5/ Y1
Inter-Integrated Circuit Interface (I2C4)			
i2c4_scl	I2C4 Clock	IOD	D23/ N3
i2c4_sda	I2C4 Data	IOD	E24/ P3
Inter-Integrated Circuit Interface (I2C5)			
i2c5_scl	I2C5 Clock	IOD	A15/ N2/ W2
i2c5_sda	I2C5 Data	IOD	B15/ N1/ V1

4.4.8 Universal Asynchronous Receiver Transmitter (UART)

NOTE

For more information see the Serial Communication Interface /UART/IrDA/CIR section of the device TRM.

Table 4-11. UART Signal Descriptions

SIGNAL NAME	DESCRIPTION	TYPE	BALL
Universal Asynchronous Receiver/Transmitter (UART1)			
uart1_dcdn	UART1 Data Carrier Detect active low	I	H23
uart1_dsrn	UART1 Data Set Ready Active Low	I	J25
uart1_dtrn	UART1 Data Terminal Ready Active Low	O	J22
uart1_rin	UART1 Ring Indicator	I	J24
uart1_rxd	UART1 Receive Data	I	G23
uart1_txd	UART1 Transmit Data	O	H22
uart1_ctsn	UART1 clear to send active low	I	H25
uart1_rtsn	UART1 request to send active low	O	H24
Universal Asynchronous Receiver/Transmitter (UART2)			
uart2_rxd	UART2 Receive Data	I	H23
uart2_txd	UART2 Transmit Data	O	J25
uart2_ctsn	UART2 clear to send active low	I	J22
uart2_rtsn	UART2 request to send active low	O	J24
Universal Asynchronous Receiver/Transmitter (UART3)/IrDA			
uart3_rxd	UART3 Receive Data for both normal UART mode and IrDA mode.	I	F24/ R1/ V2 / J22
uart3_txd	UART3 Transmit Data	O	F25/ J24/ T2/ U1
uart3_ctsn	UART3 clear to send active low	I	E16/ H23/ R6/ T1
uart3_rtsn	UART3 request to send active low	O	D17/ J25/ P6/ R3
uart3_rctx	Remote control data	O	H23
uart3_sd	Infrared transceiver configure/shutdown	O	J25
uart3_irtx	Infrared data output	O	J24
Universal Asynchronous Receiver/Transmitter (UART4)			

Table 4-11. UART Signal Descriptions (continued)

SIGNAL NAME	DESCRIPTION	TYPE	BALL
uart4_rxd	UART4 Receive Data	I	C19/ E25/ T5
uart4_txd	UART4 Transmit Data	O	C24/ E23/ T6
uart4_ctsn	UART4 clear to send active low	I	T4
uart4_rtsn	UART4 request to send active low	O	R5
Universal Asynchronous Receiver/Transmitter (UART5)			
uart5_rxd	UART5 Receive Data	I	B9/ C17/ E16/ N3/ U6
uart5_txd	UART5 Transmit Data	O	A9/ C20/ D17/ P3/ V6
uart5_ctsn	UART5 clear to send active low	I	P1/ U5
uart5_rtsn	UART5 request to send active low	O	P2/ V3
Universal Asynchronous Receiver/Transmitter (UART6)			
uart6_rxd	UART6 Receive Data	I	A14/ B15/ N2
uart6_txd	UART6 Transmit Data	O	A15/ B11/ N1
uart6_ctsn	UART6 clear to send active low	I	M5
uart6_rtsn	UART6 request to send active low	O	M4
Universal Asynchronous Receiver/Transmitter (UART7)			
uart7_rxd	UART7 Receive Data	I	AA7/ B19/ C11/ P1
uart7_txd	UART7 Transmit Data	O	AD6/ C16/ E10/ P2
uart7_ctsn	UART7 clear to send active low	I	AC6/ C17
uart7_rtsn	UART7 request to send active low	O	AC5/ C20
Universal Asynchronous Receiver/Transmitter (UART8)			
uart8_rxd	UART8 Receive Data	I	AD5/ E19/ E24/ M5
uart8_txd	UART8 Transmit Data	O	AE5/ D23/ E21/ M4
uart8_ctsn	UART8 clear to send active low	I	AA5/ E25
uart8_rtsn	UART8 request to send active low	O	E23/ Y5
Universal Asynchronous Receiver/Transmitter (UART9)			
uart9_rxd	UART9 Receive Data	I	D5/ H25/ V1
uart9_txd	UART9 Transmit Data	O	C4/ H24/ W2
uart9_ctsn	UART9 clear to send active low	I	C3/ V2
uart9_rtsn	UART9 request to send active low	O	B2/ U1
Universal Asynchronous Receiver/Transmitter (UART10)			
uart10_rxd	UART10 Receive Data	I	E7/ J22/ V5
uart10_txd	UART10 Transmit Data	O	B3/ J24/ W6
uart10_ctsn	UART10 clear to send active low	I	A3/ W3
uart10_rtsn	UART10 request to send active low	O	C6/ V4

4.4.9 Multichannel Serial Peripheral Interface (McSPI)

CAUTION

The I/O timings provided in [Section 7 Timing Requirements and Switching Characteristics](#) are applicable for all combinations of signals for SPI1 and SPI2. However, the timings are valid only for SPI3 and SPI4 if signals within a single IOSET are used. The IOSETS are defined in the [Table 7-37](#).

NOTE

For more information, see the Serial Communication Interface, McSPI section of the device TRM.

Table 4-12. SPI Signal Descriptions

SIGNAL NAME	DESCRIPTION	TYPE	BALL
Serial Peripheral Interface 1			
spi1_sclk ⁽¹⁾	SPI1 Clock	IO	C18
spi1_d1	SPI1 Data. Can be configured as either MISO or MOSI.	IO	C21
spi1_d0	SPI1 Data. Can be configured as either MISO or MOSI.	IO	E22
spi1_cs0	SPI1 Chip Select	IO	D22
spi1_cs1	SPI1 Chip Select	IO	D16
spi1_cs2	SPI1 Chip Select	IO	C19
spi1_cs3	SPI1 Chip Select	IO	C24
Serial Peripheral Interface 2			
spi2_sclk ⁽¹⁾	SPI2 Clock	IO	F24
spi2_d1	SPI2 Data. Can be configured as either MISO or MOSI.	IO	F25
spi2_d0	SPI2 Data. Can be configured as either MISO or MOSI.	IO	E16
spi2_cs0	SPI2 Chip Select	IO	D17
spi2_cs1	SPI2 Chip Select	IO	D16
spi2_cs2	SPI2 Chip Select	IO	C19
spi2_cs3	SPI2 Chip Select	IO	C24
Serial Peripheral Interface 3			
spi3_sclk ⁽¹⁾	SPI3 Clock	IO	A16/ AA7/ E13/ E24/ R1/ W4
spi3_d1	SPI3 Data. Can be configured as either MISO or MOSI.	IO	A17/ AD6/ D13/ D23/ T2/ U6
spi3_d0	SPI3 Data. Can be configured as either MISO or MOSI.	IO	A19/ AC6/ E12/ E25/ R6/ V6
spi3_cs0	SPI3 Chip Select	IO	A20/ AC5/ D10/ E23/ P6/ U5
spi3_cs1	SPI3 Chip Select	IO	A21/ E11/ V3
spi3_cs2	SPI3 Chip Select	IO	B9
spi3_cs3	SPI3 Chip Select	IO	D11
Serial Peripheral Interface 4			
spi4_sclk ⁽¹⁾	SPI4 Clock	IO	D5/ M1/ T5/ V1/ V5
spi4_d1	SPI4 Data. Can be configured as either MISO or MOSI.	IO	C4/ M3/ T6/ W2/ W6
spi4_d0	SPI4 Data. Can be configured as either MISO or MOSI.	IO	C3/ M6/ T4/ V2/ W3
spi4_cs0	SPI4 Chip Select	IO	B2/ N5/ R5/ U1/ V4
spi4_cs1	SPI4 Chip Select	IO	L5/ T2
spi4_cs2	SPI4 Chip Select	IO	L4/ R6
spi4_cs3	SPI4 Chip Select	IO	L3/ P6

- (1) This clock signal is implemented as 'pad loopback' inside the device - the output signal is looped back through the input buffer to serve as the internal reference signal. Series termination is recommended (as close to device pin as possible) to improve signal integrity of the clock input. Any nonmonotonicity in voltage that occurs at the pad loopback clock pin between V_{IH} and V_{IL} must be less than V_{HYS} .

4.4.10 Quad Serial Peripheral Interface (QSPI)

NOTE

For more information see the Serial Communication Interface / Quad Serial Peripheral Interface section of the device TRM.

Table 4-13. QSPI Signal Descriptions

SIGNAL NAME	DESCRIPTION	TYPE	BALL
qspi1_sclk	QSPI1 Serial Clock	IO	K5
qspi1_rtclk	QSPI1 Return Clock Input. Must be connected from QSPI1_SCLK on PCB. Refer to PCB Guidelines for QSPI1	I	L4
qspi1_d0	QSPI1 Data[0]. This pin is output data for all commands/writes and for dual read and quad read modes it becomes input data pin during read phase.	IO	L1
qspi1_d1	QSPI1 Data[1]. Input read data in all modes.	I	K6
qspi1_d2	QSPI1 Data[2]. This pin is used only in quad read mode as input data pin during read phase	I	L2
qspi1_d3	QSPI1 Data[3]. This pin is used only in quad read mode as input data pin during read phase	I	L3
qspi1_cs0	QSPI1 Chip Select[0]. This pin is Used for QSPI1 boot modes	O	K3
qspi1_cs1	QSPI1 Chip Select[1]	O	K2
qspi1_cs2	QSPI1 Chip Select[2]	O	P2
qspi1_cs3	QSPI1 Chip Select[3]	O	N2

4.4.11 Multichannel Audio Serial Port (McASP)

NOTE

For more information, see the Serial Communication Interface, Multichannel Audio Serial Port (McASP) section of the device TRM.

Table 4-14. McASP Signal Descriptions

SIGNAL NAME	DESCRIPTION	TYPE	BALL
Multichannel Audio Serial Port 1			
mcasp1_axr0	McASP1 Transmit/Receive Data	IO	B15
mcasp1_axr1	McASP1 Transmit/Receive Data	IO	A15
mcasp1_axr4	McASP1 Transmit/Receive Data	IO	C23
mcasp1_axr5	McASP1 Transmit/Receive Data	IO	C22
mcasp1_axr8	McASP1 Transmit/Receive Data	IO	A16
mcasp1_axr9	McASP1 Transmit/Receive Data	IO	A17
mcasp1_axr10	McASP1 Transmit/Receive Data	IO	A19
mcasp1_axr11	McASP1 Transmit/Receive Data	IO	A20
mcasp1_axr12	McASP1 Transmit/Receive Data	IO	A21
mcasp1_axr13	McASP1 Transmit/Receive Data	IO	A23
mcasp1_axr14	McASP1 Transmit/Receive Data	IO	C15
mcasp1_axr15	McASP1 Transmit/Receive Data	IO	B16
mcasp1_fsx	McASP1 Transmit Frame Sync	IO	B24
mcasp1_ahclkx	McASP1 Transmit High-Frequency Master Clock	O	C23
mcasp1_aclkx ⁽¹⁾	McASP1 Transmit Bit Clock	IO	C25

Table 4-14. McASP Signal Descriptions (continued)

SIGNAL NAME	DESCRIPTION	TYPE	BALL
Multichannel Audio Serial Port 2			
mcasp2_aclkx	McASP2 Transmit Bit Clock	IO	B21
mcasp2_ahclkx ⁽¹⁾	McASP2 Transmit High-Frequency Master Clock	O	C22
mcasp2_axr2	McASP2 Transmit/Receive Data	IO	B23
mcasp2_axr3	McASP2 Transmit/Receive Data	IO	B17
mcasp2_axr8	McASP2 Transmit/Receive Data	IO	C23
mcasp2_axr9	McASP2 Transmit/Receive Data	IO	C22
mcasp2_axr12	McASP2 Transmit/Receive Data	IO	B19
mcasp2_axr13	McASP2 Transmit/Receive Data	IO	C16
mcasp2_axr14	McASP2 Transmit/Receive Data	IO	C17
mcasp2_axr15	McASP2 Transmit/Receive Data	IO	C20
mcasp2_fsx	McASP2 Transmit Frame Sync	IO	B20
Multichannel Audio Serial Port 3			
mcasp3_aclkr	McASP3 Receive Bit Clock	IO	B19
mcasp3_aclkx ⁽¹⁾	McASP3 Transmit Bit Clock	IO	B19
mcasp3_axr0	McASP3 Transmit/Receive Data	IO	C17
mcasp3_axr1	McASP3 Transmit/Receive Data	IO	C20
mcasp3_axr2	McASP3 Transmit/Receive Data	IO	B23
mcasp3_axr3	McASP3 Transmit/Receive Data	IO	B17
mcasp3_fsr	McASP3 Receive Frame Sync	IO	C16
mcasp3_fsx	McASP3 Transmit Frame Sync	IO	C16
Multichannel Audio Serial Port 4			
mcasp4_aclkr	McASP4 Receive Bit Clock	IO	E24
mcasp4_aclkx ⁽¹⁾	McASP4 Transmit Bit Clock	IO	E24
mcasp4_axr0	McASP4 Transmit/Receive Data	IO	E25
mcasp4_axr1	McASP4 Transmit/Receive Data	IO	E23
mcasp4_fsr	McASP4 Receive Frame Sync	IO	D23
mcasp4_fsx	McASP4 Transmit Frame Sync	IO	D23
Multichannel Audio Serial Port 5			
mcasp5_aclkr	McASP5 Receive Bit Clock	IO	V1
mcasp5_aclkx ⁽¹⁾	McASP5 Transmit Bit Clock	IO	V1
mcasp5_ahclkx	McASP5 Transmit High-Frequency Master Clock	O	C23
mcasp5_axr0	McASP5 Transmit/Receive Data	IO	V2
mcasp5_axr1	McASP5 Transmit/Receive Data	IO	U1
mcasp5_fsr	McASP5 Receive Frame Sync	IO	W2
mcasp5_fsx	McASP5 Transmit Frame Sync	IO	W2
Multichannel Audio Serial Port 6			
mcasp6_aclkr	McASP6 Receive Bit Clock	IO	A19
mcasp6_aclkx ⁽¹⁾	McASP6 Transmit Bit Clock	IO	A19
mcasp6_ahclkx	McASP6 Transmit High-Frequency Master Clock	O	C22
mcasp6_axr0	McASP6 Transmit/Receive Data	IO	A16
mcasp6_axr1	McASP6 Transmit/Receive Data	IO	A17
mcasp6_fsr	McASP6 Receive Frame Sync	IO	A20
mcasp6_fsx	McASP6 Transmit Frame Sync	IO	A20
Multichannel Audio Serial Port 7			
mcasp7_aclkr	McASP7 Receive Bit Clock	IO	C15
mcasp7_aclkx ⁽¹⁾	McASP7 Transmit Bit Clock	IO	C15

Table 4-14. McASP Signal Descriptions (continued)

SIGNAL NAME	DESCRIPTION	TYPE	BALL
mcasp7_axr0	McASP7 Transmit/Receive Data	IO	A21
mcasp7_axr1	McASP7 Transmit/Receive Data	IO	A23
mcasp7_fsr	McASP7 Receive Frame Sync	IO	B16
mcasp7_fsx	McASP7 Transmit Frame Sync	IO	B16

(1) This clock signal is implemented as 'pad loopback' inside the device - the output signal is looped back through the input buffer to serve as the internal reference signal. Series termination is recommended (as close to device pin as possible) to improve signal integrity of the clock input. Any nonmonotonicity in voltage that occurs at the pad loopback clock pin between V_{IH} and V_{IL} must be less than V_{HYS} .

4.4.12 Universal Serial Bus (USB)

NOTE

For more information, see: Serial Communication Interface / SuperSpeed USB DRD Subsystem section of the device TRM.

Table 4-15. Universal Serial Bus Signal Descriptions

SIGNAL NAME	DESCRIPTION	TYPE	BALL
Universal Serial Bus 1			
usb1_dm	USB1 USB2.0 differential signal pair (negative)	IODS	AD8
usb1_dp	USB1 USB2.0 differential signal pair (positive)	IODS	AE8
usb1_drvvbus	USB1 Drive VBUS signal	O	AE6
usb_rxn0 ⁽¹⁾	USB1 USB3.0 receiver negative lane	IDS	AE9
usb_rxp0 ⁽¹⁾	USB1 USB3.0 receiver positive lane	IDS	AD9
usb_txn0 ⁽¹⁾	USB1 USB3.0 transmitter negative lane	ODS	AE7
usb_txp0 ⁽¹⁾	USB1 USB3.0 transmitter positive lane	ODS	AD7
Universal Serial Bus 3			
usb3_ulpi_clk	USB3 - ULPI functional clock	I	V4, Y2
usb3_ulpi_d0	USB1 USB3.0 transmitter negative lane	IO	AB2, V3
usb3_ulpi_d1	USB3 - ULPI 8-bit data bus	IO	U5, Y3
usb3_ulpi_d2	USB3 - ULPI 8-bit data bus	IO	AC2, V6
usb3_ulpi_d3	USB3 - ULPI 8-bit data bus	IO	AA2, U6
usb3_ulpi_d4	USB3 - ULPI 8-bit data bus	IO	AB3, W4
usb3_ulpi_d5	USB3 - ULPI 8-bit data bus	IO	AD2, W5
usb3_ulpi_d6	USB3 - ULPI 8-bit data bus	IO	AC3, W1
usb3_ulpi_d7	USB3 - ULPI 8-bit data bus	IO	AD3, Y1
usb3_ulpi_dir	USB3 - ULPI bus direction	I	AC1, W6
usb3_ulpi_nxt	USB3 - ULPI next	I	AB1, V5
usb3_ulpi_stp	USB3 - ULPI stop	O	AA1, W3
Universal Serial Bus 4			
usb4_ulpi_clk	USB4 - ULPI functional clock	I	R6
usb4_ulpi_d0	USB4 - ULPI 8-bit data bus	IO	T4
usb4_ulpi_d1	USB4 - ULPI 8-bit data bus	IO	R5
usb4_ulpi_d2	USB4 - ULPI 8-bit data bus	IO	U2
usb4_ulpi_d3	USB4 - ULPI 8-bit data bus	IO	U3
usb4_ulpi_d4	USB4 - ULPI 8-bit data bus	IO	P5
usb4_ulpi_d5	USB4 - ULPI 8-bit data bus	IO	U4
usb4_ulpi_d6	USB4 - ULPI 8-bit data bus	IO	T3
usb4_ulpi_d7	USB4 - ULPI 8-bit data bus	IO	R4
usb4_ulpi_dir	USB4 - ULPI bus direction	I	T5

Table 4-15. Universal Serial Bus Signal Descriptions (continued)

SIGNAL NAME	DESCRIPTION	TYPE	BALL
usb4_ulpi_nxt	USB4 - ULPI next	I	T6
usb4_ulpi_stp	USB4 - ULPI stop	O	P6

(1) USB 3.0 Super Speed mode is NOT supported on this device

4.4.13 Peripheral Component Interconnect Express (PCIe)

NOTE

For more information, see the Serial Communication Interfaces, PCIe section of the device TRM.

Table 4-16. PCIe Signal Descriptions

SIGNAL NAME	DESCRIPTION	TYPE	BALL
pcie_rxn0	PCIe1_PHY_RX Receive Data Lane 0 (negative) - mapped to PCIe_SS1 only.	IDS	AD10
pcie_rxp0	PCIe1_PHY_RX Receive Data Lane 0 (positive) - mapped to PCIe_SS1 only.	IDS	AE10
pcie_txn0	PCIe1_PHY_TX Transmit Data Lane 0 (negative) - mapped to PCIe_SS1 only.	ODS	AD11
pcie_txp0	PCIe1_PHY_TX Transmit Data Lane 0 (positive) - mapped to PCIe_SS1 only.	ODS	AE11
ljcb_clkp	PCIe1_PHY / PCIe2_PHY shared Reference Clock Input / Output Differential Pair (positive)	IODS	AE12
ljcb_clkn	PCIe1_PHY / PCIe2_PHY shared Reference Clock Input / Output Differential Pair (negative)	IODS	AD12

4.4.14 Controller Area Network Interface (DCAN)

NOTE

For more information / see the Serial Communication Interface / DCAN section of the device TRM.

Table 4-17. DCAN Signal Descriptions

SIGNAL NAME	DESCRIPTION	TYPE	BALL
DCAN 1			
dcan1_tx	DCAN1 transmit data pin	IO	E19
dcan1_rx	DCAN1 receive data pin	IO	AA16/ E21
DCAN 2			
dcan2_tx	DCAN2 transmit data pin	IO	C19
dcan2_rx	DCAN2 receive data pin	IO	AA17/ C24

4.4.15 Ethernet Interface (GMAC_SW)

CAUTION

The I/O timings provided in [Section 7, Timing Requirements and Switching Characteristics](#) are valid only if signals within a single IOSET are used. The IOSETs are defined in the [Table 7-66](#), [Table 7-69](#), [Table 7-74](#) and [Table 7-81](#).

NOTE

For more information, see the Serial Communication Interfaces, Ethernet Controller section of the device TRM.

Table 4-18. GMAC Signal Descriptions

SIGNAL NAME	DESCRIPTION	TYPE	BALL
RGMIIO			
rgmii0_txc	RGMIIO Transmit Clock	O	R6
rgmii0_txctl	RGMIIO Transmit Enable	O	P6
rgmii0_txd3	RGMIIO Transmit Data	O	T5
rgmii0_txd2	RGMIIO Transmit Data	O	T6
rgmii0_txd1	RGMIIO Transmit Data	O	T4
rgmii0_txd0	RGMIIO Transmit Data	O	R5
rgmii0_rxc	RGMIIO Receive Clock	I	U2
rgmii0_rxctl	RGMIIO Receive Control	I	U3
rgmii0_rxd3	RGMIIO Receive Data	I	P5
rgmii0_rxd2	RGMIIO Receive Data	I	U4
rgmii0_rxd1	RGMIIO Receive Data	I	T3
rgmii0_rxd0	RGMIIO Receive Data	I	R4
RGMI1			
rgmii1_rxc	RGMI1 Receive Clock	I	A8
rgmii1_rxctl	RGMI1 Receive Control	I	D7
rgmii1_rxd0	RGMI1 Receive Data	I	E9
rgmii1_rxd1	RGMI1 Receive Data	I	F8
rgmii1_rxd2	RGMI1 Receive Data	I	D8
rgmii1_rxd3	RGMI1 Receive Data	I	C8
rgmii1_txc	RGMI1 Transmit Clock	O	E8
rgmii1_txctl	RGMI1 Transmit Enable	O	A6
rgmii1_txd0	RGMI1 Transmit Data	O	B8
rgmii1_txd1	RGMI1 Transmit Data	O	B7
rgmii1_txd2	RGMI1 Transmit Data	O	D6
rgmii1_txd3	RGMI1 Transmit Data	O	C7
MII0			
mii0_rxd1	MII0 Receive Data	I	T4
mii0_rxd2	MII0 Receive Data	I	P6
mii0_rxd3	MII0 Receive Data	I	R6
mii0_rxd0	MII0 Receive Data	I	R5
mii0_rxclk	MII0 Receive Clock	I	T2
mii0_rxdv	MII0 Receive Data Valid	I	R1
mii0_txclk	MII0 Transmit Clock	I	U2
mii0_txd0	MII0 Transmit Data	O	R4
mii0_txd1	MII0 Transmit Data	O	T3
mii0_txd2	MII0 Transmit Data	O	P5
mii0_txd3	MII0 Transmit Data	O	U3
mii0_txer	MII0 Transmit Error	I	T1
mii0_rxer	MII0 Receive Data Error	I	T6
mii0_col	MII0 Collision Detect (Sense)	I	R3
mii0_crs	MII0 Carrier Sense	I	T5

Table 4-18. GMAC Signal Descriptions (continued)

SIGNAL NAME	DESCRIPTION	TYPE	BALL
mii0_txen	MII0 Transmit Data Enable	O	U4
MII1			
mii1_col	MII1 Collision Detect (Sense)	I	D8
mii1_crs	MII1 Carrier Sense	I	F8
mii1_rxclk	MII1 Receive Clock	I	E8
mii1_rxd0	MII1 Receive Data	I	A7
mii1_rxd1	MII1 Receive Data	I	A4
mii1_rxd2	MII1 Receive Data	I	B5
mii1_rxd3	MII1 Receive Data	I	C5
mii1_rxdv	MII1 Receive Data Valid	I	A6
mii1_rxer	MII1 Receive Data Error	I	C8
mii1_txclk	MII1 Transmit Clock	I	C7
mii1_txd0	MII1 Transmit Data	O	D6
mii1_txd1	MII1 Transmit Data	O	B7
mii1_txd2	MII1 Transmit Data	O	B8
mii1_txd3	MII1 Transmit Data	O	A8
mii1_txen	MII1 Transmit Data Enable	O	E9
mii1_txer	MII1 Transmit Error	I	D7
RMII0			
rmii0_crs	RMII0 Carrier Sense	I	T5
rmii0_rxer	RMII0 Receive Data Error	I	T6
rmii0_rxd1	RMII0 Receive Data	I	T4
rmii0_rxd0	RMII0 Receive Data	I	R5
rmii0_txen	RMII0 Transmit Data Enable	O	U4
rmii0_txd1	RMII0 Transmit Data	O	T3
rmii0_txd0	RMII0 Transmit Data	O	R4
RMII1			
rmii1_crs	RMII1 Carrier Sense	I	R1
rmii1_rxd0	RMII1 Receive Data	I	P6
rmii1_rxd1	RMII1 Receive Data	I	R6
rmii1_rxer	RMII1 Receive Data Error	I	T2
rmii1_txd0	RMII1 Transmit Data	O	P5
rmii1_txd1	RMII1 Transmit Data	O	U3
rmii1_txen	RMII1 Transmit Data Enable	O	U2
MDIO			
mdio_mclk	MDIO Clock	O	A5/ C19/ R3/ Y1
mdio_d	MDIO Data	O	B6/ C24/ T1/ W1

4.4.16 eMMC/SD/SDIO

NOTE

For more information, see the HS MMC/SDIO section of the device TRM.

Table 4-19. eMMC/SD/SDIO Signal Descriptions

SIGNAL NAME	DESCRIPTION	TYPE	BALL
Multi Media Card 2			

Table 4-19. eMMC/SD/SDIO Signal Descriptions (continued)

SIGNAL NAME	DESCRIPTION	TYPE	BALL
mmc2_clk ⁽¹⁾	MMC2 clock	IO	E1
mmc2_cmd	MMC2 command	IO	C1
mmc2_dat0	MMC2 data bit 0	IO	E2
mmc2_dat1	MMC2 data bit 1	IO	E3
mmc2_dat2	MMC2 data bit 2	IO	E4
mmc2_dat3	MMC2 data bit 3	IO	F3
mmc2_dat4	MMC2 data bit 4	IO	C2
mmc2_dat5	MMC2 data bit 5	IO	D3
mmc2_dat6	MMC2 data bit 6	IO	D2
mmc2_dat7	MMC2 data bit 7	IO	D1
mmc2_sdc	MMC2 Card Detect	I	E19
mmc2_sdwp	MMC2 Write Protect	I	E21
Multi Media Card 3			
mmc3_clk ⁽¹⁾	MMC3 clock	IO	W5
mmc3_cmd	MMC3 command	IO	W4
mmc3_dat0	MMC3 data bit 0	IO	U6
mmc3_dat1	MMC3 data bit 1	IO	V6
mmc3_dat2	MMC3 data bit 2	IO	U5
mmc3_dat3	MMC3 data bit 3	IO	V3
mmc3_dat4	MMC3 data bit 4	IO	V5
mmc3_dat5	MMC3 data bit 5	IO	W6
mmc3_dat6	MMC3 data bit 6	IO	W3
mmc3_dat7	MMC3 data bit 7	IO	V4
mmc3_sdc	MMC3 Card Detect	I	C19
mmc3_sdwp	MMC3 Write Protect	I	C24
Multi Media Card 4			
mmc4_clk ⁽¹⁾	MMC4 clock	IO	H25
mmc4_cmd	MMC4 command	IO	H24
mmc4_dat0	MMC4 data bit 0	IO	H23
mmc4_dat1	MMC4 data bit 1	IO	J25
mmc4_dat2	MMC4 data bit 2	IO	J22
mmc4_dat3	MMC4 data bit 3	IO	J24
mmc4_sdc	MMC4 Card Detect	I	G23
mmc4_sdwp	MMC4 Write Protect	I	H22

(1) By default, this clock signal is implemented as 'pad loopback' inside the device - the output signal is looped back through the input buffer to serve as the internal reference signal. mmc2_clk has an optional software programmable setting to use an 'internal loopback clock' instead of the default 'pad loopback clock'. If the 'pad loopback clock' is used, series termination is recommended (as close to device pin as possible) to improve signal integrity of the clock input. Any nonmonotonicity in voltage that occurs at the pad loopback clock pin between V_{IH} and V_{IL} must be less than V_{HYS} .

4.4.17 General-Purpose Interface (GPIO)

NOTE

For more information, see the General-Purpose Interface section of the device TRM.

Table 4-20. GPIOs Signal Descriptions

SIGNAL NAME	DESCRIPTION	TYPE	BALL
GPIO 1			

Table 4-20. GPIOs Signal Descriptions (continued)

SIGNAL NAME	DESCRIPTION	TYPE	BALL
gpio1_0	General-Purpose Input	I	AA16
gpio1_1	General-Purpose Input	I	AA17
gpio1_2	General-Purpose Input	I	AB17
gpio1_3	General-Purpose Input	I	AC17
gpio1_6	General-Purpose Input/Output	IO	J4
gpio1_7	General-Purpose Input/Output	IO	H6
gpio1_8	General-Purpose Input/Output	IO	G1
gpio1_9	General-Purpose Input/Output	IO	H2
gpio1_10	General-Purpose Input/Output	IO	H3
gpio1_11	General-Purpose Input/Output	IO	H4
gpio1_12	General-Purpose Input/Output	IO	H5
gpio1_13	General-Purpose Input/Output	IO	F1
gpio1_14	General-Purpose Input/Output	IO	E19
gpio1_15	General-Purpose Input/Output	IO	E21
gpio1_16	General-Purpose Input/Output	IO	J22
gpio1_17	General-Purpose Input/Output	IO	J24
gpio1_18	General-Purpose Input/Output	IO	G6
gpio1_19	General-Purpose Input/Output	IO	F5
gpio1_20	General-Purpose Input/Output	IO	E5
gpio1_21	General-Purpose Input/Output	IO	F4
gpio1_22	General-Purpose Input/Output	IO	V5
gpio1_23	General-Purpose Input/Output	IO	W6
gpio1_24	General-Purpose Input/Output	IO	W3
gpio1_25	General-Purpose Input/Output	IO	V4
gpio1_26	General-Purpose Input/Output	IO	N2
gpio1_27	General-Purpose Input/Output	IO	N1
gpio1_28	General-Purpose Input/Output	IO	M5
gpio1_29	General-Purpose Input/Output	IO	M4
gpio1_30	General-Purpose Input/Output	IO	M1
gpio1_31	General-Purpose Input/Output	IO	M3
GPIO 2			
gpio2_0	General-Purpose Input/Output	IO	M6
gpio2_1	General-Purpose Input/Output	IO	N5
gpio2_2	General-Purpose Input/Output	IO	L5
gpio2_3	General-Purpose Input/Output	IO	L4
gpio2_4	General-Purpose Input/Output	IO	L3
gpio2_5	General-Purpose Input/Output	IO	L2
gpio2_6	General-Purpose Input/Output	IO	L1
gpio2_7	General-Purpose Input/Output	IO	K6
gpio2_8	General-Purpose Input/Output	IO	K5
gpio2_9	General-Purpose Input/Output	IO	C2
gpio2_10	General-Purpose Input/Output	IO	D3
gpio2_11	General-Purpose Input/Output	IO	D2
gpio2_12	General-Purpose Input/Output	IO	D1
gpio2_13	General-Purpose Input/Output	IO	E1
gpio2_14	General-Purpose Input/Output	IO	E2
gpio2_15	General-Purpose Input/Output	IO	E3

Table 4-20. GPIOs Signal Descriptions (continued)

SIGNAL NAME	DESCRIPTION	TYPE	BALL
gpio2_16	General-Purpose Input/Output	IO	E4
gpio2_17	General-Purpose Input/Output	IO	F3
gpio2_18	General-Purpose Input/Output	IO	C1
gpio2_19	General-Purpose Input/Output	IO	K4
gpio2_20	General-Purpose Input/Output	IO	K3
gpio2_21	General-Purpose Input/Output	IO	K2
gpio2_22	General-Purpose Input/Output	IO	N6
gpio2_23	General-Purpose Input/Output	IO	J5
gpio2_24	General-Purpose Input/Output	IO	H1
gpio2_25	General-Purpose Input/Output	IO	F2
gpio2_26	General-Purpose Input/Output	IO	M2
gpio2_27	General-Purpose Input/Output	IO	J3
gpio2_28	General-Purpose Input/Output	IO	K1
gpio2_30	General-Purpose Input/Output	IO	AB6
gpio2_31	General-Purpose Input/Output	IO	AA6
GPIO 3			
gpio3_0	General-Purpose Input/Output	IO	AA7
gpio3_1	General-Purpose Input/Output	IO	AD6
gpio3_2	General-Purpose Input/Output	IO	AC6
gpio3_3	General-Purpose Input/Output	IO	AC5
gpio3_4	General-Purpose Input/Output	IO	AD5
gpio3_5	General-Purpose Input/Output	IO	AE5
gpio3_6	General-Purpose Input/Output	IO	AA5
gpio3_7	General-Purpose Input/Output	IO	Y5
gpio3_8	General-Purpose Input/Output	IO	AB7
gpio3_9	General-Purpose Input/Output	IO	AE4
gpio3_10	General-Purpose Input/Output	IO	AB5
gpio3_11	General-Purpose Input/Output	IO	AD4
gpio3_12	General-Purpose Input/Output	IO	AA3
gpio3_13	General-Purpose Input/Output	IO	Y4
gpio3_14	General-Purpose Input/Output	IO	AE3
gpio3_15	General-Purpose Input/Output	IO	AA4
gpio3_16	General-Purpose Input/Output	IO	AD3
gpio3_17	General-Purpose Input/Output	IO	AC3
gpio3_18	General-Purpose Input/Output	IO	AD2
gpio3_19	General-Purpose Input/Output	IO	AB3
gpio3_20	General-Purpose Input/Output	IO	AA2
gpio3_21	General-Purpose Input/Output	IO	AC2
gpio3_22	General-Purpose Input/Output	IO	Y3
gpio3_23	General-Purpose Input/Output	IO	AB2
gpio3_24	General-Purpose Input/Output	IO	AB1
gpio3_25	General-Purpose Input/Output	IO	AC1
gpio3_26	General-Purpose Input/Output	IO	AA1
gpio3_27	General-Purpose Input/Output	IO	Y2
gpio3_28	General-Purpose Input/Output	IO	D4
gpio3_29	General-Purpose Input/Output	IO	B4
gpio3_30	General-Purpose Input/Output	IO	E6

Table 4-20. GPIOs Signal Descriptions (continued)

SIGNAL NAME	DESCRIPTION	TYPE	BALL
gpio3_31	General-Purpose Input/Output	IO	D5
GPIO 4			
gpio4_0	General-Purpose Input/Output	IO	C4
gpio4_1	General-Purpose Input/Output	IO	C3
gpio4_2	General-Purpose Input/Output	IO	B2
gpio4_3	General-Purpose Input/Output	IO	E7
gpio4_4	General-Purpose Input/Output	IO	B3
gpio4_5	General-Purpose Input/Output	IO	A3
gpio4_6	General-Purpose Input/Output	IO	C6
gpio4_7	General-Purpose Input/Output	IO	A4
gpio4_8	General-Purpose Input/Output	IO	B5
gpio4_9	General-Purpose Input/Output	IO	C5
gpio4_10	General-Purpose Input/Output	IO	A7
gpio4_11	General-Purpose Input/Output	IO	A5
gpio4_12	General-Purpose Input/Output	IO	B6
gpio4_13	General-Purpose Input/Output	IO	E8
gpio4_14	General-Purpose Input/Output	IO	A6
gpio4_15	General-Purpose Input/Output	IO	C7
gpio4_16	General-Purpose Input/Output	IO	D6
gpio4_17	General-Purpose Input/Output	IO	A20
gpio4_18	General-Purpose Input/Output	IO	A21
gpio4_19	General-Purpose Input/Output	IO	D10
gpio4_20	General-Purpose Input/Output	IO	D13
gpio4_21	General-Purpose Input/Output	IO	E11
gpio4_22	General-Purpose Input/Output	IO	E12
gpio4_23	General-Purpose Input/Output	IO	E13
gpio4_24	General-Purpose Input/Output	IO	B7
gpio4_25	General-Purpose Input/Output	IO	B8
gpio4_26	General-Purpose Input/Output	IO	A8
gpio4_27	General-Purpose Input/Output	IO	D7
gpio4_28	General-Purpose Input/Output	IO	C8
gpio4_29	General-Purpose Input/Output	IO	D8
gpio4_30	General-Purpose Input/Output	IO	F8
gpio4_31	General-Purpose Input/Output	IO	E9
GPIO 5			
gpio5_2	General-Purpose Input/Output	IO	B15
gpio5_3	General-Purpose Input/Output	IO	A15
gpio5_10	General-Purpose Input/Output	IO	A16
gpio5_11	General-Purpose Input/Output	IO	A17
gpio5_12	General-Purpose Input/Output	IO	A19
gpio5_13	General-Purpose Input/Output	IO	B19
gpio5_14	General-Purpose Input/Output	IO	C16
gpio5_15	General-Purpose Input/Output	IO	R3
gpio5_16	General-Purpose Input/Output	IO	T1
gpio5_17	General-Purpose Input/Output	IO	R2
gpio5_18	General-Purpose Input/Output	IO	R1
gpio5_19	General-Purpose Input/Output	IO	T2

Table 4-20. GPIOs Signal Descriptions (continued)

SIGNAL NAME	DESCRIPTION	TYPE	BALL
gpio5_20	General-Purpose Input/Output	IO	R6
gpio5_21	General-Purpose Input/Output	IO	P6
gpio5_22	General-Purpose Input/Output	IO	T5
gpio5_23	General-Purpose Input/Output	IO	T6
gpio5_24	General-Purpose Input/Output	IO	T4
gpio5_25	General-Purpose Input/Output	IO	R5
gpio5_26	General-Purpose Input/Output	IO	U2
gpio5_27	General-Purpose Input/Output	IO	U3
gpio5_28	General-Purpose Input/Output	IO	P5
gpio5_29	General-Purpose Input/Output	IO	U4
gpio5_30	General-Purpose Input/Output	IO	T3
gpio5_31	General-Purpose Input/Output	IO	R4
GPIO 6			
gpio6_4	General-Purpose Input/Output	IO	A23
gpio6_5	General-Purpose Input/Output	IO	C15
gpio6_6	General-Purpose Input/Output	IO	B16
gpio6_8	General-Purpose Input/Output	IO	B23
gpio6_9	General-Purpose Input/Output	IO	B17
gpio6_10	General-Purpose Input/Output	IO	Y1
gpio6_11	General-Purpose Input/Output	IO	W1
gpio6_12	General-Purpose Input/Output	IO	AE6
gpio6_17	General-Purpose Input/Output	IO	C23
gpio6_18	General-Purpose Input/Output	IO	C22
gpio6_29	General-Purpose Input/Output	IO	W5
gpio6_30	General-Purpose Input/Output	IO	W4
gpio6_31	General-Purpose Input/Output	IO	U6
GPIO 7			
gpio7_0	General-Purpose Input/Output	IO	V6
gpio7_1	General-Purpose Input/Output	IO	U5
gpio7_2	General-Purpose Input/Output	IO	V3
gpio7_3	General-Purpose Input/Output	IO	N3
gpio7_4	General-Purpose Input/Output	IO	P3
gpio7_5	General-Purpose Input/Output	IO	P1
gpio7_6	General-Purpose Input/Output	IO	P2
gpio7_7	General-Purpose Input/Output	IO	C18
gpio7_8	General-Purpose Input/Output	IO	C21
gpio7_9	General-Purpose Input/Output	IO	E22
gpio7_10	General-Purpose Input/Output	IO	D22
gpio7_11	General-Purpose Input/Output	IO	D16
gpio7_12	General-Purpose Input/Output	IO	C19
gpio7_13	General-Purpose Input/Output	IO	C24
gpio7_14	General-Purpose Input/Output	IO	F24
gpio7_15	General-Purpose Input/Output	IO	F25
gpio7_16	General-Purpose Input/Output	IO	E16
gpio7_17	General-Purpose Input/Output	IO	D17
gpio7_18	General-Purpose Input/Output	IO	G2
gpio7_19	General-Purpose Input/Output	IO	G3

Table 4-20. GPIOs Signal Descriptions (continued)

SIGNAL NAME	DESCRIPTION	TYPE	BALL
gpio7_22	General-Purpose Input/Output	IO	G23
gpio7_23	General-Purpose Input/Output	IO	H22
gpio7_24	General-Purpose Input/Output	IO	H25
gpio7_25	General-Purpose Input/Output	IO	H24
gpio7_26	General-Purpose Input/Output	IO	H23
gpio7_27	General-Purpose Input/Output	IO	J25
gpio7_28	General-Purpose Input/Output	IO	G4
gpio7_29	General-Purpose Input/Output	IO	G5
gpio7_30	General-Purpose Input/Output	IO	B24
gpio7_31	General-Purpose Input/Output	IO	C25
GPIO 8			
gpio8_0	General-Purpose Input/Output	IO	B9
gpio8_1	General-Purpose Input/Output	IO	A9
gpio8_2	General-Purpose Input/Output	IO	A11
gpio8_3	General-Purpose Input/Output	IO	C9
gpio8_4	General-Purpose Input/Output	IO	A13
gpio8_5	General-Purpose Input/Output	IO	A12
gpio8_6	General-Purpose Input/Output	IO	B14
gpio8_7	General-Purpose Input/Output	IO	B13
gpio8_8	General-Purpose Input/Output	IO	A14
gpio8_9	General-Purpose Input/Output	IO	B11
gpio8_10	General-Purpose Input/Output	IO	B12
gpio8_11	General-Purpose Input/Output	IO	B10
gpio8_12	General-Purpose Input/Output	IO	C14
gpio8_13	General-Purpose Input/Output	IO	C10
gpio8_14	General-Purpose Input/Output	IO	A10
gpio8_15	General-Purpose Input/Output	IO	C13
gpio8_16	General-Purpose Input/Output	IO	C11
gpio8_17	General-Purpose Input/Output	IO	E10
gpio8_18	General-Purpose Input/Output	IO	D15
gpio8_19	General-Purpose Input/Output	IO	E15
gpio8_20	General-Purpose Input/Output	IO	D9
gpio8_21	General-Purpose Input/Output	IO	E14
gpio8_22	General-Purpose Input/Output	IO	D14
gpio8_23	General-Purpose Input/Output	IO	D11
gpio8_27	General-Purpose Input	I	D20
gpio8_28	General-Purpose Input/Output	IO	F21
gpio8_29	General-Purpose Input/Output	IO	D19
gpio8_30	General-Purpose Input/Output	IO	E20
gpio8_31	General-Purpose Input/Output	IO	D21

4.4.18 Pulse Width Modulation (PWM) Interface

NOTE

For more information, see the Pulse-Width Modulation (PWM) SS section of the device TRM.

Table 4-21. PWM Signal Descriptions

SIGNAL NAME	DESCRIPTION	TYPE	BALL
PWMSS1			
eCAP1_in_PWM1_out	ECAP1 Capture Input / PWM Output	IO	E7, Y5
ehrpwm1A	EHRPWM1 Output A	O	AD5, C4
ehrpwm1B	EHRPWM1 Output B	O	AE5, C3
ehrpwm1_syncl	EHRPWM1 Sync Input	I	AB7, B3
ehrpwm1_synco	EHRPWM1 Sync Output	O	A3, AE4
ehrpwm1_tripzone_in put	EHRPWM1 Trip Zone Input	IO	AA5, B2
eQEP1A_in	EQEP1 Quadrature Input A	I	AA7, D4
eQEP1B_in	EQEP1 Quadrature Input B	I	AD6, B4
eQEP1_index	EQEP1 Index Input	IO	AC6, E6
eQEP1_strobe	EQEP1 Strobe Input	IO	AC5, D5
PWMSS2			
eCAP2_in_PWM2_out	ECAP2 Capture Input / PWM Output	IO	E8, W4
ehrpwm2A	EHRPWM2 Output A	O	A7, Y1
ehrpwm2B	EHRPWM2 Output B	O	A5, W1
ehrpwm2_tripzone_in put	EHRPWM2 Trip Zone Input	IO	B6, W5
eQEP2A_in	EQEP2 Quadrature Input A	I	AB5, C6
eQEP2B_in	EQEP2 Quadrature Input B	I	A4, AD4
eQEP2_index	EQEP2 Index Input	IO	AA3, B5
eQEP2_strobe	EQEP2 Strobe Input	IO	C5, Y4
PWMSS3			
eCAP3_in_PWM3_out	ECAP3 Capture Input / PWM Output	IO	C8, V4
ehrpwm3A	EHRPWM3 Output A	O	B8, V5
ehrpwm3B	EHRPWM3 Output B	O	A8, W6
ehrpwm3_tripzone_in put	EHRPWM3 Trip Zone Input	IO	D7, W3
eQEP3A_in	EQEP3 Quadrature Input A	I	A6, U6
eQEP3B_in	EQEP3 Quadrature Input B	I	C7, V6
eQEP3_index	EQEP3 Index Input	IO	D6, U5
eQEP3_strobe	EQEP3 Strobe Input	IO	B7, V3

4.4.19 System and Miscellaneous

4.4.19.1 Sysboot Interface

NOTE

For more information, see the Initialization (ROM Code) section of the device TRM.

Table 4-22. Sysboot Signal Descriptions

SIGNAL NAME	DESCRIPTION	TYPE	BALL
sysboot0	Boot Mode Configuration 0. The value latched on this pin upon porz reset release will determine the boot mode configuration of the device.	I	J4
sysboot1	Boot Mode Configuration 1. The value latched on this pin upon porz reset release will determine the boot mode configuration of the device.	I	H6
sysboot2	Boot Mode Configuration 2. The value latched on this pin upon porz reset release will determine the boot mode configuration of the device.	I	G1
sysboot3	Boot Mode Configuration 3. The value latched on this pin upon porz reset release will determine the boot mode configuration of the device.	I	H2
sysboot4	Boot Mode Configuration 4. The value latched on this pin upon porz reset release will determine the boot mode configuration of the device.	I	H3
sysboot5	Boot Mode Configuration 5. The value latched on this pin upon porz reset release will determine the boot mode configuration of the device.	I	H4
sysboot6	Boot Mode Configuration 6. The value latched on this pin upon porz reset release will determine the boot mode configuration of the device.	I	H5
sysboot7	Boot Mode Configuration 7. The value latched on this pin upon porz reset release will determine the boot mode configuration of the device.	I	F1
sysboot8	Boot Mode Configuration 8. The value latched on this pin upon porz reset release will determine the boot mode configuration of the device.	I	G2
sysboot9	Boot Mode Configuration 9. The value latched on this pin upon porz reset release will determine the boot mode configuration of the device.	I	G3
sysboot10	Boot Mode Configuration 10. The value latched on this pin upon porz reset release will determine the boot mode configuration of the device.	I	G4
sysboot11	Boot Mode Configuration 11. The value latched on this pin upon porz reset release will determine the boot mode configuration of the device.	I	G5
sysboot12	Boot Mode Configuration 12. The value latched on this pin upon porz reset release will determine the boot mode configuration of the device.	I	G6
sysboot13	Boot Mode Configuration 13. The value latched on this pin upon porz reset release will determine the boot mode configuration of the device.	I	F5
sysboot14	Boot Mode Configuration 14. The value latched on this pin upon porz reset release will determine the boot mode configuration of the device.	I	E5
sysboot15	Boot Mode Configuration 15. The value latched on this pin upon porz reset release will determine the boot mode configuration of the device.	I	F4

4.4.19.2 Power, Reset, and Clock Management (PRCM)

NOTE

For more information, see PRCM section of the device TRM.

Table 4-23. PRCM Signal Descriptions

SIGNAL NAME	DESCRIPTION	TYPE	BALL
clkout1	Device Clock output 1. Can be used externally for devices with non-critical timing requirements, or for debug, or as a reference clock on GPMC as described in Table 7-22 GPMC/NOR Flash Interface Switching Characteristics - Synchronous Mode - Default and Table 7-24 GPMC/NOR Flash Interface Switching Characteristics - Synchronous Mode - Alternate .	O	N6

Table 4-23. PRCM Signal Descriptions (continued)

SIGNAL NAME	DESCRIPTION	TYPE	BALL
clkout2	Device Clock output 2. Can be used externally for devices with non-critical timing requirements, or for debug.	O	C23/ J5
rstoutn	Reset out (Active low). This pin asserts low in response to any global reset condition on the device. ⁽²⁾	O	G21
resetrn	Device Reset Input	I	H21
porz	Power on Reset (active low). This pin must be asserted low until all device supplies are valid (see reset sequence/requirements)	I	F17
xref_clk0	External Reference Clock 0. For Audio and other Peripherals.	I	C23
xref_clk1	External Reference Clock 1. For Audio and other Peripherals.	I	C22
xi_osc0	System Oscillator OSC0 Crystal input / LVCMOS clock input. Functions as the input connection to a crystal when the internal oscillator OSC0 is used. Functions as an LVCMOS-compatible input clock when an external oscillator is used	I	AC14
xo_osc0	System Oscillator OSC0 Crystal output	O	AB14
xi_osc1	Auxiliary Oscillator OSC1 Crystal input / LVCMOS clock input. Functions as the input connection to a crystal when the internal oscillator OSC1 is used. Functions as an LVCMOS-compatible input clock when an external oscillator is used	I	AC13
xo_osc1	Auxiliary Oscillator OSC1 Crystal output	O	AB13
RMII_MHZ_50_CLK ⁽¹⁾	RMII Reference Clock (50MHz). This pin is an input when external reference is used or output when internal reference is used.	IO	R2

- (1) This clock signal is implemented as 'pad loopback' inside the device - the output signal is looped back through the input buffer to serve as the internal reference signal. Series termination is recommended (as close to device pin as possible) to improve signal integrity of the clock input. Any nonmonotonicity in voltage that occurs at the pad loopback clock pin between V_{IH} and V_{IL} must be less than V_{HYS} .
- (2) Note that rstoutn is only valid after vddshv3 is valid. If the rstoutn signal will be used as a reset into other devices attached to the SOC, it must be AND'ed with porz. This will prevent glitches occurring during supply ramping being propagated.

4.4.19.3 Real Time Clock (RTC) Interface

NOTE

For more information, see the Real Time Clock (RTC) SS section of the device TRM.

Table 4-24. RTC Signal Descriptions

SIGNAL NAME	DESCRIPTION	TYPE	BALL
on_off	RTC Power Enable output pin	O	AA11
rtc_iso ⁽¹⁾	RTC domain isolation signal	I	AA9
Wakeup0	RTC External Wakeup Input 0	I	AA16
Wakeup1	RTC External Wakeup Input 1	I	AA17
Wakeup2	RTC External Wakeup Input 2	I	AB17
Wakeup3	RTC External Wakeup Input 3	I	AC17
rtc_osc_xi_clkin3_2	RTC Oscillator Input. Crystal connection to internal RTC oscillator. Functions as an RTC clock input when an external oscillator is used.	I	AA13
rtc_osc_xo	RTC Oscillator Output	O	AA12
rtc_porz	RTC Power Domain Power-On Reset Input	I	AA10

- (1) This signal must be kept 0 if device power supplies are not valid during RTC mode and 1 during normal operation. This can typically be achieved by connecting rtc_iso to the same signal driving porz (not rtc_porz) with appropriate voltage level translation if necessary.

4.4.19.4 System Direct Memory Access (SDMA)

NOTE

For more information, see the DMA Controllers, System DMA section of the device TRM.

Table 4-25. System DMA Signal Descriptions

SIGNAL NAME	DESCRIPTION	TYPE	BALL
dma_evt1	Enhanced DMA Event Input 1	I	L5/ N6
dma_evt2	Enhanced DMA Event Input 2	I	J5/ L4
dma_evt3	Enhanced DMA Event Input 3	I	M2
dma_evt4	Enhanced DMA Event Input 4	I	J3

4.4.19.5 Interrupt Controllers (INTC)

NOTE

For more information, see the Interrupt Controllers section of the device TRM.

Table 4-26. INTC Signal Descriptions

SIGNAL NAME	DESCRIPTION	TYPE	BALL
nmin_dsp	Non maskable interrupt input, active-low. This pin can be optionally routed to the DSP NMI input or as generic input to the ARM cores. Note that by default this pin has an internal pulldown resistor enabled. This internal pulldown should be disabled or countered by a stronger external pullup resistor before routing to the DSP or ARM processors.	I	G22
sys_nirq2	External interrupt event to any device INTC	I	AB17
sys_nirq1	External interrupt event to any device INTC	I	AC17

4.4.19.6 Observability

NOTE

For more information, see the Control Module section of the device TRM.

Table 4-27. Observability Signal Descriptions

SIGNAL NAME	DESCRIPTION	TYPE	BALL
obs0	Observation Output 0	O	A11
obs1	Observation Output 1	O	C9
obs2	Observation Output 2	O	A13
obs3	Observation Output 3	O	A12
obs4	Observation Output 4	O	B14
obs5	Observation Output 5	O	B12
obs6	Observation Output 6	O	B10
obs7	Observation Output 7	O	C14
obs8	Observation Output 8	O	C10
obs9	Observation Output 9	O	A10
obs10	Observation Output 10	O	C13
obs11	Observation Output 11	O	D15
obs12	Observation Output 12	O	E15
obs13	Observation Output 13	O	D9
obs14	Observation Output 14	O	E14
obs15	Observation Output 15	O	D14
obs16	Observation Output 16	O	A11
obs17	Observation Output 17	O	C9
obs18	Observation Output 18	O	A13
obs19	Observation Output 19	O	A12

Table 4-27. Observability Signal Descriptions (continued)

SIGNAL NAME	DESCRIPTION	TYPE	BALL
obs20	Observation Output 20	O	B14
obs21	Observation Output 21	O	B12
obs22	Observation Output 22	O	B10
obs23	Observation Output 23	O	C14
obs24	Observation Output 24	O	C10
obs25	Observation Output 25	O	A10
obs26	Observation Output 26	O	C13
obs27	Observation Output 27	O	D15
obs28	Observation Output 28	O	E15
obs29	Observation Output 29	O	D9
obs30	Observation Output 30	O	E14
obs31	Observation Output 31	O	D14
obs_dmarq1	DMA Request External Observation Output 1	O	C9
obs_dmarq2	DMA Request External Observation Output 2	O	B10
obs_irq1	IRQ External Observation Output 1	O	A11
obs_irq2	IRQ External Observation Output 2	O	B12

4.4.19.7 Power Supplies**NOTE**

For more information, see Power, Reset, and Clock Management, PRCM Subsystem Environment, External Voltage Inputs section of the device TRM.

Table 4-28. Power Supply Signal Descriptions

SIGNAL NAME	DESCRIPTION	TYPE	BALL
vdd	Core voltage domain supply	PWR	H9/ H10/ H13/ H14/ J19/ K19/ M12/ M13/ M14/ N9/ N12/ N13/ N14/ N15/ P9/ P10/ P12/ P15/ P16/ R8/ R10/ R12/ R15/ R16/ T11/ T12/ T13/ T15/ V18/ W14/ W15/ W16
vss	Ground	GND	A1/ A18/ A22/ A25/ C12/ D25/ F6/ F10/ F14/ F19/ G20/ H11/ J1/ J11/ J14/ J16/ J17/ J20/ K11/ K14/ K20/ L10/ L11/ L12/ L13/ L15/ M10/ M11/ M15/ M19/ M23/ N8/ N10/ N11/ N16/ N17/ P4/ P8/ P13/ P17/ R9/ R11/ R14/ R17/ T8/ T9/ T10/ T14/ T16/ T19/ T23/ U7/ U13/ U14/ U15/ U16/ V14/ V15/ V16/ V17/ W10/ W13/ W17/ Y10/ Y19/ AA23/ AB4/ AC8/ AC19/ AE1/ AE22/ AE25
vdd_dspeve	DSP-EVE voltage domain supply	PWR	M9/ L9/ K13/ J13/ K12/ J12/ H12/ K10/ J10/ L9/ J9/ J8

Table 4-28. Power Supply Signal Descriptions (continued)

SIGNAL NAME	DESCRIPTION	TYPE	BALL
vdd_iva	IVA voltage domain supply	PWR	U17/ U18/ U19/ T17/ T18
vdd_gpu	GPU voltage domain supply	PWR	U8/ U9/ U10/ U11/ U12/ V9/ V10/ V11/ V12/ V13/ W9/ W11/ W12
vdd_mpu	MPU voltage domain supply	PWR	J15/ K15/ K16/ L16/ L17/ M16/ M17/ M18/ L18/ L19/ K18/ K17/ J18/ H19/ H18/ H17/ H16/ H15
vdd_rtc	RTC voltage domain supply	PWR	Y13
vdda_usb1	DPLL_USB and HS USB1 1.8V analog power supply	PWR	AB10
vssa_usb	HS USB1 and HS USB2 analog ground	GND	AC7
vdda33v_usb1	HS USB1 3.3V analog power supply. If USB1 is not used, this pin can alternatively be connected to VSS if the following requirements are met: - The usb1_dm/usb1_dp pins are left unconnected - The USB1 PHY is kept powered down	PWR	AB8
vdda_abe_per	DPLL_ABE / DPLL_PER / and PER HSDIVIDER analog power supply	PWR	L14
vdda_ddr	DPLL_DDR and DDR HSDIVIDER analog power supply	PWR	P18
vdda_debug	DPLL_DEBUG analog power supply	PWR	M8
vdda_dsp_eve	DPLL_DSP and DPLL_EVE analog power supply	PWR	F12
vdda_gmac_core	DPLL_CORE and CORE HSDIVIDER analog power supply	PWR	P14
vdda_gpu	DPLL_GPU analog power supply	PWR	Y12
vdda_hdmi	PLL_HDMI and HDMI analog power supply	PWR	AB16
vssa_hdmi	DPLL_HDMI and HDMI PHY analog ground	GND	AC16
vdda_iva	DPLL_IVA analog power supply	PWR	Y15
vdda_pcie	DPLL_PCIE_REF and PCIe analog power supply	PWR	AC12
vssa_pcie	PCIe analog ground	GND	AC11/ AB11
vdda_pcie0	PCIe ch0 RX/TX analog power supply	PWR	AC10
vdda_usb3	DPLL_USB_OTG_SS and USB3.0 RX/TX analog power supply	PWR	AB9
vssa_usb3	DPLL_USB and USB3.0 RX/TX analog ground	GND	AC9
vdda_video	DPLL_VIDEO1 and DPLL_VIDEO2 analog power supply	PWR	P11
vssa_video	DPLL_VIDEO1 and DPLL_VIDEO2 analog ground	GND	R13
vdda_mpu	DPLL_MPU analog power supply	PWR	N18
vdda_osc	HFOSC analog power supply	PWR	AC15
vssa_osc0	OSC0 analog ground	GND	AB15
vssa_osc1	OSC1 analog ground	GND	AB12
vdda_rtc	RTC bias and RTC LFOSC analog power supply	PWR	AA14
vdds18v	1.8V power supply	PWR	Y8/ Y16/ Y17/ W8/ V8/ R18/ R19/ L8/ K8/ G10/ G11/ G17/ G18/
vdds18v_ddr1	DDR1 bias power supply	PWR	W20/ U20/ N19/ M20
vdds_ddr1	DDR1 power supply (1.8V for DDR2 mode/ 1.5V for DDR3 mode / 1.35V for DDR3L mode)	PWR	AE24/ AD19/ AD22/ AD25/ Y18/ Y20/ Y23/ W19/ V19/ V20/ R23/ P19/ L20/ L23/ K21
vddshv5	Dual Voltage (1.8V or 3.3V) power supply for the RTC Power Group pins	PWR	AA8
vddshv1	Dual Voltage (1.8V or 3.3V) power supply for the VIN2 Power Group pins	PWR	A2/ B1/ F7/ H8 / J2
vddshv10	Dual Voltage (1.8V or 3.3V) power supply for the GPMC Power Group pins	PWR	P7/ N7/ M7/ L7/ K7/ J7

Table 4-28. Power Supply Signal Descriptions (continued)

SIGNAL NAME	DESCRIPTION	TYPE	BALL
vddshv11	Dual Voltage (1.8V or 3.3V) power supply for the MMC2 Power Group pins	PWR	H7/ G7
vddshv2	Dual Voltage (1.8V or 3.3V) power supply for the VOUT Power Group pins	PWR	G8/ G9/ G12/ G13/ D12
vddshv3	Dual Voltage (1.8V or 3.3V) power supply for the GENERAL Power Group pins	PWR	G14/ G15/ G16/ G19/ F20/ D24/ B18/ B22
vddshv4	Dual Voltage (1.8V or 3.3V) power supply for the MMC4 Power Group pins	PWR	H20
vddshv6	Dual Voltage (1.8V or 3.3V) power supply for the VIN1 Power Group pins	PWR	AE2/ AD1/ AC4/ Y9
vddshv7	Dual Voltage (1.8V or 3.3V) power supply for the WIFI Power Group pins	PWR	W7/ V7
vddshv9	Dual Voltage (1.8V or 3.3V) power supply for the RGMII Power Group pins	PWR	T7/ R7/ N4
cap_vddram_dspeve2 ⁽¹⁾	External capacitor connection for the DSP-EVE SRAM array Ido2 output	CAP	F9
cap_vddram_dspeve1 ⁽¹⁾	External capacitor connection for the DSP-EVE SRAM array Ido1 output	CAP	L6
cap_vbbldo_mpu ⁽¹⁾	External capacitor connection for the MPU vbb Ido output	CAP	F13
cap_vddram_core2 ⁽¹⁾	External capacitor connection for the Core SRAM array Ido2 output	CAP	F16
cap_vbbldo_dspeve ⁽¹⁾	External capacitor connection for the DSP-EVE vbb Ido output	CAP	F11
cap_vddram_mpu1 ⁽¹⁾	External capacitor connection for the MPU SRAM array Ido1 output	CAP	F15
cap_vddram_mpu2 ⁽¹⁾	External capacitor connection for the MPU SRAM array Ido2 output	CAP	F18
cap_vddram_core1 ⁽¹⁾	External capacitor connection for the Core SRAM array Ido1 output	CAP	J6
cap_vddram_core4 ⁽¹⁾	External capacitor connection for the Core SRAM array Ido4 output	CAP	T20
cap_vbbldo_iva ⁽¹⁾	External capacitor connection for the IVA vbb Ido output	CAP	P20
cap_vddram_iva ⁽¹⁾	External capacitor connection for the IVA SRAM array Ido output	CAP	R20
cap_vddram_gpu ⁽¹⁾	External capacitor connection for the GPU SRAM array Ido output	CAP	Y11
cap_vbbldo_gpu ⁽¹⁾	External capacitor connection for the GPU vbb Ido output	CAP	AA15
cap_vddram_core3 ⁽¹⁾	External capacitor connection for the Core SRAM array Ido3 output	CAP	N20
cap_vddram_core5 ⁽¹⁾	External capacitor connection for the Core SRAM array Ido5 output	CAP	Y14

(1) This pin must always be connected via a 1- μ F capacitor to vss.

4.4.20 Test Interfaces

CAUTION

The I/O timings provided in [Section 7 Timing Requirements and Switching Characteristics](#) are valid only if signals within a single IOSET are used. The IOSETs are defined in the [Table 7-118](#).

NOTE

For more information, see the On-Chip Debug Support, Debug Ports section of the device TRM.

Table 4-29. Debug Signal Descriptions

SIGNAL NAME	DESCRIPTION	TYPE	BALL
tms	JTAG test port mode select. An external pullup resistor should be used on this ball.	IO	D18
tdi	JTAG test data	I	D20

Table 4-29. Debug Signal Descriptions (continued)

SIGNAL NAME	DESCRIPTION	TYPE	BALL
tdo	JTAG test port data	O	F21
tclk	JTAG test clock	I	E18
trstn	JTAG test reset	I	E17
rtck	JTAG return clock	O	D19
emu0	Emulator pin 0	IO	E20
emu1	Emulator pin 1	IO	D21
emu2	Emulator pin 2	O	A11
emu3	Emulator pin 3	O	B12
emu4	Emulator pin 4	O	D15
emu5	Emulator pin 5	O	C9/ D4
emu6	Emulator pin 6	O	A13/ B4
emu7	Emulator pin 7	O	A12/ E6
emu8	Emulator pin 8	O	B14/ D5
emu9	Emulator pin 9	O	B13/ C4
emu10	Emulator pin 10	O	B10/ C3
emu11	Emulator pin 11	O	B2/ C14
emu12	Emulator pin 12	O	C10/ E7
emu13	Emulator pin 13	O	A10/ B3
emu14	Emulator pin 14	O	A3/ C13
emu15	Emulator pin 15	O	C6/ E15
emu16	Emulator pin 16	O	A4/ D9
emu17	Emulator pin 17	O	B5/ E14
emu18	Emulator pin 18	O	C5/ D14
emu19	Emulator pin 19	O	A7/ D11

5 Specifications

NOTE

For more information, see Power, Reset and Clock Management / PRCM Subsystem Environment / External Voltage Inputs or Initialization / Preinitialization / Power Requirements section of the Device TRM.

NOTE

The index number 1 which is part of the EMIF1 signal prefix (ddr1_*) listed in [Table 4-7](#), EMIF Signal Descriptions, column "SIGNAL NAME" not to be confused with DDR1 and DDR2 types of SDRAM memories.

NOTE

Audio Back End (ABE) module is not supported for this family of devices, but "ABE" name is still present in some clock or DPLL names.

CAUTION

All IO Cells are NOT Fail-safe compliant and should not be externally driven in absence of their IO supply.

5.1 Absolute Maximum Ratings

Stresses beyond those listed as absolute maximum ratings may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those listed under [Section 5.4, Recommended Operating Conditions](#), is not implied. Exposure to absolute maximum rated conditions for extended periods may affect device reliability.

Table 5-1. Absolute Maximum Rating Over Junction Temperature Range

PARAMETER ⁽¹⁾		MIN	MAX	UNIT	
V _{SUPPLY} (Steady-State)	Supply Voltage Ranges (Steady-State)	Core (vdd, vdd_mpu, vdd_gpu, vdd_dspeve, vdd_iva, vdd_rtc)	-0.3	1.5	V
	Analog (vdda_usb1, vdda_abe_per, vdda_dds, vdda_debug, vdda_dsp_eve, vdda_gmac_core, vdda_gpu, vdda_hdmi, vdda_iva, vdda_pcie, vdda_pcie0, vdda_usb3, vdda_video, vdda_mpu, vdda_osc, vdda_rtc)	-0.3	2.0	V	
	Analog 3.3V (vdda33v_usb1)	-0.3	3.8	V	
	vdds18v, vdds18v_dds1, vdds_dds1	-0.3	2.1	V	
	vddshv1-11 (1.8V mode)	-0.3	2.1	V	
	vddshv1-7 (3.3V mode), vddshv10-11 (3.3V mode)	-0.3	3.8	V	
	vddshv9 (3.3V mode)	-0.3	3.6	V	

Table 5-1. Absolute Maximum Rating Over Junction Temperature Range (continued)

PARAMETER ⁽¹⁾		MIN	MAX	UNIT	
V _{IO} (Steady-State)	Input and Output Voltage Ranges (Steady-State)	Core I/Os	-0.3	1.5	V
		Analog I/Os (except HDMI)	-0.3	2.0	V
		HDMI I/Os	-0.3	3.5	V
		I/O 1.35V	-0.3	1.65	V
		I/O 1.5V	-0.3	1.8	V
		1.8V I/Os	-0.3	2.1	V
		3.3V I/Os (except those powered by vddshv9)	-0.3	3.8	V
		3.3V I/Os (powered by vddshv9)	-0.3	3.6	V
SR	Maximum slew rate, all supplies		10 ⁵	V/s	
V _{IO} (Transient Overshoot / Undershoot)	Input and Output Voltage Ranges (Transient Overshoot/Undershoot) Note: valid for up to 20% of the signal period.		0.2*VDD ⁽²⁾	V	
T _J	Operating junction temperature range	Automotive	-40	+125	°C
T _{STG}	Storage temperature range after soldered onto PC Board		-55	+150	°C
Latch-up I-Test	I-test ⁽³⁾ , All I/Os (if different levels then one line per level)		-100	100	mA
Latch-up OV-Test	Over-voltage Test ⁽⁴⁾ , All supplies (if different levels then one line per level)		N/A	1.5*V _{supply max}	V

(1) See I/Os supplied by this power pin in [Table 4-2](#).

(2) VDD is the voltage on the corresponding power-supply pin(s) for the IO.

(3) Per JEDEC JESD78 at 125°C with specified I/O pin injection current and clamp voltage of 1.5 times maximum recommended I/O voltage and negative 0.5 times maximum recommended I/O voltage.

(4) Per JEDEC JESD78 at 125°C.

5.2 ESD Ratings

Table 5-2. ESD Ratings

		VALUE	UNIT	
V _(ESD)	Electrostatic discharge	Human-Body model (HBM), per AEC Q100-002 ⁽¹⁾	±1000	
		Charged-device model (CDM), per AEC Q100-011	All pins	±250
			Corner pins (A1, A25, AE1, AE25)	±750

(1) AEC Q100-002 indicates that HBM stressing shall be in accordance with the ANSI/ESDA/JEDEC JS-001 specification.

5.3 Power on Hour (POH) Limits

The information in the section below is provided solely for your convenience and does not extend or modify the warranty provided under TI's standard terms and conditions for TI semiconductor products.

NOTE

POH is a functional of voltage, temperature and time. Usage at higher voltages and temperatures will result in a reduction in POH to achieve the same reliability performance. For assessment of alternate use cases, contact your local TI representative.

Table 5-3. Power on Hour (POH) Limits

IP	Duty Cycle	Voltage Domain	Voltage (V) (max)	Frequency (MHz) (max)	T _J (°C)	POH
All	100%	All	All Supported OPPs		Automotive Profile ⁽¹⁾	20000

- (1) Automotive profile is defined as 20000 power on hours with junction temperature as follows: 5% @ -40°C, 65% @ 70°C, 20% @ 110°C, 10% @ 125°C.

5.4 Recommended Operating Conditions

The device is used under the recommended operating conditions described in [Table 5-4](#).

NOTE

Logic functions and parameter values are not assured out of the range specified in the recommended operating conditions.

Table 5-4. Recommended Operating Conditions

PARAMETER	DESCRIPTION	MIN ⁽²⁾	NOM	MAX DC ⁽³⁾	MAX ⁽²⁾	UNIT
Input Power Supply Voltage Range						
vdd	Core voltage domain supply		See Section 5.5			V
vdd_mpu	Supply voltage range for MPU domain		See Section 5.5			V
vdd_gpu	GPU voltage domain supply		See Section 5.5			V
vdd_dspeve	DSP-EVE voltage domain supply		See Section 5.5			V
vdd_iva	IVA voltage domain supply		See Section 5.5			V
vdd_rtc	RTC voltage domain supply		See Section 5.5			V
vdda_usb1	DPLL_USB and HS USB1 1.8V analog power supply	1.71	1.80	1.836	1.89	V
	Maximum noise (peak-peak)		50			mV _{PPmax}
vdda33v_usb1	HS USB1 3.3V analog power supply. If USB1 is not used, this pin can alternatively be connected to VSS if the following requirements are met: - The usb1_dm/usb1_dp pins are left unconnected - The USB1 PHY is kept powered down	3.135	3.3	3.366	3.465	V
	Maximum noise (peak-peak)		50			mV _{PPmax}
vdda_abe_per	DPLL_ABE, DPLL_PER, and PER HSDIVIDER analog power supply	1.71	1.80	1.836	1.89	V
	Maximum noise (peak-peak)		50			mV _{PPmax}
vdda_ddr	DPLL_DDR and DDR HSDIVIDER analog power supply	1.71	1.80	1.836	1.89	V
	Maximum noise (peak-peak)		50			mV _{PPmax}
vdda_debug	DPLL_DEBUG analog power supply	1.71	1.80	1.836	1.89	V
	Maximum noise (peak-peak)		50			mV _{PPmax}
vdda_dsp_eve	DPLL_DSP and DPLL_EVE analog power supply	1.71	1.80	1.836	1.89	V
	Maximum noise (peak-peak)		50			mV _{PPmax}
vdda_gmac_core	DPLL_CORE and CORE HSDIVIDER analog power supply	1.71	1.80	1.836	1.89	V
	Maximum noise (peak-peak)		50			mV _{PPmax}
vdda_gpu	DPLL_GPU analog power supply	1.71	1.80	1.836	1.89	V
	Maximum noise (peak-peak)		50			mV _{PPmax}
vdda_hdmi	PLL_HDMI and HDMI analog power supply	1.71	1.80	1.836	1.89	V
	Maximum noise (peak-peak)		50			mV _{PPmax}
vdda_iva	DPLL_IVA analog power supply	1.71	1.80	1.836	1.89	V
	Maximum noise (peak-peak)		50			mV _{PPmax}

Table 5-4. Recommended Operating Conditions (continued)

PARAMETER	DESCRIPTION	MIN ⁽²⁾	NOM	MAX DC ⁽³⁾	MAX ⁽²⁾	UNIT	
vdda_pcie	DPLL_PCIE_REF and PCIe analog power supply	1.71	1.80	1.836	1.89	V	
	Maximum noise (peak-peak)		50			mV _{PPmax}	
vdda_pcie0	PCIe ch0 RX/TX analog power supply	1.71	1.80	1.836	1.89	V	
	Maximum noise (peak-peak)		50			mV _{PPmax}	
vdda_usb3	DPLL_USB_OTG_SS and USB3.0 RX/TX analog power supply	1.71	1.80	1.836	1.89	V	
	Maximum noise (peak-peak)		50			mV _{PPmax}	
vdda_video	DPLL_VIDEO1 and DPLL_VIDEO2 analog power supply	1.71	1.80	1.836	1.89	V	
	Maximum noise (peak-peak)		50			mV _{PPmax}	
vdda_mpu	DPLL_MPU analog power supply	1.71	1.80	1.836	1.89	V	
	Maximum noise (peak-peak)		50			mV _{PPmax}	
vdda_osc	HFOSC analog power supply	1.71	1.80		1.89	V	
	Maximum noise (peak-peak)		50			mV _{PPmax}	
vdda_rtc	RTC bias and RTC LFOSC analog power supply	1.71	1.80		1.89	V	
	Maximum noise (peak-peak)		50			mV _{PPmax}	
vdds18v	1.8V power supply	1.71	1.80	1.836	1.89	V	
	Maximum noise (peak-peak)		50			mV _{PPmax}	
vdds18v_dds1 ⁽⁴⁾	DDR1 bias power supply	1.71	1.80	1.836	1.89	V	
	Maximum noise (peak-peak)		50			mV _{PPmax}	
vdds_dds1 ⁽⁴⁾	DDR1 power supply (1.8V for DDR2 mode/ 1.5V for DDR3 mode / 1.35V for DDR3L mode)	1.35-V Mode	1.28	1.35	1.377	1.42	V
		1.5-V Mode	1.43	1.50	1.53	1.57	
		1.8-V Mode	1.71	1.80	1.836	1.89	
	Maximum noise (peak-peak)	1.35-V Mode		50			mV _{PPmax}
		1.5-V Mode					
		1.8-V Mode					
vddshv5	Dual Voltage (1.8V or 3.3V) power supply for the RTC Power Group pins	1.8-V Mode	1.71	1.80	1.836	1.89	V
		3.3-V Mode	3.135	3.30	3.366	3.465	
	Maximum noise (peak-peak)	1.8-V Mode		50			mV _{PPmax}
		3.3-V Mode					
vddshv1	Dual Voltage (1.8V or 3.3V) power supply for the VIN2 Power Group pins	1.8-V Mode	1.71	1.80	1.836	1.89	V
		3.3-V Mode	3.135	3.30	3.366	3.465	
	Maximum noise (peak-peak)	1.8-V Mode		50			mV _{PPmax}
		3.3-V Mode					
vddshv10	Dual Voltage (1.8V or 3.3V) power supply for the GPMC Power Group pins	1.8-V Mode	1.71	1.80	1.836	1.89	V
		3.3-V Mode	3.135	3.30	3.366	3.465	
	Maximum noise (peak-peak)	1.8-V Mode		50			mV _{PPmax}
		3.3-V Mode					

Table 5-4. Recommended Operating Conditions (continued)

PARAMETER	DESCRIPTION		MIN ⁽²⁾	NOM	MAX DC ⁽³⁾	MAX ⁽²⁾	UNIT
vddshv11	Dual Voltage (1.8V or 3.3V) power supply for the MMC2 Power Group pins	1.8-V Mode	1.71	1.80	1.836	1.89	V
		3.3-V Mode	3.135	3.30	3.366	3.465	
	Maximum noise (peak-peak)	1.8-V Mode		50			mV _{PPmax}
		3.3-V Mode					
vddshv2	Dual Voltage (1.8V or 3.3V) power supply for the VOUT Power Group pins	1.8-V Mode	1.71	1.80	1.836	1.89	V
		3.3-V Mode	3.135	3.30	3.366	3.465	
	Maximum noise (peak-peak)	1.8-V Mode		50			mV _{PPmax}
		3.3-V Mode					
vddshv3	Dual Voltage (1.8V or 3.3V) power supply for the GENERAL Power Group pins	1.8-V Mode	1.71	1.80	1.836	1.89	V
		3.3-V Mode	3.135	3.30	3.366	3.465	
	Maximum noise (peak-peak)	1.8-V Mode		50			mV _{PPmax}
		3.3-V Mode					
vddshv4	Dual Voltage (1.8V or 3.3V) power supply for the MMC4 Power Group pins	1.8-V Mode	1.71	1.80	1.836	1.89	V
		3.3-V Mode	3.135	3.30	3.366	3.465	
	Maximum noise (peak-peak)	1.8-V Mode		50			mV _{PPmax}
		3.3-V Mode					
vddshv6	Dual Voltage (1.8V or 3.3V) power supply for the VIN1 Power Group pins	1.8-V Mode	1.71	1.80	1.836	1.89	V
		3.3-V Mode	3.135	3.30	3.366	3.465	
	Maximum noise (peak-peak)	1.8-V Mode		50			mV _{PPmax}
		3.3-V Mode					
vddshv7	Dual Voltage (1.8V or 3.3V) power supply for the WIFI Power Group pins	1.8-V Mode	1.71	1.80	1.836	1.89	V
		3.3-V Mode	3.135	3.30	3.366	3.465	
	Maximum noise (peak-peak)	1.8-V Mode		50			mV _{PPmax}
		3.3-V Mode					
vddshv9	Dual Voltage (1.8V or 3.3V) power supply for the RGMII Power Group pins	1.8-V Mode	1.71	1.80	1.836	1.89	V
		3.3-V Mode	3.135	3.30	3.366	3.465	
	Maximum noise (peak-peak)	1.8-V Mode		50			mV _{PPmax}
		3.3-V Mode					
vss	Ground supply			0			V
vssa_hdmi	DPLL_HDMI and HDMI PHY analog ground			0			V
vssa_pcie	PCIe analog ground			0			V
vssa_usb	HS USB1 and HS USB2 analog ground			0			V
vssa_usb3	DPLL_USB and USB3.0 RX/TX analog ground			0			V
vssa_video	DPLL_VIDEO1 and DPLL_VIDEO2 analog ground			0			V
vssa_osc0	OSC0 analog ground			0			V
vssa_osc1	OSC1 analog ground			0			V

Table 5-4. Recommended Operating Conditions (continued)

PARAMETER	DESCRIPTION		MIN ⁽²⁾	NOM	MAX DC ⁽³⁾	MAX ⁽²⁾	UNIT
T _J	Operating junction temperature range	Automotive	-40			+125	°C
ddr1_vref0	Reference Power Supply DDR1			0.5*vdds_ddr1			V

(1) Refer to Power on Hours table [Table 5-3](#) for limitations.

(2) The voltage at the device ball should never be below the MIN voltage or above the MAX voltage for any amount of time. This requirement includes dynamic voltage events such as AC ripple, voltage transients, voltage dips, etc.

(3) The DC voltage at the device ball should never be above the MAX DC voltage to avoid impact on device reliability and lifetime POH (Power-On-Hours). The MAX DC voltage is defined as the highest allowed DC regulated voltage, without transients, seen at the ball.

(4) If DDR2 type of memories are used, the EMIF power supply (vdds_ddrx) and the corresponding bias power supply (vdds18v_ddrx) must be sourced from single power source.

5.5 Operating Performance Points

This section describes the operating conditions of the device. This section also contains the description of each OPP (operating performance point) for processor clocks and device core clocks.

[Table 5-5](#) describes the maximum supported frequency per speed grade for the devices.

Table 5-5. Speed Grade Maximum Frequency

Device Speed	Maximum frequency (MHz)							
	MPU	DSP	EVE	IVA	IPU	L3	DDR3/ DDR3L	DDR2
TDA2xxD	500	500	500	430	212.8	266	532 (DDR3-1066)	400 (DDR2-800)
TDA2xxR	750	750	650	532	212.8	266	532 (DDR3-1066)	400 (DDR2-800)

5.5.1 AVS and ABB Requirements

Adaptive Voltage Scaling (AVS) and Adaptive Body Biasing (ABB) are required on most of the vdd_* supplies as defined in [Table 5-6](#).

Table 5-6. AVS and ABB Requirements per vdd_* Supply

Supply	AVS Required?	ABB Required?
vd_core	Yes, for all OPPs	No
vdd_mpu	Yes, for all OPPs	Yes, for all OPPs
vdd_iva	Yes, for all OPPs	Yes, for all OPPs
vdd_dspeve	Yes, for all OPPs	Yes, for all OPPs
vdd_rtc	No	No

5.5.2 Voltage And Core Clock Specifications

Table 5-7 shows the recommended OPP per voltage domain.

Table 5-7. Voltage Domains Operating Performance Points

DOMAIN	CONDITION	OPP_LOW			OPP_NOM			OPP_OD			OPP_HIGH			
		MIN ⁽²⁾	NOM ⁽¹⁾	MAX ⁽²⁾	MIN ⁽²⁾	NOM ⁽¹⁾	MAX ⁽²⁾	MIN ⁽²⁾	NOM ⁽¹⁾	MAX ⁽²⁾	MIN ⁽²⁾	NOM ⁽¹⁾	MAX DC ⁽³⁾	MAX ⁽²⁾
VD_CORE (V)	BOOT (Before AVS is enabled) ⁽⁴⁾	Not Applicable			1.11	1.15	1.2	Not Applicable			Not Applicable			
	After AVS is enabled ⁽⁴⁾	Not Applicable			AVS Voltage ⁽⁵⁾ – 3.5%	AVS Voltage ⁽⁵⁾	1.2	Not Applicable			Not Applicable			
VD_MPU (V)	BOOT (Before AVS is enabled) ⁽⁴⁾	1.02	1.06	1.16	1.11	1.15	1.2	Not Applicable			Not Applicable			
	After AVS is enabled ⁽⁴⁾	AVS Voltage ⁽⁵⁾ – 3.5%	AVS Voltage ⁽⁵⁾	1.16	AVS Voltage ⁽⁵⁾ – 3.5%	AVS Voltage ⁽⁵⁾	1.2	AVS Voltage ⁽⁵⁾ – 3.5%	AVS Voltage ⁽⁵⁾	AVS Voltage ⁽⁵⁾ + 5%	AVS Voltage ⁽⁵⁾ – 3.5%	AVS Voltage ⁽⁵⁾	AVS Voltage ⁽⁵⁾ + 2%	AVS Voltage ⁽⁵⁾ + 5%
VD_RTC (V) ⁽⁶⁾	-	Not Applicable			0.84	0.88 to 1.06	1.2	Not Applicable			Not Applicable			
Others (V)	BOOT (Before AVS is enabled) ⁽⁴⁾	Not Applicable			1.02	1.06	1.2	Not Applicable			Not Applicable			
	After AVS is enabled ⁽⁴⁾	Not Applicable			AVS Voltage ⁽⁵⁾ – 3.5%	AVS Voltage ⁽⁵⁾	1.2	AVS Voltage ⁽⁵⁾ – 3.5%	AVS Voltage ⁽⁵⁾	AVS Voltage ⁽⁵⁾ + 5%	AVS Voltage ⁽⁵⁾ – 3.5%	AVS Voltage ⁽⁵⁾	AVS Voltage ⁽⁵⁾ + 2%	AVS Voltage ⁽⁵⁾ + 5%

- (1) In a typical implementation, the power supply should target the NOM voltage.
- (2) The voltage at the device ball should never be below the MIN voltage or above the MAX voltage for any amount of time. This requirement includes dynamic voltage events such as AC ripple, voltage transients, voltage dips, etc.
- (3) The DC voltage at the device ball should never be above the MAX DC voltage to avoid impact on device reliability and lifetime POH (Power-On-Hours). The MAX DC voltage is defined as the highest allowed DC regulated voltage, without transients, seen at the ball.
- (4) For all OPPs, AVS must be enabled to avoid impact on device reliability, lifetime POH (Power-On-Hours), and device power.
- (5) The AVS voltages are device-dependent, voltage domain-dependent, and OPP-dependent. They must be read from the STD_FUSE_OPP. For information about STD_FUSE_OPP Registers address, please refer to Control Module Section of the TRM. The power supply should be adjustable over the following ranges for each required OPP:
 - OPP_LOW: 0.85 V – 1.06 V
 - OPP_NOM for MPU: 0.85 V - 1.15 V
 - OPP_NOM for CORE and Others: 0.85 V - 1.15 V
 - OPP_OD: 0.885 V - 1.15 V
 - OPP_HIGH: 0.95 V - 1.25 V
The AVS Voltages will be within the above specified ranges.
- (6) VD_RTC can optionally be tied to VD_CORE and operate at the VD_CORE AVS voltages.
- (7) The power supply must be programmed with the AVS voltages for the MPU and the CORE voltage domain, either just after the ROM boot or at the earliest possible time in the secondary boot loader before there is significant activity seen on these domains.

Table 5-8 describes the standard processor clocks speed characteristics vs OPP of the device.

Table 5-8. Supported OPP vs Max Frequency⁽²⁾

DESCRIPTION	OPP_LOW	OPP_NOM	OPP_OD	OPP_HIGH
	Max Freq. (MHz)	Max Freq. (MHz)	Max Freq. (MHz)	Max Freq. (MHz)
VD_MPU				
MPU_CLK	500	750	750	750
VD_DSPEVE				
DSP_CLK	N/A	600	700	750

Table 5-8. Supported OPP vs Max Frequency⁽²⁾ (continued)

DESCRIPTION	OPP_LOW	OPP_NOM	OPP_OD	OPP_HIGH
	Max Freq. (MHz)	Max Freq. (MHz)	Max Freq. (MHz)	Max Freq. (MHz)
EVE_FCLK	N/A	535	650	650
VD_IVA				
IVA_GCLK	N/A	388.3	430	532
VD_CORE				
CORE_IPUx_CLK	N/A	212.8	N/A	N/A
L3_CLK	N/A	266	N/A	N/A
DDR2	N/A	400 (DDR2-800)	N/A	N/A
DDR3 / DDR3L	N/A	532 (DDR3-1066)	N/A	N/A
VD_RTC				
RTC_FCLK	N/A	0.034	N/A	N/A

(1) N/A in this table stands for Not Applicable

(2) Maximum supported frequency is limited according to the Device Speed Grade (see [Table 5-5](#)).

5.5.3 Maximum Supported Frequency

Device modules either receive their clock directly from an external clock input, directly from a PLL, or from a PRCM. [Table 5-9](#) lists the clock source options for each module on this device, along with the maximum frequency that module can accept. To ensure proper module functionality, the device PLLs and dividers must be programmed not to exceed the maximum frequencies listed in this table.

Table 5-9. Maximum Supported Frequency

Module				Clock Sources		
Instance Name	Input Clock Name	Clock Type	Max. Clock Allowed (MHz)	PRCM Clock Name	PLL / OSC / Source Clock Name	PLL / OSC / Source Name
AES1	AES1_L3_CLK	Int	266	L4SEC_L3_GICKL	CORE_X2_CLK	DPLL_CORE
AES2	AES2_L3_CLK	Int	266	L4SEC_L3_GICKL	CORE_X2_CLK	DPLL_CORE
COUNTER_32K	COUNTER_32K_FCLK	Func	0.032	FUNC_32K_CLK	SYS_CLK1/610	OSC1
	COUNTER_32K_ICLK	Int	38.4	WKUPAON_GICKL	SYS_CLK1 DPLL_ABE_X2_CLK	OSC1 DPLL_ABE
CTRL_MODULE_B ANDGAP	L3INSTR_TS_GCLK	Int	4.8	L3INSTR_TS_GCLK	SYS_CLK1	OSC1
					DPLL_ABE_X2_CLK	DPLL_ABE
CTRL_MODULE_C CORE	L4CFG_L4_GICKL	Int	133	L4CFG_L4_GICKL	CORE_X2_CLK	DPLL_CORE
CTRL_MODULE_ WKUP	WKUPAON_GICKL	Int	38.4	WKUPAON_GICKL	SYS_CLK1	OSC1
					DPLL_ABE_X2_CLK	DPLL_ABE
DCAN1	DCAN1_FCLK	Func	38.4	DCAN1_SYS_CLK	SYS_CLK1 SYS_CLK2	OSC1 OSC2
	DCAN1_ICLK	Int	266	WKUPAON_GICKL	SYS_CLK1 DPLL_ABE_X2_CLK	OSC1 DPLL_ABE
DCAN2	DCAN2_FCLK	Func	38.4	DCAN2_SYS_CLK	SYS_CLK1	OSC1
	DCAN2_ICLK	Int	266	L4PER2_L3_GICKL	CORE_X2_CLK	DPLL_CORE
DES3DES	DES_CLK_L3	Int	266	L4SEC_L3_GICKL	CORE_X2_CLK	DPLL_CORE
DLL	EMIF_DLL_FCLK	Func	EMIF_DLL_FCLK	EMIF_DLL_GICKL	EMIF_DLL_GICKL	DPLL_DDR

Table 5-9. Maximum Supported Frequency (continued)

Module				Clock Sources		
Instance Name	Input Clock Name	Clock Type	Max. Clock Allowed (MHz)	PRCM Clock Name	PLL / OSC / Source Clock Name	PLL / OSC / Source Name
DLL_AGING	FCLK	Int	38.4	L3INSTR_DLL_AGING_GCLK	SYS_CLK1	OSC1
					DPLL_ABE_X2_CLK	DPLL_ABE
DMA_CRYPT0	DMA_CRYPT0_FCLK	Int & Func	266	L4SEC_L3_GICLK	CORE_X2_CLK	DPLL_CORE
	DMA_CRYPT0_ICLK	Int	133	L4SEC_L4_GICLK	CORE_X2_CLK	DPLL_CORE
DMM	DMM_CLK	Int	266	EMIF_L3_GICLK	CORE_X2_CLK	DPLL_CORE
DPLL_DEBUG	SYSCLK	Int	38.4	EMU_SYS_CLK	SYS_CLK1	OSC1
DSP1	DSP1_FICLK	Int & Func	DSP_CLK	DSP1_GFCLK	DSP_GFCLK	DPLL_DSP
DSP2	DSP2_FICLK	Int & Func	DSP_CLK	DSP2_GFCLK	DSP_GFCLK	DPLL_DSP
DSS	DSS_HDMI_CEC_CLK	Func	0.032	HDMI_CEC_GFCLK	SYS_CLK1/610	OSC1
	DSS_HDMI_PHY_CLK	Func	48	HDMI_PHY_GFCLK	FUNC_192M_CLK	DPLL_PER
	DSS_CLK	Func	192	DSS_GFCLK	DSS_CLK	DPLL_PER
	HDMI_CLKINP	Func	38.4	HDMI_DPLL_CLK	SYS_CLK1	OSC1
					SYS_CLK2	OSC2
	DSS_L3_ICLK	Int	266	DSS_L3_GICLK	CORE_X2_CLK	DPLL_CORE
	VIDEO1_CLKINP	Func	38.4	VIDEO1_DPLL_CLK	SYS_CLK1	OSC1
					SYS_CLK2	OSC2
	VIDEO2_CLKINP	Func	38.4	VIDEO2_DPLL_CLK	SYS_CLK1	OSC1
					SYS_CLK2	OSC2
	DPLL_DSI1_A_CLK1	Func	209.3	N/A	HDMI_CLK	DPLL_HDMI
					VIDEO1_CLKOUT1	DPLL_VIDEO1
	DPLL_DSI1_B_CLK1	Func	209.3	N/A	VIDEO1_CLKOUT3	DPLL_VIDEO1
					VIDEO2_CLKOUT3	DPLL_VIDEO2
					HDMI_CLK	DPLL_HDMI
	DPLL_DSI1_C_CLK1	Func	209.3	N/A	DPLL_ABE_X2_CLK	DPLL_ABE
HDMI_CLK					DPLL_HDMI	
DPLL_DSI1_C_CLK1	Func	209.3	N/A	VIDEO1_CLKOUT3	DPLL_VIDEO1	
				VIDEO2_CLKOUT1	DPLL_VIDEO2	
DPLL_HDMI_CLK1	Func	185.6	N/A	HDMI_CLK	DPLL_HDMI	

Table 5-9. Maximum Supported Frequency (continued)

Module				Clock Sources		
Instance Name	Input Clock Name	Clock Type	Max. Clock Allowed (MHz)	PRCM Clock Name	PLL / OSC / Source Clock Name	PLL / OSC / Source Name
DSS DISPC	LCD1_CLK	Func	209.3	N/A	DPLL_DSI1_A_CLK1	See DSS data in the rows above
					DSS_CLK	
	LCD2_CLK	Func	209.3	N/A	DPLL_DSI1_B_CLK1	
					DSS_CLK	
	LCD3_CLK	Func	209.3	N/A	DPLL_DSI1_C_CLK1	
					DSS_CLK	
	F_CLK	Func	209.3	N/A	DPLL_DSI1_A_CLK1	
					DPLL_DSI1_B_CLK1	
DPLL_DSI1_C_CLK1						
DSS_CLK						
EFUSE_CTRL_CUST	ocp_clk	Int	133	CUSTEFUSE_L4_GICK	CORE_X2_CLK	DPLL_CORE
	sys_clk	Func	38.4	CUSTEFUSE_SYS_GFCLK	SYS_CLK1	OSC1
ELM	ELM_ICLK	Int	266	L4PER_L3_GICK	CORE_X2_CLK	DPLL_CORE
EMIF_OCP_FW	L3_CLK	Int	266	EMIF_L3_GICK	CORE_X2_CLK	DPLL_CORE
EMIF_PHY1	EMIF_PHY1_FCLK	Func	DDR	EMIF_PHY_GCLK	EMIF_PHY_GCLK	DPLL_DDR
EMIF_PHY2	EMIF_PHY2_FCLK	Func	DDR	EMIF_PHY_GCLK	EMIF_PHY_GCLK	DPLL_DDR
EMIF1	EMIF1_ICLK	Int	266	EMIF_L3_GICK	CORE_X2_CLK	DPLL_CORE
EMIF2	EMIF2_ICLK	Int	266	EMIF_L3_GICK	CORE_X2_CLK	DPLL_CORE
EVE1	EVE1_FCLK	Func	EVE_FCLK	EVE1_GFCLK	-	DPLL_DSP
					EVE_GFCLK	DPLL_EVE
EVE2	EVE2_FCLK	Func	EVE_FCLK	EVE2_GFCLK	-	DPLL_DSP
					EVE_GFCLK	DPLL_EVE
EVE3	EVE3_FCLK	Func	EVE_FCLK	EVE3_GFCLK	-	DPLL_DSP
					EVE_GFCLK	DPLL_EVE
EVE4	EVE4_FCLK	Func	EVE_FCLK	EVE4_GFCLK	-	DPLL_DSP
					EVE_GFCLK	DPLL_EVE
FPKA	PKA_CLK	Int & Func	266	L4SEC_L3_GICK	CORE_X2_CLK	DPLL_CORE

Table 5-9. Maximum Supported Frequency (continued)

Module				Clock Sources						
Instance Name	Input Clock Name	Clock Type	Max. Clock Allowed (MHz)	PRCM Clock Name	PLL / OSC / Source Clock Name	PLL / OSC / Source Name				
GMAC_SW	CPTS_RFT_CLK	Func	266	GMAC_RFT_CLK	PER_ABE_X1_GF_CLK	DPLL_ABE				
					VIDEO1_CLK	DPLL_VIDEO1				
					VIDEO2_CLK	DPLL_VIDEO2				
					HDMI_CLK	DPLL_HDMI				
					CORE_X2_CLK	DPLL_CORE				
	MAIN_CLK	Int	125	GMAC_MAIN_CLK	GMAC_250M_CLK	DPLL_GMAC				
	MHZ_250_CLK	Func	250	GMII_250MHZ_CLK	GMII_250MHZ_CLK	DPLL_GMAC				
	MHZ_5_CLK	Func	5	RGMII_5MHZ_CLK	GMAC_RMII_HS_CLK	DPLL_GMAC				
	MHZ_50_CLK	Func	50	RMII_50MHZ_CLK	GMAC_RMII_HS_CLK	DPLL_GMAC				
RMII1_MHZ_50_CLK	Func	50	RMII_50MHZ_CLK	GMAC_RMII_HS_CLK	DPLL_GMAC					
RMII2_MHZ_50_CLK	Func	50	RMII_50MHZ_CLK	GMAC_RMII_HS_CLK	DPLL_GMAC					
GPIO1	GPIO1_ICLK	Int	38.4	WKUPAON_GICLK	SYS_CLK1	OSC1				
					DPLL_ABE_X2_CLK	DPLL_ABE				
GPIO1	GPIO1_DBCLK	Func	0.032	WKUPAON_SYS_GFC_LK	WKUPAON_32K_G_FCLK	OSC1 RTC Oscillator				
GPIO2	GPIO2_ICLK	Int	266	L4PER_L3_GICLK	CORE_X2_CLK	DPLL_CORE				
					GPIO2_DBCLK	Func	0.032	GPIO_GFCLK	FUNC_32K_CLK	OSC1 RTC Oscillator
GPIO3	GPIO3_ICLK	Int	266	L4PER_L3_GICLK	CORE_X2_CLK	DPLL_CORE				
					GPIO3_DBCLK	Func	0.032	GPIO_GFCLK	FUNC_32K_CLK	OSC1 RTC Oscillator
GPIO4	GPIO4_ICLK	Int	266	L4PER_L3_GICLK	CORE_X2_CLK	DPLL_CORE				
					GPIO4_DBCLK	Func	0.032	GPIO_GFCLK	FUNC_32K_CLK	OSC1
					PIDBCLK	Func	0.032	GPIO_GFCLK		RTC Oscillator
GPIO5	GPIO5_ICLK	Int	266	L4PER_L3_GICLK	CORE_X2_CLK	DPLL_CORE				
					GPIO5_DBCLK	Func	0.032	GPIO_GFCLK	FUNC_32K_CLK	OSC1
					PIDBCLK	Func	0.032	GPIO_GFCLK		RTC Oscillator
GPIO6	GPIO6_ICLK	Int	266	L4PER_L3_GICLK	CORE_X2_CLK	DPLL_CORE				
					GPIO6_DBCLK	Func	0.032	GPIO_GFCLK	FUNC_32K_CLK	OSC1
					PIDBCLK	Func	0.032	GPIO_GFCLK		RTC Oscillator
GPIO7	GPIO7_ICLK	Int	266	L4PER_L3_GICLK	CORE_X2_CLK	DPLL_CORE				
					GPIO7_DBCLK	Func	0.032	GPIO_GFCLK	FUNC_32K_CLK	OSC1
					PIDBCLK	Func	0.032	GPIO_GFCLK		RTC Oscillator
GPIO8	GPIO8_ICLK	Int	266	L4PER_L3_GICLK	CORE_X2_CLK	DPLL_CORE				
					GPIO8_DBCLK	Func	0.032	GPIO_GFCLK	FUNC_32K_CLK	OSC1
					PIDBCLK	Func	0.032	GPIO_GFCLK		RTC Oscillator
GPMC	GPMC_FCLK	Int	266	L3MAIN1_L3_GICLK	CORE_X2_CLK	DPLL_CORE				

Table 5-9. Maximum Supported Frequency (continued)

Module				Clock Sources		
Instance Name	Input Clock Name	Clock Type	Max. Clock Allowed (MHz)	PRCM Clock Name	PLL / OSC / Source Clock Name	PLL / OSC / Source Name
GPU	GPU_FCLK1	Func	GPU_CLK	GPU_CORE_GCLK	CORE_GPU_CLK	DPLL_CORE
					PER_GPU_CLK	DPLL_PER
					GPU_GCLK	DPLL_GPU
	GPU_FCLK2	Func	GPU_CLK	GPU_HYD_GCLK	CORE_GPU_CLK	DPLL_CORE
					PER_GPU_CLK	DPLL_PER
					GPU_GCLK	DPLL_GPU
GPU_ICLK	Int	266	GPU_L3_GICLK	CORE_X2_CLK	DPLL_CORE	
HDMI PHY	DSS_HDMI_PHY_CLK	Func	38.4	HDMI_PHY_GFCLK	FUNC_192M_CLK	DPLL_PER
I2C1	I2C1_ICLK	Int	266	L4PER_L3_GICLK	CORE_X2_CLK	DPLL_CORE
	I2C1_FCLK	Func	96	PER_96M_GFCLK	FUNC_192M_CLK	DPLL_PER
I2C2	I2C2_ICLK	Int	266	L4PER_L3_GICLK	CORE_X2_CLK	DPLL_CORE
	I2C2_FCLK	Func	96	PER_96M_GFCLK	FUNC_192M_CLK	DPLL_PER
I2C3	I2C3_ICLK	Int	266	L4PER_L3_GICLK	CORE_X2_CLK	DPLL_CORE
	I2C3_FCLK	Func	96	PER_96M_GFCLK	FUNC_192M_CLK	DPLL_PER
I2C4	I2C4_ICLK	Int	266	L4PER_L3_GICLK	CORE_X2_CLK	DPLL_CORE
	I2C4_FCLK	Func	96	PER_96M_GFCLK	FUNC_192M_CLK	DPLL_PER
I2C5	I2C5_ICLK	Int	266	IPU_L3_GICLK	CORE_X2_CLK	DPLL_CORE
	I2C5_FCLK	Func	96	IPU_96M_GFCLK	FUNC_192M_CLK	DPLL_PER
IEEE1500_2_OCP	PI_L3CLK	Int & Func	266	L3INIT_L3_GICLK	CORE_X2_CLK	DPLL_CORE
IPU1	IPU1_GFCLK	Int & Func	425.6	IPU1_GFCLK	DPLL_ABE_X2_CLK	DPLL_ABE
					CORE_IPU_ISS_BOOST_CLK	DPLL_CORE
IPU2	IPU2_GFCLK	Int & Func	425.6	IPU2_GFCLK	CORE_IPU_ISS_BOOST_CLK	DPLL_CORE
IVA	IVA_GCLK	Int	IVA_GCLK	IVA_GCLK	IVA_GFCLK	DPLL_IVA
L3_INSTR	L3_CLK	Int	L3_CLK	L3INSTR_L3_GICLK	CORE_X2_CLK	DPLL_CORE
L3_MAIN	L3_CLK1	Int	L3_CLK	L3MAIN1_L3_GICLK	CORE_X2_CLK	DPLL_CORE
	L3_CLK2	Int	L3_CLK	L3INSTR_L3_GICLK	CORE_X2_CLK	DPLL_CORE
L4_CFG	L4_CFG_CLK	Int	133	L4CFG_L3_GICLK	CORE_X2_CLK	DPLL_CORE
L4_PER1	L4_PER1_CLK	Int	133	L4PER_L3_GICLK	CORE_X2_CLK	DPLL_CORE
L4_PER2	L4_PER2_CLK	Int	133	L4PER2_L3_GICLK	CORE_X2_CLK	DPLL_CORE
L4_PER3	L4_PER3_CLK	Int	133	L4PER3_L3_GICLK	CORE_X2_CLK	DPLL_CORE
L4_WKUP	L4_WKUP_CLK	Int	38.4	WKUPAON_GICLK	SYS_CLK1	OSC1
					DPLL_ABE_X2_CLK	DPLL_ABE
MAILBOX1	MAILBOX1_FLCK	Int	266	L4CFG_L3_GICLK	CORE_X2_CLK	DPLL_CORE
MAILBOX2	MAILBOX2_FLCK	Int	266	L4CFG_L3_GICLK	CORE_X2_CLK	DPLL_CORE
MAILBOX3	MAILBOX3_FLCK	Int	266	L4CFG_L3_GICLK	CORE_X2_CLK	DPLL_CORE
MAILBOX4	MAILBOX4_FLCK	Int	266	L4CFG_L3_GICLK	CORE_X2_CLK	DPLL_CORE
MAILBOX5	MAILBOX5_FLCK	Int	266	L4CFG_L3_GICLK	CORE_X2_CLK	DPLL_CORE
MAILBOX6	MAILBOX6_FLCK	Int	266	L4CFG_L3_GICLK	CORE_X2_CLK	DPLL_CORE
MAILBOX7	MAILBOX7_FLCK	Int	266	L4CFG_L3_GICLK	CORE_X2_CLK	DPLL_CORE
MAILBOX8	MAILBOX8_FLCK	Int	266	L4CFG_L3_GICLK	CORE_X2_CLK	DPLL_CORE
MAILBOX9	MAILBOX9_FLCK	Int	266	L4CFG_L3_GICLK	CORE_X2_CLK	DPLL_CORE

Table 5-9. Maximum Supported Frequency (continued)

Module				Clock Sources		
Instance Name	Input Clock Name	Clock Type	Max. Clock Allowed (MHz)	PRCM Clock Name	PLL / OSC / Source Clock Name	PLL / OSC / Source Name
MAILBOX10	MAILBOX10_FLCK	Int	266	L4CFG_L3_GICLK	CORE_X2_CLK	DPLL_CORE
MAILBOX11	MAILBOX11_FLCK	Int	266	L4CFG_L3_GICLK	CORE_X2_CLK	DPLL_CORE
MAILBOX12	MAILBOX12_FLCK	Int	266	L4CFG_L3_GICLK	CORE_X2_CLK	DPLL_CORE
MAILBOX13	MAILBOX13_FLCK	Int	266	L4CFG_L3_GICLK	CORE_X2_CLK	DPLL_CORE
McASP1	MCASP1_AHCLKR	Func	100	MCASP1_AHCLKR	DPLL_ABE_X2_CLK	DPLL_ABE
					SYS_CLK1	OSC1
					FUNC_96M_AON_CLK	DPLL_PER
					ATLCLK0	Module ATL
					ATLCLK1	Module ATL
					ATLCLK2	Module ATL
					ATLCLK3	Module ATL
					SYS_CLK2	OSC2
					XREF_CLK0	XREF_CLK0
					XREF_CLK1	XREF_CLK1
					XREF_CLK2	XREF_CLK2
					XREF_CLK3	XREF_CLK3
					MLB_CLK	Module MLB
	MLBP_CLK	Module MLB				
	MCASP1_AHCLKX	Func	100	MCASP1_AHCLKX	DPLL_ABE_X2_CLK	DPLL_ABE
					SYS_CLK1	OSC1
					FUNC_96M_AON_CLK	DPLL_PER
					ATLCLK0	Module ATL
					ATLCLK1	Module ATL
					ATLCLK2	Module ATL
ATLCLK3					Module ATL	
SYS_CLK2					OSC2	
XREF_CLK0					XREF_CLK0	
XREF_CLK1					XREF_CLK1	
XREF_CLK2					XREF_CLK2	
XREF_CLK3					XREF_CLK3	
MLB_CLK					Module MLB	
MLBP_CLK	Module MLB					
MCASP1_FCLK	Func	192	MCASP1_AUX_GFCLK	PER_ABE_X1_GFCLK	DPLL_ABE	
				VIDEO1_CLK	DPLL_VIDEO1	
				VIDEO2_CLK	DPLL_VIDEO2	
				HDMI_CLK	DPLL_HDMI	
McSPI1	MCASP1_ICLK	Int	266	IPU_L3_GICLK	CORE_X2_CLK	DPLL_CORE
	SPI1_ICLK	Int	266	L4PER_L3_GICLK	CORE_X2_CLK	DPLL_CORE
McSPI2	SPI1_FCLK	Func	48	PER_48M_GFCLK	PER_48M_GFCLK	DPLL_PER
	SPI2_ICLK	Int	266	L4PER_L3_GICLK	CORE_X2_CLK	DPLL_CORE
	SPI2_FCLK	Func	48	PER_48M_GFCLK	PER_48M_GFCLK	DPLL_PER

Table 5-9. Maximum Supported Frequency (continued)

Module				Clock Sources		
Instance Name	Input Clock Name	Clock Type	Max. Clock Allowed (MHz)	PRCM Clock Name	PLL / OSC / Source Clock Name	PLL / OSC / Source Name
McSPI3	SPI3_ICLK	Int	266	L4PER_L3_GICLK	CORE_X2_CLK	DPLL_CORE
	SPI3_FCLK	Func	48	PER_48M_GFCLK	PER_48M_GFCLK	DPLL_PER
McSPI4	SPI4_ICLK	Int	266	L4PER_L3_GICLK	CORE_X2_CLK	DPLL_CORE
	SPI4_FCLK	Func	48	PER_48M_GFCLK	PER_48M_GFCLK	DPLL_PER
MMC2	MMC2_CLK_32K	Func	0.032	L3INIT_32K_GFCLK	FUNC_32K_CLK	OSC1
	MMC2_FCLK	Func	192	MMC2_GFCLK	FUNC_192M_CLK	DPLL_PER
			128		FUNC_256M_CLK	DPLL_PER
	MMC2_ICLK1	Int	266	L3INIT_L3_GICLK	CORE_X2_CLK	DPLL_CORE
MMC2_ICLK2	Int	133	L3INIT_L4_GICLK	CORE_X2_CLK	DPLL_CORE	
MMC3	MMC3_ICLK	Int	266	L4PER_L3_GICLK	CORE_X2_CLK	DPLL_CORE
	MMC3_CLK_32K	Func	0.032	L4PER_32K_GFCLK	FUNC_32K_CLK	OSC1
	MMC3_FCLK	Func	48	MMC3_GFCLK	FUNC_192M_CLK	DPLL_PER
192						
MMC4	MMC4_ICLK	Int	266	L4PER_L3_GICLK	CORE_X2_CLK	DPLL_CORE
	MMC4_CLK_32K	Func	0.032	L4PER_32K_GFCLK	FUNC_32K_CLK	OSC1
	MMC4_FCLK	Func	48	MMC4_GFCLK	FUNC_192M_CLK	DPLL_PER
192						
MMU_EDMA	MMU1_CLK	Int	266	L3MAIN1_L3_GICLK	CORE_X2_CLK	DPLL_CORE
MMU_PCIESS	MMU2_CLK	Int	266	L3MAIN1_L3_GICLK	CORE_X2_CLK	DPLL_CORE
MPU	MPU_CLK	Int & Func	MPU_CLK	MPU_GCLK	MPU_GCLK	DPLL_MPU
MPU_EMU_DBG	FCLK	Int	38.4	EMU_SYS_CLK	SYS_CLK1	OSC1
					MPU_GCLK	DPLL_MPU
OCMC_RAM1	OCMC1_L3_CLK	Int	266	L3MAIN1_L3_GICLK	CORE_X2_CLK	DPLL_CORE
OCMC_RAM2	OCMC2_L3_CLK	Int	266	L3MAIN1_L3_GICLK	CORE_X2_CLK	DPLL_CORE
OCMC_RAM3	OCMC3_L3_CLK	Int	266	L3MAIN1_L3_GICLK	CORE_X2_CLK	DPLL_CORE
OCMC_ROM	OCMC_L3_CLK	Int	266	L3MAIN1_L3_GICLK	CORE_X2_CLK	DPLL_CORE
OCP_WP_NOC	PICLKOCPL3	Int	266	L3INSTR_L3_GICLK	CORE_X2_CLK	DPLL_CORE
OCP2SCP1	L4CFG1_ADAPTE R_CLKIN	Int	133	L3INIT_L4_GICLK	CORE_X2_CLK	DPLL_CORE
OCP2SCP2	L4CFG2_ADAPTE R_CLKIN	Int	133	L4CFG_L4_GICLK	CORE_X2_CLK	DPLL_CORE
OCP2SCP3	L4CFG3_ADAPTE R_CLKIN	Int	133	L3INIT_L4_GICLK	CORE_X2_CLK	DPLL_CORE
PCIESS1	PCIE1_PHY_WKU P_CLK	Func	0.032	PCIE_32K_GFCLK	FUNC_32K_CLK	RTC Oscillator
	PCle_SS1_FICLK	Int	266	PCIE_L3_GICLK	CORE_X2_CLK	DPLL_CORE
	PCIEPHY_CLK	Func	2500	PCIE_PHY_GCLK	PCIE_PHY_GCLK	APLL_PCIE
	PCIEPHY_CLK_DI V	Func	1250	PCIE_PHY_DIV_GCLK	PCIE_PHY_DIV_G CLK	APLL_PCIE
	PCIE1_REF_CLKI N	Func	34.3	PCIE_REF_GFCLK	CORE_USB_OTG_ SS_LFPS_TX_CLK	DPLL_CORE
	PCIE1_PWR_CLK	Func	38.4	PCIE_SYS_GFCLK	SYS_CLK1	OSC1
PRCM_MPU	32K_CLK	Func	0.032	FUNC_32K_CLK	SYS_CLK1/610	OSC1
	SYS_CLK	Func	38.4	WKUPAON_ICLK	SYS_CLK1	OSC1
					DPLL_ABE_X2_CL K	DPLL_ABE

Table 5-9. Maximum Supported Frequency (continued)

Module				Clock Sources		
Instance Name	Input Clock Name	Clock Type	Max. Clock Allowed (MHz)	PRCM Clock Name	PLL / OSC / Source Clock Name	PLL / OSC / Source Name
QSPI	QSPI_ICLK	Int	266	L4PER2_L3_GICLK	CORE_X2_CLK	DPLL_CORE
	QSPI_FCLK	Func	128	QSPI_GFCLK	FUNC_256M_CLK PER_QSPI_CLK	DPLL_PER DPLL_PER
RNG	RNG_ICLK	Int	266	L4SEC_L3_GICLK	CORE_X2_CLK	DPLL_CORE
RTC_SS	RTC_ICLK	Int	133	RTC_L4_GICLK	CORE_X2_CLK	DPLL_CORE
	RTC_FCLK	Func	RTC_FCLK	RTC_AUX_CLK FUNC_32K_CLK	SYS_32K SYS_CLK1/610	RTC Oscillator OSC1
SAR_ROM	PRCM_ROM_CLOCK	Int	266	L4CFG_L3_GICLK	CORE_X2_CLK	DPLL_CORE
SDMA	SDMA_FCLK	Int & Func	266	DMA_L3_GICLK	CORE_X2_CLK	DPLL_CORE
SHA2MD51	SHAM_1_CLK	Int	266	L4SEC_L3_GICLK	CORE_X2_CLK	DPLL_CORE
SHA2MD52	SHAM_2_CLK	Int	266	L4SEC_L3_GICLK	CORE_X2_CLK	DPLL_CORE
SL2	IVA_GCLK	Int	IVA_GCLK	IVA_GCLK	IVA_GFCLK	DPLL_IVA
SMARTREFLEX_CORE	MCLK	Int	133	COREAON_L4_GICLK	CORE_X2_CLK	DPLL_CORE
	SYSCLK	Func	38.4	WKUPAON_ICLK	SYS_CLK1 DPLL_ABE_X2_CLK	OSC1 DPLL_ABE
SMARTREFLEX_DSP	MCLK	Int	133	COREAON_L4_GICLK	CORE_X2_CLK	DPLL_CORE
	SYSCLK	Func	38.4	WKUPAON_ICLK	SYS_CLK1 DPLL_ABE_X2_CLK	OSC1 DPLL_ABE
SMARTREFLEX_GPU	MCLK	Int	133	COREAON_L4_GICLK	CORE_X2_CLK	DPLL_CORE
	SYSCLK	Func	38.4	WKUPAON_ICLK	SYS_CLK1 DPLL_ABE_X2_CLK	OSC1 DPLL_ABE
SMARTREFLEX_IVAHD	MCLK	Int	133	COREAON_L4_GICLK	CORE_X2_CLK	DPLL_CORE
	SYSCLK	Func	38.4	WKUPAON_ICLK	SYS_CLK1 DPLL_ABE_X2_CLK	OSC1 DPLL_ABE
SMARTREFLEX_MPU	MCLK	Int	133	COREAON_L4_GICLK	CORE_X2_CLK	DPLL_CORE
	SYSCLK	Func	38.4	WKUPAON_ICLK	SYS_CLK1 DPLL_ABE_X2_CLK	OSC1 DPLL_ABE
SPINLOCK	SPINLOCK_ICLK	Int	266	L4CFG_L3_GICLK	CORE_X2_CLK	DPLL_CORE

Table 5-9. Maximum Supported Frequency (continued)

Module				Clock Sources		
Instance Name	Input Clock Name	Clock Type	Max. Clock Allowed (MHz)	PRCM Clock Name	PLL / OSC / Source Clock Name	PLL / OSC / Source Name
TIMER1	TIMER1_ICLK	Int	38.4	WKUPAON_GICLK	SYS_CLK1	OSC1
					DPLL_ABE_X2_CLK	DPLL_ABE
	TIMER1_FCLK	Func	100	TIMER1_GFCLK	SYS_CLK1	OSC1
					FUNC_32K_CLK	OSC1
						RTC Oscillator
					SYS_CLK2	OSC2
					XREF_CLK0	XREF_CLK0
					XREF_CLK1	XREF_CLK1
					XREF_CLK2	XREF_CLK2
					XREF_CLK3	XREF_CLK3
					DPLL_ABE_X2_CLK	DPLL_ABE
					VIDEO1_CLK	DPLL_VIDEO1
VIDEO2_CLK	DPLL_VIDEO2					
HDMI_CLK	DPLL_HDMI					
TIMER2	TIMER2_ICLK	Int	266	L4PER_L3_GICLK	CORE_X2_CLK	DPLL_CORE
					DPLL_ABE_X2_CLK	DPLL_ABE
	TIMER2_FCLK	Func	100	TIMER2_GFCLK	SYS_CLK1	OSC1
					FUNC_32K_CLK	OSC1
						RTC Oscillator
					SYS_CLK2	OSC2
					XREF_CLK0	XREF_CLK0
					XREF_CLK1	XREF_CLK1
					XREF_CLK2	XREF_CLK2
					XREF_CLK3	XREF_CLK3
					DPLL_ABE_X2_CLK	DPLL_ABE
					VIDEO1_CLK	DPLL_VIDEO1
VIDEO2_CLK	DPLL_VIDEO2					
HDMI_CLK	DPLL_HDMI					
TIMER3	TIMER3_ICLK	Int	266	L4PER_L3_GICLK	CORE_X2_CLK	DPLL_CORE
					DPLL_ABE_X2_CLK	DPLL_ABE
	TIMER3_FCLK	Func	100	TIMER3_GFCLK	SYS_CLK1	OSC1
					FUNC_32K_CLK	OSC1
						RTC Oscillator
					SYS_CLK2	OSC2
					XREF_CLK0	XREF_CLK0
					XREF_CLK1	XREF_CLK1
					XREF_CLK2	XREF_CLK2
					XREF_CLK3	XREF_CLK3
					DPLL_ABE_X2_CLK	DPLL_ABE
					VIDEO1_CLK	DPLL_VIDEO1
VIDEO2_CLK	DPLL_VIDEO2					
HDMI_CLK	DPLL_HDMI					

Table 5-9. Maximum Supported Frequency (continued)

Module				Clock Sources		
Instance Name	Input Clock Name	Clock Type	Max. Clock Allowed (MHz)	PRCM Clock Name	PLL / OSC / Source Clock Name	PLL / OSC / Source Name
TIMER4	TIMER4_ICLK	Int	266	L4PER_L3_GICLK	CORE_X2_CLK	DPLL_CORE
	TIMER4_FCLK	Func	100	TIMER4_GFCLK	SYS_CLK1	OSC1
					FUNC_32K_CLK	OSC1
						RTC Oscillator
					SYS_CLK2	OSC2
					XREF_CLK0	XREF_CLK0
					XREF_CLK1	XREF_CLK1
					XREF_CLK2	XREF_CLK2
					XREF_CLK3	XREF_CLK3
					DPLL_ABE_X2_CLK	DPLL_ABE
					VIDEO1_CLK	DPLL_VIDEO1
VIDEO2_CLK	DPLL_VIDEO2					
HDMI_CLK	DPLL_HDMI					
TIMER5	TIMER5_ICLK	Int	266	IPU_L3_GICLK	CORE_X2_CLK	DPLL_CORE
	TIMER5_FCLK	Func	100	TIMER5_GFCLK	SYS_CLK1	OSC1
					FUNC_32K_CLK	OSC1
						RTC Oscillator
					SYS_CLK2	OSC2
					XREF_CLK0	XREF_CLK0
					XREF_CLK1	XREF_CLK1
					XREF_CLK2	XREF_CLK2
					XREF_CLK3	XREF_CLK3
					DPLL_ABE_X2_CLK	DPLL_ABE
					VIDEO1_CLK	DPLL_VIDEO1
VIDEO2_CLK	DPLL_VIDEO2					
HDMI_CLK	DPLL_HDMI					
CLKOUTMUX[0]	CLKOUTMUX[0]					
TIMER6	TIMER6_ICLK	Int	266	IPU_L3_GICLK	CORE_X2_CLK	DPLL_CORE
	TIMER6_FCLK	Func	100	TIMER6_GFCLK	SYS_CLK1	OSC1
					FUNC_32K_CLK	OSC1
						RTC Oscillator
					SYS_CLK2	OSC2
					XREF_CLK0	XREF_CLK0
					XREF_CLK1	XREF_CLK1
					XREF_CLK2	XREF_CLK2
					XREF_CLK3	XREF_CLK3
					DPLL_ABE_X2_CLK	DPLL_ABE
					VIDEO1_CLK	DPLL_VIDEO1
VIDEO2_CLK	DPLL_VIDEO2					
HDMI_CLK	DPLL_HDMI					
CLKOUTMUX[0]	CLKOUTMUX[0]					

Table 5-9. Maximum Supported Frequency (continued)

Module				Clock Sources		
Instance Name	Input Clock Name	Clock Type	Max. Clock Allowed (MHz)	PRCM Clock Name	PLL / OSC / Source Clock Name	PLL / OSC / Source Name
TIMER7	TIMER7_ICLK	Int	266	IPU_L3_GICLK	CORE_X2_CLK	DPLL_CORE
	TIMER7_FCLK	Func	100	TIMER7_GFCLK	SYS_CLK1	OSC1
					FUNC_32K_CLK	OSC1
						RTC Oscillator
					SYS_CLK2	OSC2
					XREF_CLK0	XREF_CLK0
					XREF_CLK1	XREF_CLK1
					XREF_CLK2	XREF_CLK2
					XREF_CLK3	XREF_CLK3
					DPLL_ABE_X2_CLK	DPLL_ABE
					VIDEO1_CLK	DPLL_VIDEO1
					VIDEO2_CLK	DPLL_VIDEO2
					HDMI_CLK	DPLL_HDMI
CLKOUTMUX[0]	CLKOUTMUX[0]					
TIMER8	TIMER8_ICLK	Int	266	IPU_L3_GICLK	CORE_X2_CLK	DPLL_CORE
	TIMER8_FCLK	Func	100	TIMER8_GFCLK	SYS_CLK1	OSC1
					FUNC_32K_CLK	OSC1
						RTC Oscillator
					SYS_CLK2	OSC2
					XREF_CLK0	XREF_CLK0
					XREF_CLK1	XREF_CLK1
					XREF_CLK2	XREF_CLK2
					XREF_CLK3	XREF_CLK3
					DPLL_ABE_X2_CLK	DPLL_ABE
					VIDEO1_CLK	DPLL_VIDEO1
					VIDEO2_CLK	DPLL_VIDEO2
					HDMI_CLK	DPLL_HDMI
CLKOUTMUX[0]	CLKOUTMUX[0]					
TIMER9	TIMER9_ICLK	Int	266	L4PER_L3_GICLK	CORE_X2_CLK	DPLL_CORE
	TIMER9_FCLK	Func	100	TIMER9_GFCLK	SYS_CLK1	OSC1
					FUNC_32K_CLK	OSC1
						RTC Oscillator
					SYS_CLK2	OSC2
					XREF_CLK0	XREF_CLK0
					XREF_CLK1	XREF_CLK1
					XREF_CLK2	XREF_CLK2
					XREF_CLK3	XREF_CLK3
					DPLL_ABE_X2_CLK	DPLL_ABE
					VIDEO1_CLK	DPLL_VIDEO1
					VIDEO2_CLK	DPLL_VIDEO2
					HDMI_CLK	DPLL_HDMI

Table 5-9. Maximum Supported Frequency (continued)

Module				Clock Sources		
Instance Name	Input Clock Name	Clock Type	Max. Clock Allowed (MHz)	PRCM Clock Name	PLL / OSC / Source Clock Name	PLL / OSC / Source Name
TIMER10	TIMER10_ICLK	Int	266	L4PER_L3_GICLK	CORE_X2_CLK	DPLL_CORE
	TIMER10_FCLK	Func	100	TIMER10_GFCLK	SYS_CLK1	OSC1
					FUNC_32K_CLK	OSC1
						RTC Oscillator
					SYS_CLK2	OSC2
					XREF_CLK0	XREF_CLK0
					XREF_CLK1	XREF_CLK1
					XREF_CLK2	XREF_CLK2
					XREF_CLK3	XREF_CLK3
					DPLL_ABE_X2_CLK	DPLL_ABE
					VIDEO1_CLK	DPLL_VIDEO1
VIDEO2_CLK	DPLL_VIDEO2					
HDMI_CLK	DPLL_HDMI					
TIMER11	TIMER11_ICLK	Int	266	L4PER_L3_GICLK	CORE_X2_CLK	DPLL_CORE
	TIMER11_FCLK	Func	100	TIMER11_GFCLK	SYS_CLK1	OSC1
					FUNC_32K_CLK	OSC1
						RTC Oscillator
					SYS_CLK2	OSC2
					XREF_CLK0	XREF_CLK0
					XREF_CLK1	XREF_CLK1
					XREF_CLK2	XREF_CLK2
					XREF_CLK3	XREF_CLK3
					DPLL_ABE_X2_CLK	DPLL_ABE
					VIDEO1_CLK	DPLL_VIDEO1
VIDEO2_CLK	DPLL_VIDEO2					
HDMI_CLK	DPLL_HDMI					
TIMER12	TIMER12_ICLK	Int	38.4	WKUPAON_GICLK	SYS_CLK1	OSC1
					DPLL_ABE_X2_CLK	DPLL_ABE
	TIMER12_FCLK	Func	0.032	OSC_32K_CLK	RC_CLK	RC oscillator
TIMER13	TIMER13_ICLK	Int	266	L4PER3_L3_GICLK	CORE_X2_CLK	DPLL_CORE
	TIMER13_FCLK	Func	100	TIMER13_GFCLK	SYS_CLK1	OSC1
					FUNC_32K_CLK	OSC1
						RTC Oscillator
					SYS_CLK2	OSC2
					XREF_CLK0	XREF_CLK0
					XREF_CLK1	XREF_CLK1
					XREF_CLK2	XREF_CLK2
					XREF_CLK3	XREF_CLK3
					DPLL_ABE_X2_CLK	DPLL_ABE
					VIDEO1_CLK	DPLL_VIDEO1
VIDEO2_CLK	DPLL_VIDEO2					
HDMI_CLK	DPLL_HDMI					

Table 5-9. Maximum Supported Frequency (continued)

Module				Clock Sources		
Instance Name	Input Clock Name	Clock Type	Max. Clock Allowed (MHz)	PRCM Clock Name	PLL / OSC / Source Clock Name	PLL / OSC / Source Name
TIMER14	TIMER14_ICLK	Int	266	L4PER3_L3_GICLK	CORE_X2_CLK	DPLL_CORE
	TIMER14_FCLK	Func	100	TIMER14_GFCLK	SYS_CLK1	OSC1
					FUNC_32K_CLK	OSC1
						RTC Oscillator
					SYS_CLK2	OSC2
					XREF_CLK0	XREF_CLK0
					XREF_CLK1	XREF_CLK1
					XREF_CLK2	XREF_CLK2
					XREF_CLK3	XREF_CLK3
					DPLL_ABE_X2_CLK	DPLL_ABE
					VIDEO1_CLK	DPLL_VIDEO1
VIDEO2_CLK	DPLL_VIDEO2					
HDMI_CLK	DPLL_HDMI					
TIMER15	TIMER15_ICLK	Int	266	L4PER3_L3_GICLK	CORE_X2_CLK	DPLL_CORE
	TIMER15_FCLK	Func	100	TIMER15_GFCLK	SYS_CLK1	OSC1
					FUNC_32K_CLK	OSC1
						RTC Oscillator
					SYS_CLK2	OSC2
					XREF_CLK0	XREF_CLK0
					XREF_CLK1	XREF_CLK1
					XREF_CLK2	XREF_CLK2
					XREF_CLK3	XREF_CLK3
					DPLL_ABE_X2_CLK	DPLL_ABE
					VIDEO1_CLK	DPLL_VIDEO1
VIDEO2_CLK	DPLL_VIDEO2					
HDMI_CLK	DPLL_HDMI					
TIMER16	TIMER16_ICLK	Int	266	L4PER3_L3_GICLK	CORE_X2_CLK	DPLL_CORE
	TIMER16_FCLK	Func	100	TIMER16_GFCLK	SYS_CLK1	OSC1
					FUNC_32K_CLK	OSC1
						RTC Oscillator
					SYS_CLK2	OSC2
					XREF_CLK0	XREF_CLK0
					XREF_CLK1	XREF_CLK1
					XREF_CLK2	XREF_CLK2
					XREF_CLK3	XREF_CLK3
					DPLL_ABE_X2_CLK	DPLL_ABE
					VIDEO1_CLK	DPLL_VIDEO1
VIDEO2_CLK	DPLL_VIDEO2					
HDMI_CLK	DPLL_HDMI					
TPCC	TPCC_GCLK	Int	266	L3MAIN1_L3_GICLK	CORE_X2_CLK	DPLL_CORE
TPTC1	TPTC0_GCLK	Int	266	L3MAIN1_L3_GICLK	CORE_X2_CLK	DPLL_CORE
TPTC2	TPTC1_GCLK	Int	266	L3MAIN1_L3_GICLK	CORE_X2_CLK	DPLL_CORE

Table 5-9. Maximum Supported Frequency (continued)

Module				Clock Sources		
Instance Name	Input Clock Name	Clock Type	Max. Clock Allowed (MHz)	PRCM Clock Name	PLL / OSC / Source Clock Name	PLL / OSC / Source Name
UART1	UART1_FCLK	Func	48	UART1_GFCLK	FUNC_192M_CLK	DPLL_PER
	UART1_ICLK	Int	266	L4PER_L3_GICLK	CORE_X2_CLK	DPLL_CORE
UART2	UART2_FCLK	Func	48	UART2_GFCLK	FUNC_192M_CLK	DPLL_PER
	UART2_ICLK	Int	266	L4PER_L3_GICLK	CORE_X2_CLK	DPLL_CORE
UART3	UART3_FCLK	Func	48	UART3_GFCLK	FUNC_192M_CLK	DPLL_PER
	UART3_ICLK	Int	266	L4PER_L3_GICLK	CORE_X2_CLK	DPLL_CORE
UART4	UART4_FCLK	Func	48	UART4_GFCLK	FUNC_192M_CLK	DPLL_PER
	UART4_ICLK	Int	266	L4PER_L3_GICLK	CORE_X2_CLK	DPLL_CORE
UART5	UART5_FCLK	Func	48	UART5_GFCLK	FUNC_192M_CLK	DPLL_PER
	UART5_ICLK	Int	266	L4PER_L3_GICLK	CORE_X2_CLK	DPLL_CORE
UART6	UART6_FCLK	Func	48	UART6_GFCLK	FUNC_192M_CLK	DPLL_PER
	UART6_ICLK	Int	266	IPU_L3_GICLK	CORE_X2_CLK	DPLL_CORE
UART7	UART7_FCLK	Func	48	UART7_GFCLK	FUNC_192M_CLK	DPLL_PER
	UART7_ICLK	Int	266	L4PER2_L3_GICLK	CORE_X2_CLK	DPLL_CORE
UART8	UART8_FCLK	Func	48	UART8_GFCLK	FUNC_192M_CLK	DPLL_PER
	UART8_ICLK	Int	266	L4PER2_L3_GICLK	CORE_X2_CLK	DPLL_CORE
UART9	UART9_FCLK	Func	48	UART9_GFCLK	FUNC_192M_CLK	DPLL_PER
	UART9_ICLK	Int	266	L4PER2_L3_GICLK	CORE_X2_CLK	DPLL_CORE
UART10	UART10_FCLK	Func	48	UART10_GFCLK	FUNC_192M_CLK	DPLL_PER
	UART10_ICLK	Int	38.4	WKUPAON_GICLK	SYS_CLK1	OSC1
					DPLL_ABE_X2_CLK	DPLL_ABE
USB_PHY1_CORE	USB2PHY1_WKUP_CLK	Func	0.032	COREAON_32K_GFCLK	SYS_CLK1/610	OSC1
USB_PHY2_CORE	USB2PHY2_WKUP_CLK	Func	0.032	COREAON_32K_GFCLK	SYS_CLK1/610	OSC1
USB_PHY3_CORE	USB3PHY_WKUP_CLK	Func	0.032	COREAON_32K_GFCLK	SYS_CLK1/610	OSC1
VCP1	VCP1_CLK	Int	266	L3MAIN1_L3_GICLK	CORE_X2_CLK	DPLL_CORE
VCP2	VCP2_CLK	Int	266	L3MAIN1_L3_GICLK	CORE_X2_CLK	DPLL_CORE
VIP1	L3_CLK_PROC_CLK	Int & Func	266	VIP1_GCLK	CORE_X2_CLK	DPLL_CORE
					CORE_ISS_MAIN_CLK	DPLL_CORE
VIP2	L3_CLK_PROC_CLK	Int & Func	266	VIP2_GCLK	CORE_X2_CLK	DPLL_CORE
					CORE_ISS_MAIN_CLK	DPLL_CORE
VIP3	L3_CLK_PROC_CLK	Int & Func	266	VIP3_GCLK	CORE_X2_CLK	DPLL_CORE
					CORE_ISS_MAIN_CLK	DPLL_CORE
VPE	L3_CLK_PROC_CLK	Int & Func	300	VPE_GCLK	CORE_ISS_MAIN_CLK	DPLL_CORE
					VIDEO1_CLKOUT4	DPLL_VIDEO1
WD_TIMER1	PIOCPCLK	Int	38.4	WKUPAON_GICLK	SYS_CLK1	OSC1
					DPLL_ABE_X2_CLK	DPLL_ABE
	PITIMERCLK	Func	0.032	OSC_32K_CLK	RC_CLK	RC oscillator

Table 5-9. Maximum Supported Frequency (continued)

Module				Clock Sources		
Instance Name	Input Clock Name	Clock Type	Max. Clock Allowed (MHz)	PRCM Clock Name	PLL / OSC / Source Clock Name	PLL / OSC / Source Name
WD_TIMER2	WD_TIMER2_ICLK	Int	38.4	WKUPAON_GICLK	SYS_CLK1	OSC1
					DPLL_ABE_X2_CLK	DPLL_ABE
	WD_TIMER2_FCLK	Func	0.032	WKUPAON_SYS_GFC_LK	WKUPAON_32K_G_FCLK	RTC Oscillator

5.6 Power Consumption Summary

NOTE

Maximum power consumption for this SoC depends on the specific use conditions for the end system. Contact your TI representative for assistance in estimating maximum power consumption for the end system use case.

5.7 Electrical Characteristics

NOTE

The data specified in [Section 5.7.1](#) through [Section 5.7.10](#) are subject to change.

NOTE

The interfaces or signals described in [Section 5.7.1](#) through [Section 5.7.10](#) correspond to the interfaces or signals available in multiplexing mode 0 (Function 1).

All interfaces or signals multiplexed on the balls described in these tables have the same DC electrical characteristics, unless multiplexing involves a PHY/GPIO combination in which case different DC electrical characteristics are specified for the different multiplexing modes (Functions).

5.7.1 LVCMOS DDR DC Electrical Characteristics

[Table 5-10](#) summarizes the DC electrical characteristics for LVCMOS DDR Buffers.

NOTE

For more information on the I/O cell configurations (i[2:0], sr[1:0]), see the Chapter *Control Module* of the Device TRM.

Table 5-10. LVCMOS DDR DC Electrical Characteristics

PARAMETER	MIN	NOM	MAX	UNIT
Signal Names in MUXMODE 0 (Single-Ended Signals): ddr1_d[31:0], ddr1_a[15:0], ddr1_dqm[3:0], ddr1_ba[2:0], ddr1_csn[0], ddr1_cke, ddr1_odt[0], ddr1_casn, ddr1_rasn, ddr1_wen, ddr1_rst, ddr1_ecc_d[7:0], ddr1_dqm_ecc;				
Balls: Y21 / Y24 / W24 / Y22 / W25 / Y25 / AA22 / AA21 / W21 / W22 / W23 / V23 / V22 / V21 / U23 / U22 / R22 / P23 / T21 / R25 / R24 / R21 / T22 / T25 / N21 / N25 / N24 / M22 / N23 / P22 / M21 / N22 / AB18 / AE20 / AD24 / AA18 / AC21 / AC20 / AC23 / AA19 / AB20 / AB23 / AB22 / AB25 / AB24 / AD17 / AE17 / AD18 / AA20 / U21 / T24 / P21 / AE18 / AE21 / AE23 / AC22 / AB19 / AD23 / AC18 / AE19 / AD21 / AD20 / M25 / M24 / J23 / L22 / K23 / L24 / L25 / L21 / K22;				
Driver Mode				
V _{OH}	High-level output threshold (I _{OH} = 0.1 mA)	0.9*V _{DD5}		V
V _{OL}	Low-level output threshold (I _{OL} = 0.1 mA)		0.1*V _{DD5}	V

Table 5-10. LVCMOS DDR DC Electrical Characteristics (continued)

PARAMETER		MIN	NOM	MAX	UNIT	
C _{PAD}	Pad capacitance (including package capacitance)			3	pF	
Z _O	Output impedance (drive strength)	I[2:0] = 000 (Imp80)		80	Ω	
		I[2:0] = 001 (Imp60)		60		
		I[2:0] = 010 (Imp48)		48		
		I[2:0] = 011 (Imp40)		40		
		I[2:0] = 100 (Imp34)		34		
Single-Ended Receiver Mode						
V _{IH}	High-level input threshold	DDR3/DDR3L	VREF+0.1		VDD5+0.2	V
		DDR2	VREF+0.125		VDD5+0.3	
V _{IL}	Low-level input threshold	DDR3/DDR3L	-0.2		VREF-0.1	V
		DDR2	-0.3		VREF-0.125	
V _{CM}	Input common-mode voltage		VREF -10%vdds		VREF+ 10%vdds	V
C _{PAD}	Pad capacitance (including package capacitance)			3	pF	
Signal Names in MUXMODE 0 (Differential Signals): ddr1_dqs[3:0], ddr1_dqsn[3:0], ddr1_ck, ddr1_nck, ddr1_dqs_ecc, ddr1_dqsn_ecc;						
Bottom Balls: AA25 / V25 / U25 / P25 / AA24 / V24 / U24 / K24 / AC25 / AC24 / K25 / K24;						
Driver Mode						
V _{OH}	High-level output threshold (I _{OH} = 0.1 mA)		0.9*VDD5			V
V _{OL}	Low-level output threshold (I _{OL} = 0.1 mA)				0.1*VDD5	V
C _{PAD}	Pad capacitance (including package capacitance)			3	pF	
Z _O	Output impedance (drive strength)	I[2:0] = 000 (Imp80)		80	Ω	
		I[2:0] = 001 (Imp60)		60		
		I[2:0] = 010 (Imp48)		48		
		I[2:0] = 011 (Imp40)		40		
		I[2:0] = 100 (Imp34)		34		
Single-Ended Receiver Mode						
V _{IH}	High-level input threshold	DDR3/DDR3L	VREF+0.1		VDD5+0.2	V
		DDR2	VREF+0.125		VDD5+0.3	
V _{IL}	Low-level input threshold	DDR3/DDR3L	-0.2		VREF-0.1	V
		DDR2	-0.3		VREF-0.125	
V _{CM}	Input common-mode voltage		VREF -10%vdds		VREF+ 10%vdds	V
C _{PAD}	Pad capacitance (including package capacitance)			3	pF	
Differential Receiver Mode						
V _{SWING}	Input voltage swing	DDR3/DDR3L	0.2		vdds+0.4	V
		DDR2	0.25		vdds+0.6	
V _{CM}	Input common-mode voltage		VREF -10%vdds		VREF+ 10%vdds	V
C _{PAD}	Pad capacitance (including package capacitance)			3	pF	

- (1) VDDS in this table stands for corresponding power supply (i.e. vdds_ddr1). For more information on the power supply name and the corresponding ball, see [Table 4-2, POWER \[11\]](#) column.
- (2) VREF in this table stands for corresponding Reference Power Supply (i.e. ddr1_vref0). For more information on the power supply name and the corresponding ball, see [Table 4-2, POWER \[11\]](#) column.

5.7.2 HDMIPHY DC Electrical Characteristics

The HDMIPHY DC Electrical Characteristics are compliant with the HDMI 1.4a specification and are not reproduced here.

5.7.3 Dual Voltage LVCMOS I²C DC Electrical Characteristics

[Table 5-11](#) summarizes the DC electrical characteristics for Dual Voltage LVCMOS I2C Buffers.

NOTE

For more information on the I/O cell configurations, see the Control Module section of the Device TRM.

Table 5-11. Dual Voltage LVCMOS I2C DC Electrical Characteristics

PARAMETER		MIN	NOM	MAX	UNIT
Signal Names in MUXMODE 0: i2c2_scl; i2c1_scl; i2c1_sda; i2c2_sda;					
Balls: F17 / C20 / C21 / C25					
I²C Standard Mode – 1.8 V					
V _{IH}	Input high-level threshold	0.7*VDDS			V
V _{IL}	Input low-level threshold			0.3*VDDS	V
V _{hys}	Hysteresis	0.1*VDDS			V
I _{IN}	Input current at each I/O pin with an input voltage between 0.1*VDDS to 0.9*VDDS			12	μA
I _{OZ}	I _{OZ} (I _{PAD} Current) for BIDI cell. This current is contributed by the tristated driver leakage + input current of the Rx + weak pullup/pulldown leakage. PAD is swept from 0 to VDDS and the Max(I _{PAD}) is measured and is reported as I _{OZ}			12	μA
C _{IN}	Input capacitance			10	pF
V _{OL3}	Output low-level threshold open-drain at 3-mA sink current			0.2*VDDS	V
I _{OLmin}	Low-level output current @V _{OL} =0.2*VDDS	3			mA
t _{OF}	Output fall time from V _{IHmin} to V _{ILmax} with a bus capacitance CB from 5 pF to 400 pF			250	ns
I²C Fast Mode – 1.8 V					
V _{IH}	Input high-level threshold	0.7*VDDS			V
V _{IL}	Input low-level threshold			0.3*VDDS	V
V _{hys}	Hysteresis	0.1*VDDS			V
I _{IN}	Input current at each I/O pin with an input voltage between 0.1*VDDS to 0.9*VDDS			12	μA
I _{OZ}	I _{OZ} (I _{PAD} Current) for BIDI cell. This current is contributed by the tristated driver leakage + input current of the Rx + weak pullup/pulldown leakage. PAD is swept from 0 to VDDS and the Max(I _{PAD}) is measured and is reported as I _{OZ}			12	μA
C _{IN}	Input capacitance			10	pF
V _{OL3}	Output low-level threshold open-drain at 3-mA sink current			0.2*VDDS	V
I _{OLmin}	Low-level output current @V _{OL} =0.2*VDDS	3			mA
t _{OF}	Output fall time from V _{IHmin} to V _{ILmax} with a bus capacitance CB from 10 pF to 400 pF	20+0.1*Cb		250	ns

Table 5-11. Dual Voltage LVC MOS I2C DC Electrical Characteristics (continued)

PARAMETER		MIN	NOM	MAX	UNIT
I²C Standard Mode – 3.3 V					
V _{IH}	Input high-level threshold	0.7*V _{DD5}			V
V _{IL}	Input low-level threshold			0.3*V _{DD5}	V
V _{hys}	Hysteresis	0.05*V _{DD5}			V
I _{IN}	Input current at each I/O pin with an input voltage between 0.1*V _{DD5} to 0.9*V _{DD5}	31		80	μA
I _{OZ}	I _{OZ} (I _{PAD} Current) for BIDI cell. This current is contributed by the tristated driver leakage + input current of the Rx + weak pullup/pulldown leakage. PAD is swept from 0 to V _{DD5} and the Max(I _{PAD}) is measured and is reported as I _{OZ}	31		80	μA
C _{IN}	Input capacitance			10	pF
V _{OL3}	Output low-level threshold open-drain at 3-mA sink current			0.4	V
I _{OLmin}	Low-level output current @V _{OL} =0.4V	3			mA
I _{OLmin}	Low-level output current @V _{OL} =0.6V for full drive load (400pF/400KHz)	6			mA
t _{OF}	Output fall time from V _{IHmin} to V _{ILmax} with a bus capacitance CB from 5 pF to 400 pF			250	ns
I²C Fast Mode – 3.3 V					
V _{IH}	Input high-level threshold	0.7*V _{DD5}			V
V _{IL}	Input low-level threshold			0.3*V _{DD5}	V
V _{hys}	Hysteresis	0.05*V _{DD5}			V
I _{IN}	Input current at each I/O pin with an input voltage between 0.1*V _{DD5} to 0.9*V _{DD5}	31		80	μA
I _{OZ}	I _{OZ} (I _{PAD} Current) for BIDI cell. This current is contributed by the tristated driver leakage + input current of the Rx + weak pullup/pulldown leakage. PAD is swept from 0 to V _{DD5} and the Max(I _{PAD}) is measured and is reported as I _{OZ}	31		80	μA
C _{IN}	Input capacitance			10	pF
V _{OL3}	Output low-level threshold open-drain at 3-mA sink current			0.4	V
I _{OLmin}	Low-level output current @V _{OL} =0.4V	3			mA
I _{OLmin}	Low-level output current @V _{OL} =0.6V for full drive load (400pF/400KHz)	6			mA
t _{OF}	Output fall time from V _{IHmin} to V _{ILmax} with a bus capacitance CB from 10 pF to 200 pF (Proper External Resistor Value should be used as per I2C spec)	20+0.1*Cb		250	ns
	Output fall time from V _{IHmin} to V _{ILmax} with a bus capacitance CB from 300 pF to 400 pF (Proper External Resistor Value should be used as per I2C spec)	40		290	

(1) V_{DD5} in this table stands for corresponding power supply (i.e. vddshv3). For more information on the power supply name and the corresponding ball, see [Table 4-2](#), POWER [11] column.

5.7.4 IQ1833 Buffers DC Electrical Characteristics

[Table 5-12](#) summarizes the DC electrical characteristics for IQ1833 Buffers.

Table 5-12. IQ1833 Buffers DC Electrical Characteristics

PARAMETER	MIN	NOM	MAX	UNIT
Signal Names in MUXMODE 0: tclk;				

Table 5-12. IQ1833 Buffers DC Electrical Characteristics (continued)

PARAMETER		MIN	NOM	MAX	UNIT
Balls: E18;					
1.8-V Mode					
V_{IH}	Input high-level threshold (Does not meet JEDEC V_{IH})	0.75 * VDD5			V
V_{IL}	Input low-level threshold (Does not meet JEDEC V_{IL})			0.25 * VDD5	V
V_{HYS}	Input hysteresis voltage	100			mV
I_{IN}	Input current at each I/O pin	2		11	μ A
C_{PAD}	Pad capacitance (including package capacitance)			1	pF
3.3-V Mode					
V_{IH}	Input high-level threshold (Does not meet JEDEC V_{IH})	2.0			V
V_{IL}	Input low-level threshold (Does not meet JEDEC V_{IL})			0.6	V
V_{HYS}	Input hysteresis voltage	400			mV
I_{IN}	Input current at each I/O pin	5		11	μ A
C_{PAD}	Pad capacitance (including package capacitance)			1	pF

(1) VDD5 in this table stands for corresponding power supply (i.e. vddshv3). For more information on the power supply name and the corresponding ball, see [Table 4-2](#), POWER [11] column.

5.7.5 IHHV1833 Buffers DC Electrical Characteristics

[Table 5-13](#) summarizes the DC electrical characteristics for IHHV1833 Buffers.

Table 5-13. IHHV1833 Buffers DC Electrical Characteristics

PARAMETER		MIN	NOM	MAX	UNIT
Signal Names in MUXMODE 0: porz / wakeup [3:0];					
Balls: F17 / AA16 / AA17 / AB17 / AC17;					
1.8-V Mode					
V_{IH}	Input high-level threshold	1.2			V
V_{IL}	Input low-level threshold			0.4	V
V_{HYS}	Input hysteresis voltage	40			mV
I_{IN}	Input current at each I/O pin	0.02		1	μ A
C_{PAD}	Pad capacitance (including package capacitance)			1	pF
3.3-V Mode					
V_{IH}	Input high-level threshold	1.2			V
V_{IL}	Input low-level threshold			0.4	V
V_{HYS}	Input hysteresis voltage	40			mV
I_{IN}	Input current at each I/O pin	5		8	μ A
C_{PAD}	Pad capacitance (including package capacitance)			1	pF

5.7.6 LVCMOS OSC Buffers DC Electrical Characteristics

[Table 5-14](#) summarizes the DC electrical characteristics for LVCMOS OSC Buffers.

Table 5-14. LVCMOS OSC Buffers DC Electrical Characteristics

PARAMETER		MIN	NOM	MAX	UNIT
Signal Names in MUXMODE 0: rtc_osc_xi_clkln32 / rtc_osc_xo;					
Balls: AA13 / AA12;					
1.8-V Mode					

Table 5-14. LVCMOS OSC Buffers DC Electrical Characteristics (continued)

PARAMETER		MIN	NOM	MAX	UNIT
V_{IH}	Input high-level threshold	0.65 * VDD5			V
V_{IL}	Input low-level threshold			0.35 * VDD5	V
V_{HYS}	Input hysteresis voltage	150			mV
C_{PAD}	Pad capacitance (including package capacitance)			3	pF

(1) VDD5 in this table stands for corresponding power supply (i.e. vdda_rtc). For more information on the power supply name and the corresponding ball, see [Table 4-2](#), POWER [11] column.

5.7.7 BC1833IHHV Buffers DC Electrical Characteristics

[Table 5-15](#) summarizes the DC electrical characteristics for BC1833IHHV Buffers.

Table 5-15. BC1833IHHV Buffers DC Electrical Characteristics

PARAMETER		MIN	NOM	MAX	UNIT
Signal Names in MUXMODE 0: on_off;					
Balls: AA11;					
1.8-V Mode					
V_{OH}	Output high-level threshold ($I_{OH} = 2$ mA)	VDD5- 0.45			V
V_{OL}	Output low-level threshold ($I_{OL} = 2$ mA)			0.45	V
I_{DRIVE}	Pin Drive strength at PAD Voltage = 0.45V or VDD5-0.45V	6			mA
I_{IN}	Input current at each I/O pin	6		12	μ A
I_{OZ}	$I_{OZ}(I_{PAD}$ Current) for BIDI cell. This current is contributed by the tristated driver leakage + input current of the Rx + weak pullup/pulldown leakage. PAD is swept from 0 to VDD5 and the Max(I_{PAD}) is measured and is reported as I_{OZ}			6	μ A
C_{PAD}	Pad capacitance (including package capacitance)			4	pF
3.3-V Mode					
V_{OH}	Output high-level threshold ($I_{OH} = 100\mu$ A)	VDD5-0.2			V
V_{OL}	Output low-level threshold ($I_{OL} = 100\mu$ A)			0.2	V
I_{DRIVE}	Pin Drive strength at PAD Voltage = 0.45V or VDD5-0.45V	6			mA
I_{IN}	Input current at each I/O pin			60	μ A
I_{OZ}	$I_{OZ}(I_{PAD}$ Current) for BIDI cell. This current is contributed by the tristated driver leakage + input current of the Rx + weak pullup/pulldown leakage. PAD is swept from 0 to VDD5 and the Max(I_{PAD}) is measured and is reported as I_{OZ}			60	μ A
C_{PAD}	Pad capacitance (including package capacitance)			4	pF

(1) VDD5 in this table stands for corresponding power supply (i.e. vddshv5). For more information on the power supply name and the corresponding ball, see [Table 4-2](#), POWER [11] column.

5.7.8 USBPHY DC Electrical Characteristics

NOTE

USB1 instance is compliant with the USB3.0 SuperSpeed Transmitter and Receiver Normative Electrical Parameters as defined in the USB3.0 Specification Rev 1.0 dated Jun 6, 2011.

NOTE

USB1 and USB2 Electrical Characteristics are compliant with USB2.0 Specification Rev 2.0 dated April 27, 2000 including ECNs and Errata as applicable.

5.7.9 Dual Voltage LVCMOS DC Electrical Characteristics

Table 5-16 summarizes the DC electrical characteristics for Dual Voltage LVCMOS Buffers.

Table 5-16. Dual Voltage LVCMOS DC Electrical Characteristics

PARAMETER		MIN	NOM	MAX	UNIT
1.8-V Mode					
V _{IH}	Input high-level threshold	0.65*V _{DD5}			V
V _{IL}	Input low-level threshold			0.35*V _{DD5}	V
V _{HYS}	Input hysteresis voltage	100			mV
V _{OH}	Output high-level threshold (I _{OH} = 2 mA)	V _{DD5} -0.45			V
V _{OL}	Output low-level threshold (I _{OL} = 2 mA)			0.45	V
I _{DRIVE}	Pin Drive strength at PAD Voltage = 0.45V or V _{DD5} -0.45V	6			mA
I _{IN}	Input current at each I/O pin			16	μA
I _{OZ}	I _{OZ} (I _{PAD} Current) for BIDI cell. This current is contributed by the tristated driver leakage + input current of the Rx + weak pullup/pulldown leakage. PAD is swept from 0 to V _{DD5} and the Max(I _{PAD}) is measured and is reported as I _{OZ}			16	μA
I _{IN} with pulldown enabled	Input current at each I/O pin with weak pulldown enabled measured when PAD = V _{DD5}	50	120	210	μA
I _{IN} with pullup enabled	Input current at each I/O pin with weak pullup enabled measured when PAD = 0	60	120	200	μA
C _{PAD}	Pad capacitance (including package capacitance)			4	pF
Z _O	Output impedance (drive strength)		40		Ω
3.3-V Mode					
V _{IH}	Input high-level threshold	2			V
V _{IL}	Input low-level threshold			0.8	V
V _{HYS}	Input hysteresis voltage	200			mV
V _{OH}	Output high-level threshold (I _{OH} = 100 μA)	V _{DD5} -0.2			V
V _{OL}	Output low-level threshold (I _{OL} = 100 μA)			0.2	V
I _{DRIVE}	Pin Drive strength at PAD Voltage = 0.45V or V _{DD5} -0.45V	6			mA
I _{IN}	Input current at each I/O pin			65	μA
I _{OZ}	I _{OZ} (I _{PAD} Current) for BIDI cell. This current is contributed by the tristated driver leakage + input current of the Rx + weak pullup/pulldown leakage. PAD is swept from 0 to V _{DD5} and the Max(I _{PAD}) is measured and is reported as I _{OZ}			65	μA
I _{IN} with pulldown enabled	Input current at each I/O pin with weak pulldown enabled measured when PAD = V _{DD5}	40	100	200	μA
I _{IN} with pullup enabled	Input current at each I/O pin with weak pullup enabled measured when PAD = 0	10	100	290	μA
C _{PAD}	Pad capacitance (including package capacitance)			4	pF
Z _O	Output impedance (drive strength)		40		Ω

- (1) VDDS in this table stands for corresponding power supply. For more information on the power supply name and the corresponding ball, see [Table 4-2, POWER \[11\]](#) column.

5.7.10 PCIEPHY DC Electrical Characteristics

NOTE

The PCIe interfaces are compliant with the electrical parameters specified in PCI Express® Base Specification Revision 3.0.

5.8 Thermal Resistance Characteristics

For reliability and operability concerns, the maximum junction temperature of the Device has to be at or below the T_J value identified in [Table 5-4, Recommended Operating Conditions](#).

A BCI compact thermal model for this Device is available and recommended for use when modeling thermal performance in a system.

Therefore, it is recommended to perform thermal simulations at the system level with the worst case device power consumption.

5.8.1 Package Thermal Characteristics

[Table 5-17](#) provides the thermal resistance characteristics for the package used on this device.

NOTE

Power dissipation of 1.5 W and an ambient temperature of 85°C is assumed for AAS package.

Table 5-17. Thermal Resistance Characteristics

NO.	PARAMETER	DESCRIPTION	°C/W ⁽¹⁾	AIR FLOW (m/s) ⁽²⁾
T1	$R_{\theta_{JC}}$	Junction-to-case	0.82	N/A
T2	$R_{\theta_{JB}}$	Junction-to-board	4.29	N/A
T3	$R_{\theta_{JA}}$	Junction-to-free air	13.8	0
T4		Junction-to-moving air	11.1	1
T5			10.0	2
T6			9.2	3
T7	Ψ_{JT}	Junction-to-package top	0.58	0
T8			0.62	1
T9			0.62	2
T10			0.62	3
T11	Ψ_{JB}	Junction-to-board	4.13	0
T12			3.74	1
T13			3.58	2
T14			3.43	3

- (1) These values are based on a JEDEC defined 2S2P system (with the exception of the Theta JC [$R_{\theta_{JC}}$] value, which is based on a JEDEC defined 1S0P system) and will change based on environment as well as application. For more information, see these EIA/JEDEC standards:

- JESD51-2, *Integrated Circuits Thermal Test Method Environment Conditions - Natural Convection (Still Air)*
- JESD51-3, *Low Effective Thermal Conductivity Test Board for Leaded Surface Mount Packages*
- JESD51-6, *Integrated Circuit Thermal Test Method Environmental Conditions - Forced Convection (Moving Air)*
- JESD51-7, *High Effective Thermal Conductivity Test Board for Leaded Surface Mount Packages*
- JESD51-9, *Test Boards for Area Array Surface Mount Packages*

- (2) m/s = meters per second

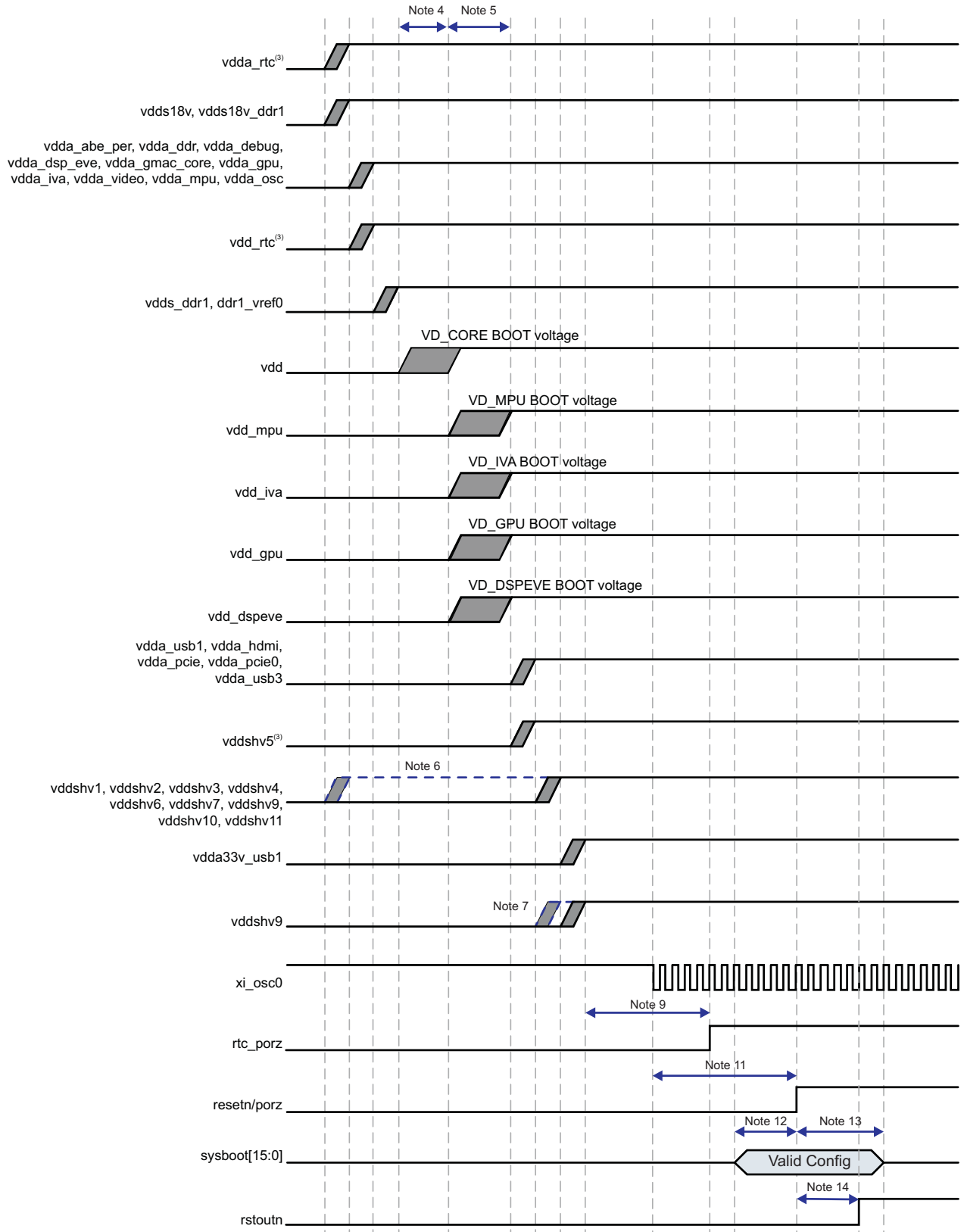
5.9 Power Supply Sequences

This section describes the power-up and power-down sequence required to ensure proper device operation. The power supply names described in this section comprise a superset of a family of compatible devices. Some members of this family will not include a subset of these power supplies and their associated device modules. Refer to [Section 4.2](#), *Ball Characteristics* for a specific device to determine which power supplies are applicable.

NOTE

For more information, see Power, Reset and Clock Management / Reset Management Functional Description / Reset Sequences of the Device TRM.

[Figure 5-1](#) and [Figure 5-2](#) describes the device Power Sequencing when RTC-mode is used.

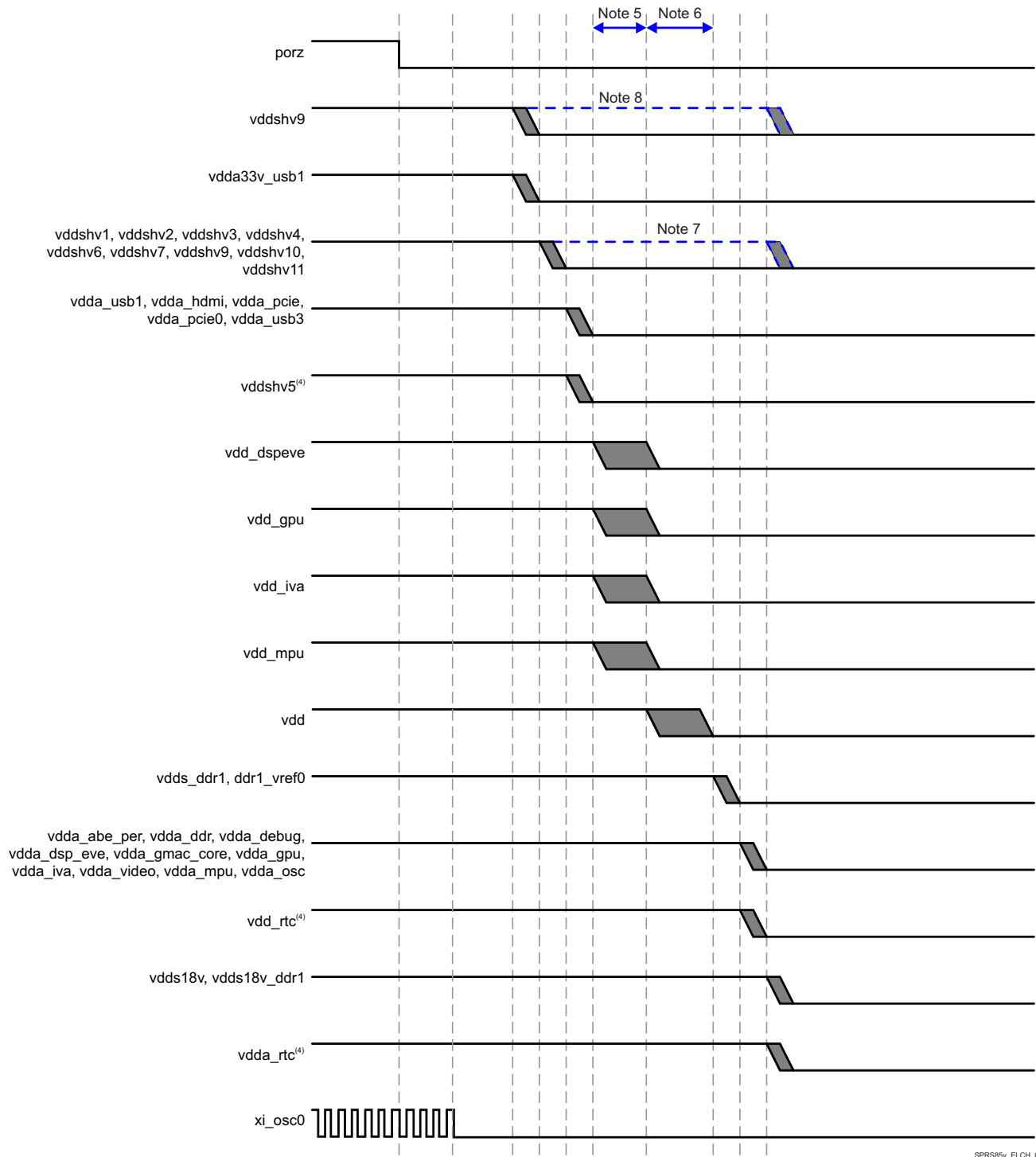


SPRS85v_ELCH_01

Figure 5-1. Power-Up Sequencing

(1) Grey shaded areas are windows where it is valid to ramp the voltage rail.

- (2) Blue dashed lines are not valid windows but show alternate ramp possibilities based on the associated note.
- (3) If RTC-mode is used then vdda_rtc, vdd_rtc and vddshv5 must be individually powered with separate power supplies and cannot be combined with other rails.
- (4) vdd must ramp before or at the same time as vdd_mpu, vdd_gpu, vdd_dspeve and vdd_iva.
- (5) vdd_mpu, vdd_gpu, vdd_dspeve, vdd_iva can be ramped at the same time or can be staggered.
- (6) If any of the vddshv[1-7,10-11] rails (not including vddshv9) are used as 1.8V only, then these rails can be combined with vdds18v.
- (7) vddshv9 is separated out to show support for dual voltage. If single voltage is used then vddshv9 can be combined with other vddshvn rails but vddshv9 must ramp after vdd.
- (8) vdds and vdda rails must not be combined together.
- (9) Pulse duration: rtc_porz must remain low 1ms after vdda_rtc, vddshv5, and vdd_rtc are ramped and stable.
- (10) The SYS_32K source must be stable and at a valid frequency 1ms prior to de-asserting rtc_porz high.
- (11) Pulse duration: resetn/porz must remain low a minimum of $12P^{(15)}$ after xi_osc0 is stable and at a valid frequency.
- (12) Setup time: sysboot[15:0] pins must be valid $2P^{(15)}$ before porz is de-asserted high.
- (13) Hold time: sysboot[15:0] pins must be valid $15P^{(15)}$ after porz is de-asserted high.
- (14) resetn to rstoutn delay is 2ms.
- (15) $P = 1/(\text{SYS_CLK1}/610)$ frequency in ns.



SPRS952D-ELCH_02

Figure 5-2. Power-Down Sequencing

- (1) **xi_osc0** can be turned off anytime after **porz** assertion and must be turned off before **vdda_osc** voltage rail is shutdown.
- (2) Grey shaded areas are windows where it is valid to ramp the voltage rail.
- (3) Blue dashed lines are not valid windows but show alternate ramp possibilities based on the associated note.
- (4) If RTC-mode is supported then **vdda_rtc**, **vdd_rtc** and **vddshv5** must be individually powered with separate power supplies and cannot be combined with other rails.
- (5) **vdd_mpu**, **vdd_gpu**, **vdd_dspeve**, **vdd_iva** can be ramped at the same time or can be staggered.

- (6) vdd must ramp after or at the same time as vdd_mpu, vdd_gpu, vdd_dspeve and vdd_iva.
- (7) If any of the vddshv[1-7, 10-11] rails (not including vddshv9) are used as 1.8V only, then these rails can be combined with vdds18v. vddshv[1-7,9-11] is allowed to ramp down at either of the two points shown in the timing diagram in either 1.8V mode or in 3.3V mode. If vddshv[1-7,9-11] ramps down at the later time in the diagram then the board design must guarantee that the vddshv[1-7,9-11] rail is never higher than 2.0 V above the vdds18v rail.
- (8) vddshv9 is separated out to show support for dual voltage. If a dedicated LDO/supply source is used for vddshv9, then vddshv9 ramp down should occur at one of the two earliest points in the timing diagram. If vddshv9 is powered by the same supply source as the other vddshv rails, then it is allowed to ramp down at either of the last two points in the timing diagram.

[Figure 5-3](#) describes the RTC-mode Power Sequencing.

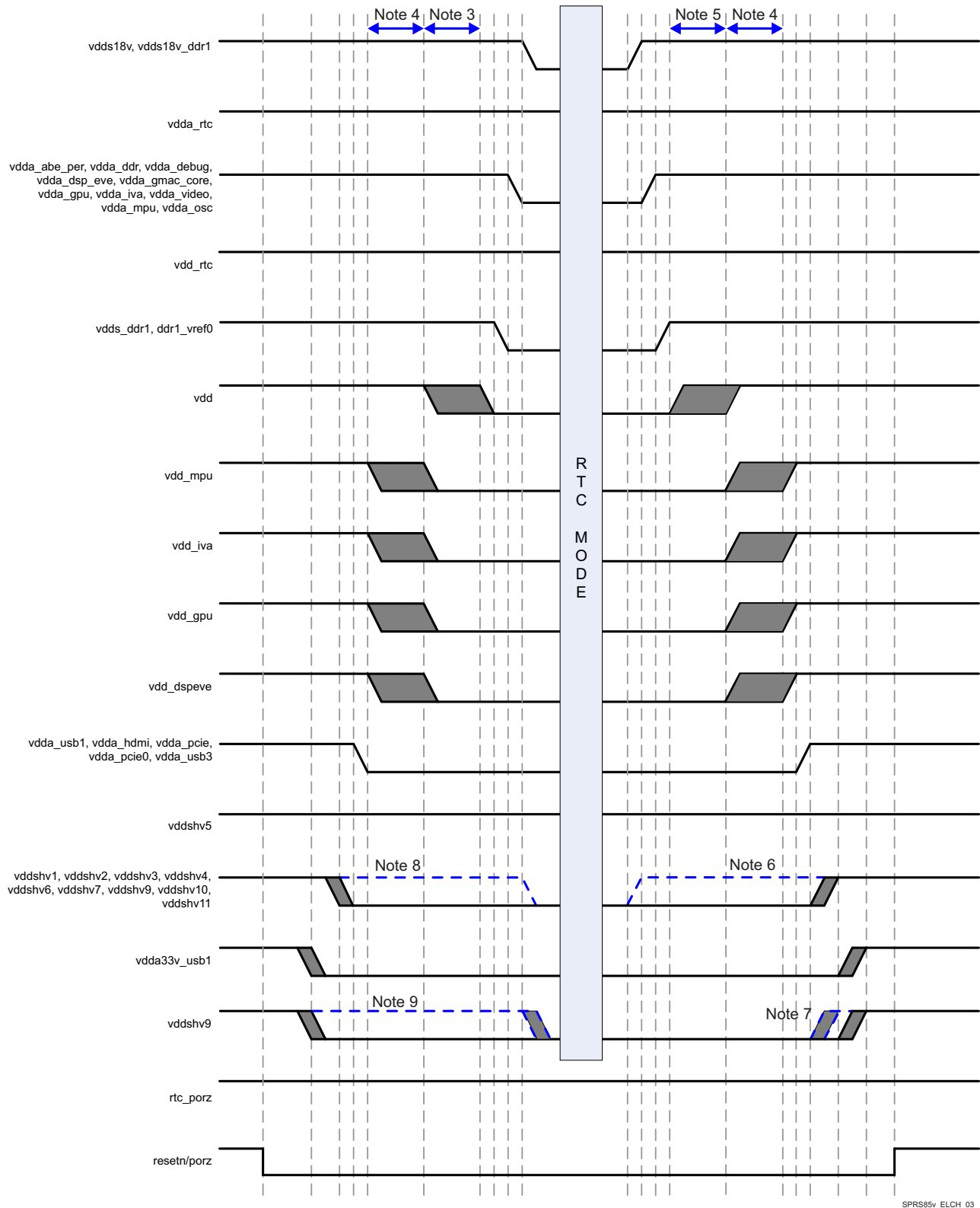
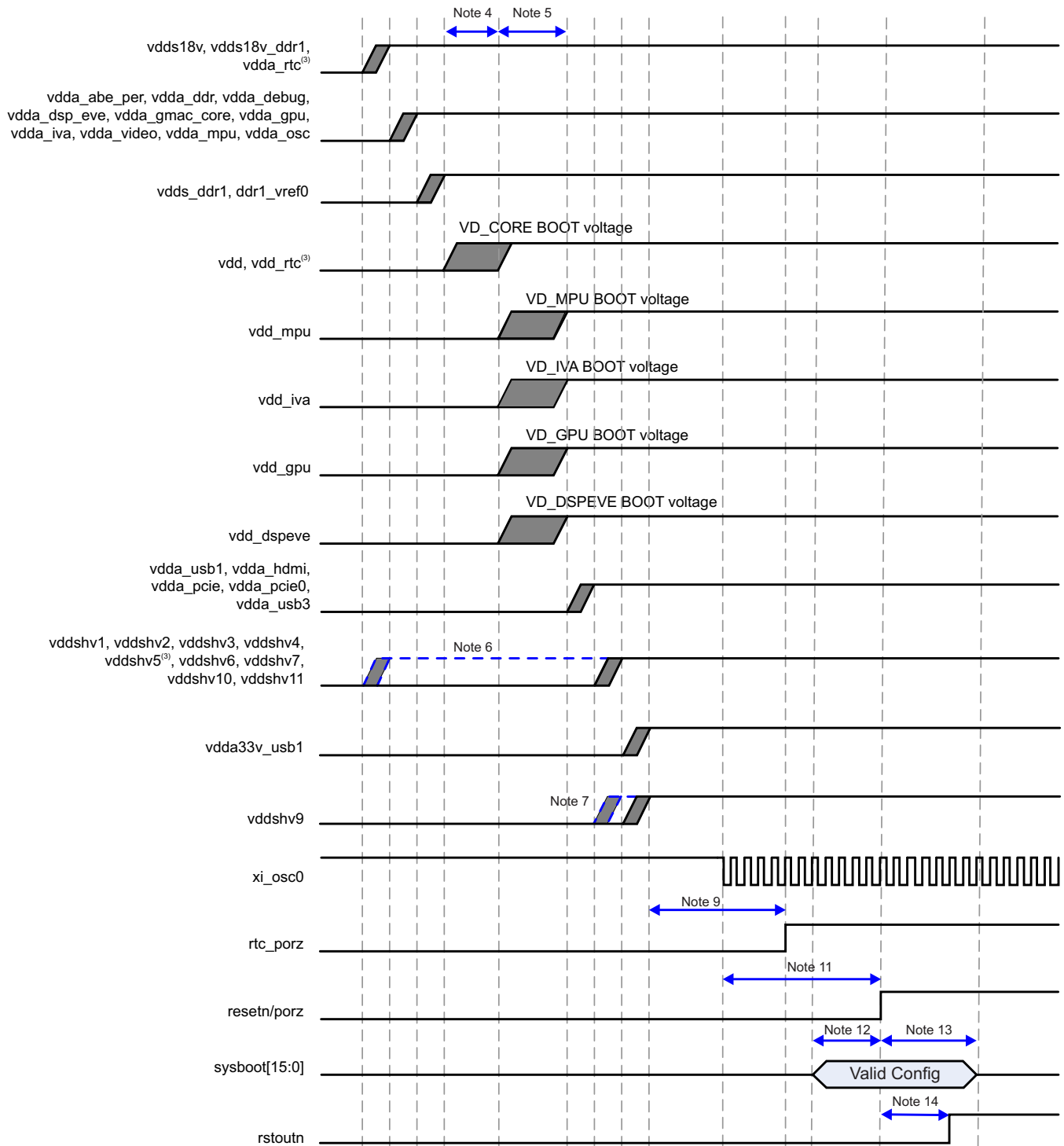


Figure 5-3. RTC Mode Sequencing

- (1) Grey shaded areas are windows where it is valid to ramp the voltage rail.
- (2) Blue dashed lines are not valid windows but show alternate ramp possibilities based on the associated note.

- (3) vdd must ramp down after or at the same time as vdd_mpu, vdd_gpu, vdd_dspeve and vdd_iva.
- (4) vdd_mpu, vdd_gpu, vdd_dspeve, vdd_iva can be ramped at the same time or can be staggered.
- (5) vdd must ramp up before or at the same time as vdd_mpu, vdd_gpu, vdd_dspeve and vdd_iva.
- (6) If any of the vddshv[1-7, 10-11] rails (not including vddshv9) are used as 1.8V only, then these rails can be combined with vdds18v.
- (7) vddshv9 is separated out to show support for dual voltage. If single voltage is used then vddshv9 can be combined with other vddshvn rails but vddshv9 must ramp down before vdd and must ramp up after vdd.
- (8) If any of the vddshv[1-7,9-11] rails (not including vddshv9) are used as 1.8V only, then these rails can be combined with vdds18v. vddshv[1-7,9-11] is allowed to ramp down at either of the two points shown in the timing diagram in either 1.8V mode or in 3.3V mode. If vddshv[1-7,9-11] ramps down at the later time in the diagram then the board design must guarantee that the vddshvn rail is never higher than 2.0 V above the vdds18v rail.
- (9) vddshv9 is separated out to show support for dual voltage. If a dedicated LDO/supply source is used for vddshv9, then vddshv9 ramp down should occur at one of the two earliest points in the timing diagram. If vddshv9 is powered by the same supply source as the other vddshvn rails, then it is allowed to ramp down at either of the last two points in the timing diagram.

Figure 5-4 and Figure 5-5 describe the device Power Sequencing when RTC-mode is NOT used.



SPRS884_ELCH_04

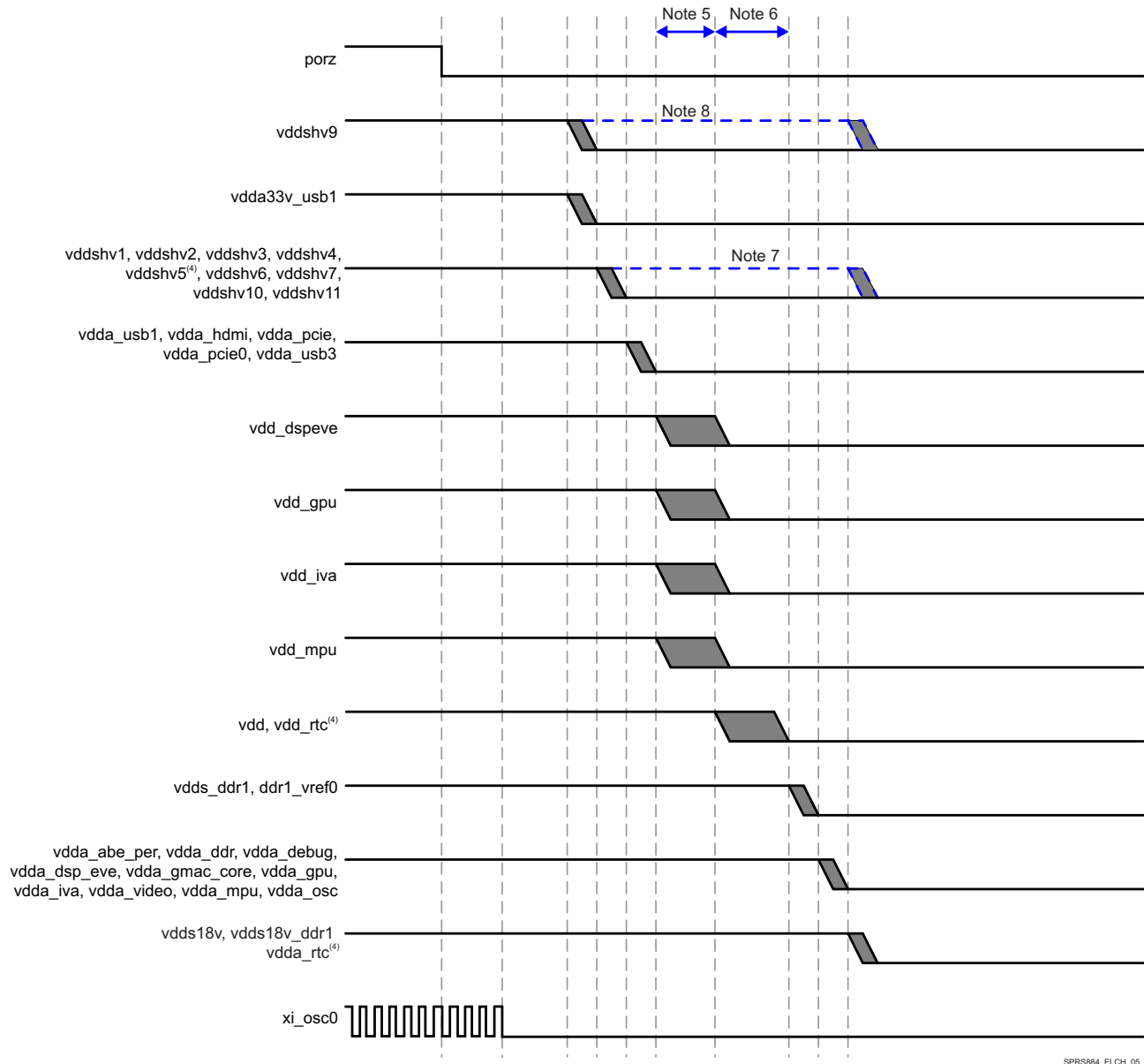
Figure 5-4. Power-Up Sequencing

- (1) Grey shaded areas are windows where it is valid to ramp the voltage rail.
- (2) Blue dashed lines are not valid windows but show alternate ramp possibilities based on the associated note.
- (3) If RTC-mode is not supported then the following combinations are approved:
 - vdda_rtc can be combined with vdds18v
 - vdd_rtc can be combined with vdd

- vddshv5 can be combined with other 1.8V or 3.3V vddshvn rails.

If combinations listed above are not followed then sequencing for these 3 voltage rails should follow the RTC mode timing requirements.

- (4) vdd must ramp before or at the same time as vdd_mpu, vdd_gpu, vdd_dspeve and vdd_iva.
- (5) vdd_mpu, vdd_gpu, vdd_dspeve, vdd_iva can be ramped at the same time or can be staggered.
- (6) If any of the vddshv[1-7,10-11] rails (not including vddshv9) are used as 1.8V only, then these rails can be combined with vdds18v.
- (7) vddshv9 is separated out to show support for dual voltage. If single voltage is used then vddshv9 can be combined with other vddshvn rails but vddshv9 must ramp after vdd.
- (8) vdds and vdda rails must not be combined together, with the one exception of vdda_rtc when RTC-mode is not supported.
- (9) Pulse duration: rtc_porz must remain low 1ms after vdda_rtc, vddshv5, and vdd_rtc are ramped and stable.
- (10) The SYS_32K source must be stable and at a valid frequency 1ms prior to de-asserting rtc_porz high.
- (11) Pulse duration: resetn/porz must remain low a minimum of $12P^{(15)}$ after xi_osc0 is stable and at a valid frequency.
- (12) Setup time: sysboot[15:0] pins must be valid $2P^{(15)}$ before porz is de-asserted high.
- (13) Hold time: sysboot[15:0] pins must be valid $15P^{(15)}$ after porz is de-asserted high.
- (14) resetn to rstoutn delay is 2ms.
- (15) $P = 1/(\text{SYS_CLK1}/610)$ frequency in ns.



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Figure 5-5. Power-Down Sequencing

- (1) Grey shaded areas are windows where it is valid to ramp the voltage rail
- (2) Blue dashed lines are not valid windows but show alternate ramp possibilities based on the associated note
- (3) xi_osc0 can be turned off anytime after porz assertion and must be turned off before vdda_osc voltage rail is shutdown
- (4) The following combinations are recommended for tying off RTC power lines:
 - vdda_rtc can be combined with vdds18v
 - vdd_rtc can be combined with vdd
 - vddshv5 can be combined with other 1.8V or 3.3V vddshvn rails.
- (5) vdd_mpu, vdd_gpu, vdd_dspeve, vdd_iva can be ramped at the same time or can be staggered.
- (6) vdd must ramp after or at the same time as vdd_mpu, vdd_gpu, vdd_dspeve and vdd_iva.
- (7) If any of the vddshv[1-7,10-11] rails (not including vddshv9) are used as 1.8V only, then these rails can be combined with vdds18v. vddshv[1-7,10-11] is allowed to ramp down at either of the two points shown in the timing diagram in either 1.8V mode or in 3.3V mode. If vddshv[1-7,10-11] ramps down at the later time in the diagram then the board design must guarantee that the vddshv[1-7,10-11] rail is never higher than 2.0 V above the vdds18v rail.
- (8) vddshv9 is separated out to show support for dual voltage. If a dedicated LDO/supply source is used for vddshv9, then vddshv9 ramp down should occur at one of the two earliest points in the timing diagram. If vddshv9 is powered by the same supply source as the other vddshvn rails, then it is allowed to ramp down at either of the last two points in the timing diagram.

Figure 5-6 describes vddshv[1-7,10-11] Supplies Falling Before vdds18v Supplies Delta.

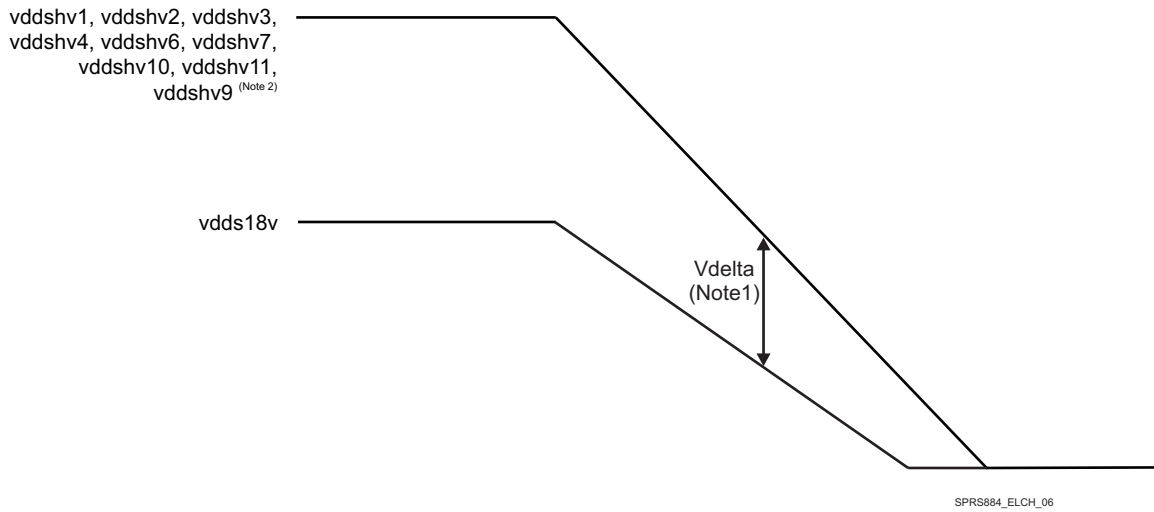


Figure 5-6. vddshv* Supplies Falling After vdds18v Supplies Delta

- (1) Vdelta MAX = 2V
- (2) If vddshv9 is powered by the same supply source as the other vddshv[1-7,10-11] rails.

6 Clock Specifications

NOTE

For more information, see Power, Reset, and Clock Management / PRCM Environment / External Clock Signal and Power Reset / PRCM Functional Description / PRCM Clock Manager Functional Description section of the Device TRM.

NOTE

Audio Back End (ABE) module is not supported for this family of devices, but “ABE” name is still present in some clock or DPLL names.

The device operation requires the following clocks:

- The 32 kHz frequency is used for low frequency operation. It supplies the wake-up domain for operation in lowest power mode. This is an optional clock and will be supplied by on chip divider + mux (FUNC_32K_CLK) incase it is not available on external pin.
- The system clocks, SYS_CLKIN1(Mandatory) and SYS_CLKIN2(Optional) are the main clock sources of the device. They supply the reference clock to the DPLLs as well as functional clock to several modules.

The Device also embeds an internal free-running 32-kHz oscillator that is always active as long as the the wake-up (WKUP) domain is supplied.

[Figure 6-1](#) shows the external input clock sources and the output clocks to peripherals.

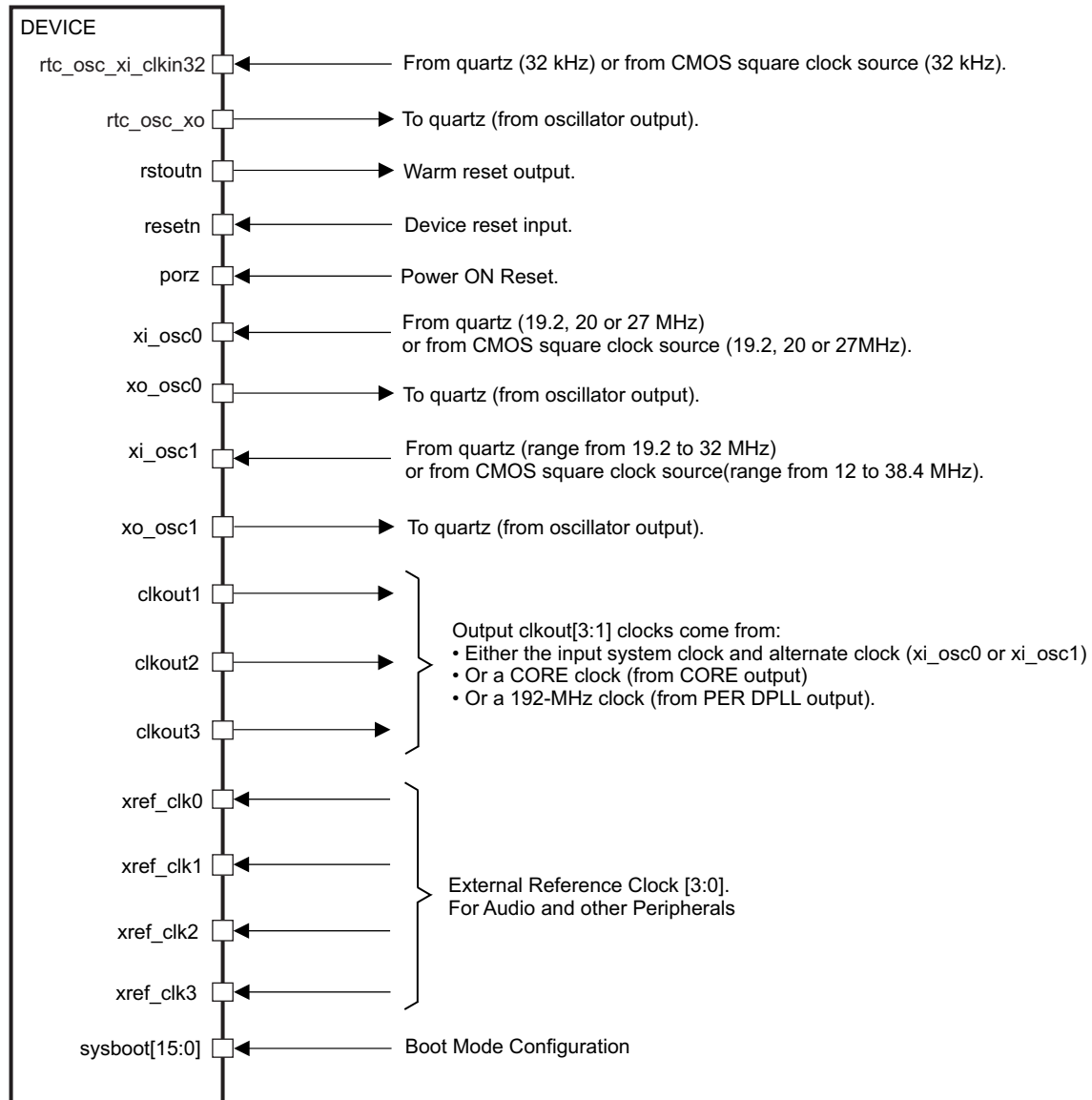


Figure 6-1. Clock Interface

6.1 Input Clock Specifications

6.1.1 Input Clock Requirements

- The source of the internal system clock (SYS_CLK1) could be either:
 - A CMOS clock that enters on the xi_osc0 ball (with xo_osc0 left unconnected on the CMOS clock case).
 - A crystal oscillator clock managed by xi_osc0 and xo_osc0.
- The source of the internal system clock (SYS_CLK2) could be either:
 - A CMOS clock that enters on the xi_osc1 ball (with xo_osc1 left unconnected on the CMOS clock case).
 - A crystal oscillator clock managed by xi_osc1 and xo_osc1.
- The source of the internal system clock (SYS_32K) could be either:
 - A CMOS clock that enters on the rtc_osc_xi_clkin32 ball and supports external LVCMOS clock generators
 - A crystal oscillator clock managed by rtc_osc_xi_clkin32 and rtc_osc_xo.

6.1.2 System Oscillator OSC0 Input Clock

SYS_CLKIN1 is received directly from oscillator OSC0. For more information about SYS_CLKIN1 see Device TRM, Chapter: *Power, Reset, and Clock Management*.

6.1.2.1 OSC0 External Crystal

An external crystal is connected to the device pins. [Figure 6-2](#) describes the crystal implementation.

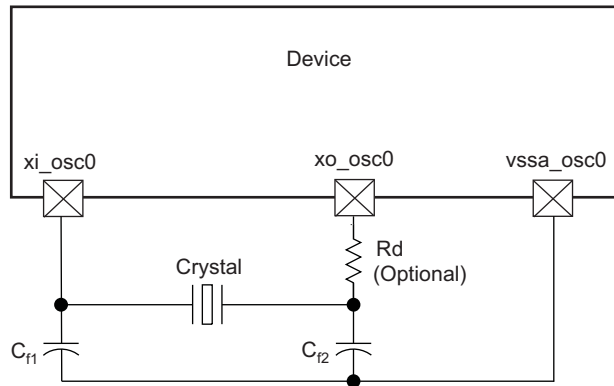


Figure 6-2. Crystal Implementation

NOTE

The load capacitors, C_{f1} and C_{f2} in [Figure 6-2](#), should be chosen such that the below equation is satisfied. C_L in the equation is the load specified by the crystal manufacturer. All discrete components used to implement the oscillator circuit should be placed as close as possible to the associated oscillator xi_osc0 , xo_osc0 , and $vssa_osc0$ pins.

$$C_L = \frac{C_{f1} C_{f2}}{(C_{f1} + C_{f2})}$$

Figure 6-3. Load Capacitance Equation

The crystal must be in the fundamental mode of operation and parallel resonant. [Table 6-1](#) summarizes the required electrical constraints.

Table 6-1. OSC0 Crystal Electrical Characteristics

NAME	DESCRIPTION	MIN	TYP	MAX	UNIT	
f_p	Parallel resonance crystal frequency	19.2, 20, 27			MHz	
C_{f1}	C_{f1} load capacitance for crystal parallel resonance with $C_{f1} = C_{f2}$	12		24	pF	
C_{f2}	C_{f2} load capacitance for crystal parallel resonance with $C_{f1} = C_{f2}$	12		24	pF	
$ESR(C_{f1}, C_{f2})$	Crystal ESR			100	Ω	
C_O	Crystal shunt capacitance	ESR = 30 Ω ESR = 40 Ω	19.2 MHz, 20 MHz, 27 MHz		7	pF
		ESR = 50 Ω	19.2 MHz, 20 MHz		7	pF
			27 MHz		5	pF
		ESR = 60 Ω	19.2 MHz, 20 MHz		7	pF
			27 MHz		Not Supported	
		ESR = 80 Ω	19.2 MHz, 20 MHz		5	pF
27 MHz			Not Supported		-	
ESR = 100 Ω	19.2 MHz, 20 MHz		3	pF		
	27 MHz		Not Supported		-	

Table 6-1. OSC0 Crystal Electrical Characteristics (continued)

NAME	DESCRIPTION	MIN	TYP	MAX	UNIT
L _M	Crystal motional inductance for f _p = 20 MHz		10.16		mH
C _M	Crystal motional capacitance		3.42		fF
t _{j(xi_osc0)}	Frequency accuracy ⁽¹⁾ , xi_osc0	Ethernet and MLB not used		±200	ppm
		Ethernet RGMII and RMII using derived clock		±50	
		Ethernet MII using derived clock		±100	
		MLB using derived clock		±50	

(1) Crystal characteristics should account for tolerance+stability+aging.

When selecting a crystal, the system design must take into account the temperature and aging characteristics of a crystal versus the user environment and expected lifetime of the system.

Table 6-2 details the switching characteristics of the oscillator and the requirements of the input clock.

Table 6-2. Oscillator Switching Characteristics—Crystal Mode

NAME	DESCRIPTION	MIN	TYP	MAX	UNIT
f _p	Oscillation frequency		19.2, 20, 27 MHz		MHz
t _{sX}	Start-up time			4	ms

6.1.2.2 OSC0 Input Clock

A 1.8-V LVCMOS-Compatible Clock Input can be used instead of the internal oscillator to provide the SYS_CLKIN1 clock input to the system. The external connections to support this are shown in Figure 6-4. The xi_osc0 pin is connected to the 1.8-V LVCMOS-Compatible clock source. The xi_osc0 pin is left unconnected. The vssa_osc0 pin is connected to board ground (VSS).

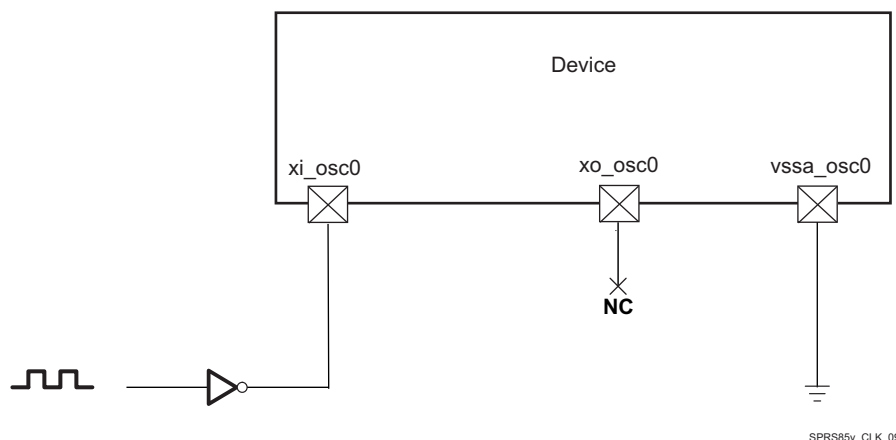


Figure 6-4. 1.8-V LVCMOS-Compatible Clock Input

Table 6-3 summarizes the OSC0 input clock electrical characteristics.

Table 6-3. OSC0 Input Clock Electrical Characteristics—Bypass Mode

NAME	DESCRIPTION	MIN	TYP	MAX	UNIT
f	Frequency		19.2, 20, or 27		MHz
C _{IN}	Input capacitance	1.867	2.067	2.267	pF
I _{IN}	Input current (3.3V mode)	4	6	10	μA

Table 6-4 details the OSC0 input clock timing requirements.

Table 6-4. OSC0 Input Clock Timing Requirements

NAME	DESCRIPTION		MIN	TYP	MAX	UNIT
CK0	$1 / t_{c(xi_osc0)}$	Frequency, xi_osc0	19.2, 20, 27			MHz
CK1	$t_{w(xi_osc0)}$	Pulse duration, xi_osc0 low or high	0.45 *		0.55 *	ns
	$t_{j(xi_osc0)}$	Period jitter ⁽¹⁾ , xi_osc0			$0.01 \times t_{c(xi_osc0)}$	ns
	$t_{R(xi_osc0)}$	Rise time, xi_osc0			5	ns
	$t_{F(xi_osc0)}$	Fall time, xi_osc0			5	ns
	$t_{j(xi_osc0)}$	Frequency accuracy ⁽²⁾ , xi_osc0	Ethernet and MLB not used		± 200	ppm
Ethernet RGMII and RMII using derived clock			± 50			
Ethernet MII using derived clock			± 100			
MLB using derived clock			± 50			

(1) Period jitter is meant here as follows:

- The maximum value is the difference between the longest measured clock period and the expected clock period
- The minimum value is the difference between the shortest measured clock period and the expected clock period

(2) Crystal characteristics should account for tolerance+stability+aging.

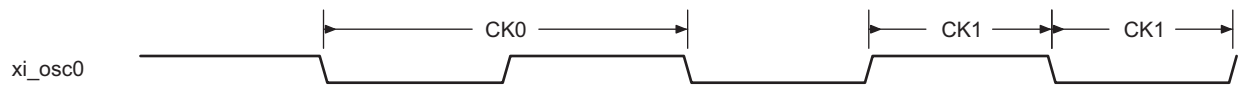


Figure 6-5. xi_osc0 Input Clock

6.1.3 Auxiliary Oscillator OSC1 Input Clock

SYS_CLKIN2 is received directly from oscillator OSC1. For more information about SYS_CLKIN2 see Device TRM, Chapter: *Power, Reset, and Clock Management*.

6.1.3.1 OSC1 External Crystal

An external crystal is connected to the device pins. Figure 6-6 describes the crystal implementation.

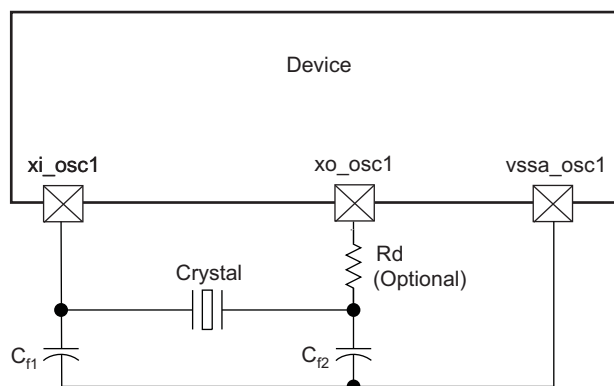


Figure 6-6. Crystal Implementation

NOTE

The load capacitors, C_{f1} and C_{f2} in Figure 6-6, should be chosen such that the below equation is satisfied. C_L in the equation is the load specified by the crystal manufacturer. All discrete components used to implement the oscillator circuit should be placed as close as possible to the associated oscillator xi_osc1, xo_osc1, and vssa_osc1 pins.

$$C_L = \frac{C_{f1} C_{f2}}{(C_{f1} + C_{f2})}$$

Figure 6-7. Load Capacitance Equation

The crystal must be in the fundamental mode of operation and parallel resonant. Table 6-5 summarizes the required electrical constraints.

Table 6-5. OSC1 Crystal Electrical Characteristics

NAME	DESCRIPTION	MIN	TYP	MAX	UNIT		
f_p	Parallel resonance crystal frequency	Range from 19.2 to 32			MHz		
C_{f1}	C_{f1} load capacitance for crystal parallel resonance with $C_{f1} = C_{f2}$	12		24	pF		
C_{f2}	C_{f2} load capacitance for crystal parallel resonance with $C_{f1} = C_{f2}$	12		24	pF		
ESR(C_{f1}, C_{f2})	Crystal ESR			100	Ω		
C_O	Crystal shunt capacitance	ESR = 30 Ω	19.2 MHz $\leq f_p \leq$ 32 MHz		7	pF	
			19.2 MHz $\leq f_p \leq$ 32 MHz		5	pF	
		ESR = 50 Ω	19.2 MHz $\leq f_p \leq$ 25 MHz		7	pF	
			25 MHz $< f_p \leq$ 27 MHz		5	pF	
		ESR = 60 Ω	27 MHz $< f_p \leq$ 32 MHz		Not Supported		-
			19.2 MHz $\leq f_p \leq$ 23 MHz			7	pF
			23 MHz $< f_p \leq$ 25 MHz			5	pF
		ESR = 80 Ω	25 MHz $< f_p \leq$ 32 MHz		Not Supported		-
			19.2 MHz $\leq f_p \leq$ 23 MHz			5	pF
			23 MHz $\leq f_p \leq$ 25 MHz			3	pF
		ESR = 100 Ω	25 MHz $< f_p \leq$ 32 MHz		Not Supported		-
			19.2 MHz $\leq f_p \leq$ 20 MHz			3	pF
	20 MHz $< f_p \leq$ 32 MHz	Not Supported			-		
L_M	Crystal motional inductance for $f_p = 20$ MHz		10.16		mH		
C_M	Crystal motional capacitance		3.42		fF		
$t_j(xiosc1)$	Frequency accuracy ⁽¹⁾ , xi_osc1	Ethernet and MLB not used			± 200	ppm	
		Ethernet RGMII and RMII using derived clock			± 50		
		Ethernet MII using derived clock			± 100		
		MLB using derived clock			± 50		

(1) Crystal characteristics should account for tolerance+stability+aging.

When selecting a crystal, the system design must take into account the temperature and aging characteristics of a crystal versus the user environment and expected lifetime of the system.

Table 6-6 details the switching characteristics of the oscillator and the requirements of the input clock.

Table 6-6. Oscillator Switching Characteristics—Crystal Mode

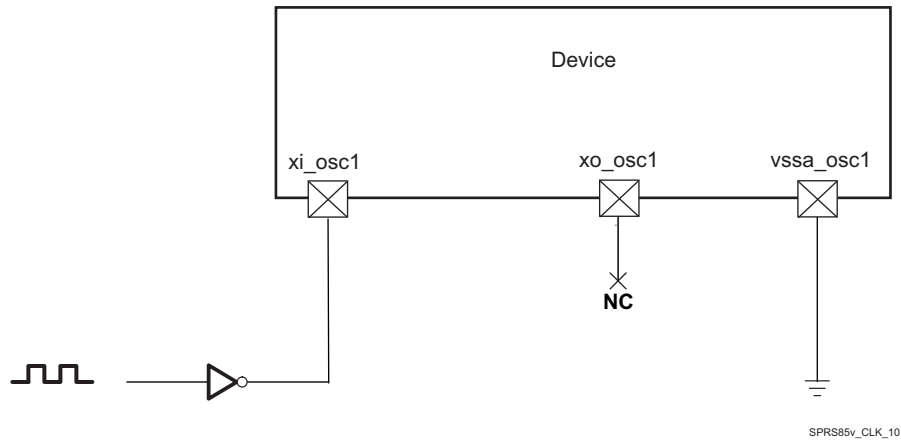
NAME	DESCRIPTION	MIN	TYP	MAX	UNIT
f_p	Oscillation frequency	Range from 19.2 to 32			MHz

Table 6-6. Oscillator Switching Characteristics—Crystal Mode (continued)

NAME	DESCRIPTION	MIN	TYP	MAX	UNIT
t_{sX}	Start-up time			4	ms

6.1.3.2 OSC1 Input Clock

A 1.8-V LVCMOS-Compatible Clock Input can be used instead of the internal oscillator to provide the SYS_CLKIN2 clock input to the system. The external connections to support this are shown in, [Figure 6-8](#). The xi_osc1 pin is connected to the 1.8-V LVCMOS-Compatible clock sources. The xo_osc1 pin is left unconnected. The vssa_osc1 pin is connected to board ground (vss).

**Figure 6-8. 1.8-V LVCMOS-Compatible Clock Input**

[Table 6-7](#) summarizes the OSC1 input clock electrical characteristics.

Table 6-7. OSC1 Input Clock Electrical Characteristics—Bypass Mode

NAME	DESCRIPTION	MIN	TYP	MAX	UNIT
f	Frequency	Range from 12 to 38.4			MHz
C_{IN}	Input capacitance	1.850	2.050	2.250	pF
I_{IN}	Input current (3.3V mode)	4	6	10	μ A
t_{sX}	Start-up time ⁽¹⁾	See ⁽²⁾			ms

- (1) To switch from bypass mode to crystal or from crystal mode to bypass mode, there is a waiting time about 100 μ s; however, if the chip comes from bypass mode to crystal mode the crystal will start-up after time mentioned in [Table 6-6](#), t_{sX} parameter.
- (2) Before the processor boots up and the oscillator is set to bypass mode, there is a waiting time when the internal oscillator is in application mode and receives a wave. The switching time in this case is about 100 μ s.

[Table 6-8](#) details the OSC1 input clock timing requirements.

Table 6-8. OSC1 Input Clock Timing Requirements

NAME	DESCRIPTION		MIN	TYP	MAX	UNIT
CK0	$1 / t_{c(xiosc1)}$	Frequency, xi_osc1	Range from 12 to 38.4			MHz
CK1	$t_{w(xiosc1)}$	Pulse duration, xi_osc1 low or high	0.45 * $t_{c(xiosc1)}$		0.55 * $t_{c(xiosc1)}$	ns
	$t_{j(xiosc1)}$	Period jitter ⁽¹⁾ , xi_osc1			$0.01 \times t_{c(xiosc1)}$ ⁽³⁾	ns
	$t_{R(xiosc1)}$	Rise time, xi_osc1			5	ns
	$t_{F(xiosc1)}$	Fall time, xi_osc1			5	ns

Table 6-8. OSC1 Input Clock Timing Requirements (continued)

NAME	DESCRIPTION		MIN	TYP	MAX	UNIT
$t_{j(xiosc1)}$	Frequency accuracy ⁽²⁾ , xi_osc1	Ethernet and MLB not used			±200	ppm
		Ethernet RGMII and RMII using derived clock			±50	
		Ethernet MII using derived clock			±100	
		MLB using derived clock			±50	

(1) Period jitter is meant here as follows:

- The maximum value is the difference between the longest measured clock period and the expected clock period
- The minimum value is the difference between the shortest measured clock period and the expected clock period

(2) Crystal characteristics should account for tolerance+stability+aging.

(3) The Period jitter requirement for osc1 can be relaxed to $0.02 \cdot t_{c(xiosc1)}$ under the following constraints:

- a. The osc1/SYS_CLK2 clock bypasses all device PLLs
- b. The osc1/SYS_CLK2 clock is only used to source the DSS pixel clock outputs

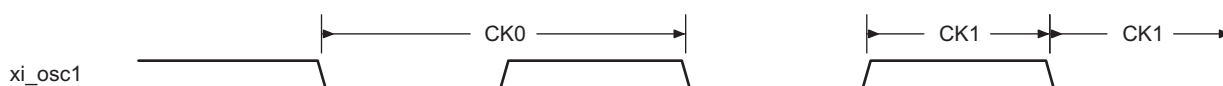


Figure 6-9. xi_osc1 Input Clock

6.1.4 RTC Oscillator Input Clock

SYS_32K is received directly from RTC Oscillator. For more information about SYS_32K see Device TRM, Chapter: *Power, Reset, and Clock Management*.

6.1.4.1 RTC Oscillator External Crystal

An external crystal is connected to the device pins. [Figure 6-2](#) describes the crystal implementation.

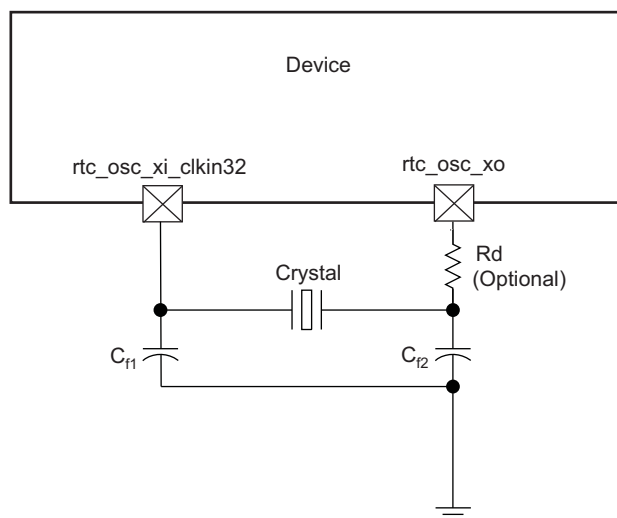


Figure 6-10. Crystal Implementation

NOTE

The load capacitors, C_{f1} and C_{f2} in [Figure 6-10](#), should be chosen such that the below equation is satisfied. C_L in the equation is the load specified by the crystal manufacturer. All discrete components used to implement the oscillator circuit should be placed as close as possible to the associated oscillator $rtc_osc_xi_clkln32$ and rtc_osc_xo pins.

$$C_L = \frac{C_{f1} C_{f2}}{(C_{f1} + C_{f2})}$$

Figure 6-11. Load Capacitance Equation

The crystal must be in the fundamental mode of operation and parallel resonant. [Table 6-1](#) summarizes the required electrical constraints.

Table 6-9. RTC Crystal Electrical Characteristics

NAME	DESCRIPTION	MIN	TYP	MAX	UNIT
f_p	Parallel resonance crystal frequency	32.768			kHz
C_{f1}	C_{f1} load capacitance for crystal parallel resonance with $C_{f1} = C_{f2}$	12		24	pF
C_{f2}	C_{f2} load capacitance for crystal parallel resonance with $C_{f1} = C_{f2}$	12		24	pF
ESR(C_{f1}, C_{f2})	Crystal ESR			80	k Ω
C_O	Crystal shunt capacitance			5	pF
L_M	Crystal motional inductance for $f_p = 32,768$ kHz		10.7		mH
C_M	Crystal motional capacitance		2.2		fF
$t_{j}(\text{rtc_osc_xi_clk}32)$	Frequency accuracy, rtc_osc_xi_clk32			± 200	ppm

When selecting a crystal, the system design must take into account the temperature and aging characteristics of a crystal versus the user environment and expected lifetime of the system.

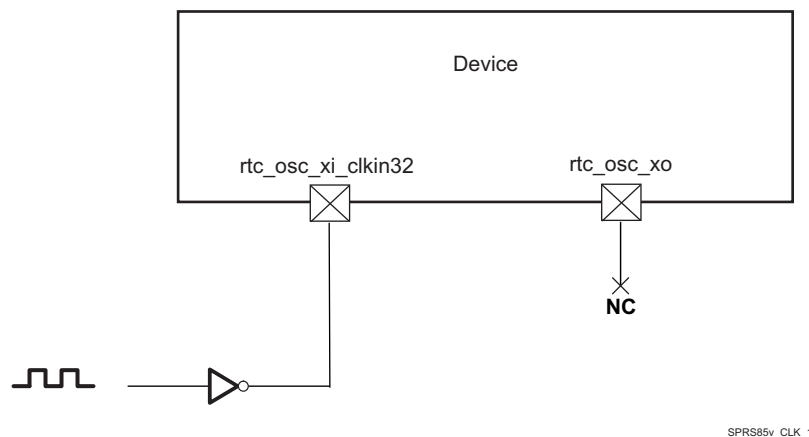
[Table 6-10](#) details the switching characteristics of the oscillator and the requirements of the input clock.

Table 6-10. Oscillator Switching Characteristics—Crystal Mode

NAME	DESCRIPTION	MIN	TYP	MAX	UNIT
f_p	Oscillation frequency	32.768			kHz
t_{sX}	Start-up time			4	ms

6.1.4.2 RTC Oscillator Input Clock

A 1.8-V LVCMOS-Compatible Clock Input can be used instead of the internal oscillator to provide the SYS_32K clock input to the system. The external connections to support this are shown in [Figure 6-12](#). The rtc_osc_xi_clk32 pin is connected to the 1.8-V LVCMOS-Compatible clock sources. The rtc_osc_xo pin is left unconnected.

**Figure 6-12. LVCMOS-Compatible Clock Input**

[Table 6-11](#) summarizes the RTC Oscillator input clock electrical characteristics.

Table 6-11. RTC Oscillator Input Clock Electrical Characteristics—Bypass Mode

NAME	DESCRIPTION	MIN	TYP	MAX	UNIT
CK0	$1/t_{c(\text{rtc_osc_xi_clkin32})}$ Frequency, rtc_osc_xi_clkin32	32.768			kHz
CK1	$t_{w(\text{rtc_osc_xi_clkin32})}$ Pulse duration, rtc_osc_xi_clkin32 low or high	0.45 * $t_{c(\text{rtc_osc_xi_clkin32})}$		0.55 * $t_{c(\text{rtc_osc_xi_clkin32})}$	ns
	C_{IN} Input capacitance	1.750	1.950	2.150	pF
	I_{IN} Input current (3.3V mode)	4	6	10	μA
	t_{sX} Start-up time	See ⁽¹⁾			ms

(1) Before the processor boots up and the oscillator is set to bypass mode, there is a waiting time when the internal oscillator is in application mode and receives a wave. The switching time in this case is about 100 μs.

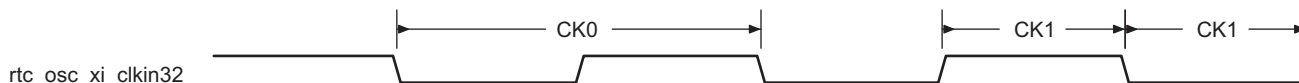


Figure 6-13. rtc_osc_xi_clkin32 Input Clock

6.2 RC On-die Oscillator Clock

NOTE

The OSC_32K_CLK clock, provided by the On-die 32K RC oscillator, inside of the SoC, is not accurate 32kHz clock.

The frequency may significantly vary with temperature and silicon characteristics.

For more information about OSC_32K_CLK see the Device TRM, Chapter: *Power, Reset, and Clock Management*.

6.3 DPLLs, DLLs Specifications

NOTE

For more information, see:

- Power, Reset, and Clock Management / Clock Management Functional / Internal Clock Sources / Generators / Generic DPLL Overview Section and
- Display Subsystem / Display Subsystem Overview section of the Device TRM.

To generate high-frequency clocks, the device supports multiple on-chip DPLLs controlled directly by the PRCM module. They are of two types: type A and type B DPLLs.

- They have their own independent power domain (each one embeds its own switch and can be controlled as an independent functional power domain)
- They are fed with ALWAYS ON system clock, with independent control per DPLL.

The different DPLLs managed by the PRCM are listed below:

- DPLL_MPU: It supplies the MPU subsystem clocking internally.
- DPLL_IVA: It feeds the IVA subsystem clocking.
- DPLL_CORE: It supplies all interface clocks and also few module functional clocks.
- DPLL_PER: It supplies several clock sources: a 192-MHz clock for the display functional clock, a 96-MHz functional clock to subsystems and peripherals.
- DPLL_ABE: It provides clocks to various modules within the device.
- DPLL_USB: It provides 960M clock for USB modules (USB1/2/3/4).
- DPLL_GMAC: It supplies several clocks for the Gigabit Ethernet Switch (GMAC_SW).
- DPLL_EVE: It provides the Embedded Vision Engine Subsystem (EVE1/2/3/4) clocking.

- DPLL_DSP: It feeds the DSP Subsystem clocking.
- DPLL_GPU: It supplies clock for the GPU Subsystem.
- DPLL_DDR: It generates clocks for the two External Memory Interface (EMIF) controllers and their associated EMIF PHYs.
- DPLL_PCIE_REF: It provides reference clock for the APLL_PCIE in PCIE Subsystem.
- APLL_PCIE: It feeds clocks for the device Peripheral Component Interconnect Express (PCIe) controllers.

NOTE

The following DPLLs are controlled by the clock manager located in the always-on Core power domain (CM_CORE_AON):

- DPLL_MPU, DPLL_IVA, DPLL_CORE, DPLL_ABE, DPLL_DDR, DPLL_GMAC, DPLL_PCIE_REF, DPLL_PER, DPLL_USB, DPLL_EVE, DPLL_DSP, DPLL_GPU, APLL_PCIE_REF.
-

For more information on CM_CORE_AON and CM_CORE or PRCM DPLLs, see the Power, Reset, and Clock Management (PRCM) chapter of the Device TRM.

The following DPLLs are not managed by the PRCM:

- DPLL_VIDEO1; (It is controlled from DSS)
 - DPLL_VIDEO2; (It is controlled from DSS)
 - DPLL_HDMI; (It is controlled from DSS)
 - DPLL_SATA; (It is controlled from SATA)
 - DPLL_DEBUG; (It is controlled from DEBUGSS)
 - DPLL_USB_OTG_SS; (It is controlled from OCP2SCP1)
-

NOTE

For more information for not controlled from PRCM DPLL's see the related chapters in TRM.

6.3.1 DPLL Characteristics

The DPLL has three relevant input clocks. One of them is the reference clock (CLKINP) used to generate the synthesized clock but can also be used as the bypass clock whenever the DPLL enters a bypass mode. It is therefore mandatory. The second one is a fast bypass clock (CLKINPULOW) used when selected as the bypass clock and is optional. The third clock (CLKINPHIF) is explained in the next paragraph.

The DPLL has three output clocks (namely CLKOUT, CLKOUTX2, and CLKOUTHIF). CLKOUT and CLKOUTX2 run at the bypass frequency whenever the DPLL enters a bypass mode. Both of them are generated from the lock frequency divided by a post-divider (namely M2 post-divider). The third clock, CLKOUTHIF, has no automatic bypass capability. It is an output of a post-divider (M3 post-divider) with the input clock selectable between the internal lock clock (Fdpll) and CLKINPHIF input of the PLL through an asynchronous multiplexing.

For more information, see the Power Reset Controller Management chapter of the Device TRM.

Table 6-12 summarizes DPLL type described in Section 6.3, *DPLLs, DLLs Specifications* introduction.

Table 6-12. DPLL Control Type

DPLL NAME	TYPE	CONTROLLED BY PRCM
DPLL_ABE	Table 6-13 (Type A)	Yes ⁽¹⁾
DPLL_CORE	Table 6-13 (Type A)	Yes ⁽¹⁾

Table 6-12. DPLL Control Type (continued)

DPLL NAME	TYPE	CONTROLLED BY PRCM
DPLL_DEBUGSS	Table 6-13 (Type A)	No ⁽²⁾
DPLL_DSP	Table 6-13 (Type A)	Yes ⁽¹⁾
DPLL_EVE	Table 6-13 (Type A)	Yes ⁽¹⁾
DPLL_GMAC	Table 6-13 (Type A)	Yes ⁽¹⁾
DPLL_HDMI	Table 6-14 (Type B)	No ⁽²⁾
DPLL_IVA	Table 6-13 (Type A)	Yes ⁽¹⁾
DPLL_MPU	Table 6-13 (Type A)	Yes ⁽¹⁾
DPLL_PER	Table 6-13 (Type A)	Yes ⁽¹⁾
APLL_PCIE	Table 6-13 (Type A)	Yes ⁽¹⁾
DPLL_PCIE_REF	Table 6-14 (Type B)	Yes ⁽¹⁾
DPLL_SATA	Table 6-14 (Type B)	No ⁽²⁾
DPLL_USB	Table 6-14 (Type B)	Yes ⁽¹⁾
DPLL_USB_OTG_SS	Table 6-14 (Type B)	No ⁽²⁾
DPLL_VIDEO1	Table 6-13 (Type A)	No ⁽²⁾
DPLL_VIDEO2	Table 6-13 (Type A)	No ⁽²⁾
DPLL_DDR	Table 6-13 (Type A)	Yes ⁽¹⁾
DPLL_GPU	Table 6-13 (Type A)	Yes ⁽¹⁾

(1) DPLL is in the always-on domain.

(2) DPLL is not controlled by the PRCM.

Table 6-13 and Table 6-14 summarize the DPLL characteristics and assume testing over recommended operating conditions.

Table 6-13. DPLL Type A Characteristics

NAME	DESCRIPTION	MIN	TYP	MAX	UNIT	COMMENTS
f _{input}	CLKINP input frequency	0.032		52	MHz	F _{INP}
f _{internal}	Internal reference frequency	0.15		52	MHz	REFCLK
f _{CLKINPHIF}	CLKINPHIF input frequency	10		1400	MHz	F _{INPHIF}
f _{CLKINPULOW}	CLKINPULOW input frequency	0.001		600	MHz	Bypass mode: f _{CLKOUT} = f _{CLKINPULOW} / (M1 + 1) if ulowclken = 1 ⁽⁶⁾
f _{CLKOUT}	CLKOUT output frequency	20 ⁽¹⁾		1800 ⁽²⁾	MHz	[M / (N + 1)] × F _{INP} × [1 / M2] (in locked condition)
f _{CLKOUTx2}	CLKOUTx2 output frequency	40 ⁽¹⁾		2200 ⁽²⁾	MHz	2 × [M / (N + 1)] × F _{INP} × [1 / M2] (in locked condition)
f _{CLKOUTHIF}	CLKOUTHIF output frequency	20 ⁽³⁾		1400 ⁽⁴⁾	MHz	F _{INPHIF} / M3 if clkiphifsel = 1
		40 ⁽³⁾		2200 ⁽⁴⁾	MHz	2 × [M / (N + 1)] × F _{INP} × [1 / M3] if clkiphifsel = 0
f _{CLKDCOLDO}	DCOCLKLDO output frequency	40		2800	MHz	2 × [M / (N + 1)] × F _{INP} (in locked condition)
t _{lock}	Frequency lock time			6 + 350 × REFCLK	μs	
p _{lock}	Phase lock time			6 + 500 × REFCLK	μs	
t _{relock-L}	Relock time—Frequency lock ⁽⁵⁾ (LP relock time from bypass)			6 + 70 × REFCLK	μs	DPLL in LP relock time: lowcurrstdby = 1
p _{relock-L}	Relock time—Phase lock ⁽⁵⁾ (LP relock time from bypass)			6 + 120 × REFCLK	μs	DPLL in LP relock time: lowcurrstdby = 1
t _{relock-F}	Relock time—Frequency lock ⁽⁵⁾ (fast relock time from bypass)			3.55 + 70 × REFCLK	μs	DPLL in fast relock time: lowcurrstdby = 0

Table 6-13. DPLL Type A Characteristics (continued)

NAME	DESCRIPTION	MIN	TYP	MAX	UNIT	COMMENTS
P _{relock-F}	Relock time—Phase lock ⁽⁵⁾ (fast relock time from bypass)			3.55 + 120 × REFCLK	μs	DPLL in fast relock time: lowcurrstbby = 0

(1) The minimum frequencies on CLKOUT and CLKOUTX2 are assuming M2 = 1.

For M2 > 1, the minimum frequency on these clocks will further scale down by factor of M2.

(2) The maximum frequencies on CLKOUT and CLKOUTX2 are assuming M2 = 1.

(3) The minimum frequency on CLKOUTHIF is assuming M3 = 1. For M3 > 1, the minimum frequency on this clock will further scale down by factor of M3.

(4) The maximum frequency on CLKOUTHIF is assuming M3 = 1.

(5) Relock time assumes typical operating conditions, 10°C maximum temperature drift.

(6) Bypass mode: f_{CLKOUT} = F_{INP} if ulowclken = 0. For more information, see the Device TRM.

Table 6-14. DPLL Type B Characteristics

NAME	DESCRIPTION	MIN	TYP	MAX	UNIT	COMMENTS
f _{input}	CLKINP input clock frequency	0.62		60	MHz	F _{INP}
f _{internal}	REFCLK internal reference clock frequency	0.62		2.5	MHz	[1 / (N + 1)] × F _{INP}
f _{CLKINPULOW}	CLKINPULOW bypass input clock frequency	0.001		600	MHz	Bypass mode: f _{CLKOUT} = f _{CLKINPULOW} / (M1 + 1) if ulowclken = 1 ⁽⁴⁾
f _{CLKLDOOUT}	CLKOUTLDO output clock frequency	20 ⁽¹⁾⁽⁵⁾		2500 ⁽²⁾⁽⁵⁾	MHz	M / (N + 1) × F _{INP} × [1 / M2] (in locked condition)
f _{CLKOUT}	CLKOUT output clock frequency	20 ⁽¹⁾⁽⁵⁾		1450 ⁽²⁾⁽⁵⁾	MHz	[M / (N + 1)] × F _{INP} × [1 / M2] (in locked condition)
f _{CLKDCOLDO}	Internal oscillator (DCO) output clock frequency	750 ⁽⁵⁾		1500 ⁽⁵⁾	MHz	[M / (N + 1)] × F _{INP} (in locked condition)
		1250 ⁽⁵⁾		2500 ⁽⁵⁾	MHz	
t _j	CLKOUTLDO period jitter	–2.5%		2.5%		The period jitter at the output clocks is ± 2.5% peak to peak
	CLKOUT period jitter					
	CLKDCOLDO period jitter					
t _{lock}	Frequency lock time			350 × REFCLKs	μs	
p _{lock}	Phase lock time			500 × REFCLKs	μs	
t _{relock-L}	Relock time—Frequency lock ⁽³⁾ (LP relock time from bypass)			9 + 30 × REFCLKs	μs	
P _{relock-L}	Relock time—Phase lock ⁽³⁾ (LP relock time from bypass)			9 + 125 × REFCLKs	μs	

(1) The minimum frequency on CLKOUT is assuming M2 = 1.

For M2 > 1, the minimum frequency on this clock will further scale down by factor of M2.

(2) The maximum frequency on CLKOUT is assuming M2 = 1.

(3) Relock time assumes typical operating conditions, 10°C maximum temperature drift.

(4) Bypass mode: f_{CLKOUT} = F_{INP} if ULOWCLKEN = 0. For more information, see the Device TRM.

(5) For output clocks, there are two frequency ranges according to the SELFREQDCO setting. For more information, see the Device TRM.

6.3.2 DLL Characteristics

Table 6-15 summarizes the DLL characteristics and assumes testing over recommended operating conditions.

Table 6-15. DLL Characteristics

NAME	DESCRIPTION	MIN	TYP	MAX	UNIT
f _{input}	Input clock frequency (EMIF_DLL_FCLK)			266	MHz

Table 6-15. DLL Characteristics (continued)

NAME	DESCRIPTION	MIN	TYP	MAX	UNIT
t_{lock}	Lock time			50k	cycles
t_{relock}	Relock time (a change of the DLL frequency implies that DLL must relock)			50k	cycles

6.3.3 DPLL and DLL Noise Isolation

NOTE

For more information on DPLL and DLL decoupling capacitor requirements, see the External Capacitors / Voltage Decoupling Capacitors / I/O and Analog Voltage Decoupling / VDDA Power Domain section.

7 Timing Requirements and Switching Characteristics

7.1 Timing Test Conditions

All timing requirements and switching characteristics are valid over the recommended operating conditions unless otherwise specified.

7.2 Interface Clock Specifications

7.2.1 Interface Clock Terminology

The interface clock is used at the system level to sequence the data and/or to control transfers accordingly with the interface protocol.

7.2.2 Interface Clock Frequency

The two interface clock characteristics are:

- The maximum clock frequency
- The maximum operating frequency

The interface clock frequency documented in this document is the maximum clock frequency, which corresponds to the maximum frequency programmable on this output clock. This frequency defines the maximum limit supported by the Device IC and does not take into account any system consideration (PCB, peripherals).

The system designer will have to consider these system considerations and the Device IC timing characteristics as well to define properly the maximum operating frequency that corresponds to the maximum frequency supported to transfer the data on this interface.

7.3 Timing Parameters and Information

The timing parameter symbols used in the timing requirement and switching characteristic tables are created in accordance with JEDEC Standard 100. To shorten the symbols, some of pin names and other related terminologies have been abbreviated as follows:

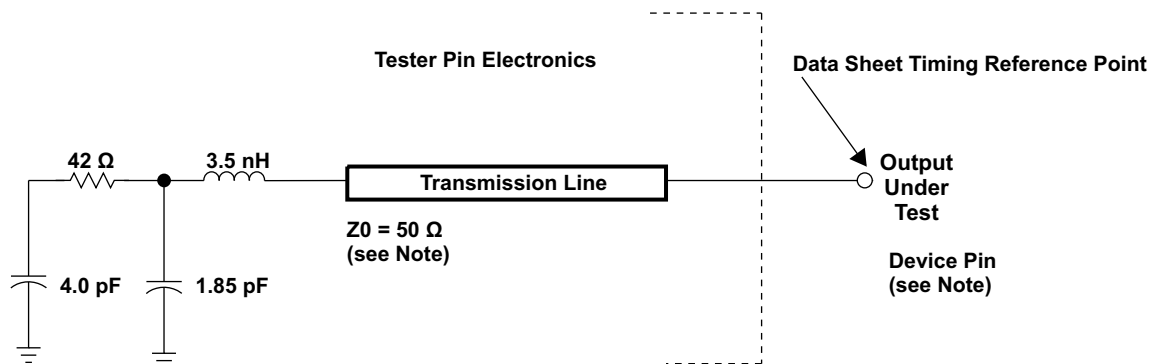
Table 7-1. Timing Parameters

SUBSCRIPTS	
SYMBOL	PARAMETER
c	Cycle time (period)
d	Delay time
dis	Disable time
en	Enable time
h	Hold time
su	Setup time
START	Start bit
t	Transition time
v	Valid time
w	Pulse duration (width)
X	Unknown, changing, or don't care level
F	Fall time
H	High
L	Low
R	Rise time
V	Valid
IV	Invalid

Table 7-1. Timing Parameters (continued)

SUBSCRIPTS	
SYMBOL	PARAMETER
AE	Active Edge
FE	First Edge
LE	Last Edge
Z	High impedance

7.3.1 Parameter Information



NOTE: The data sheet provides timing at the device pin. For output timing analysis, the tester pin electronics and its transmission line effects must be taken into account. A transmission line with a delay of 2 ns can be used to produce the desired transmission line effect. The transmission line is intended as a load only. It is not necessary to add or subtract the transmission line delay (2 ns) from the data sheet timings.

Input requirements in this data sheet are tested with an input slew rate of < 4 Volts per nanosecond (4 V/ns) at the device pin.

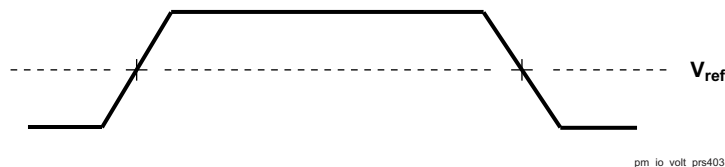
pm_tstcirc_prs403

Figure 7-1. Test Load Circuit for AC Timing Measurements

The load capacitance value stated is only for characterization and measurement of AC timing signals. This load capacitance value does not indicate the maximum load the device is capable of driving.

7.3.1.1 1.8V and 3.3V Signal Transition Levels

All input and output timing parameters are referenced to V_{ref} for both "0" and "1" logic levels. $V_{ref} = (VDD I/O)/2$.



pm_io_volt_prs403

Figure 7-2. Input and Output Voltage Reference Levels for AC Timing Measurements

All rise and fall transition timing parameters are referenced to $V_{IL MAX}$ and $V_{IH MIN}$ for input clocks, $V_{OL MAX}$ and $V_{OH MIN}$ for output clocks.

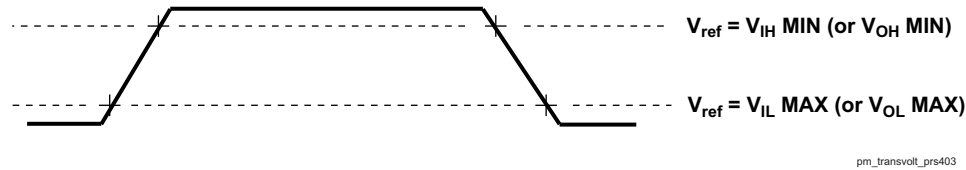


Figure 7-3. Rise and Fall Transition Time Voltage Reference Levels

7.3.1.2 1.8V and 3.3V Signal Transition Rates

The default SLEWCONTROL settings in each pad configuration register must be used to guarantee timings, unless specific instructions otherwise are given in the individual timing sub-sections of the datasheet.

All timings are tested with an input edge rate of 4 volts per nanosecond (4 V/ns).

7.3.1.3 Timing Parameters and Board Routing Analysis

The timing parameter values specified in this data manual do not include delays by board routes. As a good board design practice, such delays must always be taken into account. Timing values may be adjusted by increasing/decreasing such delays. TI recommends using the available I/O buffer information specification (IBIS) models to analyze the timing characteristics correctly. To properly use IBIS models to attain accurate timing analysis for a given system, see the *Using IBIS Models for timing Analysis* application report (literature number [SPRA839](#)). If needed, external logic hardware such as buffers may be used to compensate any timing differences.

7.4 Recommended Clock and Control Signal Transition Behavior

All clocks and control signals must transition between V_{IH} and V_{IL} (or between V_{IL} and V_{IH}) in a monotonic manner. Monotonic transitions are more easily guaranteed with faster switching signals. Slower input transitions are more susceptible to glitches due to noise and special care should be taken for slow input clocks.

7.5 Virtual and Manual I/O Timing Modes

Some of the timings described in the following sections require the use of Virtual or Manual I/O Timing Modes. [Table 7-2](#) provides a summary of the Virtual and Manual I/O Timing Modes across all device interfaces. The individual interface timing sections found later in this document provide the full description of each applicable Virtual and Manual I/O Timing Mode. Refer to the "Pad Configuration" section of the TRM for the procedure on implementing the Virtual and Manual Timing Modes in a system.

Table 7-2. Modes Summary

Virtual or Manual IO Mode Name	Data Manual Timing Mode
VIP	
VIP1_MANUAL1	VIN1A/1B/2A Rise-Edge Capture Mode Timings
VIP1_2B_MANUAL1	VIN2B Rise-Edge Capture Mode Timings
VIP1_MANUAL2	VIN1A/1B/2A Fall-Edge Capture Mode Timings
VIP1_2B_MANUAL2	VIN2B Fall-Edge Capture Mode Timings
VIP2_MANUAL1	VIN3A, VIN3B IOSET1 Rise-Edge Capture Mode Timings
VIP2_4B_MANUAL1	VIN4B Rise-Edge Capture Mode Timings
VIP2_3B_IOSET2_MANUAL1	VIN3B IOSET2 Rise-Edge Capture Mode Timings
VIP2_3B_IOSET2_MANUAL2	VIN3B IOSET2 Fall-Edge Capture Mode Timings
VIP2_MANUAL2	VIN3A, VIN3B IOSET1, Fall-Edge Capture Mode Timings
VIP2_4B_MANUAL2	VIN4B Fall-Edge Capture Mode Timings
DPI Video Output	
VOUT1_MANUAL1	DPI1 Video Output Alternate Timings

Table 7-2. Modes Summary (continued)

Virtual or Manual IO Mode Name	Data Manual Timing Mode
VOUT1_MANUAL2	DPI1 Video Output Default Timings
VOUT1_MANUAL3	DPI1 Video Output MANUAL3 Timings
VOUT1_MANUAL4	DPI1 Video Output MANUAL4 Timings
VOUT2_IOSET1_MANUAL1	DPI2 Video Output IOSET1 Alternate Timings
VOUT2_IOSET1_MANUAL2	DPI2 Video Output IOSET1 Default Timings
VOUT2_IOSET1_MANUAL3	DPI2 Video Output IOSET1 MANUAL3 Timings
VOUT2_IOSET1_MANUAL4	DPI2 Video Output IOSET1 MANUAL4 Timings
VOUT3_MANUAL1	DPI3 Video Output Alternate Timings
VOUT3_MANUAL2	DPI3 Video Output Default Timings
VOUT3_MANUAL3	DPI3 Video Output MANUAL3 Timings
VOUT3_MANUAL4	DPI3 Video Output MANUAL4 Timings
HDMI, EMIF, Timers, I2C, UART, McSPI, USB, PCIe, DCAN, GPIO, PWM, JTAG, TPIU, RTC, SDMA, INTC	
No Virtual or Manual IO Timing Mode Required	All Modes
GPMC	
No Virtual or Manual IO Timing Mode Required	GPMC Asynchronous Mode Timings and Synchronous Mode - Default Timings
GPMC_VIRTUAL1	GPMC Synchronous Mode - Alternate Timings
QSPI	
No Virtual or Manual IO Timing Mode Required	QSPI Mode 3 Default Timing Mode
QSPI_MODE0_MANUAL1	QSPI Mode 0 Default Timing Mode
McASP	
No Virtual or Manual IO Timing Mode Required	McASP1 Synchronous Transmit Timings
MCASP1_VIRTUAL1_ASYNC_TX	See Table 7-47
MCASP1_VIRTUAL2_SYNC_RX	See Table 7-47
MCASP1_VIRTUAL3_ASYNC_RX	See Table 7-47
No Virtual or Manual IO Timing Mode Required	McASP2 Synchronous Transmit Timings
MCASP2_VIRTUAL1_ASYNC_RX_80M	See Table 7-48
MCASP2_VIRTUAL2_ASYNC_RX	See Table 7-48
MCASP2_VIRTUAL3_ASYNC_TX	See Table 7-48
MCASP2_VIRTUAL4_SYNC_RX	See Table 7-48
MCASP2_VIRTUAL5_SYNC_RX_80M	See Table 7-48
No Virtual or Manual IO Timing Mode Required	McASP3 Synchronous Transmit Timings
MCASP3_VIRTUAL2_SYNC_RX	See Table 7-49
No Virtual or Manual IO Timing Mode Required	McASP4 Synchronous Transmit Timings
MCASP4_VIRTUAL1_SYNC_RX	See Table 7-50
No Virtual or Manual IO Timing Mode Required	McASP5 Synchronous Transmit Timings
MCASP5_VIRTUAL1_SYNC_RX	See Table 7-51
No Virtual or Manual IO Timing Mode Required	McASP6 Synchronous Transmit Timings
MCASP6_VIRTUAL1_SYNC_RX	See Table 7-52
No Virtual or Manual IO Timing Mode Required	McASP7 Synchronous Transmit Timings

Table 7-2. Modes Summary (continued)

Virtual or Manual IO Mode Name	Data Manual Timing Mode
MCASP7_VIRTUAL2_SYNC_RX	See Table 7-53
GMAC	
No Virtual or Manual IO Timing Mode Required	GMAC MII1/2 Timings
GMAC_RMII0_MANUAL1	GMAC RMII0 Timings
GMAC_RMII1_MANUAL1	GMAC RMII1 Timings
GMAC_RGMII0_MANUAL1	GMAC RGMII0 Internal Delay Enabled Timings Mode
GMAC_RGMII1_MANUAL1	GMAC RGMII1 Internal Delay Enabled Timings Mode
eMMC/SD/SDIO	
No Virtual or Manual IO Timing Mode Required	MMC2 Standard (Pad Loopback), High Speed (Pad Loopback), and DDR (Pad Loopback) Timings
MMC2_DDR_LB_MANUAL1	MMC2 DDR (Internal Loopback) Timings
MMC2_STD_HS_LB_MANUAL1	MMC2 Standard (Internal Loopback), High Speed (Internal Loopback) Timings
MMC3_MANUAL1	MMC3 DS, SDR12, HS, SDR25, SDR50 Timings
MMC4_MANUAL1	MMC4 SDR12, HS, SDR25 Timings
MMC4_DS_MANUAL1	MMC4 DS Timings

7.6 Video Input Ports (VIP)

The Device includes 3 Video Input Ports (VIP).

Table 7-3, Figure 7-4 and Figure 7-5 present timings and switching characteristics of the VIPs.

CAUTION

The IO timings provided in this section are applicable for all combinations of signals for vin1. However, the timings are only valid for vin2, vin3, and vin4 if signals within a single IOSET are used. The IOSETs are defined in the Table 7-4, Table 7-5 and Table 7-6.

Table 7-3. Timing Requirements for VIP (1)(2)

NO.	PARAMETER	DESCRIPTION	MODE	MIN	MAX	UNIT
V1	$t_{c}(\text{CLK})$	Cycle time, vinx_clki (3) (5)		6.06 (1)		ns
V2	$t_{w}(\text{CLKH})$	Pulse duration, vinx_clki high (3) (5)		0.45*P (2)		ns
V3	$t_{w}(\text{CLKL})$	Pulse duration, vinx_clki low (3) (5)		0.45*P (2)		ns
V4	$t_{su}(\text{CTL/DATA-CLK})$	Input setup time, Control (vinx_dei, vinx_vsynci, vinx_fldi, vinx_hsynci) and Data (vinx_dn) valid to vinx_clki transition (3) (4) (5)	vin1x, vin2x	2.93		ns
			vin3x, vin4b	3.11		ns
V5	$t_{h}(\text{CLK-CTL/DATA})$	Input hold time, Control (vinx_dei, vinx_vsynci, vinx_fldi, vinx_hsynci) and Data (vinx_dn) valid from vinx_clki transition (3) (4) (5)		-0.05		ns

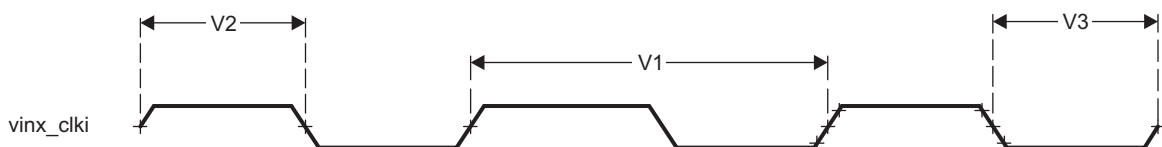
(1) For maximum frequency of 165 MHz.

(2) P = vinx_clki period.

(3) x in vinx = 1a, 1b, 2a, 2b, 3a, 3b, 4b

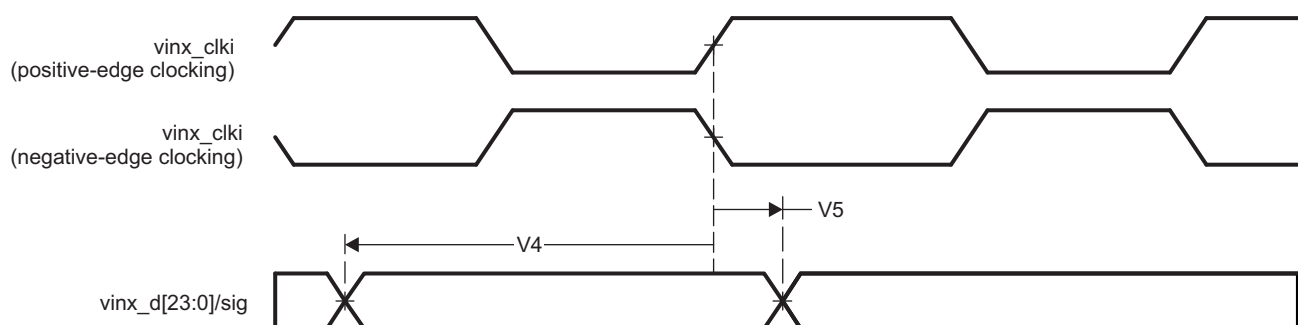
(4) n in dn = 0 to 7 when x = 1b, 2b, 3b and 4b;
n = 0 to 23 when x = 1a, 2a, 3a;

(5) i in clki, dei, vsynci, hsynci and fldi = 0 or 1.



SPRS8xx_VIP_01

Figure 7-4. Video Input Ports clock signal



SPRS8xx_VIP_02

Figure 7-5. Video Input Ports timings

In [Table 7-4](#), [Table 7-5](#) and [Table 7-6](#) are presented the specific groupings of signals (IOSET) for use with vin2, vin3, and vin4.

Table 7-4. VIN2 IOSETs

Signals	IOSET1		IOSET2		IOSET3	
	BALL	MUX	BALL	MUX	BALL	MUX
vin2a						
vin2a_d0	C3	0	C3	0	T1	4
vin2a_d1	B2	0	B2	0	R1	4
vin2a_d2	E7	0	E7	0	T2	4
vin2a_d3	B3	0	B3	0	R6	4
vin2a_d4	A3	0	A3	0	P6	4
vin2a_d5	C6	0	C6	0	U2	4
vin2a_d6	A4	0	A4	0	U3	4
vin2a_d7	B5	0	B5	0	P5	4
vin2a_d8	C5	0	C5	0	U4	4
vin2a_d9	A7	0	A7	0	T3	4
vin2a_d10	A5	0	A5	0	R5	4
vin2a_d11	B6	0	B6	0	R2	4
vin2a_d12	E8	0	E8	0	-	-
vin2a_d13	A6	0	A6	0	-	-
vin2a_d14	C7	0	C7	0	-	-
vin2a_d15	D6	0	D6	0	-	-
vin2a_d16	B7	0	B7	0	-	-
vin2a_d17	B8	0	B8	0	-	-
vin2a_d18	A8	0	A8	0	-	-
vin2a_d19	D7	0	D7	0	-	-
vin2a_d20	C8	0	C8	0	-	-
vin2a_d21	D8	0	D8	0	-	-
vin2a_d22	F8	0	F8	0	-	-
vin2a_d23	E9	0	E9	0	-	-
vin2a_hsync0	D5	0	D5	0	T6	4
vin2a_vsync0	C4	0	C4	0	T4	4
vin2a_de0	B4	0	-	-	T5	4
vin2a_fld0	E6	0	B4	1	R4	4
vin2a_clk0	D4	0	D4	0	R3	4
vin2b						
vin2b_clk1	E6	2	E6	2	V4	4
vin2b_de1	-	-	B4	3	W3	4
vin2b_fld1	B4	2	-	-	-	-
vin2b_d0	E9	2	E9	2	W6	4
vin2b_d1	F8	2	F8	2	V5	4
vin2b_d2	D8	2	D8	2	V3	4
vin2b_d3	C8	2	C8	2	U5	4
vin2b_d4	D7	2	D7	2	V6	4
vin2b_d5	A8	2	A8	2	U6	4
vin2b_d6	B8	2	B8	2	W4	4
vin2b_d7	B7	2	B7	2	W5	4
vin2b_hsync1	D5	3	D5	3	Y1	4

Table 7-4. VIN2 IOSETs (continued)

Signals	IOSET1		IOSET2		IOSET3	
	BALL	MUX	BALL	MUX	BALL	MUX
vin2b_vsync1	C4	3	C4	3	W1	4

Table 7-5. VIN3 IOSETs

Signals	IOSET1		IOSET2		IOSET3		IOSET4	
	BALL	MUX	BALL	MUX	BALL	MUX	BALL	MUX
vin3a								
vin3a_d0	J4	2	AA2	6	AA2	6	C11	4
vin3a_d1	H6	2	AC2	6	AC2	6	E10	4
vin3a_d2	G1	2	Y3	6	Y3	6	D15	4
vin3a_d3	H2	2	AB2	6	AB2	6	E15	4
vin3a_d4	H3	2	AB1	6	AB1	6	D9	4
vin3a_d5	H4	2	AC1	6	AC1	6	E14	4
vin3a_d6	H5	2	AA1	6	AA1	6	D14	4
vin3a_d7	F1	2	Y2	6	Y2	6	D11	4
vin3a_d8	G2	2	B7	6	B7	6	A14	4
vin3a_d9	G3	2	B8	6	B8	6	B11	4
vin3a_d10	G4	2	A8	6	A8	6	B12	4
vin3a_d11	G5	2	D7	6	D7	6	B10	4
vin3a_d12	G6	2	C8	6	-	-	C14	4
vin3a_d13	F5	2	D8	6	-	-	C10	4
vin3a_d14	E5	2	F8	6	-	-	A10	4
vin3a_d15	F4	2	E9	6	-	-	C13	4
vin3a_d16	N3	2	-	-	-	-	B9	4
vin3a_d17	P3	2	-	-	-	-	A9	4
vin3a_d18	P1	2	-	-	-	-	A11	4
vin3a_d19	P2	2	-	-	-	-	C9	4
vin3a_d20	N2	2	-	-	-	-	A13	4
vin3a_d21	N1	2	-	-	-	-	A12	4
vin3a_d22	M5	2	-	-	-	-	B14	4
vin3a_d23	M4	2	-	-	-	-	B13	4
vin3a_hsync0	M1	2	M1	2	F8	5	E12	4
vin3a_vsync0	M3	2	M3	2	E9	5	E13	4
vin3a_de0	M6	2	M6	2	C8	5	D13	4
vin3a_fld0	N5	2	N5	2	D8	5	D10	4
vin3a_clk0	K2	2	AA6	6	AA6	6	E11	4
vin3b								
vin3b_clk1	N6	6	J3	4	-	-	-	-
vin3b_de1	M2	6	M2	6	-	-	-	-
vin3b_fld1	J3	6	-	-	-	-	-	-
vin3b_d0	C2	6	C2	6	-	-	-	-
vin3b_d1	D3	6	D3	6	-	-	-	-
vin3b_d2	D2	6	D2	6	-	-	-	-
vin3b_d3	D1	6	D1	6	-	-	-	-
vin3b_d4	E1	6	E1	6	-	-	-	-
vin3b_d5	E2	6	E2	6	-	-	-	-
vin3b_d6	E3	6	E3	6	-	-	-	-

Table 7-5. VIN3 IOSETs (continued)

Signals	IOSET1		IOSET2		IOSET3		IOSET4	
	BALL	MUX	BALL	MUX	BALL	MUX	BALL	MUX
vin3b_d7	E4	6	E4	6	-	-	-	-
vin3b_hsync1	F3	6	F3	6	-	-	-	-
vin3b_vsync1	C1	6	C1	6	-	-	-	-

Table 7-6. VIN4 IOSETs

Signals	IOSET1		IOSET2	
	BALL	MUX	BALL	MUX
vin4b				
vin4b_clk1	M6	6	R3	5
vin4b_de1	N5	6	T5	5
vin4b_fld1	L5	6	R4	5
vin4b_d0	N3	6	T1	5
vin4b_d1	P3	6	R1	5
vin4b_d2	P1	6	T2	5
vin4b_d3	P2	6	R6	5
vin4b_d4	N2	6	P6	5
vin4b_d5	N1	6	U2	5
vin4b_d6	M5	6	U3	5
vin4b_d7	M4	6	P5	5
vin4b_hsync1	M1	6	T6	5
vin4b_vsync1	M3	6	T4	5

NOTE

To configure the desired Manual IO Timing Mode the user must follow the steps described in section "Manual IO Timing Modes" of the Device TRM.

The associated registers to configure are listed in the CFG REGISTER column. For more information please see the *Control Module Chapter* in the Device TRM.

Manual IO Timings Modes must be used to guarantee some IO timings for VIP1. See [Table 7-2 Modes Summary](#) for a list of IO timings requiring the use of Manual IO Timings Modes. See [Table 7-7 Manual Functions Mapping for VIP1](#) for a definition of the Manual modes.

[Table 7-7](#) lists the A_DELAY and G_DELAY values needed to calculate the correct values to be set in the CFG_x registers.

Table 7-7. Manual Functions Mapping for VIP1

BALL	BALL NAME	VIP1_MANUAL1		VIP1_MANUAL2		CFG REGISTER	MUXMODE				
		A_DELAY (ps)	G_DELAY (ps)	A_DELAY (ps)	G_DELAY (ps)		0	1	2	3	4
R2	RMII_MHZ_50_CLK	1621	614	2018	279	CFG_RMII_MHZ_50_CLK_IN	-	-	-	-	vin2a_d11
M2	gpmc_ben0	1756	1019	2235	494	CFG_GPMC_BEN0_IN	-	-	-	vin1b_hsync1	-
J3	gpmc_ben1	1684	1107	2198	568	CFG_GPMC_BEN1_IN	-	-	-	vin1b_de1	-
T1	mdio_d	1594	417	2007	36	CFG_MDIO_D_IN	-	-	-	-	vin2a_d0
R3	mdio_mclk	0	0	0	0	CFG_MDIO_MCLK_IN	-	-	-	-	vin2a_clk0
U2	rgmii0_rxc	1005	935	1932	0	CFG_RGMII0_RXC_IN	-	-	-	-	vin2a_d5
U3	rgmii0_rxctl	1579	836	1982	485	CFG_RGMII0_RXCTL_IN	-	-	-	-	vin2a_d6
R4	rgmii0_rxd0	1032	1033	1995	0	CFG_RGMII0_RXD0_IN	-	-	-	-	vin2a_fld0
T3	rgmii0_rxd1	950	1625	1993	673	CFG_RGMII0_RXD1_IN	-	-	-	-	vin2a_d9
U4	rgmii0_rxd2	1578	832	1973	535	CFG_RGMII0_RXD2_IN	-	-	-	-	vin2a_d8
P5	rgmii0_rxd3	1022	1648	2017	740	CFG_RGMII0_RXD3_IN	-	-	-	-	vin2a_d7
R6	rgmii0_txc	1604	769	2020	393	CFG_RGMII0_TXC_IN	-	-	-	-	vin2a_d3
P6	rgmii0_txctl	1060	1389	2074	396	CFG_RGMII0_TXCTL_IN	-	-	-	-	vin2a_d4
R5	rgmii0_txd0	938	1242	2021	194	CFG_RGMII0_TXD0_IN	-	-	-	-	vin2a_d10
T4	rgmii0_txd1	1013	1679	2036	730	CFG_RGMII0_TXD1_IN	-	-	-	-	vin2a_vsync0
T6	rgmii0_txd2	1524	886	1933	526	CFG_RGMII0_TXD2_IN	-	-	-	-	vin2a_hsync0
T5	rgmii0_txd3	1079	1504	2090	490	CFG_RGMII0_TXD3_IN	-	-	-	-	vin2a_de0
R1	uart3_rxd	1530	125	1586	0	CFG_UART3_RXD_IN	-	-	-	-	vin2a_d1
T2	uart3_txd	1572	487	1980	16	CFG_UART3_TXD_IN	-	-	-	-	vin2a_d2
AB6	vin1a_clk0	0	0	0	0	CFG_VIN1A_CLK0_IN	vin1a_clk0	-	-	-	-
AD5	vin1a_d0	1697	1087	2105	619	CFG_VIN1A_D0_IN	vin1a_d0	-	-	-	-
AE5	vin1a_d1	1589	1164	2017	757	CFG_VIN1A_D1_IN	vin1a_d1	-	-	-	-
AE3	vin1a_d10	1733	1119	2107	739	CFG_VIN1A_D10_IN	vin1a_d10	vin1b_d5	-	-	-
AA4	vin1a_d11	1563	1210	2005	788	CFG_VIN1A_D11_IN	vin1a_d11	vin1b_d4	-	-	-
AD3	vin1a_d12	1705	1647	2059	1297	CFG_VIN1A_D12_IN	vin1a_d12	vin1b_d3	-	-	-
AC3	vin1a_d13	1624	1525	2027	1141	CFG_VIN1A_D13_IN	vin1a_d13	vin1b_d2	-	-	-
AD2	vin1a_d14	1730	1655	2071	1332	CFG_VIN1A_D14_IN	vin1a_d14	vin1b_d1	-	-	-
AB3	vin1a_d15	1681	2004	1995	1764	CFG_VIN1A_D15_IN	vin1a_d15	vin1b_d0	-	-	-
AA2	vin1a_d16	1659	1813	1999	1542	CFG_VIN1A_D16_IN	vin1a_d16	vin1b_d7	-	-	-
AC2	vin1a_d17	1715	1887	2072	1540	CFG_VIN1A_D17_IN	vin1a_d17	vin1b_d6	-	-	-
Y3	vin1a_d18	1728	1898	2034	1629	CFG_VIN1A_D18_IN	vin1a_d18	vin1b_d5	-	-	-

Table 7-7. Manual Functions Mapping for VIP1 (continued)

BALL	BALL NAME	VIP1_MANUAL1		VIP1_MANUAL2		CFG REGISTER	MUXMODE				
		A_DELAY (ps)	G_DELAY (ps)	A_DELAY (ps)	G_DELAY (ps)		0	1	2	3	4
AB2	vin1a_d19	1707	2006	2026	1761	CFG_VIN1A_D19_IN	vin1a_d19	vin1b_d4	-	-	-
AA5	vin1a_d2	1557	1414	1996	962	CFG_VIN1A_D2_IN	vin1a_d2	-	-	-	-
AB1	vin1a_d20	1695	1814	2037	1469	CFG_VIN1A_D20_IN	vin1a_d20	vin1b_d3	-	-	-
AC1	vin1a_d21	1757	1682	2077	1349	CFG_VIN1A_D21_IN	vin1a_d21	vin1b_d2	-	-	-
AA1	vin1a_d22	1683	1813	2022	1545	CFG_VIN1A_D22_IN	vin1a_d22	vin1b_d1	-	-	-
Y2	vin1a_d23	1833	1187	2168	784	CFG_VIN1A_D23_IN	vin1a_d23	vin1b_d0	-	-	-
Y5	vin1a_d3	1588	1289	1993	901	CFG_VIN1A_D3_IN	vin1a_d3	-	-	-	-
AB7	vin1a_d4	1687	949	2098	499	CFG_VIN1A_D4_IN	vin1a_d4	-	-	-	-
AE4	vin1a_d5	1616	1257	2038	844	CFG_VIN1A_D5_IN	vin1a_d5	-	-	-	-
AB5	vin1a_d6	1582	1265	2002	863	CFG_VIN1A_D6_IN	vin1a_d6	-	-	-	-
AD4	vin1a_d7	1659	1255	2063	873	CFG_VIN1A_D7_IN	vin1a_d7	-	-	-	-
AA3	vin1a_d8	1681	1205	2088	759	CFG_VIN1A_D8_IN	vin1a_d8	vin1b_d7	-	-	-
Y4	vin1a_d9	1778	1168	2152	701	CFG_VIN1A_D9_IN	vin1a_d9	vin1b_d6	-	-	-
AA7	vin1a_de0	1468	1290	1926	728	CFG_VIN1A_DE0_IN	vin1a_de0	vin1b_hsync1	-	-	-
AD6	vin1a_fld0	1633	1425	2043	937	CFG_VIN1A_FLD0_IN	vin1a_fld0	vin1b_vsync1	-	-	-
AC6	vin1a_hsync0	1561	1424	1978	909	CFG_VIN1A_HSYNC0_IN	vin1a_hsync0	vin1b_fld1	-	-	-
AC5	vin1a_vsync0	1470	1369	1926	987	CFG_VIN1A_VSYNC0_IN	vin1a_vsync0	vin1b_de1	-	-	-
AA6	vin1b_clk1	69	150	242	0	CFG_VIN1B_CLK1_IN	vin1b_clk1	-	-	-	-
D4	vin2a_clk0	0	0	0	0	CFG_VIN2A_CLK0_IN	vin2a_clk0	-	-	-	-
C3	vin2a_d0	1597	561	2009	147	CFG_VIN2A_D0_IN	vin2a_d0	-	-	-	-
B2	vin2a_d1	1598	801	2015	561	CFG_VIN2A_D1_IN	vin2a_d1	-	-	-	-
A5	vin2a_d10	1576	655	2021	377	CFG_VIN2A_D10_IN	vin2a_d10	-	-	-	-
B6	vin2a_d11	1488	340	1940	19	CFG_VIN2A_D11_IN	vin2a_d11	-	-	-	-
E8	vin2a_d12	1399	612	1895	181	CFG_VIN2A_D12_IN	vin2a_d12	-	-	-	-
A6	vin2a_d13	1595	439	2063	15	CFG_VIN2A_D13_IN	vin2a_d13	-	-	-	-
C7	vin2a_d14	1480	243	1709	0	CFG_VIN2A_D14_IN	vin2a_d14	-	-	-	-
D6	vin2a_d15	1415	755	1899	369	CFG_VIN2A_D15_IN	vin2a_d15	-	-	-	-
B7	vin2a_d16	1341	653	1821	317	CFG_VIN2A_D16_IN	vin2a_d16	-	vin2b_d7	-	-
B8	vin2a_d17	1396	724	1880	349	CFG_VIN2A_D17_IN	vin2a_d17	-	vin2b_d6	-	-
A8	vin2a_d18	1582	364	1963	0	CFG_VIN2A_D18_IN	vin2a_d18	-	vin2b_d5	-	-
D7	vin2a_d19	1308	289	1681	0	CFG_VIN2A_D19_IN	vin2a_d19	-	vin2b_d4	-	-
E7	vin2a_d2	1600	323	2021	0	CFG_VIN2A_D2_IN	vin2a_d2	-	-	-	-

Table 7-7. Manual Functions Mapping for VIP1 (continued)

BALL	BALL NAME	VIP1_MANUAL1		VIP1_MANUAL2		CFG REGISTER	MUXMODE				
		A_DELAY (ps)	G_DELAY (ps)	A_DELAY (ps)	G_DELAY (ps)		0	1	2	3	4
C8	vin2a_d20	1307	586	1772	299	CFG_VIN2A_D20_IN	vin2a_d20	-	vin2b_d3	-	-
D8	vin2a_d21	1301	640	1787	282	CFG_VIN2A_D21_IN	vin2a_d21	-	vin2b_d2	-	-
F8	vin2a_d22	1316	534	1789	223	CFG_VIN2A_D22_IN	vin2a_d22	-	vin2b_d1	-	-
E9	vin2a_d23	1311	613	1788	286	CFG_VIN2A_D23_IN	vin2a_d23	-	vin2b_d0	-	-
B3	vin2a_d3	1765	720	2142	492	CFG_VIN2A_D3_IN	vin2a_d3	-	-	-	-
A3	vin2a_d4	1680	282	2071	0	CFG_VIN2A_D4_IN	vin2a_d4	-	-	-	-
C6	vin2a_d5	1791	696	2155	461	CFG_VIN2A_D5_IN	vin2a_d5	-	-	-	-
A4	vin2a_d6	1538	175	1849	0	CFG_VIN2A_D6_IN	vin2a_d6	-	-	-	-
B5	vin2a_d7	1546	451	1977	192	CFG_VIN2A_D7_IN	vin2a_d7	-	-	-	-
C5	vin2a_d8	1522	650	1966	391	CFG_VIN2A_D8_IN	vin2a_d8	-	-	-	-
A7	vin2a_d9	1546	578	1996	270	CFG_VIN2A_D9_IN	vin2a_d9	-	-	-	-
B4	vin2a_de0	1548	623	2036	213	CFG_VIN2A_DE0_IN	vin2a_de0	vin2a_fld0	vin2b_fld1	vin2b_de1	-
E6	vin2a_fld0	1771	815	2162	566	CFG_VIN2A_FLD0_IN	vin2a_fld0	-	vin2b_clk1	-	-
D5	vin2a_hsync0	1703	587	2071	225	CFG_VIN2A_HSYNC0_IN	vin2a_hsync0	-	-	vin2b_hsync1	-
C4	vin2a_vsync0	1486	464	1895	53	CFG_VIN2A_VSYNC0_IN	vin2a_vsync0	-	-	vin2b_vsync1	-

Manual IO Timings Modes must be used to guarantee some IO timings for VIP1. See [Table 7-2 Modes Summary](#) for a list of IO timings requiring the use of Manual IO Timings Modes. See [Table 7-8 Manual Functions Mapping for VIP1 2B](#) for a definition of the Manual modes.

[Table 7-8](#) lists the A_DELAY and G_DELAY values needed to calculate the correct values to be set in the CFG_x registers.

Table 7-8. Manual Functions Mapping for VIP1 2B

BALL	BALL NAME	VIP1_2B_MANUAL1		VIP1_2B_MANUAL2		CFG REGISTER	MUXMODE		
		A_DELAY (ps)	G_DELAY (ps)	A_DELAY (ps)	G_DELAY (ps)		2	3	4
Y1	gpio6_10	1830	911	2136	593	CFG_GPIO6_10_IN	-	-	vin2b_hsync1
W1	gpio6_11	1797	1159	2088	926	CFG_GPIO6_11_IN	-	-	vin2b_vsync1
W5	mmc3_clk	(1)	(1)	(1)	(1)	CFG_MMC3_CLK_IN	-	-	vin2b_d7
W4	mmc3_cmd	1769	980	2092	650	CFG_MMC3_CMD_IN	-	-	vin2b_d6
U6	mmc3_dat0	1678	984	2027	691	CFG_MMC3_DAT0_IN	-	-	vin2b_d5
V6	mmc3_dat1	1664	883	2031	491	CFG_MMC3_DAT1_IN	-	-	vin2b_d4
U5	mmc3_dat2	1672	439	2065	0	CFG_MMC3_DAT2_IN	-	-	vin2b_d3
V3	mmc3_dat3	1762	1078	2089	799	CFG_MMC3_DAT3_IN	-	-	vin2b_d2
V5	mmc3_dat4	1766	583	2125	135	CFG_MMC3_DAT4_IN	-	-	vin2b_d1

Table 7-8. Manual Functions Mapping for VIP1 2B (continued)

BALL	BALL NAME	VIP1_2B_MANUAL1		VIP1_2B_MANUAL2		CFG REGISTER	MUXMODE		
		A_DELAY (ps)	G_DELAY (ps)	A_DELAY (ps)	G_DELAY (ps)		2	3	4
W6	mmc3_dat5	1777	577	2072	362	CFG_MMC3_DAT5_IN	-	-	vin2b_d0
W3	mmc3_dat6	1675	808	2035	431	CFG_MMC3_DAT6_IN	-	-	vin2b_de1
V4	mmc3_dat7	0	0	0	0	CFG_MMC3_DAT7_IN	-	-	vin2b_clk1
B7	vin2a_d16	1181	0	1424	0	CFG_VIN2A_D16_IN	vin2b_d7	-	-
B8	vin2a_d17	1317	0	1545	0	CFG_VIN2A_D17_IN	vin2b_d6	-	-
A8	vin2a_d18	1132	0	1240	0	CFG_VIN2A_D18_IN	vin2b_d5	-	-
D7	vin2a_d19	749	0	919	0	CFG_VIN2A_D19_IN	vin2b_d4	-	-
C8	vin2a_d20	1078	0	1320	0	CFG_VIN2A_D20_IN	vin2b_d3	-	-
D8	vin2a_d21	1119	0	1357	0	CFG_VIN2A_D21_IN	vin2b_d2	-	-
F8	vin2a_d22	1089	0	1306	0	CFG_VIN2A_D22_IN	vin2b_d1	-	-
E9	vin2a_d23	1118	0	1362	0	CFG_VIN2A_D23_IN	vin2b_d0	-	-
B4	vin2a_de0	1371	420	1813	86	CFG_VIN2A_DE0_IN	vin2b_fld1	vin2b_de1	-
E6	vin2a_fld0	0	0	0	0	CFG_VIN2A_FLD0_IN	vin2b_clk1	-	-
D5	vin2a_hsync0	1605	0	1674	0	CFG_VIN2A_HSYNC0_IN	-	vin2b_hsync1	-
C4	vin2a_vsync0	1231	0	1300	0	CFG_VIN2A_VSYNC0_IN	-	vin2b_vsync1	-

(1) The CFG_MMC3_CLK_IN register should remain at its Default value, which is programmed automatically by hardware during the recalibration process.

Manual IO Timings Modes must be used to guarantee some IO timings for VIP2. See [Table 7-2 Modes Summary](#) for a list of IO timings requiring the use of Manual IO Timings Modes. See [Table 7-9 Manual Functions Mapping for VIP2](#) for a definition of the Manual modes.

[Table 7-9](#) lists the A_DELAY and G_DELAY values needed to calculate the correct values to be set in the CFG_x registers.

Table 7-9. Manual Functions Mapping for VIP2

BALL	BALL NAME	VIP2_MANUAL 1		VIP2_MANUAL2		CFG REGISTER	MUXMODE			
		A_DELAY (ps)	G_DELAY (ps)	A_DELAY (ps)	G_DELAY (ps)		2	4	5	6
N3	gpmc_a0	2216	947	2519	702	CFG_GPMC_A0_IN	vin3a_d16	-	-	-
P3	gpmc_a1	2078	1022	2384	778	CFG_GPMC_A1_IN	vin3a_d17	-	-	-
M6	gpmc_a10	2108	823	2435	411	CFG_GPMC_A10_IN	vin3a_de0	-	-	-
N5	gpmc_a11	2068	977	2379	755	CFG_GPMC_A11_IN	vin3a_fld0	-	-	-
C2	gpmc_a19	1740	123	1743	0	CFG_GPMC_A19_IN	-	-	-	vin3b_d0
P1	gpmc_a2	2280	1298	2499	1127	CFG_GPMC_A2_IN	vin3a_d18	-	-	-
D3	gpmc_a20	1628	30	1529	0	CFG_GPMC_A20_IN	-	-	-	vin3b_d1
D2	gpmc_a21	1687	217	1779	0	CFG_GPMC_A21_IN	-	-	-	vin3b_d2

Table 7-9. Manual Functions Mapping for VIP2 (continued)

BALL	BALL NAME	VIP2_MANUAL 1		VIP2_MANUAL2		CFG REGISTER	MUXMODE			
		A_DELAY (ps)	G_DELAY (ps)	A_DELAY (ps)	G_DELAY (ps)		2	4	5	6
D1	gpmc_a22	1595	151	1620	0	CFG_GPMC_A22_IN	-	-	-	vin3b_d3
E1	gpmc_a23	1366	0	1363	0	CFG_GPMC_A23_IN	-	-	-	vin3b_d4
E2	gpmc_a24	1554	343	1765	0	CFG_GPMC_A24_IN	-	-	-	vin3b_d5
E3	gpmc_a25	1652	268	1808	0	CFG_GPMC_A25_IN	-	-	-	vin3b_d6
E4	gpmc_a26	1546	281	1669	0	CFG_GPMC_A26_IN	-	-	-	vin3b_d7
F3	gpmc_a27	1534	198	1611	0	CFG_GPMC_A27_IN	-	-	-	vin3b_hsync1
P2	gpmc_a3	2246	1318	2455	1181	CFG_GPMC_A3_IN	vin3a_d19	-	-	-
N2	gpmc_a4	2266	1216	2486	1039	CFG_GPMC_A4_IN	vin3a_d20	-	-	-
N1	gpmc_a5	2185	1122	2456	938	CFG_GPMC_A5_IN	vin3a_d21	-	-	-
M5	gpmc_a6	2206	782	2463	573	CFG_GPMC_A6_IN	vin3a_d22	-	-	-
M4	gpmc_a7	2369	1025	2608	783	CFG_GPMC_A7_IN	vin3a_d23	-	-	-
M1	gpmc_a8	2154	978	2430	656	CFG_GPMC_A8_IN	vin3a_hsync0	-	-	-
M3	gpmc_a9	2185	1152	2465	850	CFG_GPMC_A9_IN	vin3a_vsync0	-	-	-
J4	gpmc_ad0	1908	620	2316	301	CFG_GPMC_AD0_IN	vin3a_d0	-	-	-
H6	gpmc_ad1	2117	382	2440	70	CFG_GPMC_AD1_IN	vin3a_d1	-	-	-
G4	gpmc_ad10	1968	686	2324	406	CFG_GPMC_AD10_IN	vin3a_d10	-	-	-
G5	gpmc_ad11	1853	689	2278	352	CFG_GPMC_AD11_IN	vin3a_d11	-	-	-
G6	gpmc_ad12	1910	497	2297	160	CFG_GPMC_AD12_IN	vin3a_d12	-	-	-
F5	gpmc_ad13	1869	436	2278	108	CFG_GPMC_AD13_IN	vin3a_d13	-	-	-
E5	gpmc_ad14	1895	147	2035	0	CFG_GPMC_AD14_IN	vin3a_d14	-	-	-
F4	gpmc_ad15	1917	655	2279	378	CFG_GPMC_AD15_IN	vin3a_d15	-	-	-
G1	gpmc_ad2	2097	666	2404	446	CFG_GPMC_AD2_IN	vin3a_d2	-	-	-
H2	gpmc_ad3	1954	581	2343	212	CFG_GPMC_AD3_IN	vin3a_d3	-	-	-
H3	gpmc_ad4	2034	610	2355	322	CFG_GPMC_AD4_IN	vin3a_d4	-	-	-
H4	gpmc_ad5	1965	484	2337	192	CFG_GPMC_AD5_IN	vin3a_d5	-	-	-
H5	gpmc_ad6	1861	635	2270	314	CFG_GPMC_AD6_IN	vin3a_d6	-	-	-
F1	gpmc_ad7	2004	507	2339	259	CFG_GPMC_AD7_IN	vin3a_d7	-	-	-
G2	gpmc_ad8	1945	853	2308	577	CFG_GPMC_AD8_IN	vin3a_d8	-	-	-
G3	gpmc_ad9	1914	539	2334	166	CFG_GPMC_AD9_IN	vin3a_d9	-	-	-
M2	gpmc_ben0	1806	0	1722	0	CFG_GPMC_BEN0_IN	-	-	-	vin3b_de1
J3	gpmc_ben1	1879	20	1840	0	CFG_GPMC_BEN1_IN	-	vin3b_clk1	-	vin3b_fld1
N6	gpmc_clk	0	0	0	0	CFG_GPMC_CLK_IN	-	-	-	vin3b_clk1

Table 7-9. Manual Functions Mapping for VIP2 (continued)

BALL	BALL NAME	VIP2_MANUAL 1		VIP2_MANUAL2		CFG REGISTER	MUXMODE			
		A_DELAY (ps)	G_DELAY (ps)	A_DELAY (ps)	G_DELAY (ps)		2	4	5	6
C1	gpmc_cs1	1505	41	1388	0	CFG_GPMC_CS1_IN	-	-	-	vin3b_vsync1
K2	gpmc_cs3	0	0	0	0	CFG_GPMC_CS3_IN	vin3a_clk0	-	-	-
AA2	vin1a_d16	1803	1679	2244	1202	CFG_VIN1A_D16_IN	-	-	-	vin3a_d0
AC2	vin1a_d17	1871	1654	2321	1116	CFG_VIN1A_D17_IN	-	-	-	vin3a_d1
Y3	vin1a_d18	1875	1742	2280	1288	CFG_VIN1A_D18_IN	-	-	-	vin3a_d2
AB2	vin1a_d19	1844	1759	2282	1281	CFG_VIN1A_D19_IN	-	-	-	vin3a_d3
AB1	vin1a_d20	1845	1624	2284	1090	CFG_VIN1A_D20_IN	-	-	-	vin3a_d4
AC1	vin1a_d21	1906	1520	2324	1000	CFG_VIN1A_D21_IN	-	-	-	vin3a_d5
AA1	vin1a_d22	1807	1437	2278	915	CFG_VIN1A_D22_IN	-	-	-	vin3a_d6
Y2	vin1a_d23	1996	997	2423	398	CFG_VIN1A_D23_IN	-	-	-	vin3a_d7
AA6	vin1b_clk1	0	0	0	0	CFG_VIN1B_CLK1_IN	-	-	-	vin3a_clk0
B7	vin2a_d16	1329	528	1779	0	CFG_VIN2A_D16_IN	-	-	-	vin3a_d8
B8	vin2a_d17	1270	677	1844	0	CFG_VIN2A_D17_IN	-	-	-	vin3a_d9
A8	vin2a_d18	1494	411	1767	0	CFG_VIN2A_D18_IN	-	-	-	vin3a_d10
D7	vin2a_d19	1225	154	1254	0	CFG_VIN2A_D19_IN	-	-	-	vin3a_d11
C8	vin2a_d20	1212	450	1597	0	CFG_VIN2A_D20_IN	-	-	vin3a_de0	vin3a_d12
D8	vin2a_d21	1232	494	1662	0	CFG_VIN2A_D21_IN	-	-	vin3a_fld0	vin3a_d13
F8	vin2a_d22	1203	503	1641	0	CFG_VIN2A_D22_IN	-	-	vin3a_hsync0	vin3a_d14
E9	vin2a_d23	1214	599	1748	0	CFG_VIN2A_D23_IN	-	-	vin3a_vsync0	vin3a_d15
D10	vout1_clk	2047	735	2391	637	CFG_VOUT1_CLK_IN	-	vin3a_fld0	-	-
B9	vout1_d0	2135	987	2403	965	CFG_VOUT1_D0_IN	-	vin3a_d16	-	-
A9	vout1_d1	2048	955	2368	880	CFG_VOUT1_D1_IN	-	vin3a_d17	-	-
B12	vout1_d10	1970	855	2347	724	CFG_VOUT1_D10_IN	-	vin3a_d10	-	-
B10	vout1_d11	2111	893	2389	861	CFG_VOUT1_D11_IN	-	vin3a_d11	-	-
C14	vout1_d12	2018	841	2356	748	CFG_VOUT1_D12_IN	-	vin3a_d12	-	-
C10	vout1_d13	2073	805	2382	731	CFG_VOUT1_D13_IN	-	vin3a_d13	-	-
A10	vout1_d14	2112	770	2401	703	CFG_VOUT1_D14_IN	-	vin3a_d14	-	-
C13	vout1_d15	2132	831	2434	771	CFG_VOUT1_D15_IN	-	vin3a_d15	-	-
C11	vout1_d16	1996	632	2338	536	CFG_VOUT1_D16_IN	-	vin3a_d0	-	-
E10	vout1_d17	2190	790	2442	775	CFG_VOUT1_D17_IN	-	vin3a_d1	-	-
D15	vout1_d18	2100	604	2385	565	CFG_VOUT1_D18_IN	-	vin3a_d2	-	-
E15	vout1_d19	2108	286	2424	168	CFG_VOUT1_D19_IN	-	vin3a_d3	-	-

Table 7-9. Manual Functions Mapping for VIP2 (continued)

BALL	BALL NAME	VIP2_MANUAL1		VIP2_MANUAL2		CFG REGISTER	MUXMODE			
		A_DELAY (ps)	G_DELAY (ps)	A_DELAY (ps)	G_DELAY (ps)		2	4	5	6
A11	vout1_d2	1979	1020	2335	909	CFG_VOUT1_D2_IN	-	vin3a_d18	-	-
D9	vout1_d20	2031	967	2362	881	CFG_VOUT1_D20_IN	-	vin3a_d4	-	-
E14	vout1_d21	2039	450	2350	384	CFG_VOUT1_D21_IN	-	vin3a_d5	-	-
D14	vout1_d22	2037	583	2369	497	CFG_VOUT1_D22_IN	-	vin3a_d6	-	-
D11	vout1_d23	1768	740	2246	508	CFG_VOUT1_D23_IN	-	vin3a_d7	-	-
C9	vout1_d3	2099	881	2382	844	CFG_VOUT1_D3_IN	-	vin3a_d19	-	-
A13	vout1_d4	2120	786	2387	756	CFG_VOUT1_D4_IN	-	vin3a_d20	-	-
A12	vout1_d5	1965	857	2299	769	CFG_VOUT1_D5_IN	-	vin3a_d21	-	-
B14	vout1_d6	2139	680	2366	699	CFG_VOUT1_D6_IN	-	vin3a_d22	-	-
B13	vout1_d7	2122	912	2360	920	CFG_VOUT1_D7_IN	-	vin3a_d23	-	-
A14	vout1_d8	2073	906	2372	853	CFG_VOUT1_D8_IN	-	vin3a_d8	-	-
B11	vout1_d9	2097	934	2386	879	CFG_VOUT1_D9_IN	-	vin3a_d9	-	-
D13	vout1_de	2021	527	2366	428	CFG_VOUT1_DE_IN	-	vin3a_de0	-	-
E11	vout1_fld	0	0	0	0	CFG_VOUT1_FLD_IN	-	vin3a_clk0	-	-
E12	vout1_hsync	1775	486	2272	164	CFG_VOUT1_HSYNC_IN	-	vin3a_hsync0	-	-
E13	vout1_vsync	1917	314	2301	0	CFG_VOUT1_VSYNC_IN	-	vin3a_vsync0	-	-

Manual IO Timings Modes must be used to guarantee some IO timings for VIP2. See [Table 7-2 Modes Summary](#) for a list of IO timings requiring the use of Manual IO Timings Modes. See [Table 7-10 Manual Functions Mapping for VIP2 4B](#) for a definition of the Manual modes.

[Table 7-10](#) lists the A_DELAY and G_DELAY values needed to calculate the correct values to be set in the CFG_x registers.

Table 7-10. Manual Functions Mapping for VIP2 4B

BALL	BALL NAME	VIP2_4B_MANUAL1		VIP2_4B_MANUAL2		CFG REGISTER	MUXMODE	
		A_DELAY (ps)	G_DELAY (ps)	A_DELAY (ps)	G_DELAY (ps)		5	6
N3	gpmc_a0	1861	901	2102	660	CFG_GPMC_A0_IN	-	vin4b_d0
P3	gpmc_a1	1652	891	1955	583	CFG_GPMC_A1_IN	-	vin4b_d1
M6	gpmc_a10	0	0	0	0	CFG_GPMC_A10_IN	-	vin4b_clk1
N5	gpmc_a11	1783	1178	1975	1021	CFG_GPMC_A11_IN	-	vin4b_de1
L5	gpmc_a12	1903	853	2076	664	CFG_GPMC_A12_IN	-	vin4b_fld1
P1	gpmc_a2	1888	1212	2065	994	CFG_GPMC_A2_IN	-	vin4b_d2
P2	gpmc_a3	1839	1274	2025	1075	CFG_GPMC_A3_IN	-	vin4b_d3
N2	gpmc_a4	1868	1113	2058	869	CFG_GPMC_A4_IN	-	vin4b_d4

Table 7-10. Manual Functions Mapping for VIP2 4B (continued)

BALL	BALL NAME	VIP2_4B_MANUAL1		VIP2_4B_MANUAL2		CFG REGISTER	MUXMODE	
		A_DELAY (ps)	G_DELAY (ps)	A_DELAY (ps)	G_DELAY (ps)		5	6
N1	gpmc_a5	1757	1079	2028	802	CFG_GPMC_A5_IN	-	vin4b_d5
M5	gpmc_a6	1800	670	2032	421	CFG_GPMC_A6_IN	-	vin4b_d6
M4	gpmc_a7	1967	898	2179	597	CFG_GPMC_A7_IN	-	vin4b_d7
M1	gpmc_a8	1731	959	1993	559	CFG_GPMC_A8_IN	-	vin4b_hsync1
M3	gpmc_a9	1766	1150	2022	834	CFG_GPMC_A9_IN	-	vin4b_vsync1
T1	mdio_d	1602	506	1931	283	CFG_MDIO_D_IN	vin4b_d0	-
R3	mdio_mclk	0	0	0	0	CFG_MDIO_MCLK_IN	vin4b_clk1	-
U2	rgmii0_rxc	1678	887	1987	663	CFG_RGMII0_RXC_IN	vin4b_d5	-
U3	rgmii0_rxctl	1595	932	1903	748	CFG_RGMII0_RXCTL_IN	vin4b_d6	-
R4	rgmii0_rxd0	1707	464	2010	160	CFG_RGMII0_RXD0_IN	vin4b fld1	-
P5	rgmii0_rxd3	1662	1146	1943	996	CFG_RGMII0_RXD3_IN	vin4b_d7	-
R6	rgmii0_txc	1639	1195	1970	1006	CFG_RGMII0_TXC_IN	vin4b_d3	-
P6	rgmii0_txctl	1695	1226	1952	1113	CFG_RGMII0_TXCTL_IN	vin4b_d4	-
T4	rgmii0_txd1	1693	1118	1951	1003	CFG_RGMII0_TXD1_IN	vin4b_vsync1	-
T6	rgmii0_txd2	1522	1004	1895	685	CFG_RGMII0_TXD2_IN	vin4b_hsync1	-
T5	rgmii0_txd3	1777	957	2018	787	CFG_RGMII0_TXD3_IN	vin4b_de1	-
R1	uart3_rxd	1537	236	1762	0	CFG_UART3_RXD_IN	vin4b_d1	-
T2	uart3_txd	1575	645	1933	276	CFG_UART3_TXD_IN	vin4b_d2	-

Manual IO Timings Modes must be used to guarantee some IO timings for VIP2. See [Table 7-2 Modes Summary](#) for a list of IO timings requiring the use of Manual IO Timings Modes. See [Table 7-11 Manual Functions Mapping for VIP2 3B IOSET2](#) for a definition of the Manual modes.

[Table 7-11](#) lists the A_DELAY and G_DELAY values needed to calculate the correct values to be set in the CFG_x registers.

Table 7-11. Manual Functions Mapping for VIP2 3B IOSET2

BALL	BALL NAME	VIP2_3B_IOSET2_MANUAL1		VIP2_3B_IOSET2_MANUAL2		CFG REGISTER	MUXMODE	
		A_DELAY (ps)	G_DELAY (ps)	A_DELAY (ps)	G_DELAY (ps)		4	6
C2	gpmc_a19	1505	1172	1854	799	CFG_GPMC_A19_IN	-	vin3b_d0
D3	gpmc_a20	1394	1074	1723	716	CFG_GPMC_A20_IN	-	vin3b_d1
D2	gpmc_a21	1452	1266	1789	900	CFG_GPMC_A21_IN	-	vin3b_d2
D1	gpmc_a22	1360	1200	1684	847	CFG_GPMC_A22_IN	-	vin3b_d3
E1	gpmc_a23	1446	735	1831	443	CFG_GPMC_A23_IN	-	vin3b_d4
E2	gpmc_a24	1329	1360	1686	970	CFG_GPMC_A24_IN	-	vin3b_d5

Table 7-11. Manual Functions Mapping for VIP2 3B IOSET2 (continued)

BALL	BALL NAME	VIP2_3B_IOSET2_MANUAL1		VIP2_3B_IOSET2_MANUAL2		CFG REGISTER	MUXMODE	
		A_DELAY (ps)	G_DELAY (ps)	A_DELAY (ps)	G_DELAY (ps)		4	6
E3	gpmc_a25	1417	1318	1757	962	CFG_GPMC_A25_IN	-	vin3b_d6
E4	gpmc_a26	1321	1298	1680	880	CFG_GPMC_A26_IN	-	vin3b_d7
F3	gpmc_a27	1309	1215	1669	834	CFG_GPMC_A27_IN	-	vin3b_hsync1
M2	gpmc_ben0	1677	944	1994	638	CFG_GPMC_BEN0_IN	-	vin3b_de1
J3	gpmc_ben1	0	0	0	0	CFG_GPMC_BEN1_IN	vin3b_clk1	vin3b_fld1
C1	gpmc_cs1	1280	1058	1620	664	CFG_GPMC_CS1_IN	-	vin3b_vsync1

7.7 Display Subsystem – Video Output Ports

Three Display Parallel Interfaces (DPI) channels are available in DSS named DPI Video Output 1, DPI Video Output 2 and DPI Video Output 3.

NOTE

The DPI Video Output i ($i = 1$ to 3) interface is also referred to as VOUT i .

Every VOUT interface consists of:

- 24-bit data bus (data[23:0])
- Horizontal synchronization signal (HSYNC)
- Vertical synchronization signal (VSYNC)
- Data enable (DE)
- Field ID (FID)
- Pixel clock (CLK)

NOTE

For more information, see the Display Subsystem chapter of the Device TRM.

CAUTION

The IO Timings provided in this section are only valid if signals within a single IOSET are used. The IOSETs are defined in the [Table 7-16](#) and [Table 7-17](#).

CAUTION

The IO Timings provided in this section are only valid for some DSS usage modes when the corresponding Virtual IO Timings or Manual IO Timings are configured as described in the tables found in this section.

CAUTION

All pads/balls configured as vout i _* signals are recommended to use slow slew rate by setting the corresponding CTRL_CORE_PAD_*[SLEWCONTROL] register field to SLOW (0b1). FAST slew setting is allowed, but results in faster edge rates on the VOUT n bus, higher power/ground noise, and higher EMI emissions compared to SLOW slew rate.

[Table 7-12](#), [Table 7-13](#) and [Figure 7-6](#) assume testing over the recommended operating conditions and electrical characteristic conditions

Table 7-12. DPI Video Output i ($i = 1..3$) Default Switching Characteristics

NO.	PARAMETER	DESCRIPTION	MODE	MIN	MAX	UNIT
D1	$t_{c(\text{clk})}$	Cycle time, output pixel clock vout i _clk		11.76 (2)		ns

Table 7-12. DPI Video Output i (i = 1..3) Default Switching Characteristics (continued)

NO.	PARAMETER	DESCRIPTION	MODE	MIN	MAX	UNIT
D2	$t_{w(\text{clkL})}$	Pulse duration, output pixel clock vouti_clk low	DPI1, DPI2 (IOSET1), DPI3	$P \cdot 0.5 - 1$ ⁽¹⁾		ns
			DPI2 (IOSET2)	$P \cdot 0.5 - 1.35$ ⁽¹⁾		ns
D3	$t_{w(\text{clkH})}$	Pulse duration, output pixel clock vouti_clk high	DPI1, DPI2 (IOSET1), DPI3	$P \cdot 0.5 - 1$ ⁽¹⁾		ns
			DPI2 (IOSET2)	$P \cdot 0.5 - 1.35$ ⁽¹⁾		ns
D5	$t_{d(\text{clk-dV})}$	Delay time, output pixel clock vouti_clk transition to output data vouti_d[23:0] valid	DPI1	-2.5	2.5	ns
			DPI2 (IOSET1)	-2.5	2.5	ns
			DPI2 (IOSET2)	-2.5	2.5	ns
			DPI3 (IOSET1)	-2.5	2.5	ns
			DPI3 (IOSET2/3)	-2.5	2.5	ns
D6	$t_{d(\text{clk-ctlV})}$	Delay time, output pixel clock vouti_clk transition to output control signals vouti_vsync, vouti_hsync, vouti_de, and vouti_fld valid	DPI1	-2.5	2.5	ns
			DPI2 (IOSET1)	-2.5	2.5	ns
			DPI2 (IOSET2)	-2.5	2.5	ns
			DPI3 (IOSET1)	-2.5	2.5	ns
			DPI3 (IOSET2/3)	-2.5	2.5	ns

(1) P = output vouti_clk period in ns.

(2) All pads/balls configured as vouti_* signals are recommended to use slow slew rate by setting the corresponding CTRL_CORE_PAD_*[SLEWCONTROL] register field to SLOW (0b1). FAST slew setting is allowed, but results in faster edge rates on the VOUTn bus, higher power/ground noise, and higher EMI emissions compared to SLOW slew rate.

(3) SERDES transceivers may be sensitive to the jitter profile of vouti_clk. See Application Note [SPRAC62](#) for additional guidance.

Table 7-13. DPI Video Output i (i = 1..3) Alternate Switching Characteristics

NO.	PARAMETER	DESCRIPTION	MODE	MIN	MAX	UNIT
D1	$t_c(\text{clk})$	Cycle time, output pixel clock vouti_clk		6.06 ⁽²⁾		ns
D2	$t_{w(\text{clkL})}$	Pulse duration, output pixel clock vouti_clk low		$P \cdot 0.5 - 1$ ⁽¹⁾		ns
D3	$t_{w(\text{clkH})}$	Pulse duration, output pixel clock vouti_clk high		$P \cdot 0.5 - 1$ ⁽¹⁾		ns
D5	$t_{d(\text{clk-ctlV})}$	Delay time, output pixel clock vouti_clk transition to output data vouti_d[23:0] valid	DPI1	1.51	4.55	ns
			DPI2 (IOSET1)	1.51	4.55	ns
			DPI2 (IOSET2)	1.51	4.55	ns
			DPI3	1.51	4.55	ns
D6	$t_{d(\text{clk-dV})}$	Delay time, output pixel clock vouti_clk transition to output control signals vouti_vsync, vouti_hsync, vouti_de, and vouti_fld valid	DPI1	1.51	4.55	ns
			DPI2 (IOSET1)	1.51	4.55	ns
			DPI2 (IOSET2)	1.51	4.55	ns
			DPI3	1.51	4.55	ns

(1) P = output vouti_clk period in ns.

(2) All pads/balls configured as vouti_* signals are recommended to use slow slew rate by setting the corresponding CTRL_CORE_PAD_*[SLEWCONTROL] register field to SLOW (0b1). FAST slew setting is allowed, but results in faster edge rates on the VOUTn bus, higher power/ground noise, and higher EMI emissions compared to SLOW slew rate.

(3) SERDES transceivers may be sensitive to the jitter profile of vouti_clk. See Application Note [SPRAC62](#) for additional guidance.

Table 7-14. DPI Video Output i (i = 1..3) MANUAL3 Switching Characteristics

NO.	PARAMETER	DESCRIPTION	MODE	MIN	MAX	UNIT
D1	$t_c(\text{clk})$	Cycle time, output pixel clock vouti_clk		6.06 ⁽²⁾		ns
D2	$t_{w(\text{clkL})}$	Pulse duration, output pixel clock vouti_clk low		$P \cdot 0.5 - 1$ ⁽¹⁾		ns

Table 7-14. DPI Video Output i (i = 1..3) MANUAL3 Switching Characteristics (continued)

NO.	PARAMETER	DESCRIPTION	MODE	MIN	MAX	UNIT
D3	$t_{w(\text{clkH})}$	Pulse duration, output pixel clock vouti_clk high		$P*0.5-1$ ⁽¹⁾		ns
D5	$t_{d(\text{clk-ctIV})}$	Delay time, output pixel clock vouti_clk transition to output data vouti_d[23:0] valid	DPI1	2.85	5.56	ns
			DPI2, DPI3	2.78	5.91	ns
D6	$t_{d(\text{clk-dV})}$	Delay time, output pixel clock vouti_clk transition to output control signals vouti_vsync, vouti_hsync, vouti_de, and vouti_fld valid	DPI1	2.85	5.56	ns
			DPI2, DPI3	2.78	5.91	ns

(1) P = output vouti_clk period in ns.

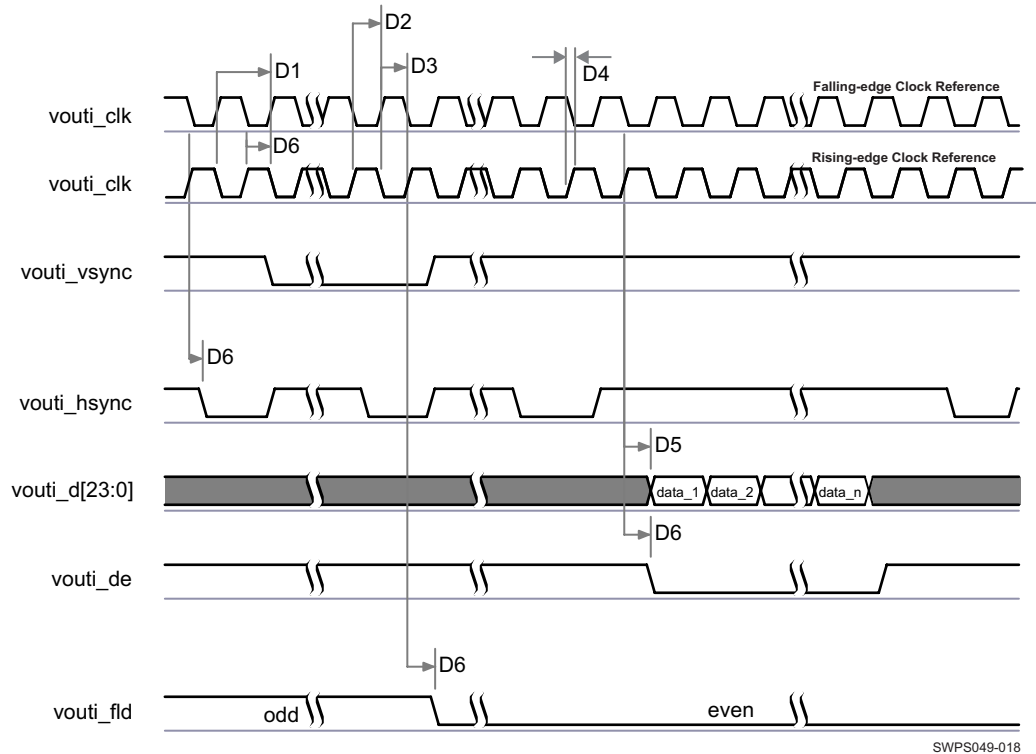
(2) SERDES transceivers may be sensitive to the jitter profile of vouti_clk. See Application Note [SPRAC62](#) for additional guidance.

Table 7-15. DPI Video Output i (i = 1..3) MANUAL4 Switching Characteristics

NO.	PARAMETER	DESCRIPTION	MODE	MIN	MAX	UNIT
D1	$t_{c(\text{clk})}$	Cycle time, output pixel clock vouti_clk		6.06 ⁽²⁾		ns
D2	$t_{w(\text{clkL})}$	Pulse duration, output pixel clock vouti_clk low		$P*0.5-1$ ⁽¹⁾		ns
D3	$t_{w(\text{clkH})}$	Pulse duration, output pixel clock vouti_clk high		$P*0.5-1$ ⁽¹⁾		ns
D5	$t_{d(\text{clk-ctIV})}$	Delay time, output pixel clock vouti_clk transition to output data vouti_d[23:0] valid	DPI1, DPI2, DPI3	3.55	6.61	ns
D6	$t_{d(\text{clk-dV})}$	Delay time, output pixel clock vouti_clk transition to output control signals vouti_vsync, vouti_hsync, vouti_de, and vouti_fld valid	DPI1, DPI2, DPI3	3.55	6.61	ns

(1) P = output vouti_clk period in ns.

(2) SERDES transceivers may be sensitive to the jitter profile of vouti_clk. See Application Note [SPRAC62](#) for additional guidance.



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Figure 7-6. DPI Video Output⁽¹⁾⁽²⁾⁽³⁾

(1) The configuration of assertion of the data can be programmed on the falling or rising edge of the pixel clock.

(2) The polarity and the pulse width of vouti_hsync and vouti_vsync are programmable, refer to the DSS section of the device TRM.

(3) The vouti_clk frequency can be configured, refer to the DSS section of the device TRM.

NOTE

To configure the desired virtual mode the user must set MODESELECT bit and DELAYMODE bitfield for each corresponding pad control register.

The pad control registers are presented in [Table 4-3](#) and described in Device TRM, *Chapter 18 - Control Module*.

In [Table 7-16](#) are presented the specific groupings of signals (IOSET) for use with VOUT2.

Table 7-16. VOUT2 IOSETs

SIGNALS	IOSET1	
	BALL	MUX
vout2_d23	C3	4
vout2_d22	B2	4
vout2_d21	E7	4
vout2_d20	B3	4
vout2_d19	A3	4
vout2_d18	C6	4
vout2_d17	A4	4
vout2_d16	B5	4
vout2_d15	C5	4
vout2_d14	A7	4
vout2_d13	A5	4
vout2_d12	B6	4
vout2_d11	E8	4
vout2_d10	A6	4
vout2_d9	C7	4
vout2_d8	D6	4
vout2_d7	B7	4
vout2_d6	B8	4
vout2_d5	A8	4
vout2_d4	D7	4
vout2_d3	C8	4
vout2_d2	D8	4
vout2_d1	F8	4
vout2_d0	E9	4
vout2_vsync	C4	4
vout2_hsync	D5	4
vout2_clk	E6	4
vout2_fld	D4	4
vout2_de	B4	4

In [Table 7-17](#) are presented the specific groupings of signals (IOSET) for use with VOUT3.

Table 7-17. VOUT3 IOSETs

SIGNALS	IOSET1		IOSET2 ⁽¹⁾		IOSET3 ⁽¹⁾	
	BALL	MUX	BALL	MUX	BALL	MUX
vout3_d23	M4	3	AD5	4		
vout3_d22	M5	3	AE5	4		

Table 7-17. VOUT3 IOSETs (continued)

SIGNALS	IOSET1		IOSET2 ⁽¹⁾		IOSET3 ⁽¹⁾	
	BALL	MUX	BALL	MUX	BALL	MUX
vout3_d21	N1	3	AA5	4		
vout3_d20	N2	3	Y5	4		
vout3_d19	P2	3	AB7	4		
vout3_d18	P1	3	AE4	4		
vout3_d17	P3	3	AB5	4	AA7	3
vout3_d16	N3	3	AD4	4	AB6	3
vout3_d15	F4	3	AA3	4	AA3	4
vout3_d14	E5	3	Y4	4	Y4	4
vout3_d13	F5	3	AE3	4	AE3	4
vout3_d12	G6	3	AA4	4	AA4	4
vout3_d11	G5	3	AD3	4	AD3	4
vout3_d10	G4	3	AC3	4	AC3	4
vout3_d9	G3	3	AD2	4	AD2	4
vout3_d8	G2	3	AB3	4	AB3	4
vout3_d7	F1	3	AA2	4	AD5	3
vout3_d6	H5	3	AC2	4	AE5	3
vout3_d5	H4	3	Y3	4	AA5	3
vout3_d4	H3	3	AB2	4	Y5	3
vout3_d3	H2	3	AB1	4	AB7	3
vout3_d2	G1	3	AC1	4	AE4	3
vout3_d1	H6	3	AA1	4	AB5	3
vout3_d0	J4	3	Y2	4	AD4	3
vout3_de	M6	3	AA7	4		
vout3_vsync	M3	3	AC5	4	AC5	4
vout3_clk	K2	3	AD6	4	AD6	4
vout3_hsync	M1	3	AC6	4	AC6	4
vout3 fld	N5	3	AB6	4		

(1) The VOUT3 interface when multiplexed onto balls mapped to the VDDSHV6 supply rail is restricted to operating in 1.8V mode only (i.e., VDDSHV6 must be supplied with 1.8V). 3.3V mode is not supported. This must be considered in the pin mux programming and VDDSHVx supply connections.

NOTE

To configure the desired Manual IO Timing Mode the user must follow the steps described in section "Manual IO Timing Modes" of the Device TRM.

The associated registers to configure are listed in the CFG REGISTER column. For more information please see the *Control Module Chapter* in the Device TRM.

Manual IO Timings Modes must be used to guarantee some IO timings for VOUT1. See [Table 7-2 Modes Summary](#) for a list of IO timings requiring the use of Manual IO Timings Modes. See [Table 7-18 Manual Functions Mapping for DSS VOUT1](#) for a definition of the Manual modes.

[Table 7-18](#) lists the A_DELAY and G_DELAY values needed to calculate the correct values to be set in the CFG_x registers.

Table 7-18. Manual Functions Mapping for DSS VOUT1

BALL	BALL NAME	VOUT1_MANUAL1		VOUT1_MANUAL2		VOUT1_MANUAL3		VOUT1_MANUAL4		CFG REGISTER	MUXMODE
		A_DELAY (ps)	G_DELAY (ps)	A_DELAY (ps)	G_DELAY (ps)	A_DELAY (ps)	G_DELAY (ps)	A_DELAY (ps)	G_DELAY (ps)		0
D10	vout1_clk	0	706	1126	751	0	466	0	466	CFG_VOUT1_CLK_OUT	vout1_clk
B9	vout1_d0	2313	0	395	0	3436	0	4306	0	CFG_VOUT1_D0_OUT	vout1_d0
A9	vout1_d1	2439	0	521	0	3562	0	4432	0	CFG_VOUT1_D1_OUT	vout1_d1
B12	vout1_d10	2199	0	282	0	3323	0	3993	0	CFG_VOUT1_D10_OUT	vout1_d10
B10	vout1_d11	2266	0	348	0	3390	0	4060	0	CFG_VOUT1_D11_OUT	vout1_d11
C14	vout1_d12	3159	0	1240	0	4281	0	4951	0	CFG_VOUT1_D12_OUT	vout1_d12
C10	vout1_d13	2100	0	182	0	3223	0	4093	0	CFG_VOUT1_D13_OUT	vout1_d13
A10	vout1_d14	2229	0	311	0	3353	0	4223	0	CFG_VOUT1_D14_OUT	vout1_d14
C13	vout1_d15	2202	0	285	0	3326	0	4196	0	CFG_VOUT1_D15_OUT	vout1_d15
C11	vout1_d16	2084	0	166	0	3208	0	4078	0	CFG_VOUT1_D16_OUT	vout1_d16
E10	vout1_d17	2195	0	278	0	3319	0	4189	0	CFG_VOUT1_D17_OUT	vout1_d17
D15	vout1_d18	2342	0	425	0	3466	0	4136	0	CFG_VOUT1_D18_OUT	vout1_d18
E15	vout1_d19	2463	0	516	0	3557	0	4227	0	CFG_VOUT1_D19_OUT	vout1_d19
A11	vout1_d2	2200	0	282	0	3324	0	4194	0	CFG_VOUT1_D2_OUT	vout1_d2
D9	vout1_d20	2304	0	386	0	3428	0	4298	0	CFG_VOUT1_D20_OUT	vout1_d20
E14	vout1_d21	2103	0	111	0	3193	0	4063	0	CFG_VOUT1_D21_OUT	vout1_d21
D14	vout1_d22	2145	0	227	0	3268	0	4138	0	CFG_VOUT1_D22_OUT	vout1_d22
D11	vout1_d23	1932	0	0	0	3039	0	3909	0	CFG_VOUT1_D23_OUT	vout1_d23
C9	vout1_d3	2355	0	438	0	3479	0	4349	0	CFG_VOUT1_D3_OUT	vout1_d3
A13	vout1_d4	3215	0	1298	0	4339	0	5209	0	CFG_VOUT1_D4_OUT	vout1_d4
A12	vout1_d5	2314	0	397	0	3438	0	4308	0	CFG_VOUT1_D5_OUT	vout1_d5
B14	vout1_d6	2238	0	321	0	3362	0	4082	0	CFG_VOUT1_D6_OUT	vout1_d6
B13	vout1_d7	2381	0	155	309	3505	0	4175	0	CFG_VOUT1_D7_OUT	vout1_d7
A14	vout1_d8	2138	0	212	0	3253	0	4123	0	CFG_VOUT1_D8_OUT	vout1_d8
B11	vout1_d9	2383	0	466	0	3507	0	4377	0	CFG_VOUT1_D9_OUT	vout1_d9
D13	vout1_de	1984	0	0	0	3085	0	3955	0	CFG_VOUT1_DE_OUT	vout1_de
E11	vout1_fld	2265	0	236	0	3337	0	4207	0	CFG_VOUT1_FLD_OUT	vout1_fld
E12	vout1_hsync	1947	0	0	0	3052	0	3922	0	CFG_VOUT1_HSYNC_OUT	vout1_hsync
E13	vout1_vsync	2739	0	139	701	3863	0	4733	0	CFG_VOUT1_VSYNC_OUT	vout1_vsync

Manual IO Timings Modes must be used to guarantee some IO timings for VOUT2. See [Table 7-2 Modes Summary](#) for a list of IO timings requiring the use of Manual IO Timings Modes. See [Table 7-19 Manual Functions Mapping for DSS VOUT2](#) for a definition of the Manual modes.

[Table 7-19](#) lists the A_DELAY and G_DELAY values needed to calculate the correct values to be set in the CFG_x registers.

Table 7-19. Manual Functions Mapping for DSS VOUT2 IOSET1

BALL	BALL NAME	VOUT2_IOSET1_MANUAL 1		VOUT2_IOSET1_MANUAL 2		VOUT2_IOSET1_MANUAL 3		VOUT2_IOSET1_MANUAL 4		CFG REGISTER	MUXMODE 4
		A_DELAY (ps)	G_DELAY (ps)	A_DELAY (ps)	G_DELAY (ps)	A_DELAY (ps)	G_DELAY (ps)	A_DELAY (ps)	G_DELAY (ps)		
D4	vin2a_clk0	2718	0	819	0	3794	0	4664	0	CFG_VIN2A_CLK0_OUT	vout2_fld
C3	vin2a_d0	2680	0	485	296	3757	0	4627	0	CFG_VIN2A_D0_OUT	vout2_d23
B2	vin2a_d1	2633	0	733	0	3710	0	4580	0	CFG_VIN2A_D1_OUT	vout2_d22
A5	vin2a_d10	1867	0	0	0	2954	0	3824	0	CFG_VIN2A_D10_OUT	vout2_d13
B6	vin2a_d11	2457	0	431	127	3534	0	4404	0	CFG_VIN2A_D11_OUT	vout2_d12
E8	vin2a_d12	2683	1016	1286	514	3628	648	4498	648	CFG_VIN2A_D12_OUT	vout2_d11
A6	vin2a_d13	2629	985	1229	486	3569	622	4439	622	CFG_VIN2A_D13_OUT	vout2_d10
C7	vin2a_d14	2531	804	1126	309	3460	452	4530	452	CFG_VIN2A_D14_OUT	vout2_d9
D6	vin2a_d15	2624	818	1227	315	3567	452	4537	452	CFG_VIN2A_D15_OUT	vout2_d8
B7	vin2a_d16	2747	767	1357	256	3704	386	4574	386	CFG_VIN2A_D16_OUT	vout2_d7
B8	vin2a_d17	2622	841	1226	337	3616	474	4686	474	CFG_VIN2A_D17_OUT	vout2_d6
A8	vin2a_d18	2328	0	430	0	3406	0	4276	0	CFG_VIN2A_D18_OUT	vout2_d5
D7	vin2a_d19	2300	0	401	0	3427	0	4197	0	CFG_VIN2A_D19_OUT	vout2_d4
E7	vin2a_d2	2452	0	446	106	3528	0	4398	0	CFG_VIN2A_D2_OUT	vout2_d21
C8	vin2a_d20	1998	0	98	0	3075	0	3845	0	CFG_VIN2A_D20_OUT	vout2_d3
D8	vin2a_d21	1953	0	54	0	3030	0	3900	0	CFG_VIN2A_D21_OUT	vout2_d2
F8	vin2a_d22	1893	0	0	0	3030	0	3900	0	CFG_VIN2A_D22_OUT	vout2_d1
E9	vin2a_d23	1936	0	36	0	3013	0	3883	0	CFG_VIN2A_D23_OUT	vout2_d0
B3	vin2a_d3	2494	0	595	0	3571	0	4441	0	CFG_VIN2A_D3_OUT	vout2_d20
A3	vin2a_d4	3001	153	1254	0	4231	0	4901	0	CFG_VIN2A_D4_OUT	vout2_d19
C6	vin2a_d5	2463	0	563	0	3539	0	4409	0	CFG_VIN2A_D5_OUT	vout2_d18
A4	vin2a_d6	2456	0	558	0	3334	0	4404	0	CFG_VIN2A_D6_OUT	vout2_d17
B5	vin2a_d7	2431	0	532	0	3509	0	4379	0	CFG_VIN2A_D7_OUT	vout2_d16
C5	vin2a_d8	2262	0	363	0	3340	0	4210	0	CFG_VIN2A_D8_OUT	vout2_d15
A7	vin2a_d9	2145	0	246	0	3222	0	4092	0	CFG_VIN2A_D9_OUT	vout2_d14
B4	vin2a_de0	2597	0	550	149	3675	0	4545	0	CFG_VIN2A_DE0_OUT	vout2_de
E6	vin2a_fld0	0	957	1208	969	0	686	0	686	CFG_VIN2A_FLD0_OUT	vout2_clk

Table 7-19. Manual Functions Mapping for DSS VOUT2 IOSET1 (continued)

BALL	BALL NAME	VOUT2_IOSET1_MANUAL 1		VOUT2_IOSET1_MANUAL 2		VOUT2_IOSET1_MANUAL 3		VOUT2_IOSET1_MANUAL 4		CFG REGISTER	MUXMODE 4
		A_DELAY (ps)	G_DELAY (ps)	A_DELAY (ps)	G_DELAY (ps)	A_DELAY (ps)	G_DELAY (ps)	A_DELAY (ps)	G_DELAY (ps)		
D5	vin2a_hsync 0	2958	0	1059	0	4035	0	4905	0	CFG_VIN2A_HSYNC0_OUT	vout2_hsync
C4	vin2a_vsync 0	2752	0	853	0	3829	0	4699	0	CFG_VIN2A_VSYNC0_OUT	vout2_vsync

Manual IO Timings Modes must be used to guarantee some IO timings for VOUT3. See [Table 7-2 Modes Summary](#) for a list of IO timings requiring the use of Manual IO Timings Modes. See [Table 7-20 Manual Functions Mapping for DSS VOUT3](#) for a definition of the Manual modes.

[Table 7-20](#) lists the A_DELAY and G_DELAY values needed to calculate the correct values to be set in the CFG_x registers.

Table 7-20. Manual Functions Mapping for DSS VOUT3

BALL	BALL NAME	VOUT3_MANUAL1		VOUT3_MANUAL2		VOUT3_MANUAL3		VOUT3_MANUAL4		CFG REGISTER	MUXMODE	
		A_DELAY (ps)	G_DELAY (ps)	A_DELAY (ps)	G_DELAY (ps)	A_DELAY (ps)	G_DELAY (ps)	A_DELAY (ps)	G_DELAY (ps)		3	4
N3	gpmc_a0	3069	0	565	267	3365	0	4235	0	CFG_GPMC_A0_OUT	vout3_d16	-
P3	gpmc_a1	2888	0	650	0	3183	0	4053	0	CFG_GPMC_A1_OUT	vout3_d17	-
M6	gpmc_a10	3595	0	1157	0	3690	0	4560	0	CFG_GPMC_A10_OUT	vout3_de	-
N5	gpmc_a11	3891	14	669	970	4170	0	5040	0	CFG_GPMC_A11_OUT	vout3_fld	-
P1	gpmc_a2	2934	0	705	0	3238	0	4108	0	CFG_GPMC_A2_OUT	vout3_d18	-
P2	gpmc_a3	3944	4	1521	0	4054	0	4924	0	CFG_GPMC_A3_OUT	vout3_d19	-
N2	gpmc_a4	4456	261	1837	0	4370	0	5240	0	CFG_GPMC_A4_OUT	vout3_d20	-
N1	gpmc_a5	2915	0	739	0	3273	0	4143	0	CFG_GPMC_A5_OUT	vout3_d21	-
M5	gpmc_a6	3192	0	937	0	3471	0	4341	0	CFG_GPMC_A6_OUT	vout3_d22	-
M4	gpmc_a7	3182	0	944	0	3477	0	4347	0	CFG_GPMC_A7_OUT	vout3_d23	-
M1	gpmc_a8	4124	75	1843	0	4375	0	5245	0	CFG_GPMC_A8_OUT	vout3_hsync	-
M3	gpmc_a9	4252	0	998	0	3530	0	4400	0	CFG_GPMC_A9_OUT	vout3_vsync	-
J4	gpmc_ad0	3501	52	1151	0	3684	0	4534	0	CFG_GPMC_AD0_OUT	vout3_d0	-
H6	gpmc_ad1	3163	0	956	0	3489	0	4339	0	CFG_GPMC_AD1_OUT	vout3_d1	-
G4	gpmc_ad10	3130	0	1064	0	3598	0	4148	0	CFG_GPMC_AD10_OUT	vout3_d10	-
G5	gpmc_ad11	2821	0	809	0	3344	0	3894	0	CFG_GPMC_AD11_OUT	vout3_d11	-
G6	gpmc_ad12	3290	0	1161	0	3694	0	4244	0	CFG_GPMC_AD12_OUT	vout3_d12	-
F5	gpmc_ad13	2573	0	524	0	3058	0	3908	0	CFG_GPMC_AD13_OUT	vout3_d13	-
E5	gpmc_ad14	2540	0	632	0	3165	0	3715	0	CFG_GPMC_AD14_OUT	vout3_d14	-

Table 7-20. Manual Functions Mapping for DSS VOUT3 (continued)

BALL	BALL NAME	VOUT3_MANUAL1		VOUT3_MANUAL2		VOUT3_MANUAL3		VOUT3_MANUAL4		CFG REGISTER	MUXMODE	
		A_DELAY (ps)	G_DELAY (ps)	A_DELAY (ps)	G_DELAY (ps)	A_DELAY (ps)	G_DELAY (ps)	A_DELAY (ps)	G_DELAY (ps)		3	4
F4	gpmc_ad15	3181	0	1012	0	3545	0	4295	0	CFG_GPMC_AD15_OUT	vout3_d15	-
G1	gpmc_ad2	3550	45	1222	0	3756	0	4506	0	CFG_GPMC_AD2_OUT	vout3_d2	-
H2	gpmc_ad3	2922	0	875	0	3408	0	4158	0	CFG_GPMC_AD3_OUT	vout3_d3	-
H3	gpmc_ad4	3463	36	1170	0	3703	0	4453	0	CFG_GPMC_AD4_OUT	vout3_d4	-
H4	gpmc_ad5	2299	17	358	0	2930	0	3780	0	CFG_GPMC_AD5_OUT	vout3_d5	-
H5	gpmc_ad6	3346	0	1184	0	3717	0	4267	0	CFG_GPMC_AD6_OUT	vout3_d6	-
F1	gpmc_ad7	2971	0	908	0	3441	0	3991	0	CFG_GPMC_AD7_OUT	vout3_d7	-
G2	gpmc_ad8	874	234	0	0	1923	0	2873	0	CFG_GPMC_AD8_OUT	vout3_d8	-
G3	gpmc_ad9	1160	221	0	0	2402	0	3252	0	CFG_GPMC_AD9_OUT	vout3_d9	-
K2	gpmc_cs3	0	600	1505	1379	0	947	0	947	CFG_GPMC_CS3_OUT	vout3_clk	-
AB6	vin1a_clk0	2670	0	1280	0	3511	0	4381	0	CFG_VIN1A_CLK0_OUT	vout3_d16	vout3_fld
AD5	vin1a_d0	2750	196	1286	0	3820	0	4690	0	CFG_VIN1A_D0_OUT	vout3_d7	vout3_d23
AE5	vin1a_d1	2409	240	1282	0	3816	0	4686	0	CFG_VIN1A_D1_OUT	vout3_d6	vout3_d22
AE3	vin1a_d10	3026	270	1038	622	4228	0	5098	0	CFG_VIN1A_D10_OUT	-	vout3_d13
AA4	vin1a_d11	2711	203	1141	0	3867	0	4737	0	CFG_VIN1A_D11_OUT	-	vout3_d12
AD3	vin1a_d12	2924	539	1154	0	4422	0	5292	0	CFG_VIN1A_D12_OUT	-	vout3_d11
AC3	vin1a_d13	2861	235	1339	0	3815	0	4685	0	CFG_VIN1A_D13_OUT	-	vout3_d10
AD2	vin1a_d14	3176	377	892	0	4559	0	5429	0	CFG_VIN1A_D14_OUT	-	vout3_d9
AB3	vin1a_d15	2806	232	1221	89	3755	0	4625	0	CFG_VIN1A_D15_OUT	-	vout3_d8
AA2	vin1a_d16	2402	396	692	0	3873	0	4743	0	CFG_VIN1A_D16_OUT	-	vout3_d7
AC2	vin1a_d17	2132	374	353	0	3860	0	4730	0	CFG_VIN1A_D17_OUT	-	vout3_d6
Y3	vin1a_d18	2547	284	1109	0	3857	0	4727	0	CFG_VIN1A_D18_OUT	-	vout3_d5
AB2	vin1a_d19	2095	575	640	180	3929	0	4799	0	CFG_VIN1A_D19_OUT	-	vout3_d4
AA5	vin1a_d2	2546	189	1273	0	3806	0	4476	0	CFG_VIN1A_D2_OUT	vout3_d5	vout3_d21
AB1	vin1a_d20	1825	735	628	0	3552	0	4622	0	CFG_VIN1A_D20_OUT	-	vout3_d3
AC1	vin1a_d21	2720	210	1322	0	4021	0	4891	0	CFG_VIN1A_D21_OUT	-	vout3_d2
AA1	vin1a_d22	2361	413	746	0	3659	0	4729	0	CFG_VIN1A_D22_OUT	-	vout3_d1
Y2	vin1a_d23	2731	273	1547	0	3775	0	4845	0	CFG_VIN1A_D23_OUT	-	vout3_d0
Y5	vin1a_d3	2534	219	1357	0	3890	0	4760	0	CFG_VIN1A_D3_OUT	vout3_d4	vout3_d20
AB7	vin1a_d4	3015	538	2033	19	4585	0	5455	0	CFG_VIN1A_D4_OUT	vout3_d3	vout3_d19
AE4	vin1a_d5	2451	237	1039	0	3572	0	4442	0	CFG_VIN1A_D5_OUT	vout3_d2	vout3_d18
AB5	vin1a_d6	2505	191	1230	0	3763	0	4433	0	CFG_VIN1A_D6_OUT	vout3_d1	vout3_d17

Table 7-20. Manual Functions Mapping for DSS VOUT3 (continued)

BALL	BALL NAME	VOUT3_MANUAL1		VOUT3_MANUAL2		VOUT3_MANUAL3		VOUT3_MANUAL4		CFG REGISTER	MUXMODE	
		A_DELAY (ps)	G_DELAY (ps)	A_DELAY (ps)	G_DELAY (ps)	A_DELAY (ps)	G_DELAY (ps)	A_DELAY (ps)	G_DELAY (ps)		3	4
AD4	vin1a_d7	2550	170	1235	0	3768	0	4638	0	CFG_VIN1A_D7_OUT	vout3_d0	vout3_d16
AA3	vin1a_d8	2847	285	1219	0	3850	0	4720	0	CFG_VIN1A_D8_OUT	-	vout3_d15
Y4	vin1a_d9	2857	247	1113	256	3900	0	4770	0	CFG_VIN1A_D9_OUT	-	vout3_d14
AA7	vin1a_de0	3164	0	1494	0	3728	0	4848	0	CFG_VIN1A_DE0_OUT	vout3_d17	vout3_de
AD6	vin1a_fld0	0	1100	1718	869	261	384	261	384	CFG_VIN1A_FLD0_OUT	-	vout3_clk
AC6	vin1a_hsync0	3171	41	1439	0	3798	0	4668	0	CFG_VIN1A_HSYNC0_OUT	-	vout3_hsync
AC5	vin1a_vsync0	2956	110	1268	88	3610	0	4480	0	CFG_VIN1A_VSYNC0_OUT	-	vout3_vsync

7.8 Display Subsystem – High-Definition Multimedia Interface (HDMI)

The High-Definition Multimedia Interface is provided for transmitting digital television audiovisual signals from DVD players, set-top boxes and other audiovisual sources to television sets, projectors and other video displays. The HDMI interface is aligned with the HDMI TMDS single stream standard v1.4a (720p @60Hz to 1080p @24Hz) and the HDMI v1.3 (1080p @60Hz): 3 data channels, plus 1 clock channel is supported (differential).

NOTE

For more information, see the High-Definition Multimedia Interface chapter of the device TRM

7.9 External Memory Interface (EMIF)

The device has a dedicated interface to DDR3 and DDR2 SDRAM. It supports JEDEC standard compliant DDR2 and DDR3 SDRAM devices with the following features:

- 16-bit or 32-bit data path to external SDRAM memory
- Memory device capacity: 128Mb, 256Mb, 512Mb, 1Gb, 2Gb, 4Gb and 8Gb devices (Single die only)
- One interface with associated DDR2/DDR3 PHYs

NOTE

For more information, see the EMIF Controller section of the Device TRM.

7.10 General-Purpose Memory Controller (GPMC)

The GPMC is the unified memory controller that interfaces external memory devices such as:

- Asynchronous SRAM-like memories and ASIC devices
- Asynchronous page mode and synchronous burst NOR flash
- NAND flash

NOTE

For more information, see the General-Purpose Memory Controller section of the Device TRM.

7.10.1 GPMC/NOR Flash Interface Synchronous Timing

CAUTION

The IO Timings provided in this section are only valid for some GPMC usage modes when the corresponding Virtual IO Timings or Manual IO Timings are configured as described in the tables found in this section.

Table 7-21 and Table 7-22 assume testing over the recommended operating conditions and electrical characteristic conditions below (see Figure 7-7, Figure 7-8, Figure 7-9, Figure 7-10, Figure 7-11 and Figure 7-12).

Table 7-21. GPMC/NOR Flash Interface Timing Requirements - Synchronous Mode - Default

NO.	PARAMETER	DESCRIPTION	MIN	MAX	UNIT
F12	$t_{su(dV-clkH)}$	Setup time, read gpmc_ad[15:0] valid before gpmc_clk high	2.69		ns
F13	$t_{h(clkH-dV)}$	Hold time, read gpmc_ad[15:0] valid after gpmc_clk high	1.53		ns

Table 7-21. GPMC/NOR Flash Interface Timing Requirements - Synchronous Mode - Default (continued)

NO.	PARAMETER	DESCRIPTION	MIN	MAX	UNIT
F21	$t_{su}(waitV-clkH)$	Setup time, gpmc_wait[1:0] valid before gpmc_clk high	2.23		ns
F22	$t_h(clkH-waitV)$	Hold Time, gpmc_wait[1:0] valid after gpmc_clk high	1.52		ns

NOTE

Wait monitoring support is limited to a WaitMonitoringTime value > 0. For a full description of wait monitoring feature, see the Device TRM.

Table 7-22. GPMC/NOR Flash Interface Switching Characteristics - Synchronous Mode - Default

NO.	PARAMETER	DESCRIPTION	MIN	MAX	UNIT
F0	$t_c(clk)$	Cycle time, output clock gpmc_clk period	11.3		ns
F2	$t_d(clkH-nCSV)$	Delay time, gpmc_clk rising edge to gpmc_cs[7:0] transition	F-1.48(6)	F+3.84(6)	ns
F3	$t_d(clkH-nCSIV)$	Delay time, gpmc_clk rising edge to gpmc_cs[7:0] invalid	E-1.48(5)	E +3.84(5)	ns
F4	$t_d(ADDV-clk)$	Delay time, gpmc_a[27:0] address bus valid to gpmc_clk first edge	B-1.69(2)	B+3.76(2)	ns
F5	$t_d(clkH-ADDIV)$	Delay time, gpmc_clk rising edge to gpmc_a[27:0] gpmc address bus invalid	-1.69		ns
F6	$t_d(nBEV-clk)$	Delay time, gpmc_ben[1:0] valid to gpmc_clk rising edge	B-3.8(2)	B+2.37(2)	ns
F7	$t_d(clkH-nBEIV)$	Delay time, gpmc_clk rising edge to gpmc_ben[1:0] invalid	D-0.4(4)	D+1.1(4)	ns
F8	$t_d(clkH-nADV)$	Delay time, gpmc_clk rising edge to gpmc_advn_ale transition	G-1.48 (7)	G+3.84 (7)	ns
F9	$t_d(clkH-nADVIV)$	Delay time, gpmc_clk rising edge to gpmc_advn_ale invalid	D-1.48 (4)	G+3.84 (7)	ns
F10	$t_d(clkH-nOE)$	Delay time, gpmc_clk rising edge to gpmc_oen_ren transition	H-1.41 (8)	H+2.45 (8)	ns
F11	$t_d(clkH-nOEIV)$	Delay time, gpmc_clk rising edge to gpmc_oen_ren invalid	E-1.41 (5)	E+2.1 (5)	ns
F14	$t_d(clkH-nWE)$	Delay time, gpmc_clk rising edge to gpmc_wen transition	I-1.18 (9)	I+3.68 (9)	ns
F15	$t_d(clkH-Data)$	Delay time, gpmc_clk rising edge to gpmc_ad[15:0] data bus transition	J-1.89 (10)	J+4.89 (10)	ns
F17	$t_d(clkH-nBE)$	Delay time, gpmc_clk rising edge to gpmc_ben[1:0] transition	J-1.3 (10)	J+3.8 (10)	ns
F18	$t_w(nCSV)$	Pulse duration, gpmc_cs[7:0] low	A (1)		ns
F19	$t_w(nBEV)$	Pulse duration, gpmc_ben[1:0] low	C (3)		ns
F20	$t_w(nADV)$	Pulse duration, gpmc_advn_ale low	K (11)		ns
F23	$t_d(CLK-GPIO)$	Delay time, gpmc_clk transition to gpio6_16.clkout1 transition	1.2	6.1	ns

Table 7-23. GPMC/NOR Flash Interface Timing Requirements - Synchronous Mode - Alternate

NO.	PARAMETER	DESCRIPTION	MIN	MAX	UNIT
F12	$t_{su}(dV-clkH)$	Setup time, read gpmc_ad[15:0] valid before gpmc_clk high	3.56		ns
F13	$t_h(clkH-dV)$	Hold time, read gpmc_ad[15:0] valid after gpmc_clk high	1.9		ns
F21	$t_{su}(waitV-clkH)$	Setup time, gpmc_wait[1:0] valid before gpmc_clk high	3.1		ns
F22	$t_h(clkH-waitV)$	Hold Time, gpmc_wait[1:0] valid after gpmc_clk high	1.9		ns

Table 7-24. GPMC/NOR Flash Interface Switching Characteristics - Synchronous Mode - Alternate

NO.	PARAMETER	DESCRIPTION	MIN	MAX	UNIT
F0	$t_c(clk)$	Cycle time, output clock gpmc_clk period ⁽¹²⁾	15.04		ns
F2	$t_d(clkH-nCSV)$	Delay time, gpmc_clk rising edge to gpmc_cs[7:0] transition	F-0.84 (6)	F+6.73 (6)	ns

Table 7-24. GPMC/NOR Flash Interface Switching Characteristics - Synchronous Mode - Alternate (continued)

NO.	PARAMETER	DESCRIPTION	MIN	MAX	UNIT
F3	$t_{d(\text{clkH-nCSIV})}$	Delay time, gpmc_clk rising edge to gpmc_cs[7:0] invalid	E-0.84 (5)	E+6.73 (5)	ns
F4	$t_{d(\text{ADDV-clk})}$	Delay time, gpmc_a[27:0] address bus valid to gpmc_clk first edge	B-1.36 (2)	B+6.73 (2)	ns
F5	$t_{d(\text{clkH-ADDIV})}$	Delay time, gpmc_clk rising edge to gpmc_a[27:0] gpmc address bus invalid	-1.36		ns
F6	$t_{d(\text{nBEV-clk})}$	Delay time, gpmc_ben[1:0] valid to gpmc_clk rising edge	B-6.34 (2)	B+0.6 (2)	ns
F7	$t_{d(\text{clkH-nBEIV})}$	Delay time, gpmc_clk rising edge to gpmc_ben[1:0] invalid	D-0.4 (4)	D+4.9 (4)	ns
F8	$t_{d(\text{clkH-nADV})}$	Delay time, gpmc_clk rising edge to gpmc_advn_ale transition	G-0.67 (7)	G+6.1 (7)	ns
F9	$t_{d(\text{clkH-nADVIV})}$	Delay time, gpmc_clk rising edge to gpmc_advn_ale invalid	D-0.67 (4)	D+6.1 (4)	ns
F10	$t_{d(\text{clkH-nOE})}$	Delay time, gpmc_clk rising edge to gpmc_oen_ren transition	H-0.67 (8)	H+5.65 (8)	ns
F11	$t_{d(\text{clkH-nOEIV})}$	Delay time, gpmc_clk rising edge to gpmc_oen_ren invalid	E-0.67 (5)	E+5.65 (5)	ns
F14	$t_{d(\text{clkH-nWE})}$	Delay time, gpmc_clk rising edge to gpmc_wen transition	I-0.6 (9)	I+6.1 (9)	ns
F15	$t_{d(\text{clkH-Data})}$	Delay time, gpmc_clk rising edge to gpmc_ad[15:0] data bus transition	J-1.76 (10)	J+6.39 (10)	ns
F17	$t_{d(\text{clkH-nBE})}$	Delay time, gpmc_clk rising edge to gpmc_ben[1:0] transition	J-0.6 (10)	J+6.34 (10)	ns
F18	$t_w(\text{nCSV})$	Pulse duration, gpmc_cs[7:0] low	A (10)		ns
F19	$t_w(\text{nBEV})$	Pulse duration, gpmc_ben[1:0] low	C (3)		ns
F20	$t_w(\text{nADV})$	Pulse duration, gpmc_advn_ale low	K (11)		ns
F23	$t_{d(\text{CLK-GPIO})}$	Delay time, gpmc_clk transition to gpio6_16.clkout1 transition ⁽¹³⁾	0.96	6.1	ns

- (1) For single read: $A = (\text{CSRdOffTime} - \text{CSOnTime}) * (\text{TimeParaGranularity} + 1) * \text{GPMC_FCLK period}$
 For burst read: $A = (\text{CSRdOffTime} - \text{CSOnTime} + (n - 1) * \text{PageBurstAccessTime}) * (\text{TimeParaGranularity} + 1) * \text{GPMC_FCLK period}$
 For burst write: $A = (\text{CSWrOffTime} - \text{CSOnTime} + (n - 1) * \text{PageBurstAccessTime}) * (\text{TimeParaGranularity} + 1) * \text{GPMC_FCLK period}$
 with n the page burst access number.
- (2) $B = \text{ClkActivationTime} * \text{GPMC_FCLK}$
- (3) For single read: $C = \text{RdCycleTime} * (\text{TimeParaGranularity} + 1) * \text{GPMC_FCLK}$
 For burst read: $C = (\text{RdCycleTime} + (n - 1) * \text{PageBurstAccessTime}) * (\text{TimeParaGranularity} + 1) * \text{GPMC_FCLK}$
 For Burst write: $C = (\text{WrCycleTime} + (n - 1) * \text{PageBurstAccessTime}) * (\text{TimeParaGranularity} + 1) * \text{GPMC_FCLK}$ with n the page burst access number.
- (4) For single read: $D = (\text{RdCycleTime} - \text{AccessTime}) * (\text{TimeParaGranularity} + 1) * \text{GPMC_FCLK}$
 For burst read: $D = (\text{RdCycleTime} - \text{AccessTime}) * (\text{TimeParaGranularity} + 1) * \text{GPMC_FCLK}$
 For burst write: $D = (\text{WrCycleTime} - \text{AccessTime}) * (\text{TimeParaGranularity} + 1) * \text{GPMC_FCLK}$
- (5) For single read: $E = (\text{CSRdOffTime} - \text{AccessTime}) * (\text{TimeParaGranularity} + 1) * \text{GPMC_FCLK}$
 For burst read: $E = (\text{CSRdOffTime} - \text{AccessTime}) * (\text{TimeParaGranularity} + 1) * \text{GPMC_FCLK}$
 For burst write: $E = (\text{CSWrOffTime} - \text{AccessTime}) * (\text{TimeParaGranularity} + 1) * \text{GPMC_FCLK}$
- (6) For nCS falling edge (CS activated):
 Case GpmcFCLKDivider = 0 :
 $F = 0.5 * \text{CSExtraDelay} * \text{GPMC_FCLK}$ Case GpmcFCLKDivider = 1 :
 $F = 0.5 * \text{CSExtraDelay} * \text{GPMC_FCLK}$ if (ClkActivationTime and CSOnTime are odd) or (ClkActivationTime and CSOnTime are even)
 $F = (1 + 0.5 * \text{CSExtraDelay}) * \text{GPMC_FCLK}$ otherwise
 Case GpmcFCLKDivider = 2 :
 $F = 0.5 * \text{CSExtraDelay} * \text{GPMC_FCLK}$ if ((CSOnTime - ClkActivationTime) is a multiple of 3)
 $F = (1 + 0.5 * \text{CSExtraDelay}) * \text{GPMC_FCLK}$ if ((CSOnTime - ClkActivationTime - 1) is a multiple of 3)
 $F = (2 + 0.5 * \text{CSExtraDelay}) * \text{GPMC_FCLK}$ if ((CSOnTime - ClkActivationTime - 2) is a multiple of 3)
 Case GpmcFCLKDivider = 3 :
 $F = 0.5 * \text{CSExtraDelay} * \text{GPMC_FCLK}$ if ((CSOnTime - ClkActivationTime) is a multiple of 4)
 $F = (1 + 0.5 * \text{CSExtraDelay}) * \text{GPMC_FCLK}$ if ((CSOnTime - ClkActivationTime - 1) is a multiple of 4)
 $F = (2 + 0.5 * \text{CSExtraDelay}) * \text{GPMC_FCLK}$ if ((CSOnTime - ClkActivationTime - 2) is a multiple of 4)
 $F = (3 + 0.5 * \text{CSExtraDelay}) * \text{GPMC_FCLK}$ if ((CSOnTime - ClkActivationTime - 3) is a multiple of 4)
- (7) For ADV falling edge (ADV activated):
 Case GpmcFCLKDivider = 0 :
 $G = 0.5 * \text{ADVExtraDelay} * \text{GPMC_FCLK}$
 Case GpmcFCLKDivider = 1 :
 $G = 0.5 * \text{ADVExtraDelay} * \text{GPMC_FCLK}$ if (ClkActivationTime and ADVOnTime are odd) or (ClkActivationTime and ADVOnTime are even)
 $G = (1 + 0.5 * \text{ADVExtraDelay}) * \text{GPMC_FCLK}$ otherwise

Case GpmcFCLKDivider = 2:

$G = 0.5 * ADVExtraDelay * GPMC_FCLK$ if ((ADVOnTime – ClkActivationTime) is a multiple of 3)

$G = (1 + 0.5 * ADVExtraDelay) * GPMC_FCLK$ if ((ADVOnTime – ClkActivationTime – 1) is a multiple of 3)

$G = (2 + 0.5 * ADVExtraDelay) * GPMC_FCLK$ if ((ADVOnTime – ClkActivationTime – 2) is a multiple of 3)

For ADV rising edge (ADV deactivated) in Reading mode:

Case GpmcFCLKDivider = 0:

$G = 0.5 * ADVExtraDelay * GPMC_FCLK$

Case GpmcFCLKDivider = 1:

$G = 0.5 * ADVExtraDelay * GPMC_FCLK$ if (ClkActivationTime and ADVRdOffTime are odd) or (ClkActivationTime and ADVRdOffTime are even)

$G = (1 + 0.5 * ADVExtraDelay) * GPMC_FCLK$ otherwise

Case GpmcFCLKDivider = 2:

$G = 0.5 * ADVExtraDelay * GPMC_FCLK$ if ((ADVRdOffTime – ClkActivationTime) is a multiple of 3)

$G = (1 + 0.5 * ADVExtraDelay) * GPMC_FCLK$ if ((ADVRdOffTime – ClkActivationTime – 1) is a multiple of 3)

$G = (2 + 0.5 * ADVExtraDelay) * GPMC_FCLK$ if ((ADVRdOffTime – ClkActivationTime – 2) is a multiple of 3)

Case GpmcFCLKDivider = 3:

$G = 0.5 * ADVExtraDelay * GPMC_FCLK$ if ((ADVRdOffTime – ClkActivationTime) is a multiple of 4)

$G = (1 + 0.5 * ADVExtraDelay) * GPMC_FCLK$ if ((ADVRdOffTime – ClkActivationTime – 1) is a multiple of 4)

$G = (2 + 0.5 * ADVExtraDelay) * GPMC_FCLK$ if ((ADVRdOffTime – ClkActivationTime – 2) is a multiple of 4)

$G = (3 + 0.5 * ADVExtraDelay) * GPMC_FCLK$ if ((ADVRdOffTime – ClkActivationTime – 3) is a multiple of 4)

For ADV rising edge (ADV deactivated) in Writing mode:

Case GpmcFCLKDivider = 0:

$G = 0.5 * ADVExtraDelay * GPMC_FCLK$

Case GpmcFCLKDivider = 1:

$G = 0.5 * ADVExtraDelay * GPMC_FCLK$ if (ClkActivationTime and ADVWrOffTime are odd) or (ClkActivationTime and ADVWrOffTime are even)

$G = (1 + 0.5 * ADVExtraDelay) * GPMC_FCLK$ otherwise

Case GpmcFCLKDivider = 2:

$G = 0.5 * ADVExtraDelay * GPMC_FCLK$ if ((ADVWrOffTime – ClkActivationTime) is a multiple of 3)

$G = (1 + 0.5 * ADVExtraDelay) * GPMC_FCLK$ if ((ADVWrOffTime – ClkActivationTime – 1) is a multiple of 3)

$G = (2 + 0.5 * ADVExtraDelay) * GPMC_FCLK$ if ((ADVWrOffTime – ClkActivationTime – 2) is a multiple of 3)

Case GpmcFCLKDivider = 3:

$G = 0.5 * ADVExtraDelay * GPMC_FCLK$ if ((ADVWrOffTime – ClkActivationTime) is a multiple of 4)

$G = (1 + 0.5 * ADVExtraDelay) * GPMC_FCLK$ if ((ADVWrOffTime – ClkActivationTime – 1) is a multiple of 4)

$G = (2 + 0.5 * ADVExtraDelay) * GPMC_FCLK$ if ((ADVWrOffTime – ClkActivationTime – 2) is a multiple of 4)

$G = (3 + 0.5 * ADVExtraDelay) * GPMC_FCLK$ if ((ADVWrOffTime – ClkActivationTime – 3) is a multiple of 4)

(8) For OE falling edge (OE activated):

Case GpmcFCLKDivider = 0:

$H = 0.5 * OEEExtraDelay * GPMC_FCLK$

Case GpmcFCLKDivider = 1:

$H = 0.5 * OEEExtraDelay * GPMC_FCLK$ if (ClkActivationTime and OEOnTime are odd) or (ClkActivationTime and OEOnTime are even)

$H = (1 + 0.5 * OEEExtraDelay) * GPMC_FCLK$ otherwise

Case GpmcFCLKDivider = 2:

$H = 0.5 * OEEExtraDelay * GPMC_FCLK$ if ((OEOnTime – ClkActivationTime) is a multiple of 3)

$H = (1 + 0.5 * OEEExtraDelay) * GPMC_FCLK$ if ((OEOnTime – ClkActivationTime – 1) is a multiple of 3)

$H = (2 + 0.5 * OEEExtraDelay) * GPMC_FCLK$ if ((OEOnTime – ClkActivationTime – 2) is a multiple of 3)

Case GpmcFCLKDivider = 3:

$H = 0.5 * OEEExtraDelay * GPMC_FCLK$ if ((OEOnTime – ClkActivationTime) is a multiple of 4)

$H = (1 + 0.5 * OEEExtraDelay) * GPMC_FCLK$ if ((OEOnTime – ClkActivationTime – 1) is a multiple of 4)

$H = (2 + 0.5 * OEEExtraDelay) * GPMC_FCLK$ if ((OEOnTime – ClkActivationTime – 2) is a multiple of 4)

$H = (3 + 0.5 * OEEExtraDelay) * GPMC_FCLK$ if ((OEOnTime – ClkActivationTime – 3) is a multiple of 4)

For OE rising edge (OE deactivated):

Case GpmcFCLKDivider = 0:

$H = 0.5 * OEEExtraDelay * GPMC_FCLK$

Case GpmcFCLKDivider = 1:

$H = 0.5 * OEEExtraDelay * GPMC_FCLK$ if (ClkActivationTime and OEOffTime are odd) or (ClkActivationTime and OEOffTime are even)

$H = (1 + 0.5 * OEEExtraDelay) * GPMC_FCLK$ otherwise

Case GpmcFCLKDivider = 2:

$H = 0.5 * OEEExtraDelay * GPMC_FCLK$ if ((OEOffTime – ClkActivationTime) is a multiple of 3)

$H = (1 + 0.5 * OEEExtraDelay) * GPMC_FCLK$ if ((OEOffTime – ClkActivationTime – 1) is a multiple of 3)

$H = (2 + 0.5 * OEEExtraDelay) * GPMC_FCLK$ if ((OEOffTime – ClkActivationTime – 2) is a multiple of 3)

Case GpmcFCLKDivider = 3:

$H = 0.5 * OEEExtraDelay * GPMC_FCLK$ if ((OEOffTime – ClkActivationTime) is a multiple of 4)

$H = (1 + 0.5 * OEEExtraDelay) * GPMC_FCLK$ if ((OEOffTime – ClkActivationTime – 1) is a multiple of 4)

$H = (2 + 0.5 * OEEExtraDelay) * GPMC_FCLK$ if ((OEOffTime – ClkActivationTime – 2) is a multiple of 4)

$H = (3 + 0.5 * OEEExtraDelay) * GPMC_FCLK$ if ((OEOffTime – ClkActivationTime – 3) is a multiple of 4)

(9) For WE falling edge (WE activated):

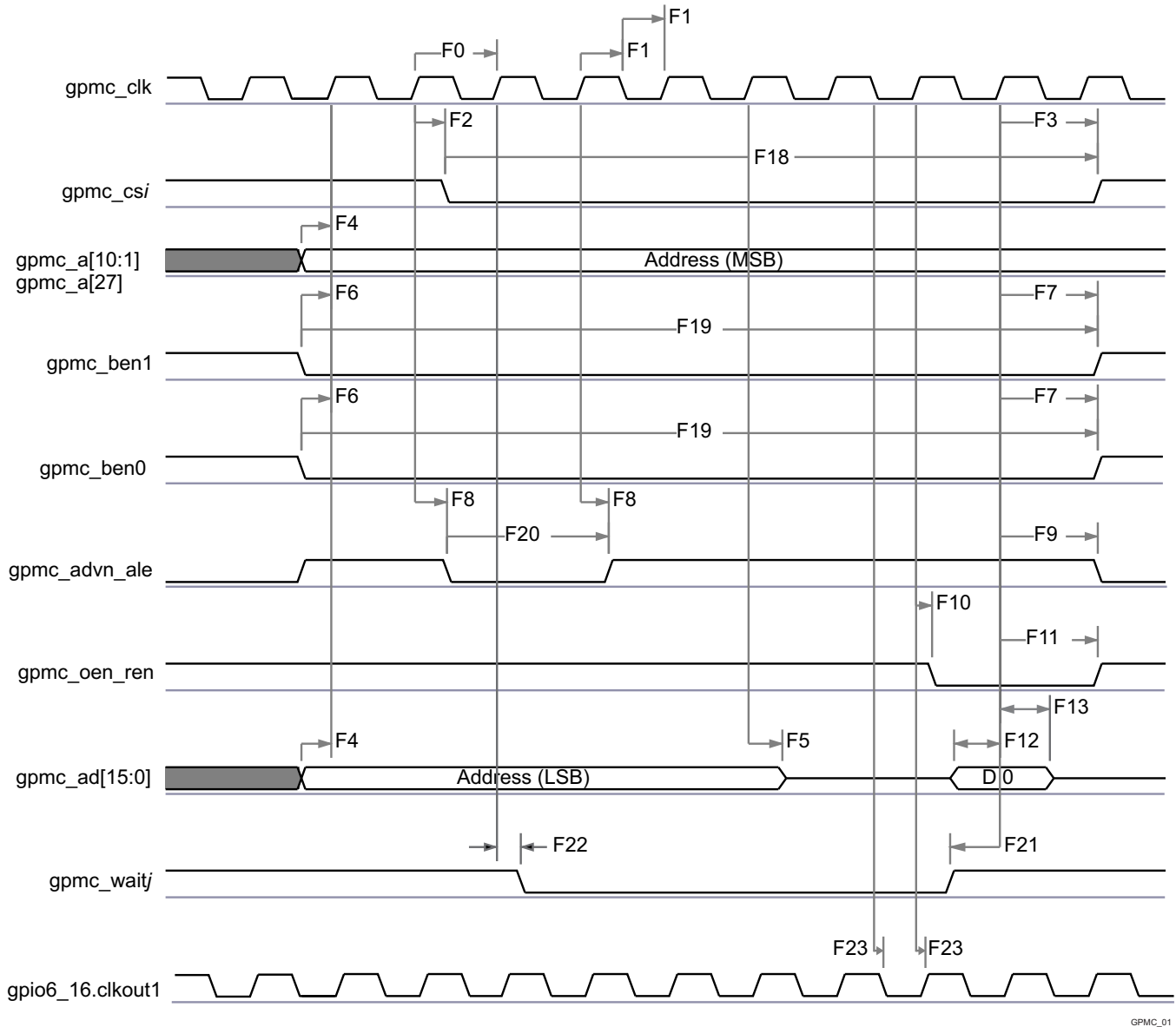
Case GpmcFCLKDivider = 0:

$I = 0.5 * WEExtraDelay * GPMC_FCLK$

Case GpmcFCLKDivider = 1:

$I = 0.5 * WEExtraDelay * GPMC_FCLK$ if (ClkActivationTime and WEOnTime are odd) or (ClkActivationTime and WEOnTime are even)

- $I = (1 + 0.5 * WEExtraDelay) * GPMC_FCLK$ otherwise
 - Case GpmcFCLKDivider = 2:
 - $I = 0.5 * WEExtraDelay * GPMC_FCLK$ if $((WEOnTime - ClkActivationTime)$ is a multiple of 3)
 - $I = (1 + 0.5 * WEExtraDelay) * GPMC_FCLK$ if $((WEOnTime - ClkActivationTime - 1)$ is a multiple of 3)
 - $I = (2 + 0.5 * WEExtraDelay) * GPMC_FCLK$ if $((WEOnTime - ClkActivationTime - 2)$ is a multiple of 3)
 - Case GpmcFCLKDivider = 3:
 - $I = 0.5 * WEExtraDelay * GPMC_FCLK$ if $((WEOnTime - ClkActivationTime)$ is a multiple of 4)
 - $I = (1 + 0.5 * WEExtraDelay) * GPMC_FCLK$ if $((WEOnTime - ClkActivationTime - 1)$ is a multiple of 4)
 - $I = (2 + 0.5 * WEExtraDelay) * GPMC_FCLK$ if $((WEOnTime - ClkActivationTime - 2)$ is a multiple of 4)
 - $I = (3 + 0.5 * WEExtraDelay) * GPMC_FCLK$ if $((WEOnTime - ClkActivationTime - 3)$ is a multiple of 4)
 - For WE rising edge (WE deactivated):
 - Case GpmcFCLKDivider = 0:
 - $I = 0.5 * WEExtraDelay * GPMC_FCLK$
 - Case GpmcFCLKDivider = 1:
 - $I = 0.5 * WEExtraDelay * GPMC_FCLK$ if (ClkActivationTime and WEOffTime are odd) or (ClkActivationTime and WEOffTime are even)
 - $I = (1 + 0.5 * WEExtraDelay) * GPMC_FCLK$ otherwise
 - Case GpmcFCLKDivider = 2:
 - $I = 0.5 * WEExtraDelay * GPMC_FCLK$ if $((WEOffTime - ClkActivationTime)$ is a multiple of 3)
 - $I = (1 + 0.5 * WEExtraDelay) * GPMC_FCLK$ if $((WEOffTime - ClkActivationTime - 1)$ is a multiple of 3)
 - $I = (2 + 0.5 * WEExtraDelay) * GPMC_FCLK$ if $((WEOffTime - ClkActivationTime - 2)$ is a multiple of 3)
 - Case GpmcFCLKDivider = 3:
 - $I = 0.5 * WEExtraDelay * GPMC_FCLK$ if $((WEOffTime - ClkActivationTime)$ is a multiple of 4)
 - $I = (1 + 0.5 * WEExtraDelay) * GPMC_FCLK$ if $((WEOffTime - ClkActivationTime - 1)$ is a multiple of 4)
 - $I = (2 + 0.5 * WEExtraDelay) * GPMC_FCLK$ if $((WEOffTime - ClkActivationTime - 2)$ is a multiple of 4)
 - $I = (3 + 0.5 * WEExtraDelay) * GPMC_FCLK$ if $((WEOffTime - ClkActivationTime - 3)$ is a multiple of 4)
- (10) J = GPMC_FCLK period, where GPMC_FCLK is the General Purpose Memory Controller internal functional clock
- (11) For read:
 $K = (ADVrdOffTime - ADVrdOnTime) * (TimeParaGranularity + 1) * GPMC_FCLK$
 For write: $K = (ADVwrOffTime - ADVwrOnTime) * (TimeParaGranularity + 1) * GPMC_FCLK$
- (12) The gpmc_clk output clock maximum and minimum frequency is programmable in the I/F module by setting the GPMC_CONFIG1_CSx configuration register bit fields GpmcFCLKDivider
- (13) gpio6_16 programmed to MUXMODE=9 (clkout1), CM_CLKSEL_CLKOUTMUX1 programmed to 7 (CORE_DPLL_OUT_DCLK), CM_CLKSEL_CORE_DPLL_OUT_CLK_CLKOUTMUX programmed to 1.
- (14) CSEXTRADelay = 0, ADVEXTRADelay = 0, WEEXTRADelay = 0, OEEXTRADelay = 0. Extra half-GPMC_FCLK cycle delay mode is not timed.



GPMC_01

Figure 7-7. GPMC / Multiplexed 16bits NOR Flash - Synchronous Single Read - (GpmcFCLKDivider = 0)⁽¹⁾⁽²⁾

(1) In gpmc_csi, i = 0 to 7.

(2) In gpmc_waitj, j = 0 to 1.

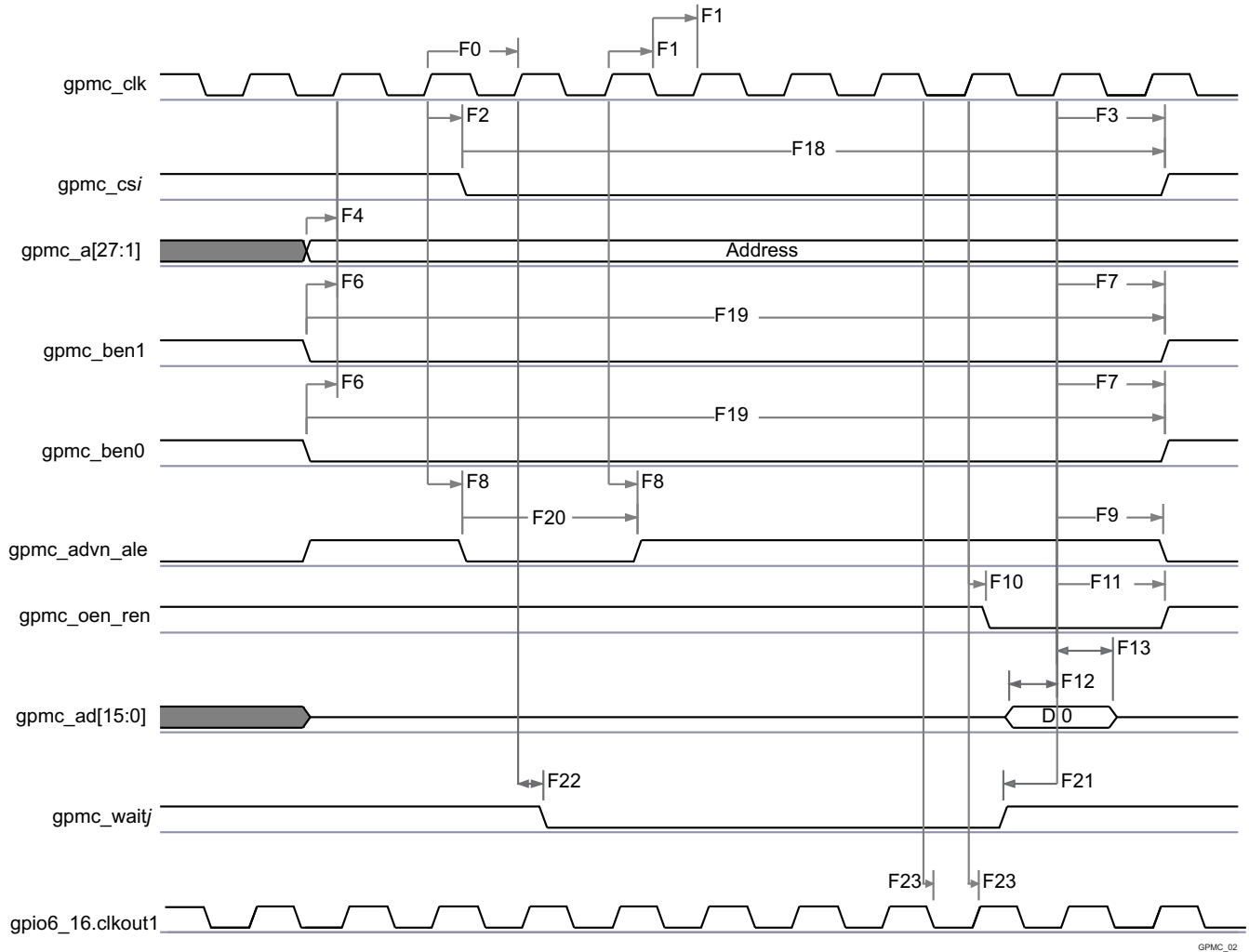
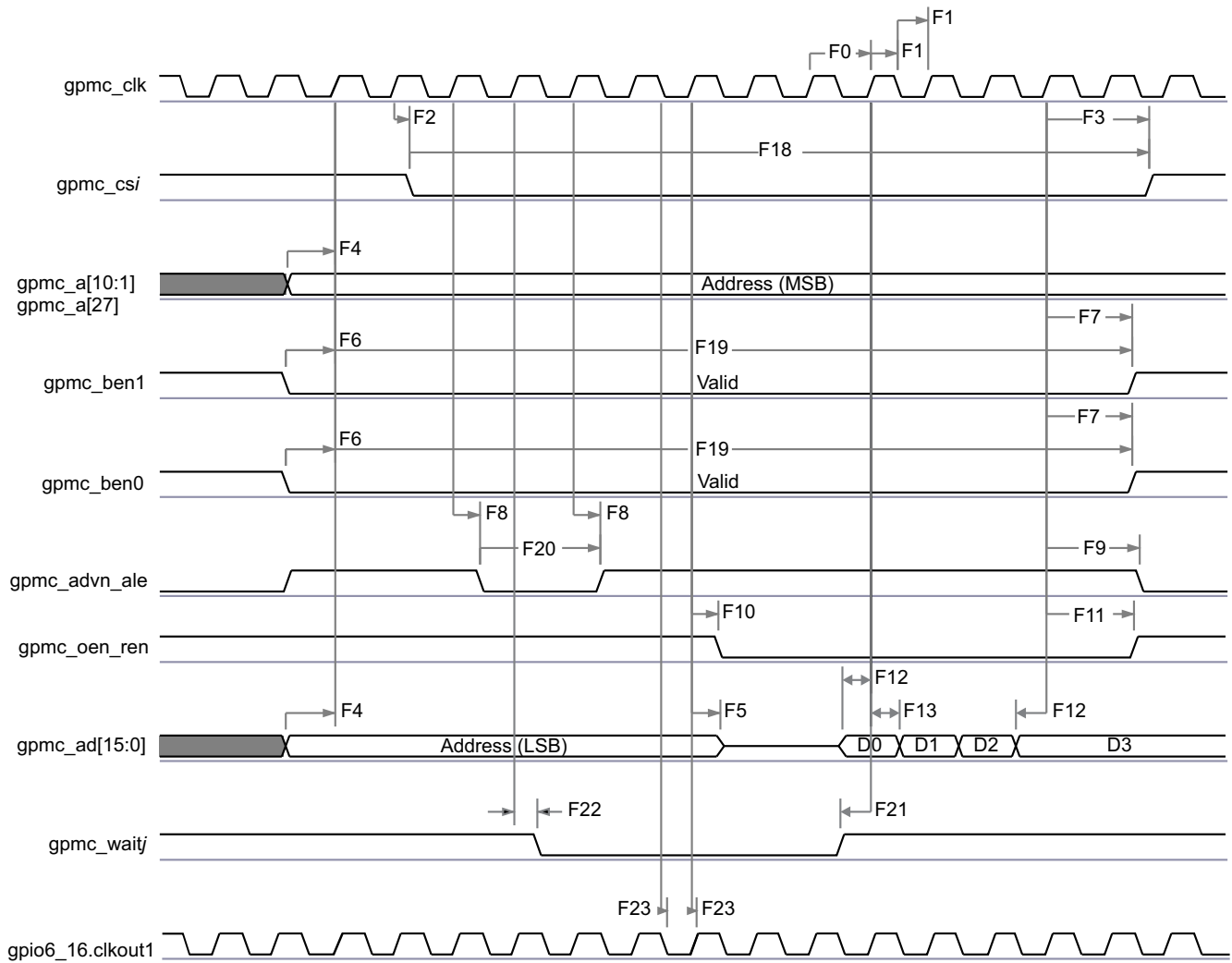


Figure 7-8. GPMC / Nonmultiplexed 16bits NOR Flash - Synchronous Single Read - (GpmcFCLKDivider = 0)⁽¹⁾⁽²⁾

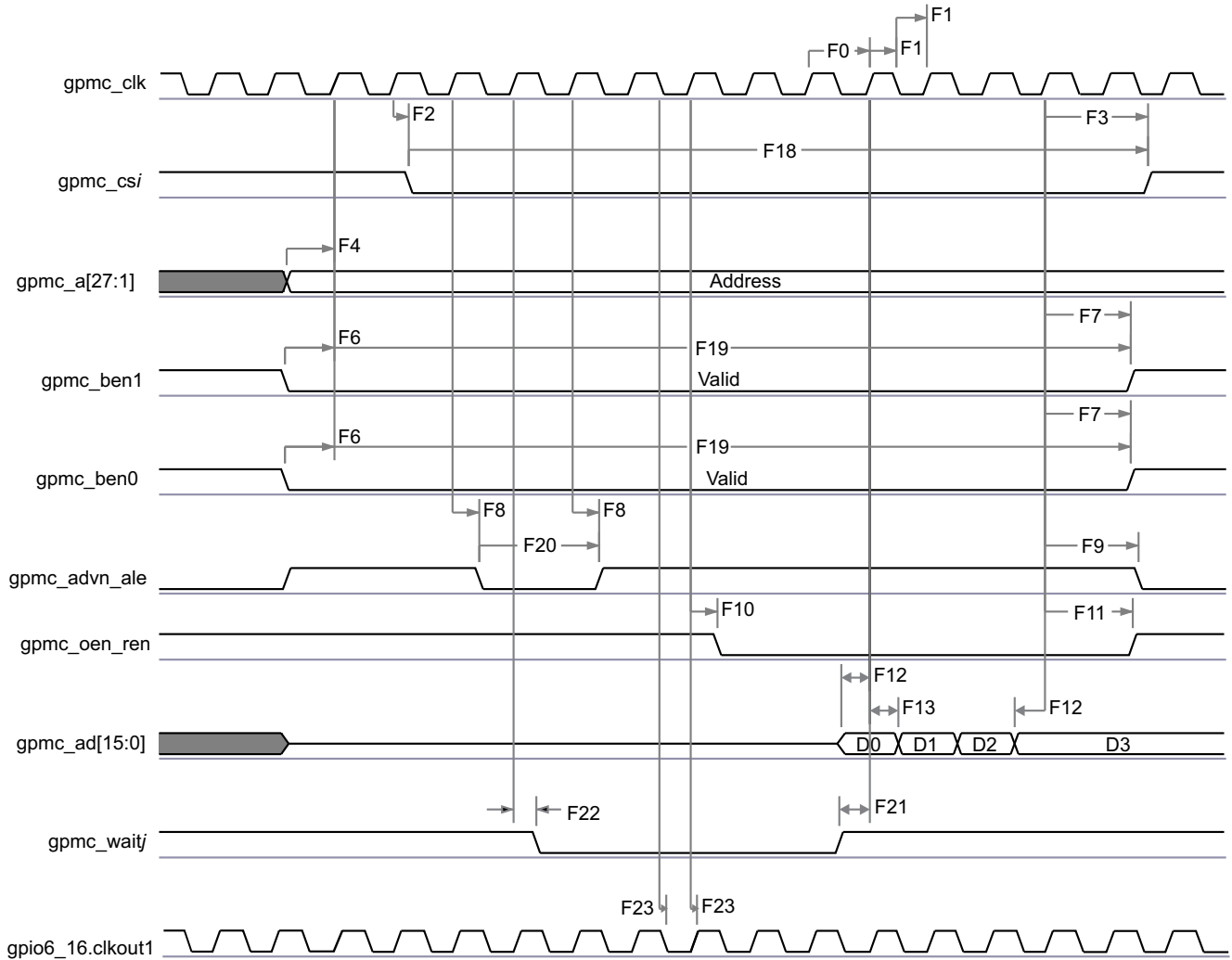
- (1) In gpmc_csi, i = 0 to 7.
- (2) In gpmc_waitj, j = 0 to 1.



GPMC_03

Figure 7-9. GPMC / Multiplexed 16bits NOR Flash - Synchronous Burst Read 4x16 bits - (GpmcFCLKDivider = 0)⁽¹⁾⁽²⁾

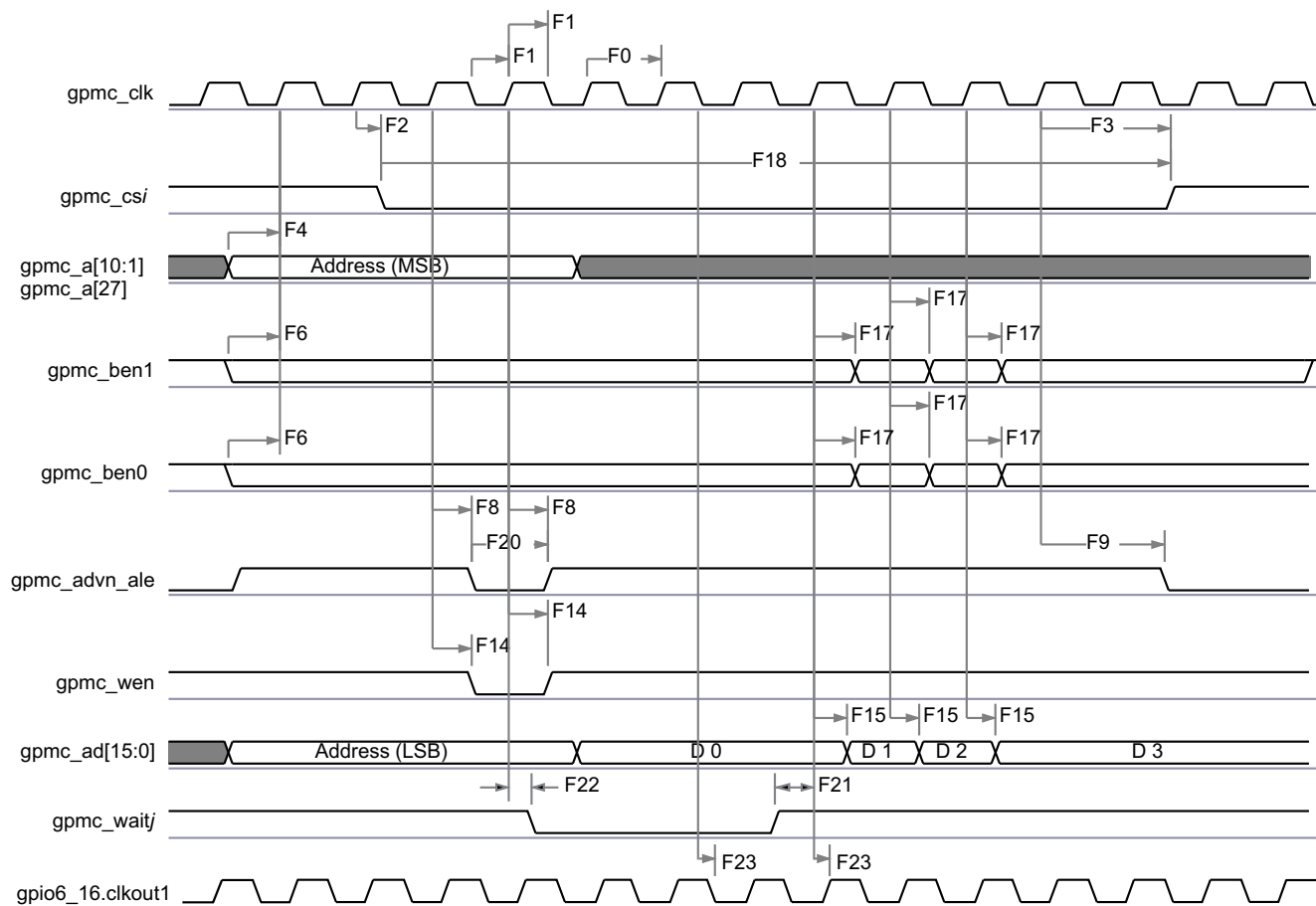
- (1) In gpmc_csi, i= 0 to 7.
- (2) In gpmc_waitj, j = 0 to 1.



GPMC_04

Figure 7-10. GPMC / Nonmultiplexed 16bits NOR Flash - Synchronous Burst Read 4x16 bits - (GpmcFCLKDivider = 0)⁽¹⁾⁽²⁾

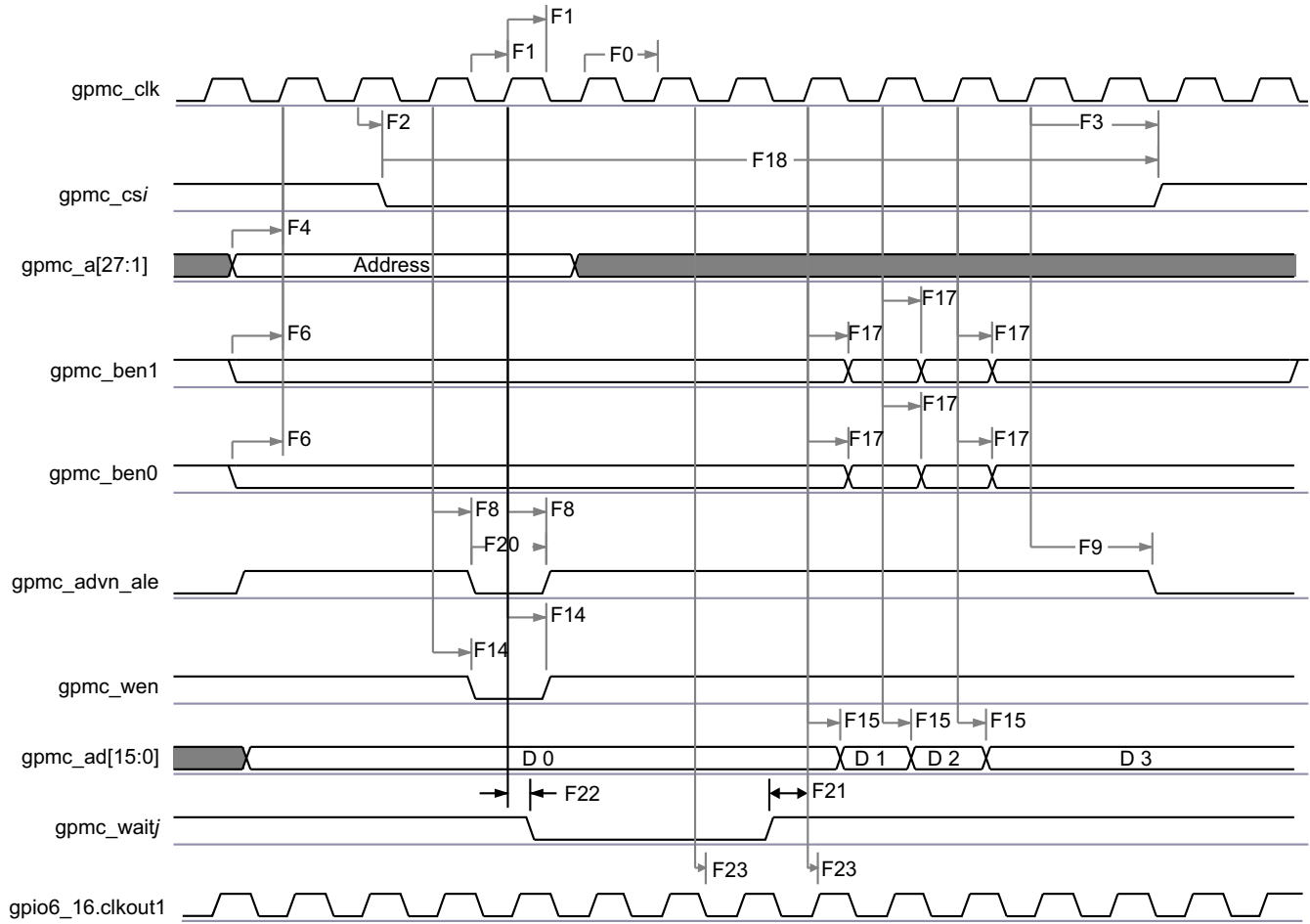
- (1) In gpmc_csi, i = 0 to 7.
- (2) In gpmc_waitj, j = 0 to 1.



GPMC_05

Figure 7-11. GPMC / Multiplexed 16bits NOR Flash - Synchronous Burst Write 4x16bits - (GpmcFCLKDivider = 0)⁽¹⁾⁽²⁾

- (1) In gpmc_csi, i = 0 to 7.
- (2) In gpmc_waitj, j = 0 to 1.



GPMC_06

Figure 7-12. GPMC / Nonmultiplexed 16bits NOR Flash - Synchronous Burst Write 4x16bits - (GpmcFCLKDivider = 0)⁽¹⁾⁽²⁾

- (1) In gpmc_csi, i = 1 to 7.
- (2) In gpmc_waitj, j = 0 to 1.

7.10.2 GPMC/NOR Flash Interface Asynchronous Timing

CAUTION

The IO Timings provided in this section are only valid for some GPMC usage modes when the corresponding Virtual IO Timings or Manual IO Timings are configured as described in the tables found in this section.

Table 7-25 and Table 7-26 assume testing over the recommended operating conditions and electrical characteristic conditions below (see Figure 7-13, Figure 7-14, Figure 7-15, Figure 7-16, Figure 7-17 and Figure 7-18).

Table 7-25. GPMC/NOR Flash Interface Timing Requirements - Asynchronous Mode

NO.	PARAMETER	DESCRIPTION	MIN	MAX	UNIT
FA5	t _{acc(DAT)}	Data Maximum Access Time (GPMC_FCLK cycles)		H ⁽¹⁾	cycles

Table 7-25. GPMC/NOR Flash Interface Timing Requirements - Asynchronous Mode (continued)

NO.	PARAMETER	DESCRIPTION	MIN	MAX	UNIT
FA20	$t_{acc1-pgmode}(DAT)$	Page Mode Successive Data Maximum Access Time (GPMC_FCLK cycles)		P ⁽²⁾	cycles
FA21	$t_{acc2-pgmode}(DAT)$	Page Mode First Data Maximum Access Time (GPMC_FCLK cycles)		H ⁽¹⁾	cycles
-	$t_{su}(DV-OEH)$	Setup time, read gpmc_ad[15:0] valid before gpmc_oen_ren high	1.9		ns
-	$t_h(OEH-DV)$	Hold time, read gpmc_ad[15:0] valid after gpmc_oen_ren high	1		ns

(1) H = Access Time * (TimeParaGranularity + 1)

(2) P = PageBurstAccessTime * (TimeParaGranularity + 1)

Table 7-26. GPMC/NOR Flash Interface Switching Characteristics - Asynchronous Mode

NO.	PARAMETER	DESCRIPTION	MIN	MAX	UNIT
-	$t_r(DO)$	Rising time, gpmc_ad[15:0] output data	0.447	4.067	ns
-	$t_f(DO)$	Falling time, gpmc_ad[15:0] output data	0.43	4.463	ns
FA0	$t_w(nBEV)$	Pulse duration, gpmc_ben[1:0] valid time		N ⁽¹⁾	ns
FA1	$t_w(nCSV)$	Pulse duration, gpmc_cs[7:0] low		A ⁽²⁾	ns
FA3	$t_d(nCSV-nADVIV)$	Delay time, gpmc_cs[7:0] valid to gpmc_advn_ale invalid	B - 2 ⁽³⁾	B + 4 ⁽³⁾	ns
FA4	$t_d(nCSV-nOEIV)$	Delay time, gpmc_cs[7:0] valid to gpmc_oen_ren invalid (Single read)	C - 2 ⁽⁴⁾	C + 4 ⁽⁴⁾	ns
FA9	$t_d(AV-nCSV)$	Delay time, address bus valid to gpmc_cs[7:0] valid	J - 2 ⁽⁵⁾	J + 4 ⁽⁵⁾	ns
FA10	$t_d(nBEV-nCSV)$	Delay time, gpmc_ben[1:0] valid to gpmc_cs[7:0] valid	J - 2 ⁽⁵⁾	J + 4 ⁽⁵⁾	ns
FA12	$t_d(nCSV-nADVIV)$	Delay time, gpmc_cs[7:0] valid to gpmc_advn_ale valid	K - 2 ⁽⁶⁾	K + 4 ⁽⁶⁾	ns
FA13	$t_d(nCSV-nOEIV)$	Delay time, gpmc_cs[7:0] valid to gpmc_oen_ren valid	L - 2 ⁽⁷⁾	L + 4 ⁽⁷⁾	ns
FA16	$t_w(AIV)$	Pulse duration, address invalid between 2 successive R/W accesses	G ⁽⁸⁾		ns
FA18	$t_d(nCSV-nOEIV)$	Delay time, gpmc_cs[7:0] valid to gpmc_oen_ren invalid (Burst read)	I - 2 ⁽⁹⁾	I + 4 ⁽⁹⁾	ns
FA20	$t_w(AV)$	Pulse duration, address valid : 2nd, 3rd and 4th accesses	D ⁽¹⁰⁾		ns
FA25	$t_d(nCSV-nWEV)$	Delay time, gpmc_cs[7:0] valid to gpmc_wen valid	E - 2 ⁽¹¹⁾	E + 4 ⁽¹¹⁾	ns
FA27	$t_d(nCSV-nWEIV)$	Delay time, gpmc_cs[7:0] valid to gpmc_wen invalid	F - 2 ⁽¹²⁾	F + 4 ⁽¹²⁾	ns
FA28	$t_d(nWEV-DV)$	Delay time, gpmc_wen valid to data bus valid		2	ns
FA29	$t_d(DV-nCSV)$	Delay time, data bus valid to gpmc_cs[7:0] valid	J - 2 ⁽⁵⁾	J + 4 ⁽⁵⁾	ns
FA37	$t_d(nOEIV-AIV)$	Delay time, gpmc_oen_ren valid to gpmc_ad[15:0] multiplexed address bus phase end		2	ns

(1) For single read: N = RdCycleTime * (TimeParaGranularity + 1) * GPMC_FCLK
For single write: N = WrCycleTime * (TimeParaGranularity + 1) * GPMC_FCLK
For burst read: N = (RdCycleTime + (n - 1) * PageBurstAccessTime) * (TimeParaGranularity + 1) * GPMC_FCLK
For burst write: N = (WrCycleTime + (n - 1) * PageBurstAccessTime) * (TimeParaGranularity + 1) * GPMC_FCLK

(2) For single read: A = (CSRdOffTime - CSOnTime) * (TimeParaGranularity + 1) * GPMC_FCLK
For single write: A = (CSWrOffTime - CSOnTime) * (TimeParaGranularity + 1) * GPMC_FCLK
For burst read: A = (CSRdOffTime - CSOnTime + (n - 1) * PageBurstAccessTime) * (TimeParaGranularity + 1) * GPMC_FCLK
For burst write: A = (CSWrOffTime - CSOnTime + (n - 1) * PageBurstAccessTime) * (TimeParaGranularity + 1) * GPMC_FCLK

(3) For reading: B = ((ADVrOffTime - CSOnTime) * (TimeParaGranularity + 1) + 0.5 * (ADVExtraDelay - CSEExtraDelay)) * GPMC_FCLK
For writing: B = ((ADVWrOffTime - CSOnTime) * (TimeParaGranularity + 1) + 0.5 * (ADVExtraDelay - CSEExtraDelay)) * GPMC_FCLK

(4) C = ((OEOffTime - CSOnTime) * (TimeParaGranularity + 1) + 0.5 * (OEEExtraDelay - CSEExtraDelay)) * GPMC_FCLK

(5) J = (CSOnTime * (TimeParaGranularity + 1) + 0.5 * CSEExtraDelay) * GPMC_FCLK

(6) K = ((ADVOnTime - CSOnTime) * (TimeParaGranularity + 1) + 0.5 * (ADVExtraDelay - CSEExtraDelay)) * GPMC_FCLK

(7) L = ((OEOnTime - CSOnTime) * (TimeParaGranularity + 1) + 0.5 * (OEEExtraDelay - CSEExtraDelay)) * GPMC_FCLK

(8) G = Cycle2CycleDelay * GPMC_FCLK * (TimeParaGranularity + 1)

(9) I = ((OEOffTime + (n - 1) * PageBurstAccessTime - CSOnTime) * (TimeParaGranularity + 1) + 0.5 * (OEEExtraDelay - CSEExtraDelay)) * GPMC_FCLK

(10) D = PageBurstAccessTime * (TimeParaGranularity + 1) * GPMC_FCLK

(11) E = ((WEOnTime - CSOnTime) * (TimeParaGranularity + 1) + 0.5 * (WEExtraDelay - CSEExtraDelay)) * GPMC_FCLK

(12) F = ((WEOffTime - CSOnTime) * (TimeParaGranularity + 1) + 0.5 * (WEExtraDelay - CSEExtraDelay)) * GPMC_FCLK

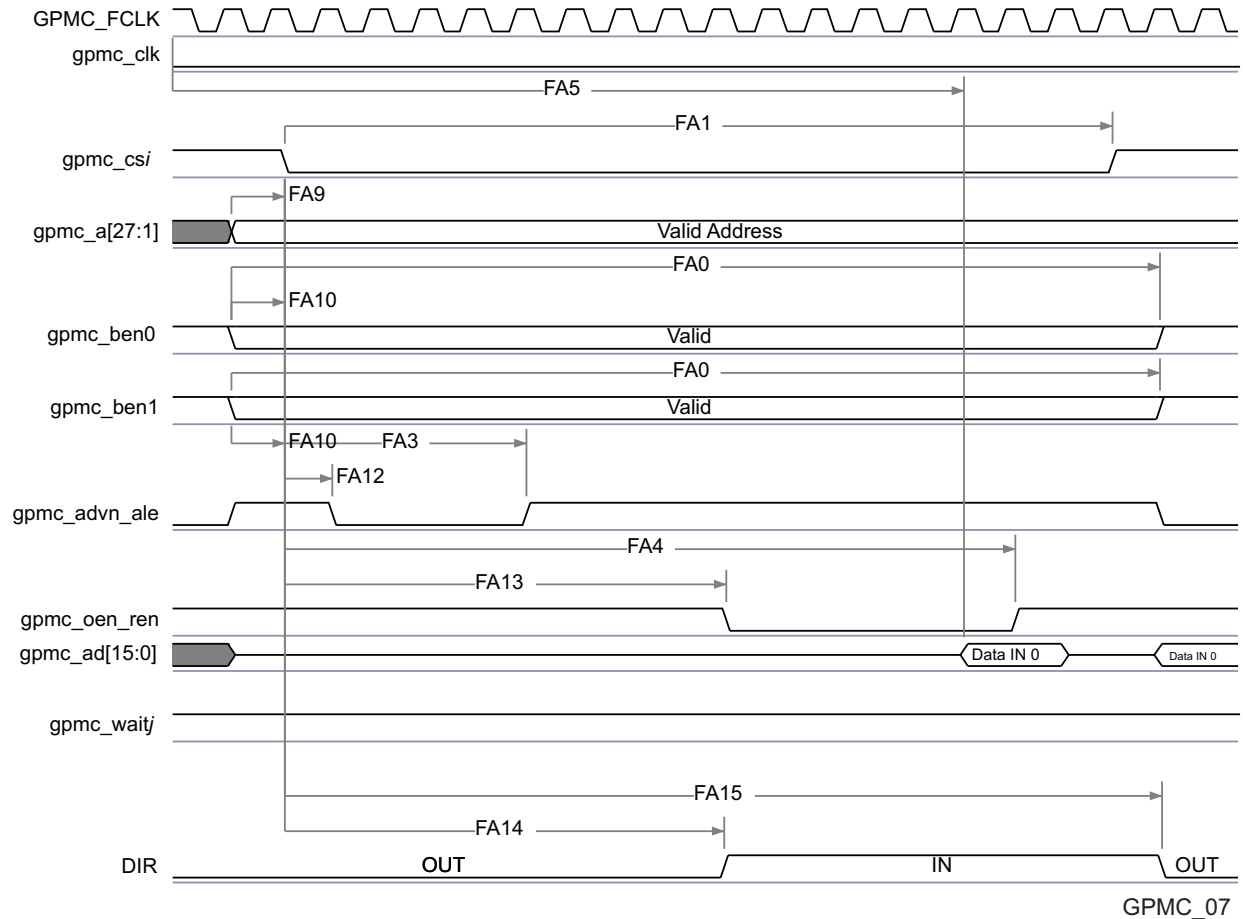
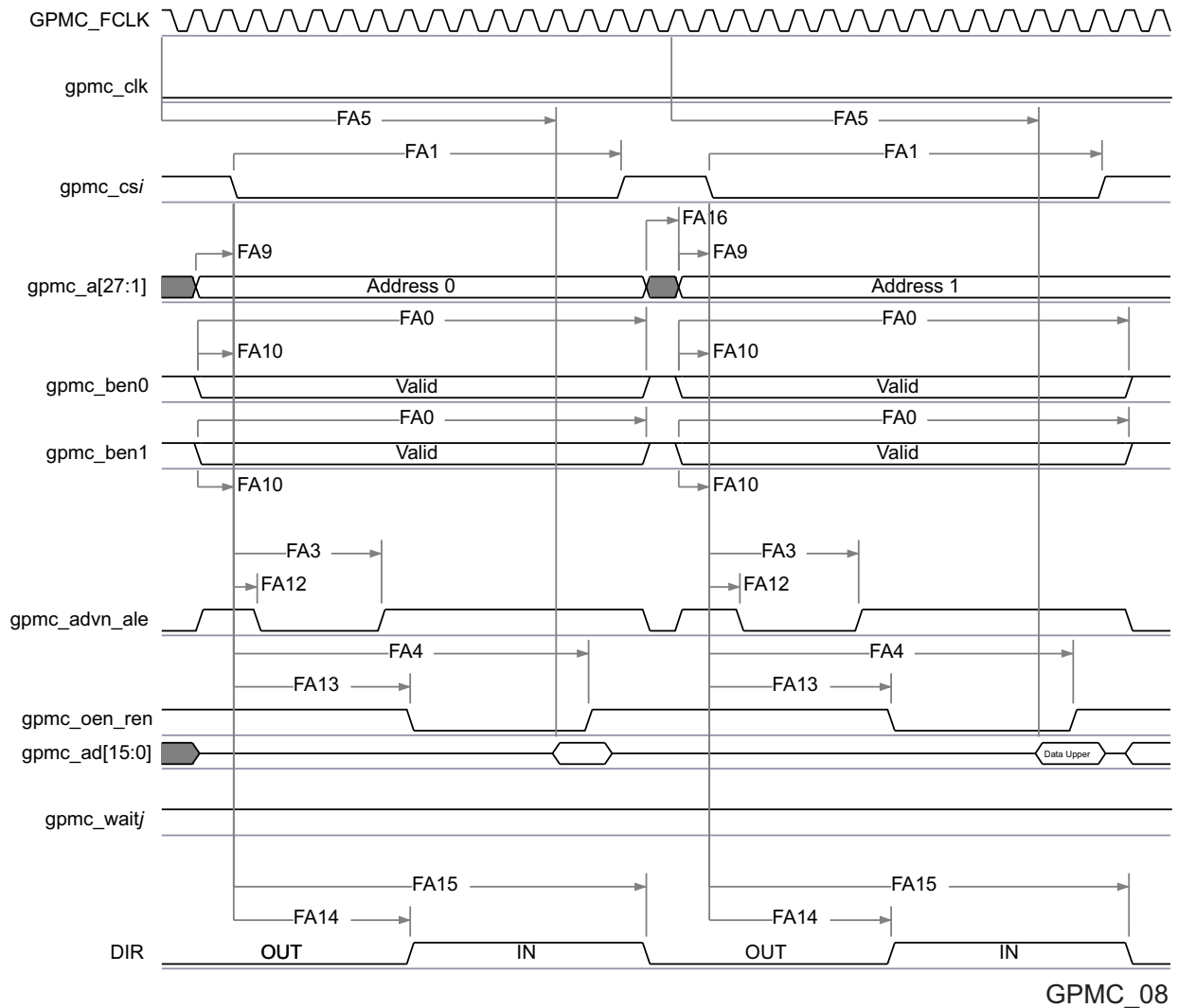


Figure 7-13. GPMC / NOR Flash - Asynchronous Read - Single Word Timing⁽¹⁾⁽²⁾⁽³⁾⁽⁴⁾

- (1) In `gpmc_csi`, $i = 0$ to 7. In `gpmc_waitj`, $j = 0$ to 1.
- (2) FA5 parameter illustrates amount of time required to internally sample input data. It is expressed in number of GPMC functional clock cycles. From start of read cycle and after FA5 functional clock cycles, input Data will be internally sampled by active functional clock edge. FA5 value must be stored inside AccessTime register bits field.
- (3) GPMC_FCLK is an internal clock (GPMC functional clock) not provided externally.
- (4) The "DIR" (direction control) output signal is NOT pinned out on any of the device pads. It is an internal signal only representing a signal direction on the GPMC data bus.



GPMC_08

Figure 7-14. GPMC / NOR Flash - Asynchronous Read - 32-bit Timing⁽¹⁾⁽²⁾⁽³⁾⁽⁴⁾

- (1) In gpmc_csi, i = 0 to 7. In gpmc_waitj, j = 0 to 1.
- (2) FA5 parameter illustrates amount of time required to internally sample input Data. It is expressed in number of GPMC functional clock cycles. From start of read cycle and after FA5 functional clock cycles, input Data will be internally sampled by active functional clock edge. FA5 value should be stored inside AccessTime register bits field.
- (3) GPMC_FCLK is an internal clock (GPMC functional clock) not provided externally.
- (4) The "DIR" (direction control) output signal is NOT pinned out on any of the device pads. It is an internal signal only representing a signal direction on the GPMC data bus.

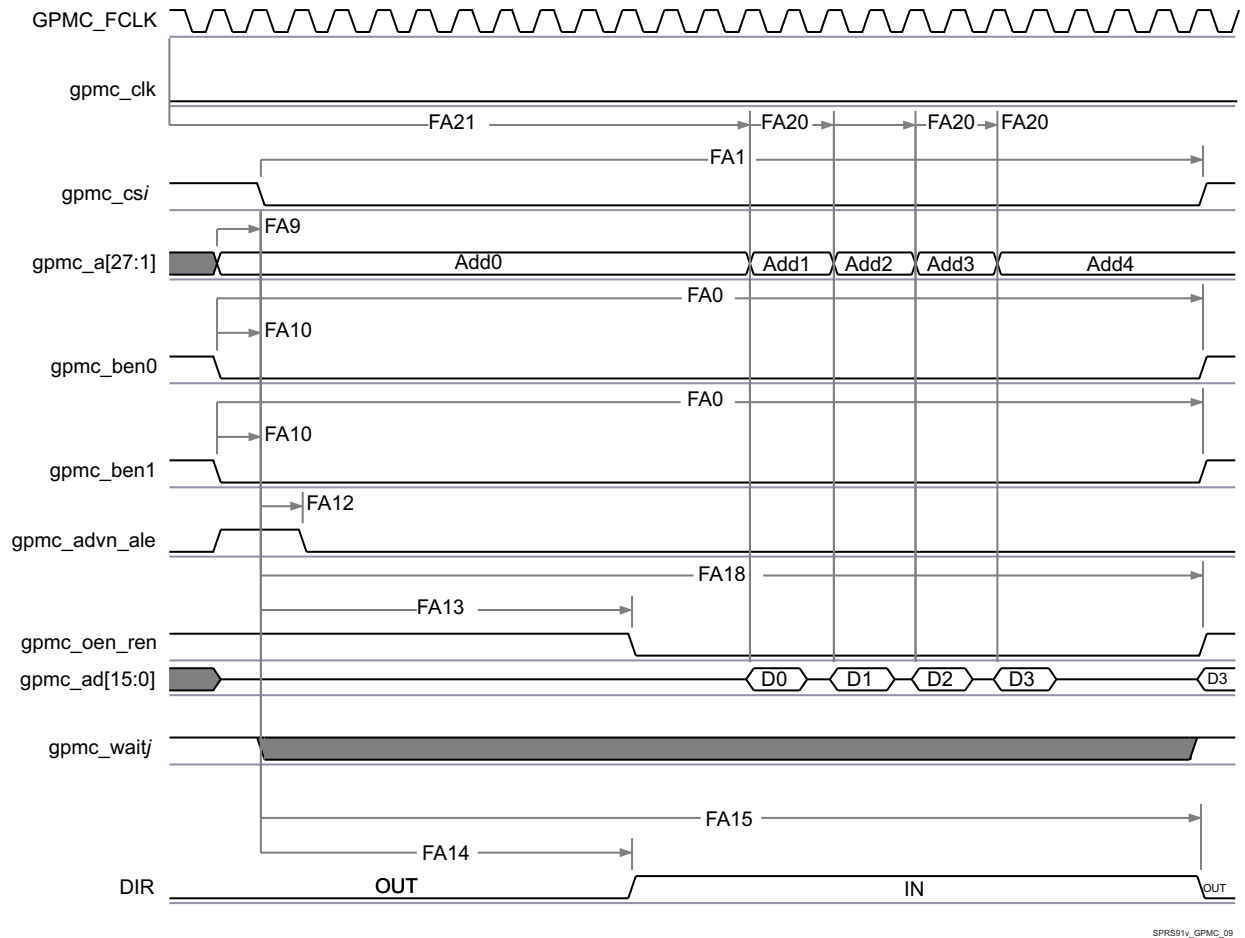


Figure 7-15. GPMC / NOR Flash - Asynchronous Read - Page Mode 4x16-bit Timing ⁽¹⁾⁽²⁾⁽³⁾⁽⁴⁾⁽⁵⁾

- (1) In $gpmc_csi$, $i = 0$ to 7. In $gpmc_waitj$, $j = 0$ to 1.
- (2) FA21 parameter illustrates amount of time required to internally sample first input Page Data. It is expressed in number of GPMC functional clock cycles. From start of read cycle and after FA21 functional clock cycles, First input Page Data will be internally sampled by active functional clock edge. FA21 calculation is detailed in a separated application note and should be stored inside AccessTime register bits field.
- (3) FA20 parameter illustrates amount of time required to internally sample successive input Page Data. It is expressed in number of GPMC functional clock cycles. After each access to input Page Data, next input Page Data will be internally sampled by active functional clock edge after FA20 functional clock cycles. FA20 is also the duration of address phases for successive input Page Data (excluding first input Page Data). FA20 value should be stored in PageBurstAccessTime register bits field.
- (4) GPMC_FCLK is an internal clock (GPMC functional clock) not provided externally.
- (5) The "DIR" (direction control) output signal is NOT pinned out on any of the device pads. It is an internal signal only representing a signal direction on the GPMC data bus.

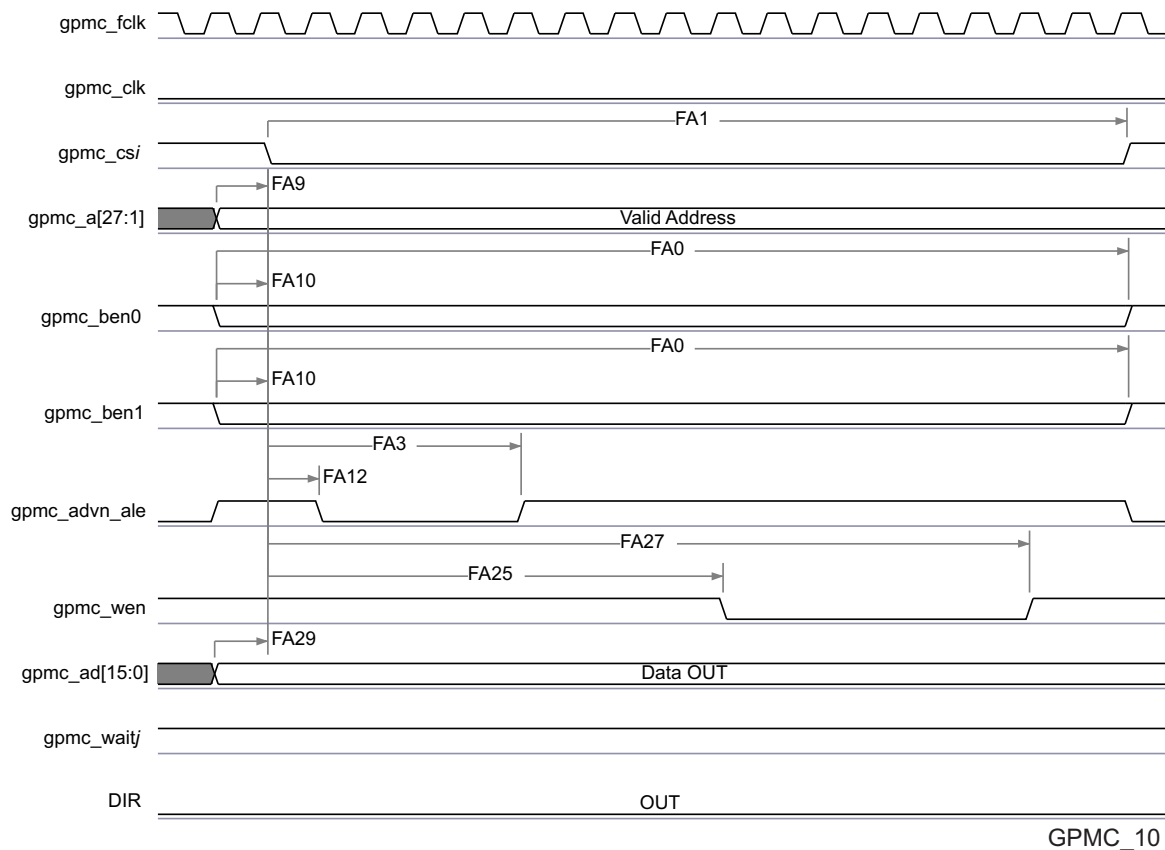


Figure 7-16. GPMC / NOR Flash - Asynchronous Write - Single Word Timing⁽¹⁾⁽²⁾

- (1) In *gpmc_csi*, *i* = 0 to 7. In *gpmc_waitj*, *j* = 0 to 1.
- (2) The "DIR" (direction control) output signal is NOT pinned out on any of the device pads. It is an internal signal only representing a signal direction on the GPMC data bus.

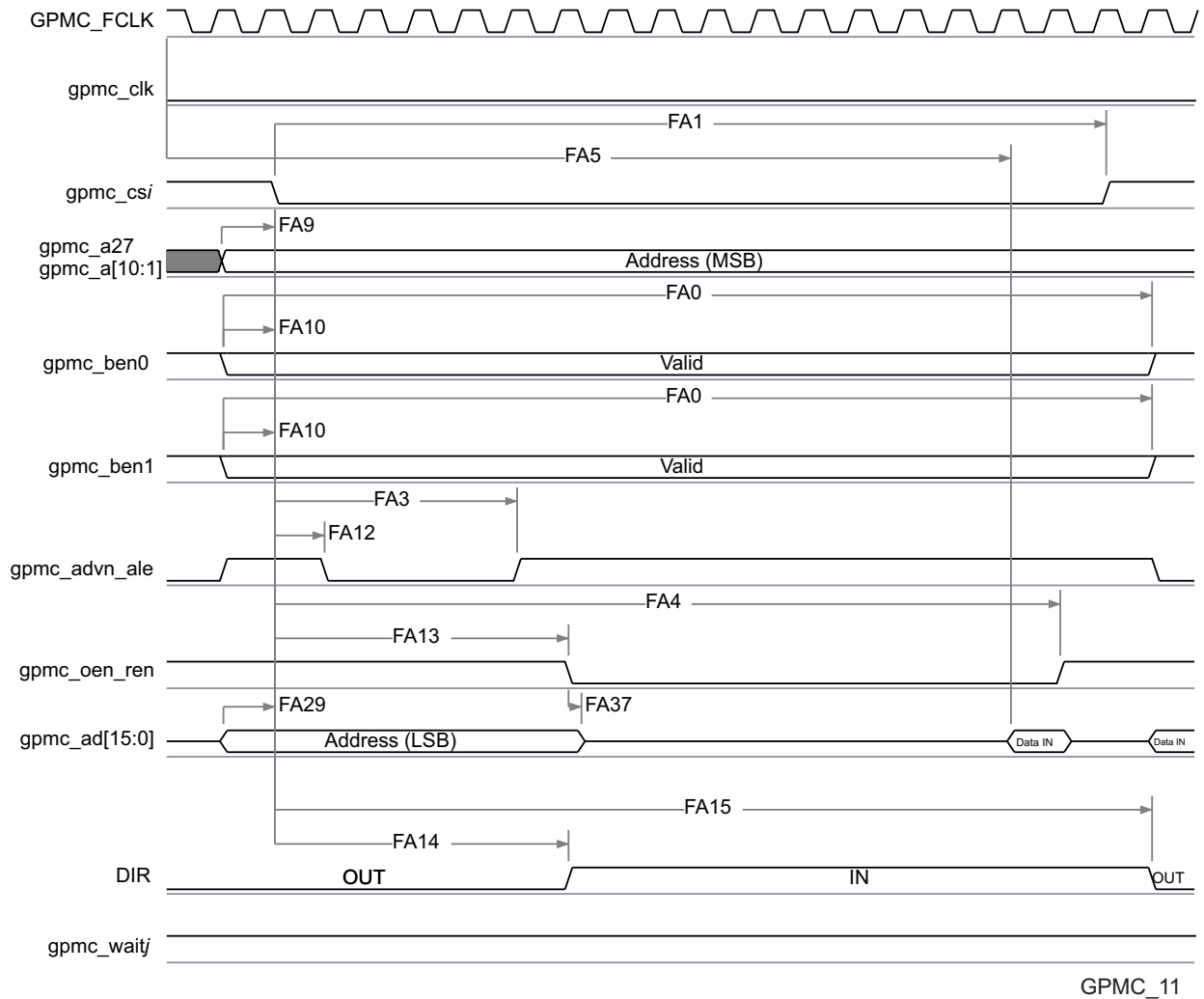


Figure 7-17. GPMC / Multiplexed NOR Flash - Asynchronous Read - Single Word Timing⁽¹⁾⁽²⁾⁽³⁾⁽⁴⁾

- (1) In $gpmc_csi$, $i = 0$ to 7. In $gpmc_waitj$, $j = 0$ to 1
- (2) FA5 parameter illustrates amount of time required to internally sample input Data. It is expressed in number of GPMC functional clock cycles. From start of read cycle and after FA5 functional clock cycles, input Data will be internally sampled by active functional clock edge. FA5 value should be stored inside AccessTime register bits field.
- (3) GPMC_FCLK is an internal clock (GPMC functional clock) not provided externally
- (4) The "DIR" (direction control) output signal is NOT pinned out on any of the device pads. It is an internal signal only representing a signal direction on the GPMC data bus.

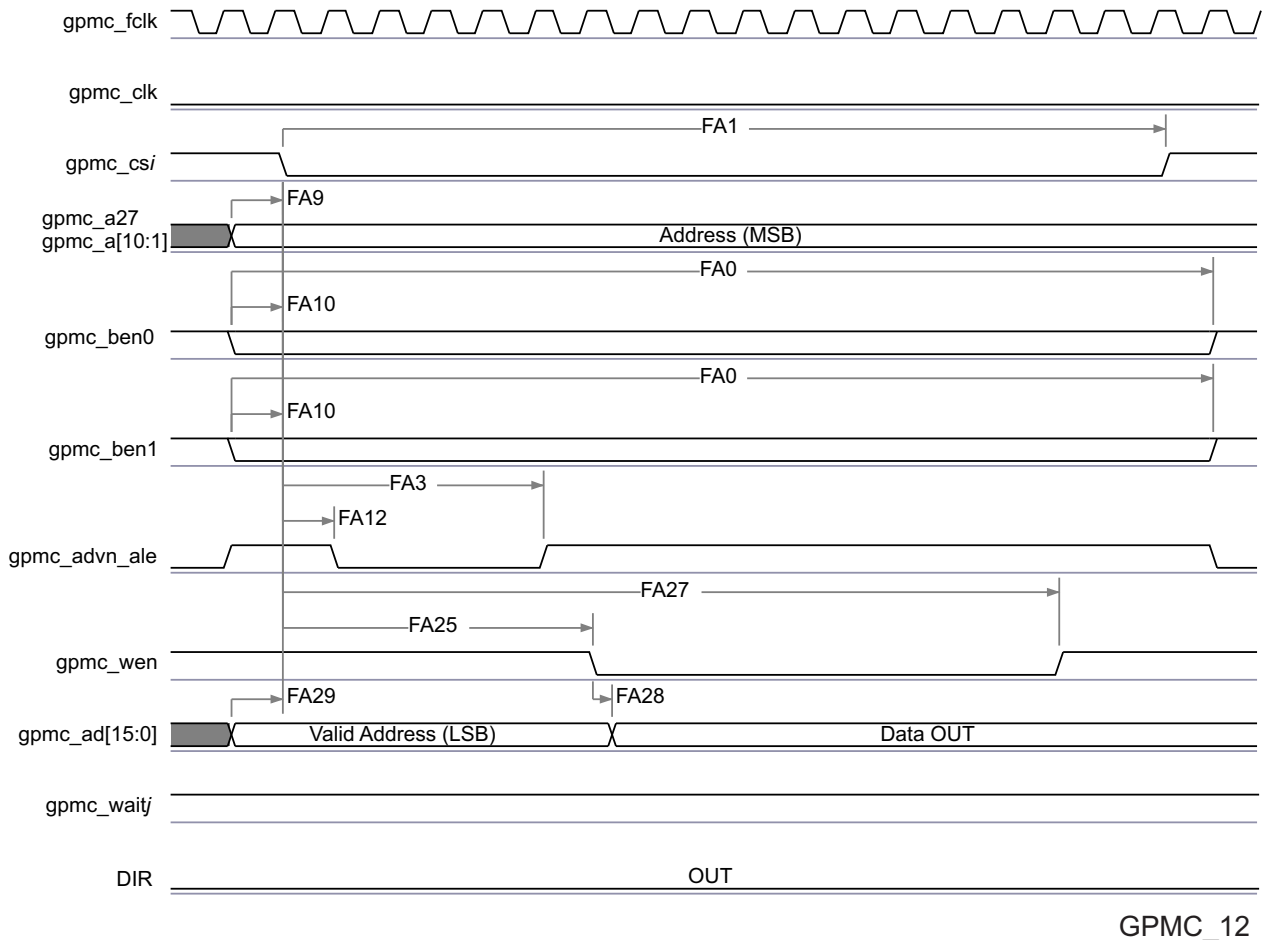


Figure 7-18. GPMC / Multiplexed NOR Flash - Asynchronous Write - Single Word Timing⁽¹⁾⁽²⁾

- (1) In gpmc_csi, i = 0 to 7. In gpmc_waitj, j = 0 to 1.
- (2) The "DIR" (direction control) output signal is NOT pinned out on any of the device pads. It is an internal signal only representing a signal direction on the GPMC data bus.

7.10.3 GPMC/NAND Flash Interface Asynchronous Timing

CAUTION

The IO Timings provided in this section are only valid for some GPMC usage modes when the corresponding Virtual IO Timings or Manual IO Timings are configured as described in the tables found in this section.

Table 7-27 and Table 7-28 assume testing over the recommended operating conditions and electrical characteristic conditions below (see Figure 7-19, Figure 7-20, Figure 7-21 and Figure 7-22).

Table 7-27. GPMC/NAND Flash Interface Timing Requirements

NO.	PARAMETER	DESCRIPTION	MIN	MAX	UNIT
GNF12	$t_{acc}(DAT)$	Data maximum access time (GPMC_FCLK Cycles)		J ⁽¹⁾	cycles
-	$t_{su}(DV-OEH)$	Setup time, read gpmc_ad[15:0] valid before gpmc_oen_ren high	1.9		ns
-	$t_h(OEH-DV)$	Hold time, read gpmc_ad[15:0] valid after gpmc_oen_ren high	1		ns

$$(1) J = \text{AccessTime} * (\text{TimeParaGranularity} + 1)$$

Table 7-28. GPMC/NAND Flash Interface Switching Characteristics

NO.	PARAMETER	DESCRIPTION	MIN	MAX	UNIT
-	$t_{r(\text{DO})}$	Rising time, gpmc_ad[15:0] output data	0.447	4.067	ns
-	$t_{f(\text{DO})}$	Falling time, gpmc_ad[15:0] output data	0.43	4.463	ns
GNF0	$t_{w(\text{nWEV})}$	Pulse duration, gpmc_wen valid time		A ⁽¹⁾	ns
GNF1	$t_{d(\text{nCSV-nWEV})}$	Delay time, gpmc_cs[7:0] valid to gpmc_wen valid	B - 2 ⁽²⁾	B + 4 ⁽²⁾	ns
GNF2	$t_{d(\text{CLEH-nWEV})}$	Delay time, gpmc_ben[1:0] high to gpmc_wen valid	C - 2 ⁽³⁾	C + 4 ⁽³⁾	ns
GNF3	$t_{d(\text{nWEV-DV})}$	Delay time, gpmc_ad[15:0] valid to gpmc_wen valid	D - 2 ⁽⁴⁾	D + 4 ⁽⁴⁾	ns
GNF4	$t_{d(\text{nWEIV-DIV})}$	Delay time, gpmc_wen invalid to gpmc_ad[15:0] invalid	E - 2 ⁽⁵⁾	E + 4 ⁽⁵⁾	ns
GNF5	$t_{d(\text{nWEIV-CLEIV})}$	Delay time, gpmc_wen invalid to gpmc_ben[1:0] invalid	F - 2 ⁽⁶⁾	F + 4 ⁽⁶⁾	ns
GNF6	$t_{d(\text{nWEIV-nCSIV})}$	Delay time, gpmc_wen invalid to gpmc_cs[7:0] invalid	G - 2 ⁽⁷⁾	G + 4 ⁽⁷⁾	ns
GNF7	$t_{d(\text{ALEH-nWEV})}$	Delay time, gpmc_advn_ale high to gpmc_wen valid	C - 2 ⁽³⁾	C + 4 ⁽³⁾	ns
GNF8	$t_{d(\text{nWEIV-ALEIV})}$	Delay time, gpmc_wen invalid to gpmc_advn_ale invalid	F - 2 ⁽⁶⁾	F + 4 ⁽⁶⁾	ns
GNF9	$t_{c(\text{nWE})}$	Cycle time, write cycle time		H ⁽⁸⁾	ns
GNF10	$t_{d(\text{nCSV-nOEV})}$	Delay time, gpmc_cs[7:0] valid to gpmc_oen_ren valid	I - 2 ⁽⁹⁾	I + 4 ⁽⁹⁾	ns
GNF13	$t_{w(\text{nOEV})}$	Pulse duration, gpmc_oen_ren valid time		K ⁽¹⁰⁾	ns
GNF14	$t_{c(\text{nOE})}$	Cycle time, read cycle time		L ⁽¹¹⁾	ns
GNF15	$t_{d(\text{nOEIV-nCSIV})}$	Delay time, gpmc_oen_ren invalid to gpmc_cs[7:0] invalid	M - 2 ⁽¹²⁾	M + 4 ⁽¹²⁾	ns

$$(1) A = (\text{WEOffTime} - \text{WEOnTime}) * (\text{TimeParaGranularity} + 1) * \text{GPMC_FCLK}$$

$$(2) B = ((\text{WEOnTime} - \text{CSONTime}) * (\text{TimeParaGranularity} + 1) + 0.5 * (\text{WEEExtraDelay} - \text{CSEExtraDelay})) * \text{GPMC_FCLK}$$

$$(3) C = ((\text{WEOnTime} - \text{ADVOnTime}) * (\text{TimeParaGranularity} + 1) + 0.5 * (\text{WEEExtraDelay} - \text{ADVExtraDelay})) * \text{GPMC_FCLK}$$

$$(4) D = (\text{WEOnTime} * (\text{TimeParaGranularity} + 1) + 0.5 * \text{WEEExtraDelay}) * \text{GPMC_FCLK}$$

$$(5) E = (\text{WrCycleTime} - \text{WEOffTime} * (\text{TimeParaGranularity} + 1) - 0.5 * \text{WEEExtraDelay}) * \text{GPMC_FCLK}$$

$$(6) F = (\text{ADVWrOffTime} - \text{WEOffTime} * (\text{TimeParaGranularity} + 1) + 0.5 * (\text{ADVExtraDelay} - \text{WEEExtraDelay})) * \text{GPMC_FCLK}$$

$$(7) G = (\text{CSWrOffTime} - \text{WEOffTime} * (\text{TimeParaGranularity} + 1) + 0.5 * (\text{CSEExtraDelay} - \text{WEEExtraDelay})) * \text{GPMC_FCLK}$$

$$(8) H = \text{WrCycleTime} * (1 + \text{TimeParaGranularity}) * \text{GPMC_FCLK}$$

$$(9) I = ((\text{OEOffTime} + (n - 1) * \text{PageBurstAccessTime} - \text{CSONTime}) * (\text{TimeParaGranularity} + 1) + 0.5 * (\text{OEEExtraDelay} - \text{CSEExtraDelay})) * \text{GPMC_FCLK}$$

$$(10) K = (\text{OEOffTime} - \text{OEOnTime}) * (1 + \text{TimeParaGranularity}) * \text{GPMC_FCLK}$$

$$(11) L = \text{RdCycleTime} * (1 + \text{TimeParaGranularity}) * \text{GPMC_FCLK}$$

$$(12) M = (\text{CSRdOffTime} - \text{OEOffTime} * (\text{TimeParaGranularity} + 1) + 0.5 * (\text{CSEExtraDelay} - \text{OEEExtraDelay})) * \text{GPMC_FCLK}$$

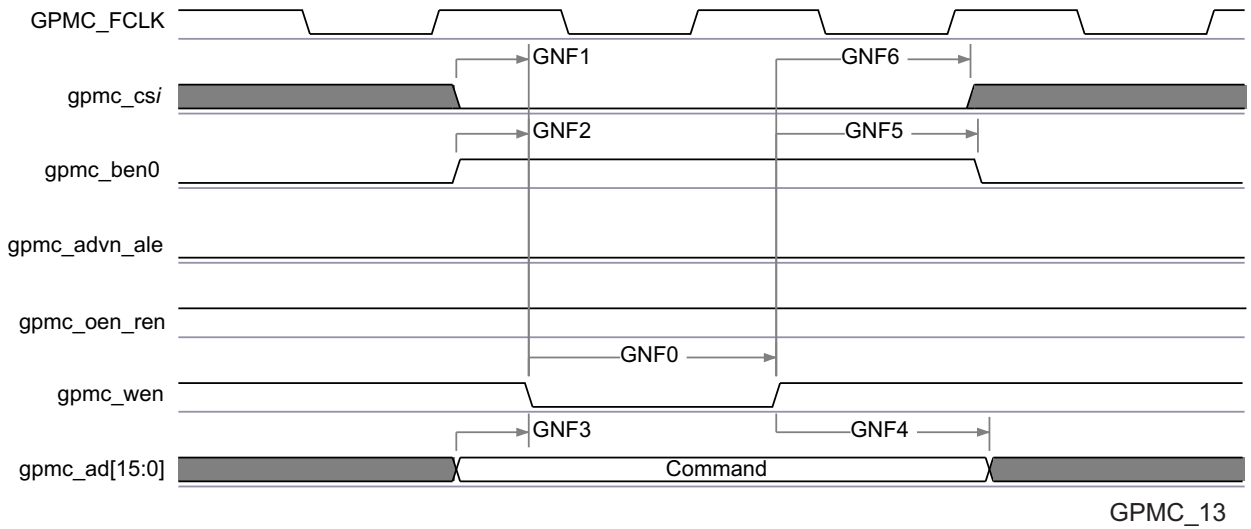


Figure 7-19. GPMC / NAND Flash - Command Latch Cycle Timing⁽¹⁾

(1) In gpmc_csi, i = 0 to 7.

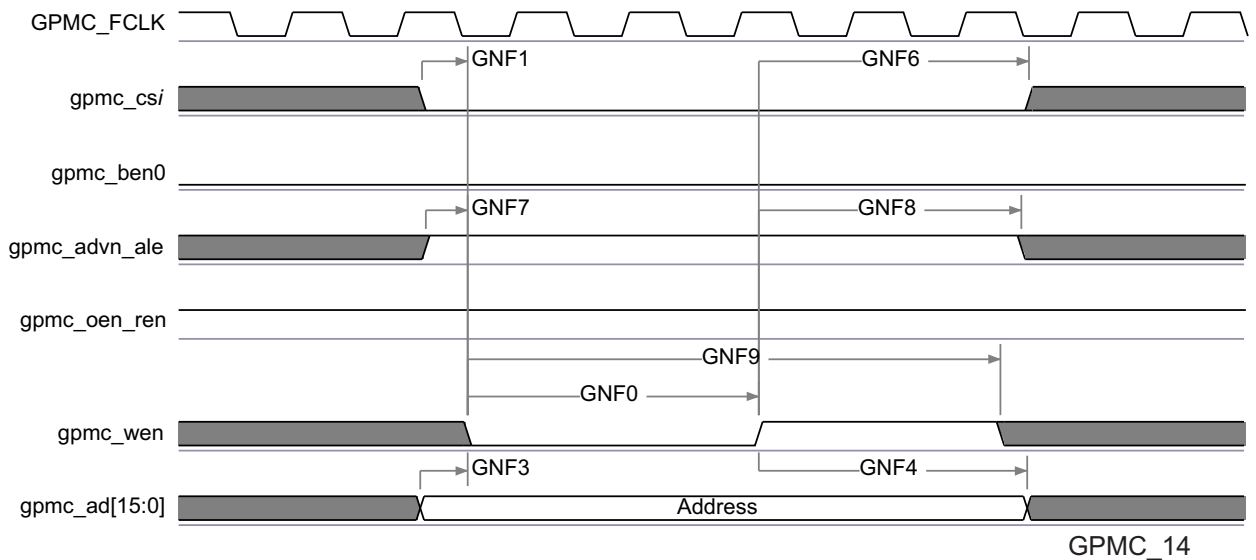


Figure 7-20. GPMC / NAND Flash - Address Latch Cycle Timing⁽¹⁾

(1) In gpmc_csi, i = 0 to 7.

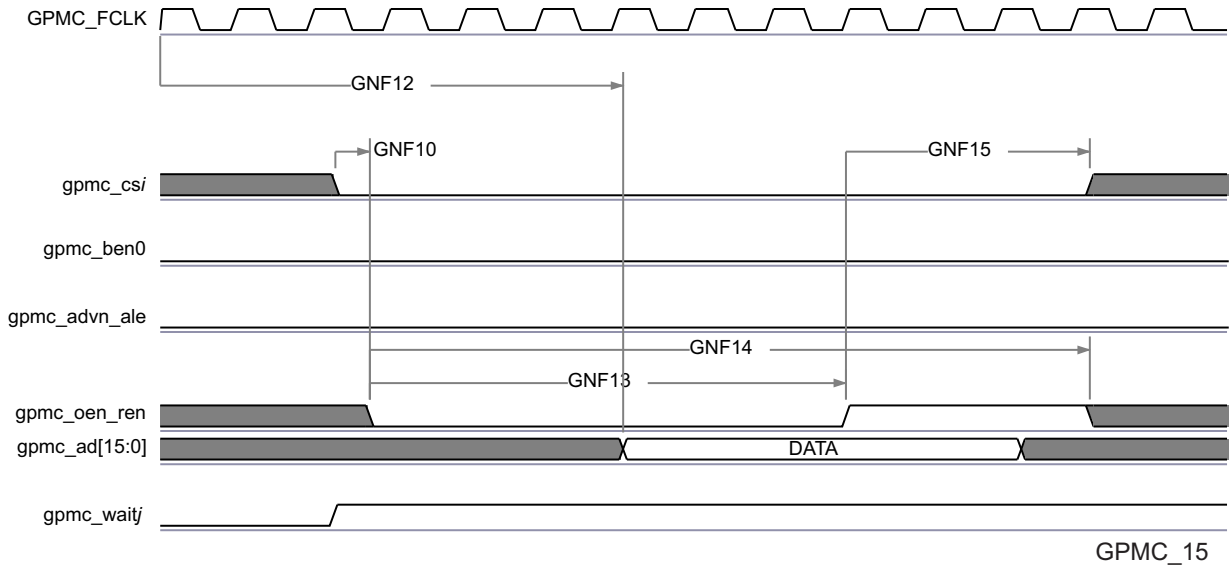


Figure 7-21. GPMC / NAND Flash - Data Read Cycle Timing⁽¹⁾⁽²⁾⁽³⁾

- (1) GNF12 parameter illustrates amount of time required to internally sample input Data. It is expressed in number of GPMC functional clock cycles. From start of read cycle and after GNF12 functional clock cycles, input data will be internally sampled by active functional clock edge. GNF12 value must be stored inside AccessTime register bits field.
- (2) GPMC_FCLK is an internal clock (GPMC functional clock) not provided externally.
- (3) In gpmc_csi, i = 0 to 7. In gpmc_waitj, j = 0 to 1.

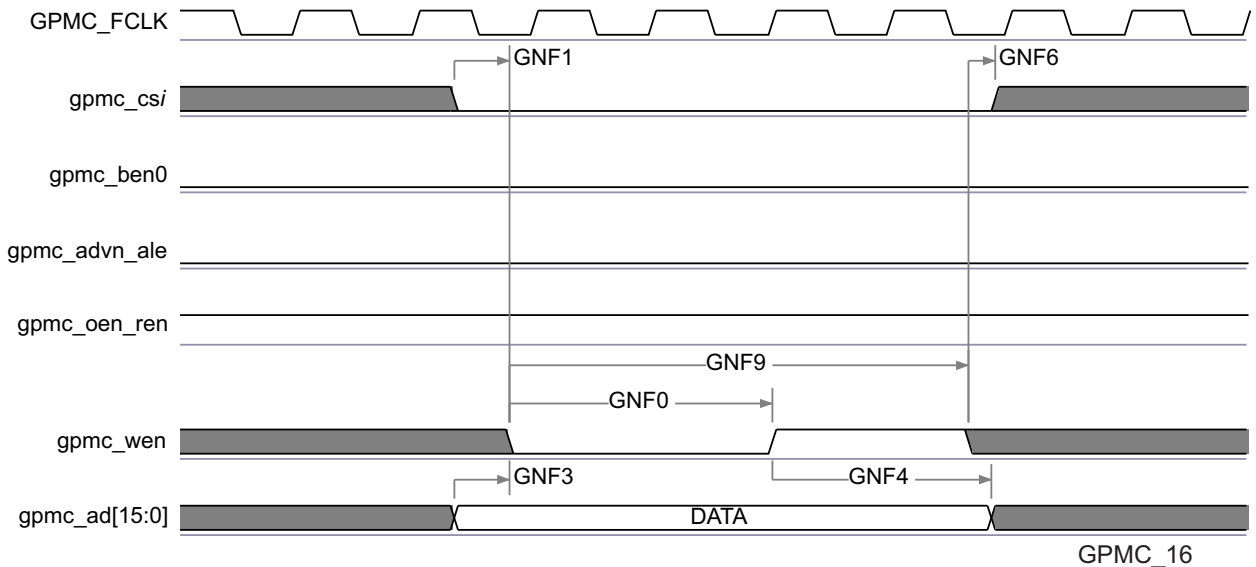


Figure 7-22. GPMC / NAND Flash - Data Write Cycle Timing⁽¹⁾

- (1) In gpmc_csi, i = 0 to 7.

NOTE

To configure the desired virtual mode the user must set MODESELECT bit and DELAYMODE bitfield for each corresponding pad control register.

The pad control registers are presented in [Table 4-3](#) and described in Device TRM, *Chapter 18 - Control Module*.

Virtual IO Timings Modes must be used to guarantee some IO timings for GPMC. See [Table 7-2 Modes Summary](#) for a list of IO timings requiring the use of Virtual IO Timings Modes. See [Table 7-29 Virtual Functions Mapping for GPMC](#) for a definition of the Virtual modes.

[Table 7-29](#) presents the values for DELAYMODE bitfield.

Table 7-29. Virtual Functions Mapping for GPMC

BALL	BALL NAME	Delay Mode Value	MUXMODE[15:0]						
			GPMC_VIRTUAL1	0	1	2	3	5	6
J4	gpmc_ad0	11	gpmc_ad0						
H6	gpmc_ad1	11	gpmc_ad1						
G1	gpmc_ad2	11	gpmc_ad2						
H2	gpmc_ad3	11	gpmc_ad3						
H3	gpmc_ad4	11	gpmc_ad4						
H4	gpmc_ad5	11	gpmc_ad5						
H5	gpmc_ad6	11	gpmc_ad6						
F1	gpmc_ad7	11	gpmc_ad7						
G2	gpmc_ad8	11	gpmc_ad8						
G3	gpmc_ad9	11	gpmc_ad9						
G4	gpmc_ad10	11	gpmc_ad10						
G5	gpmc_ad11	11	gpmc_ad11						
G6	gpmc_ad12	11	gpmc_ad12						
F5	gpmc_ad13	11	gpmc_ad13						
E5	gpmc_ad14	11	gpmc_ad14						
F4	gpmc_ad15	11	gpmc_ad15						
N3	gpmc_a0	11	gpmc_a0						
P3	gpmc_a1	11	gpmc_a1						
P1	gpmc_a2	11	gpmc_a2						
P2	gpmc_a3	10	gpmc_a3						
N2	gpmc_a4	10	gpmc_a4						
N1	gpmc_a5	11	gpmc_a5						
M5	gpmc_a6	11	gpmc_a6						
M4	gpmc_a7	11	gpmc_a7						
M1	gpmc_a8	12	gpmc_a8						
M3	gpmc_a9	12	gpmc_a9						
M6	gpmc_a10	12	gpmc_a10						
N5	gpmc_a11	11	gpmc_a11						

Table 7-29. Virtual Functions Mapping for GPMC (continued)

BALL	BALL NAME	Delay Mode Value	MUXMODE[15:0]						
			GPMC_VIRTUAL1	0	1	2	3	5	6
L5	gpmc_a12	13	gpmc_a12					gpmc_a0	
L4	gpmc_a13	12	gpmc_a13						
L3	gpmc_a14	12	gpmc_a14						
L2	gpmc_a15	12	gpmc_a15						
L1	gpmc_a16	12	gpmc_a16						
K6	gpmc_a17	12	gpmc_a17						
K5	gpmc_a18	12	gpmc_a18						
C2	gpmc_a19	11	gpmc_a19			gpmc_a13			
D3	gpmc_a20	11	gpmc_a20			gpmc_a14			
D2	gpmc_a21	11	gpmc_a21			gpmc_a15			
D1	gpmc_a22	11	gpmc_a22			gpmc_a16			
E1	gpmc_a23	11	gpmc_a23			gpmc_a17			
E2	gpmc_a24	11	gpmc_a24			gpmc_a18			
E3	gpmc_a25	11	gpmc_a25			gpmc_a19			
E4	gpmc_a26	11	gpmc_a26			gpmc_a20			
F3	gpmc_a27	11	gpmc_a27			gpmc_a21			
C1	gpmc_cs1	11	gpmc_cs1			gpmc_a22			
K4	gpmc_cs0	14	gpmc_cs0						
K3	gpmc_cs2	12	gpmc_cs2						
K2	gpmc_cs3	10	gpmc_cs3					gpmc_a1	
N6	gpmc_clk	12	gpmc_clk	gpmc_cs7			gpmc_wait1		
J5	gpmc_advn_ale	13	gpmc_advn_ale	gpmc_cs6			gpmc_wait1	gpmc_a2	gpmc_a23
H1	gpmc_oen_ren	14	gpmc_oen_ren						
F2	gpmc_wen	14	gpmc_wen						
M2	gpmc_ben0	11	gpmc_ben0	gpmc_cs4					
J3	gpmc_ben1	11	gpmc_ben1	gpmc_cs5				gpmc_a3	
K1	gpmc_wait0	14	gpmc_wait0						
AA4	vin1a_d11	9						gpmc_a23	
AD3	vin1a_d12	9						gpmc_a24	
AC3	vin1a_d13	9						gpmc_a25	
AD2	vin1a_d14	9						gpmc_a26	
AB3	vin1a_d15	9						gpmc_a27	

7.11 Timers

The device has 16 general-purpose (GP) timers (TIMER1 - TIMER16), two watchdog timers, and a 32-kHz synchronized timer (COUNTER_32K) that have the following features:

- Dedicated input trigger for capture mode and dedicated output trigger/pulse width modulation (PWM) signal
- Interrupts generated on overflow, compare, and capture
- Free-running 32-bit upward counter
- Supported modes:
 - Compare and capture modes
 - Auto-reload mode
 - Start-stop mode
- On-the-fly read/write register (while counting)

The device has two system watchdog timer (WD_TIMER1 and WD_TIMER2) that have the following features:

- Free-running 32-bit upward counter
- On-the-fly read/write register (while counting)
- Reset upon occurrence of a timer overflow condition

The device includes one instance of the 32-bit watchdog timer: WD_TIMER2, also called the MPU watchdog timer.

The watchdog timer is used to provide a recovery mechanism for the device in the event of a fault condition, such as a non-exiting code loop.

NOTE

For additional information on the Timer Module, see the Device TRM.

7.12 Inter-Integrated Circuit Interface (I2C)

The device includes 5 inter-integrated circuit (I2C) modules which provide an interface to other devices compliant with Philips Semiconductors Inter-IC bus (I2C-bus™) specification version 2.1. External components attached to this 2-wire serial bus can transmit/receive 8-bit data to/from the device through the I2C module.

NOTE

Note that, on I2C1 and I2C2, due to characteristics of the open drain IO cells, HS mode is not supported.

NOTE

Inter-integrated circuit i ($i=1$ to 5) module is also referred to as I2Ci.

NOTE

For more information, see the Multimaster High-Speed I2C Controller section of the Device TRM.

[Table 7-30](#), [Table 7-31](#) and [Figure 7-23](#) assume testing over the recommended operating conditions and electrical characteristic conditions below.

Table 7-30. Timing Requirements for I2C Input Timings⁽¹⁾

NO.	PARAMETER	DESCRIPTION	STANDARD MODE		FAST MODE		UNIT
			MIN	MAX	MIN	MAX	
1	$t_{c(SCL)}$	Cycle time, SCL	10		2.5		μ s
2	$t_{su(SCLH-SDAL)}$	Setup time, SCL high before SDA low (for a repeated START condition)	4.7		0.6		μ s
3	$t_{h(SDAL-SCLL)}$	Hold time, SCL low after SDA low (for a START and a repeated START condition)	4		0.6		μ s
4	$t_{w(SCLL)}$	Pulse duration, SCL low	4.7		1.3		μ s
5	$t_{w(SCLH)}$	Pulse duration, SCL high	4		0.6		μ s
6	$t_{su(SDAV-SCLH)}$	Setup time, SDA valid before SCL high	250		100 ⁽²⁾		ns
7	$t_{h(SCLL-SDAV)}$	Hold time, SDA valid after SCL low	0 ⁽³⁾	3.45 ⁽⁴⁾	0 ⁽³⁾	0.9 ⁽⁴⁾	μ s
8	$t_{w(SDAH)}$	Pulse duration, SDA high between STOP and START conditions	4.7		1.3		μ s
9	$t_{r(SDA)}$	Rise time, SDA		1000	$20 + 0.1C_b$ ⁽⁵⁾	300 ⁽³⁾	ns
10	$t_{r(SCL)}$	Rise time, SCL		1000	$20 + 0.1C_b$ ⁽⁵⁾	300 ⁽³⁾	ns
11	$t_{f(SDA)}$	Fall time, SDA		300	$20 + 0.1C_b$ ⁽⁵⁾	300 ⁽³⁾	ns
12	$t_{f(SCL)}$	Fall time, SCL		300	$20 + 0.1C_b$ ⁽⁵⁾	300 ⁽³⁾	ns
13	$t_{su(SCLH-SDAH)}$	Setup time, SCL high before SDA high (for STOP condition)	4		0.6		μ s
14	$t_{w(SP)}$	Pulse duration, spike (must be suppressed)			0	50	ns
15	C_b ⁽⁵⁾	Capacitive load for each bus line		400		400	pF

- (1) The I2C pins SDA and SCL do not feature fail-safe I/O buffers. These pins could potentially draw current when the device is powered down.
- (2) A Fast-mode I²C-bus™ device can be used in a Standard-mode I²C-bus system, but the requirement $t_{su(SDA-SCLH)} \geq 250$ ns must then be met. This will automatically be the case if the device does not stretch the LOW period of the SCL signal. If such a device does stretch the LOW period of the SCL signal, it must output the next data bit to the SDA line $t_r \max + t_{su(SDA-SCLH)} = 1000 + 250 = 1250$ ns (according to the Standard-mode I²C-Bus Specification) before the SCL line is released.
- (3) A device must internally provide a hold time of at least 300 ns for the SDA signal (referred to the V_{IHmin} of the SCL signal) to bridge the undefined region of the falling edge of SCL.
- (4) The maximum $t_{h(SDA-SCLL)}$ has only to be met if the device does not stretch the low period [$t_{w(SCLL)}$] of the SCL signal.
- (5) C_b = total capacitance of one bus line in pF. If mixed with HS-mode devices, faster fall-times are allowed.

Table 7-31. Timing Requirements for I²C HS-Mode (I²C3/4/5 Only)⁽¹⁾

NO.	PARAMETER	DESCRIPTION	$C_b = 100$ pF MAX		$C_b = 400$ pF ⁽²⁾		UNIT
			MIN	MAX	MIN	MAX	
1	$t_{c(SCL)}$	Cycle time, SCL	0.294		0.588		μ s
2	$t_{su(SCLH-SDAL)}$	Set-up time, SCL high before SDA low (for a repeated START condition)	160		160		ns
3	$t_{h(SDAL-SCLL)}$	Hold time, SCL low after SDA low (for a repeated START condition)	160		160		ns
4	$t_{w(SCLL)}$	LOW period of the SCLH clock	160		320		ns
5	$t_{w(SCLH)}$	HIGH period of the SCLH clock	60		120		ns
6	$t_{su(SDAV-SCLH)}$	Setup time, SDA valid before SCL high	10		10		ns
7	$t_{h(SCLL-SDAV)}$	Hold time, SDA valid after SCL low	0 ⁽³⁾	70	0 ⁽³⁾	150	ns
13	$t_{su(SCLH-SDAH)}$	Setup time, SCL high before SDA high (for a STOP condition)	160		160		ns

Table 7-31. Timing Requirements for I²C HS-Mode (I²C3/4/5 Only)⁽¹⁾ (continued)

NO.	PARAMETER	DESCRIPTION	C _b = 100 pF MAX		C _b = 400 pF ⁽²⁾		UNIT
			MIN	MAX	MIN	MAX	
14	t _{w(SP)}	Pulse duration, spike (must be suppressed)	0	10	0	10	ns
15	C _b ⁽²⁾	Capacitive load for SDAH and SCLH lines		100		400	pF
16	C _b	Capacitive load for SDAH + SDA line and SCLH + SCL line		400		400	pF

(1) I²C HS-Mode is only supported on I²C3/4/5. I²C HS-Mode is not supported on I²C1/2.

(2) For bus line loads C_b between 100 and 400 pF the timing parameters must be linearly interpolated.

(3) A device must internally provide a Data hold time to bridge the undefined part between V_{IH} and V_{IL} of the falling edge of the SCLH signal. An input circuit with a threshold as low as possible for the falling edge of the SCLH signal minimizes this hold time.

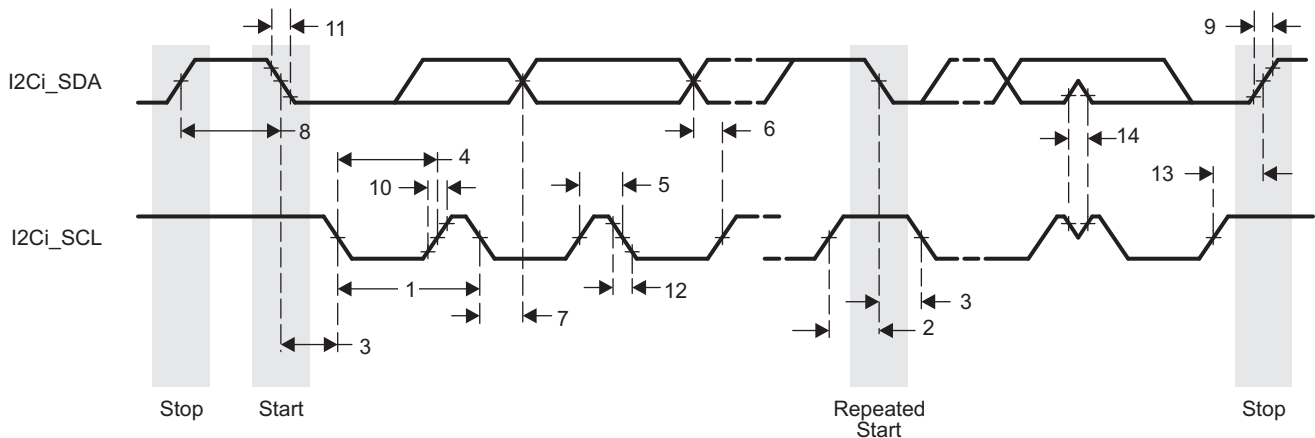


Figure 7-23. I2C Receive Timing

Table 7-32 and Figure 7-24 assume testing over the recommended operating conditions and electrical characteristic conditions below.

Table 7-32. Switching Characteristics Over Recommended Operating Conditions for I2C Output Timings⁽²⁾

NO.	PARAMETER	DESCRIPTION	STANDARD MODE		FAST MODE		UNIT
			MIN	MAX	MIN	MAX	
16	t _{c(SCL)}	Cycle time, SCL	10		2.5		μs
17	t _{su(SCLH-SDAL)}	Setup time, SCL high before SDA low (for a repeated START condition)	4.7		0.6		μs
18	t _{h(SDAL-SCLL)}	Hold time, SCL low after SDA low (for a START and a repeated START condition)	4		0.6		μs
19	t _{w(SCLL)}	Pulse duration, SCL low	4.7		1.3		μs
20	t _{w(SCLH)}	Pulse duration, SCL high	4		0.6		μs
21	t _{su(SDAV-SCLH)}	Setup time, SDA valid before SCL high	250		100		ns
22	t _{h(SCLL-SDAV)}	Hold time, SDA valid after SCL low (for I2C bus devices)	0	3.45	0	0.9	μs
23	t _{w(SDAH)}	Pulse duration, SDA high between STOP and START conditions	4.7		1.3		μs
24	t _{r(SDA)}	Rise time, SDA		1000	20 + 0.1C _b (1) (3)	300 ⁽³⁾	ns
25	t _{r(SCL)}	Rise time, SCL		1000	20 + 0.1C _b (1) (3)	300 ⁽³⁾	ns
26	t _{f(SDA)}	Fall time, SDA		300	20 + 0.1C _b (1) (3)	300 ⁽³⁾	ns

Table 7-32. Switching Characteristics Over Recommended Operating Conditions for I2C Output Timings⁽²⁾ (continued)

NO.	PARAMETER	DESCRIPTION	STANDARD MODE		FAST MODE		UNIT
			MIN	MAX	MIN	MAX	
27	$t_f(\text{SCL})$	Fall time, SCL		300	$20 + 0.1C_b$ (1) (3)	$300^{(3)}$	ns
28	$t_{su}(\text{SCLH-SDAH})$	Setup time, SCL high before SDA high (for STOP condition)	4		0.6		μs
29	C_p	Capacitance for each I2C pin		10		10	pF

(1) C_b = total capacitance of one bus line in pF. If mixed with HS-mode devices, faster fall-times are allowed.

(2) Software must properly configure the I2C module registers to achieve the timings shown in this table. See the Device TRM for details.

(3) These timings apply only to I2C1 and I2C2. I2C3, I2C4, and I2C5 use standard LVCMOS buffers to emulate open-drain buffers and their rise/fall times should be referenced in the device IBIS model.

NOTE

I2C emulation is achieved by configuring the LVCMOS buffers to output Hi-Z instead of driving high when transmitting logic-1.

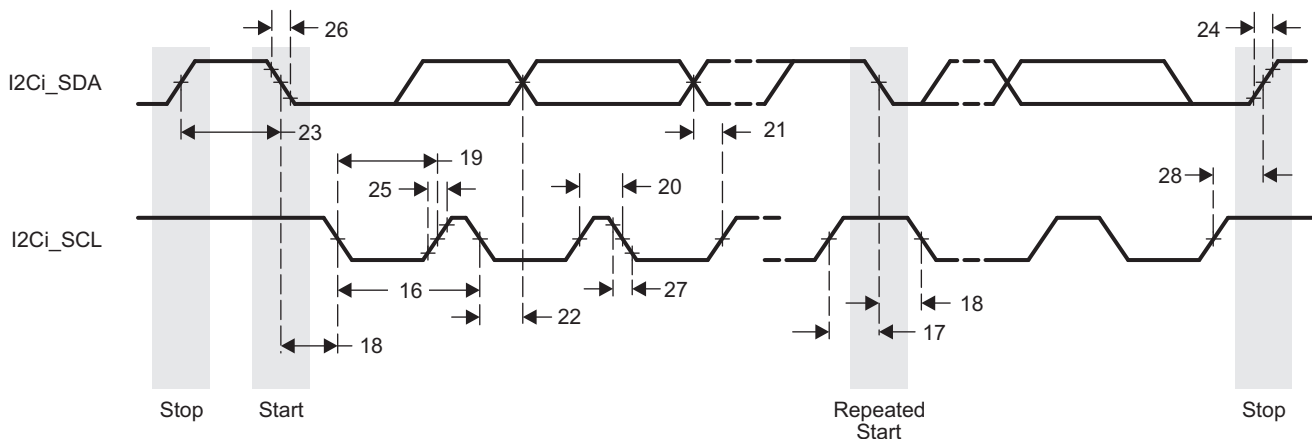


Figure 7-24. I2C Transmit Timing

7.13 Universal Asynchronous Receiver Transmitter (UART)

The UART performs serial-to-parallel conversions on data received from a peripheral device and parallel-to-serial conversion on data received from the CPU. There are 10 UART modules in the device. Only one UART supports IrDA features. Each UART can be used for configuration and data exchange with a number of external peripheral devices or interprocessor communication between devices

The UART_i (where $i = 1$ to 10) include the following features:

- 16C750 compatibility
- 64-byte FIFO buffer for receiver and 64-byte FIFO for transmitter
- Baud generation based on programmable divisors N (where $N = 1 \dots 16\,384$) operating from a fixed functional clock of 48 MHz or 192 MHz
- Break character detection and generation
- Configurable data format:
 - Data bit: 5, 6, 7, or 8 bits
 - Parity bit: Even, odd, none
 - Stop-bit: 1, 1.5, 2 bit(s)
- Flow control: Hardware (RTS/CTS) or software (XON/XOFF)
- Only UART1 module has extended modem control signals (CD, RI, DTR, DSR)

- Only UART3 supports IrDA

NOTE

For more information, see the UART section of the Device TRM.

Table 7-33, Table 7-34 and Figure 7-25 assume testing over the recommended operating conditions and electrical characteristic conditions below.

Table 7-33. Timing Requirements for UART

NO.	PARAMETER	DESCRIPTION	MIN	MAX	UNIT
4	$t_{w(RX)}$	Pulse width, receive data bit, 15/30/100pF high or low	$0.96U^{(1)}$	$1.05U^{(1)}$	ns
5	$t_{w(CTS)}$	Pulse width, receive start bit, 15/30/100pF high or low	$0.96U^{(1)}$	$1.05U^{(1)}$	ns
	$t_d(RTS-TX)$	Delay time, transmit start bit to transmit data	$P^{(2)}$		ns
	$t_d(CTS-TX)$	Delay time, receive start bit to transmit data	$P^{(2)}$		ns

(1) U = UART baud time = 1/programmed baud rate

(2) P = Clock period of the reference clock (FCLK, usually 48 MHz or 192MHz).

Table 7-34. Switching Characteristics Over Recommended Operating Conditions for UART

NO.	PARAMETER	DESCRIPTION	MIN	MAX	UNIT
	$f_{(baud)}$	Maximum programmable baud rate	15 pF	12	MHz
			30 pF	0.23	
			100 pF	0.115	
2	$t_{w(TX)}$	Pulse width, transmit data bit, 15/30/100 pF high or low	$U - 2^{(1)}$	$U + 2^{(1)}$	ns
3	$t_{w(RTS)}$	Pulse width, transmit start bit, 15/30/100 pF high or low	$U - 2^{(1)}$	$U + 2^{(1)}$	ns

(1) U = UART baud time = 1/programmed baud rate

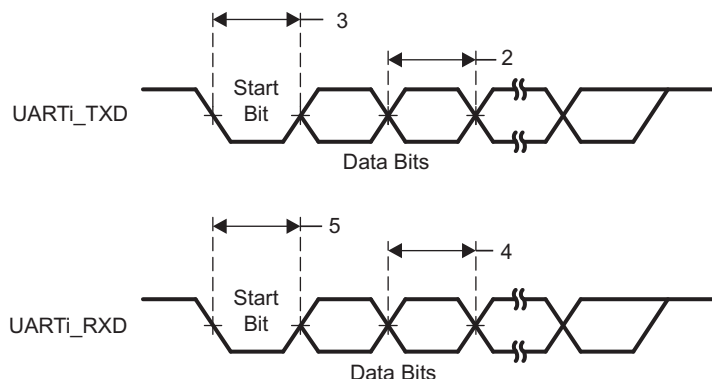


Figure 7-25. UART Timing

7.14 Multichannel Serial Peripheral Interface (McSPI)

The McSPI is a master/slave synchronous serial bus. There are four separate McSPI modules (SPI1, SPI2, SPI3, and SPI4) in the device. All these four modules support up to four external devices (four chip selects) and are able to work as both master and slave.

The McSPI modules include the following main features:

- Serial clock with programmable frequency, polarity, and phase for each channel
- Wide selection of SPI word lengths, ranging from 4 to 32 bits
- Up to four master channels, or single channel in slave mode

- Master multichannel mode:
 - Full duplex/half duplex
 - Transmit-only/receive-only/transmit-and-receive modes
 - Flexible input/output (I/O) port controls per channel
 - Programmable clock granularity
 - SPI configuration per channel. This means, clock definition, polarity enabling and word width
- Power management through wake-up capabilities
- Programmable timing control between chip select and external clock generation
- Built-in FIFO available for a single channel.
- Each SPI module supports multiple chip select pins `spim_cs[i]`, where $i = 1$ to 4.

NOTE

For more information, see the Serial Communication Interface section of the device TRM.

NOTE

The McSPI m module ($m = 1$ to 4) is also referred to as SPI m .

CAUTION

The IO timings provided in this section are applicable for all combinations of signals for SPI1 and SPI2. However, the timings are only valid for SPI3 and SPI4 if signals within a single IOSET are used. The IOSETS are defined in the [Table 7-37](#).

[Table 7-35](#), [Figure 7-26](#) and [Figure 7-27](#) present Timing Requirements for McSPI - Master Mode.

Table 7-35. Timing Requirements for SPI - Master Mode ⁽¹⁾⁽⁸⁾

NO.	PARAMETER	DESCRIPTION	MODE	MIN	MAX	UNIT
SM1	$t_c(\text{SPICLK})$	Cycle time, <code>spi_sclk</code> ⁽¹⁾ ⁽²⁾	SPI1/2/3/4	20.8 ⁽³⁾		ns
SM2	$t_w(\text{SPICLK})$	Typical Pulse duration, <code>spi_sclk</code> low ⁽¹⁾		0.5*P-1 ⁽⁴⁾		ns
SM3	$t_w(\text{SPICLK})$	Typical Pulse duration, <code>spi_sclk</code> high ⁽¹⁾		0.5*P-1 ⁽⁴⁾		ns
SM4	$t_{su}(\text{MISO-SPICLK})$	Setup time, <code>spi_d[x]</code> valid before <code>spi_sclk</code> active edge ⁽¹⁾		4.4		ns
SM5	$t_h(\text{SPICLK-MISO})$	Hold time, <code>spi_d[x]</code> valid after <code>spi_sclk</code> active edge ⁽¹⁾		3.9		ns
SM6	$t_d(\text{SPICLK-SIMO})$	Delay time, <code>spi_sclk</code> active edge to <code>spi_d[x]</code> transition ⁽¹⁾	SPI1	-4.27	4.27	ns
			SPI2	-4.32	4.32	ns
			SPI3	-5.37	4.23	ns
			SPI4	-3.81	4.41	ns
SM7	$t_d(\text{CS-SIMO})$	Delay time, <code>spi_cs[x]</code> active edge to <code>spi_d[x]</code> transition			5	ns
SM8	$t_d(\text{CS-SPICLK})$	Delay time, <code>spi_cs[x]</code> active to <code>spi_sclk</code> first edge ⁽¹⁾	MASTER_PHA0 ⁽⁵⁾	B-4.6 ⁽⁶⁾		ns
			MASTER_PHA1 ⁽⁵⁾	A-4.6 ⁽⁷⁾		ns
SM9	$t_d(\text{SPICLK-CS})$	Delay time, <code>spi_sclk</code> last edge to <code>spi_cs[x]</code> inactive ⁽¹⁾	MASTER_PHA0 ⁽⁵⁾	A-4.6 ⁽⁷⁾		ns
			MASTER_PHA1 ⁽⁵⁾	B-4.6 ⁽⁶⁾		ns

- (1) This timing applies to all configurations regardless of SPI_CLK polarity and which clock edges are used to drive output data and capture input data.
- (2) Related to the SPI_CLK maximum frequency.
- (3) 20.8ns cycle time = 48MHz, 26ns cycle time = 38.4MHz
- (4) P = SPICLK period.
- (5) SPI_CLK phase is programmable with the PHA bit of the SPI_CH(i)CONF register.
- (6) $B = (TCS + 0.5) * TSPICLKREF * Fratio$, where TCS is a bit field of the SPI_CH(i)CONF register and Fratio = Even ≥ 2 .
- (7) When P = 20.8 ns, $A = (TCS + 1) * TSPICLKREF$, where TCS is a bit field of the SPI_CH(i)CONF register. When P > 20.8 ns, $A = (TCS + 0.5) * Fratio * TSPICLKREF$, where TCS is a bit field of the SPI_CH(i)CONF register.
- (8) The IO timings provided in this section are applicable for all combinations of signals for SPI1 and SPI2. However, the timings are only valid for SPI3 and SPI4 if signals within a single IOSET are used. The IOSETs are defined in the following tables.

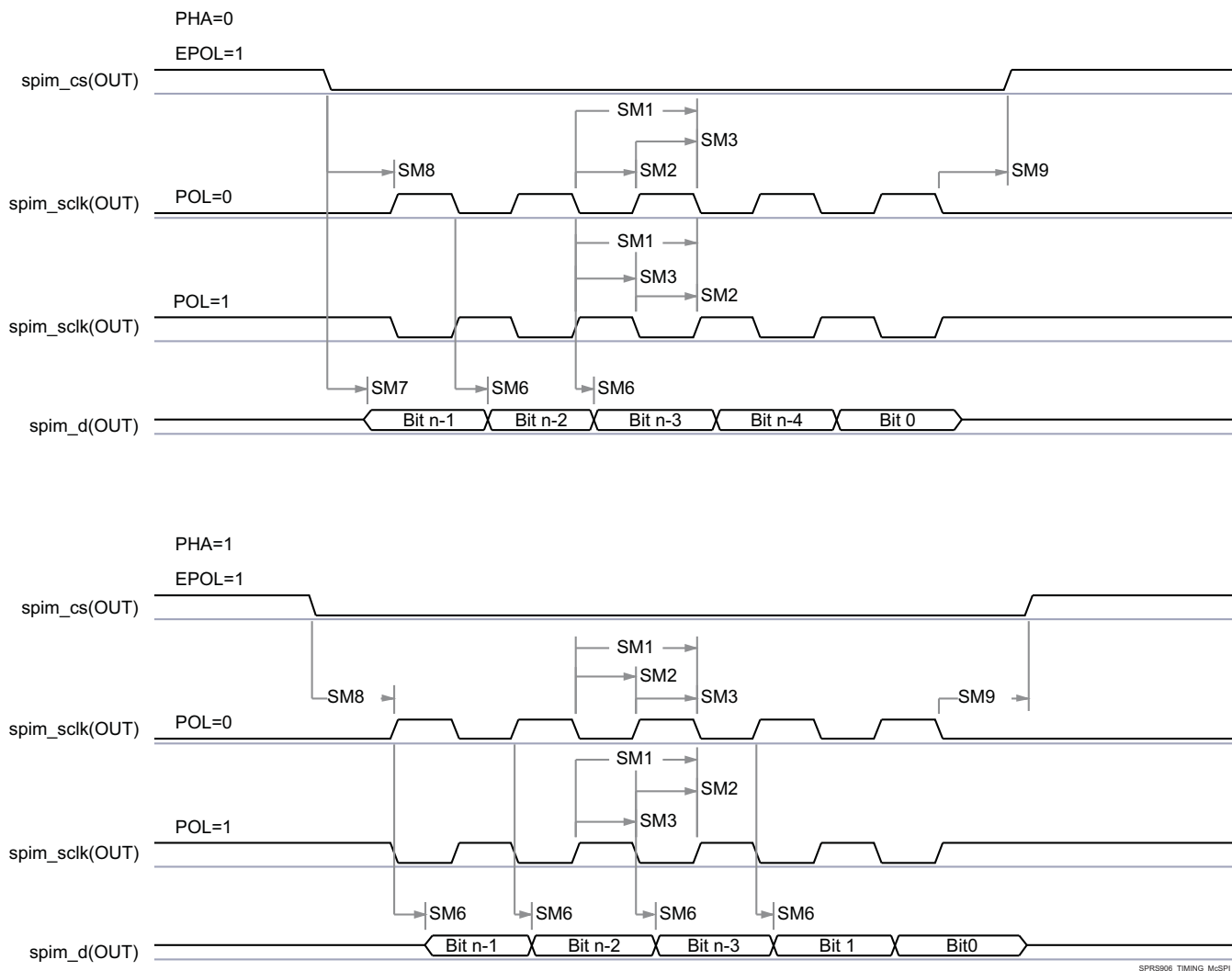


Figure 7-26. McSPI - Master Mode Transmit

SPRS952D_TIMING_McSPI_01

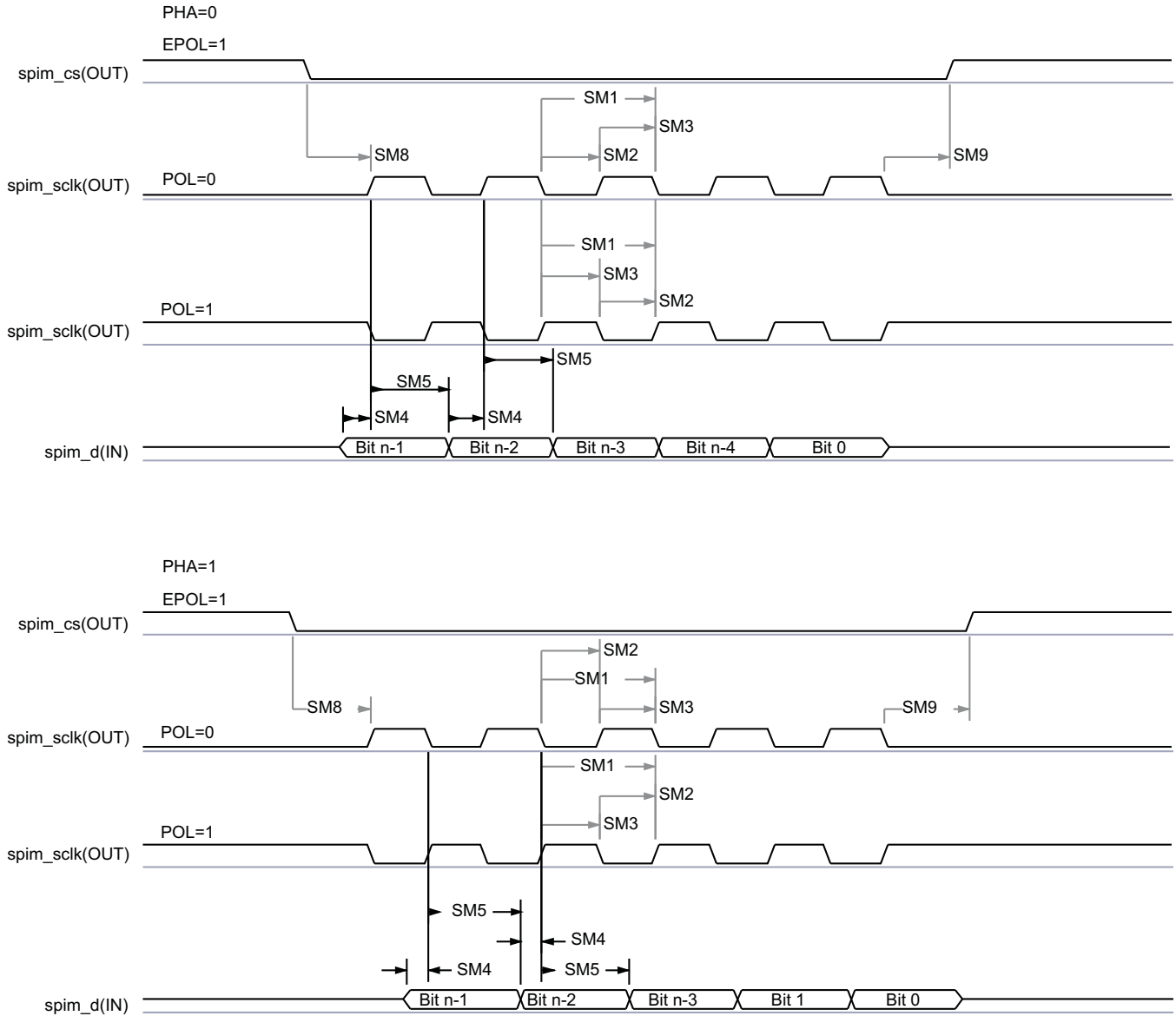


Figure 7-27. McSPI - Master Mode Receive

Table 7-36, Figure 7-28 and Figure 7-29 present Timing Requirements for McSPI - Slave Mode.

Table 7-36. Timing Requirements for SPI - Slave Mode

NO.	PARAMETER	DESCRIPTION	MODE	MIN	MAX	UNIT
SS1	$t_c(\text{SPICLK})$	Cycle time, spi_sclk ^{(1) (2)}	⁽³⁾	62.5		ns
SS2	$t_w(\text{SPICLK}_L)$	Typical Pulse duration, spi_sclk low ⁽¹⁾		0.45*P ⁽⁴⁾		ns
SS3	$t_w(\text{SPICLK}_H)$	Typical Pulse duration, spi_sclk high ⁽¹⁾		0.45*P ⁽⁴⁾		ns
SS4	$t_{su}(\text{SIMO-SPICLK})$	Setup time, spi_d[x] valid before spi_sclk active edge ⁽¹⁾		5		ns
SS5	$t_h(\text{SPICLK-SIMO})$	Hold time, spi_d[x] valid after spi_sclk active edge ⁽¹⁾		5		ns
SS6	$t_d(\text{SPICLK-SOMI})$	Delay time, spi_sclk active edge to mcspi_somi transition ⁽¹⁾	SPI1/2/3	2	26.1	ns
			SPI4	2	18	ns
SS7	$t_d(\text{CS-SOMI})$	Delay time, spi_cs[x] active edge to mcspi_somi transition ⁽¹⁾			20.95	ns
SS8	$t_{su}(\text{CS-SPICLK})$	Setup time, spi_cs[x] valid before spi_sclk first edge ⁽¹⁾		5		ns
SS9	$t_h(\text{SPICLK-CS})$	Hold time, spi_cs[x] valid after spi_sclk last edge ⁽¹⁾		5		ns

- (1) This timing applies to all configurations regardless of SPI_CLK polarity and which clock edges are used to drive output data and capture input data.
- (2) When operating the SPI interface in RX-only mode, the minimum Cycle time is 26ns (38.4MHz)
- (3) 62.5ns Cycle time = 16 MHz
- (4) P = SPICLK period.
- (5) PHA = 0; SPI_CLK phase is programmable with the PHA bit of the SPI_CH(i)CONF register.

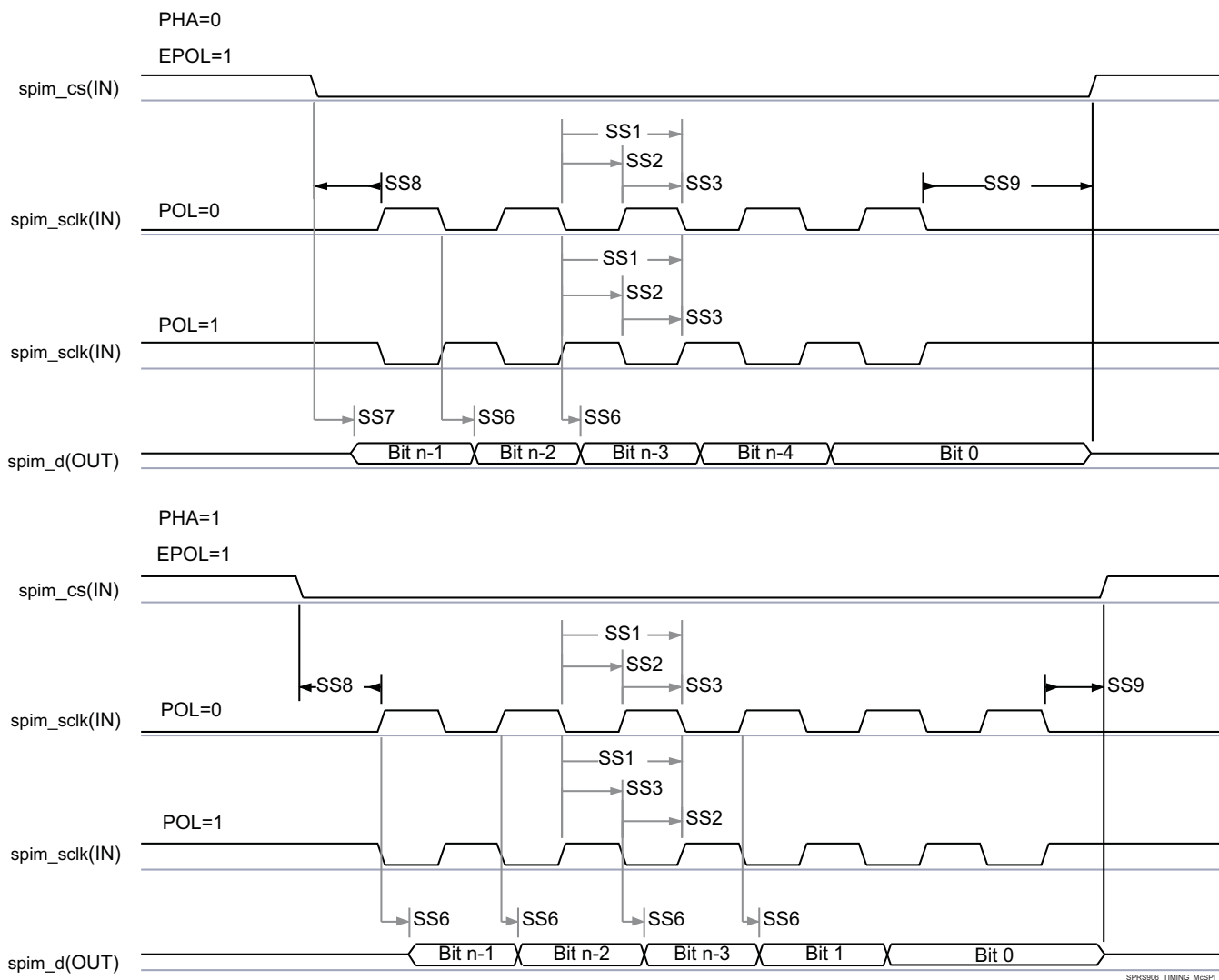


Figure 7-28. McSPI - Slave Mode Transmit

SPRS906_TIMING_McSPI_03

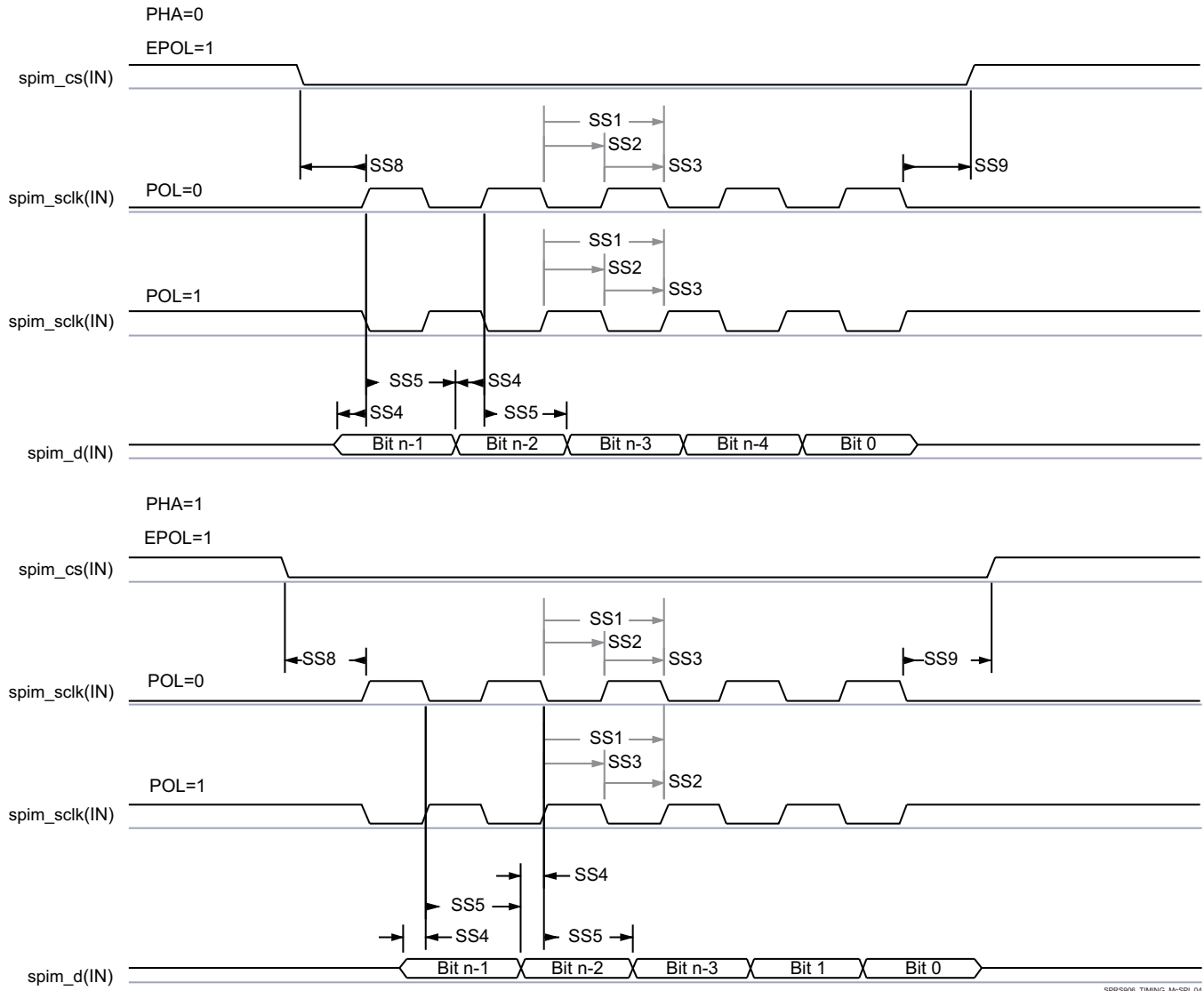


Figure 7-29. McSPI - Slave Mode Receive

In Table 7-37 are presented the specific groupings of signals (IOSET) for use with SPI3 and SPI4.

Table 7-37. McSPI3/4 IOSETs

Signal	IOSET1		IOSET2		IOSET3		IOSET4		IOSET5		IOSET6	
	BALL	MUX	BALL	MUX	BALL	MUX	BALL	MUX	BALL	MUX	BALL	MUX
SPI3												
spi3_sclk	AA7	8	E13	8	R1	7	A16	3	E24	2	W4	1
spi3_d1	AD6	8	D13	8	T2	7	A17	3	D23	2	U6	1
spi3_d0	AC6	8	E12	8	R6	7	A19	3	E25	2	V6	1
spi3_cs0	AC5	8	D10	8	P6	7	A20	3	E23	2	U5	1
spi3_cs1	-	-	E11	8	-	-	A21	3	-	-	V3	1
spi3_cs2	-	-	B9	8	-	-	-	-	-	-	-	-
spi3_cs3	-	-	D11	8	-	-	-	-	-	-	-	-
SPI4												
spi4_sclk	M1	8	D5	8	T5	7	V1	2	V5	1	-	-
spi4_d1	M3	8	C4	8	T6	7	W2	2	W6	1	-	-

Table 7-37. McSPI3/4 IOSETs (continued)

Signal	IOSET1		IOSET2		IOSET3		IOSET4		IOSET5		IOSET6	
	BALL	MUX	BALL	MUX	BALL	MUX	BALL	MUX	BALL	MUX	BALL	MUX
spi4_d0	M6	8	C3	8	T4	7	V2	2	W3	1	-	-
spi4_cs0	N5	8	B2	8	R5	7	U1	2	V4	1	-	-
spi4_cs1	L5	8	-	-	T2	8	-	-	-	-	-	-
spi4_cs2	L4	8	-	-	R6	8	-	-	-	-	-	-
spi4_cs3	L3	8	-	-	P6	8	-	-	-	-	-	-

7.15 Quad Serial Peripheral Interface (QSPI)

The Quad SPI (QSPI) module is a type of SPI module that allows single, dual or quad read access to external SPI devices. This module has a memory mapped register interface, which provides a direct interface for accessing data from external SPI devices and thus simplifying software requirements. It works as a master only. There is one QSPI module in the device and it is primary intended for fast booting from quad-SPI flash memories.

General SPI features:

- Programmable clock divider
- Six pin interface (DCLK, CS_N, DOUT, DIN, QDIN1, QDIN2)
- 4 external chip select signals
- Support for 3-, 4- or 6-pin SPI interface
- Programmable CS_N to DOUT delay from 0 to 3 DCLKs
- Programmable signal polarities
- Programmable active clock edge
- Software controllable interface allowing for any type of SPI transfer

NOTE

For more information, see the Quad Serial Peripheral Interface section of the Device TRM.

CAUTION

The IO Timings provided in this section are only valid for some QSPI usage modes when the corresponding Virtual IO Timings or Manual IO Timings are configured as described in the tables found in this section.

CAUTION

The IO Timings provided in this section are only valid when all QSPI Chip Selects used in a system are configured to use the same Clock Mode (either Clock Mode 0 or Clock Mode3).

Table 7-38 and Table 7-39 present Timing and Switching Characteristics for Quad SPI Interface.

Table 7-38. Switching Characteristics for QSPI

No	PARAMETER	DESCRIPTION	Mode	MIN	MAX	UNIT
Q1	$t_c(\text{SCLK})$	Cycle time, sclk	Default Timing Mode, Clock Mode 0	13.02		ns
			Default Timing Mode, Clock Mode 3	20.8		ns
Q2	$t_w(\text{SCLKL})$	Pulse duration, sclk low		$Y * P - 1$ (1)		ns
Q3	$t_w(\text{SCLKH})$	Pulse duration, sclk high		$Y * P - 1$ (1)		ns
Q4	$t_d(\text{CS-SCLK})$	Delay time, sclk falling edge to cs active edge, CS3:0	Default Timing Mode	$-M * P - 2.0$ (2) (3)	$-M * P + 2.0$ (2) (3)	ns
Q5	$t_d(\text{SCLK-CS})$	Delay time, sclk falling edge to cs inactive edge, CS3:0	Default Timing Mode	$N * P - 2.0$ (2) (3)	$N * P + 2.0$ (2) (3)	ns
Q6	$t_d(\text{SCLK-D1})$	Delay time, sclk falling edge to d[0] transition	Default Timing Mode	-2	2	ns
Q7	$t_{\text{ena}}(\text{CS-D1LZ})$	Enable time, cs active edge to d[0] driven (lo-z)		-P-3.5	-P+2.5	ns
Q8	$t_{\text{dis}}(\text{CS-D1Z})$	Disable time, cs active edge to d[0] tri-stated (hi-z)		-P-2.5	-P+2.0	ns
Q9	$t_d(\text{SCLK-D0})$	Delay time, sclk first falling edge to first d[0] transition	PHA=0 Only, Default Timing Mode	$-2.45 - P$	$1.45 - P$	ns

(1) The Y parameter is defined as follows:

If DCLK_DIV is 0 or ODD then, Y equals 0.5.

If DCLK_DIV is EVEN then, Y equals $(\text{DCLK_DIV}/2) / (\text{DCLK_DIV}+1)$.

For best performance, it is recommended to use a DCLK_DIV of 0 or ODD to minimize the duty cycle distortion. The HSDIVIDER on CLKOUTX2_H13 output of DPLL_PER can be used to achieve the desired clock divider ratio. All required details about clock division factor DCLK_DIV can be found in the device TRM.

(2) P = SCLK period.

(3) M=QSPI_SPI_DC_REG.DDx + 1 when Clock Mode 0.

M=QSPI_SPI_DC_REG.DDx when Clock Mode 3.

N = 2 when Clock Mode 0.

N = 3 when Clock Mode 3.

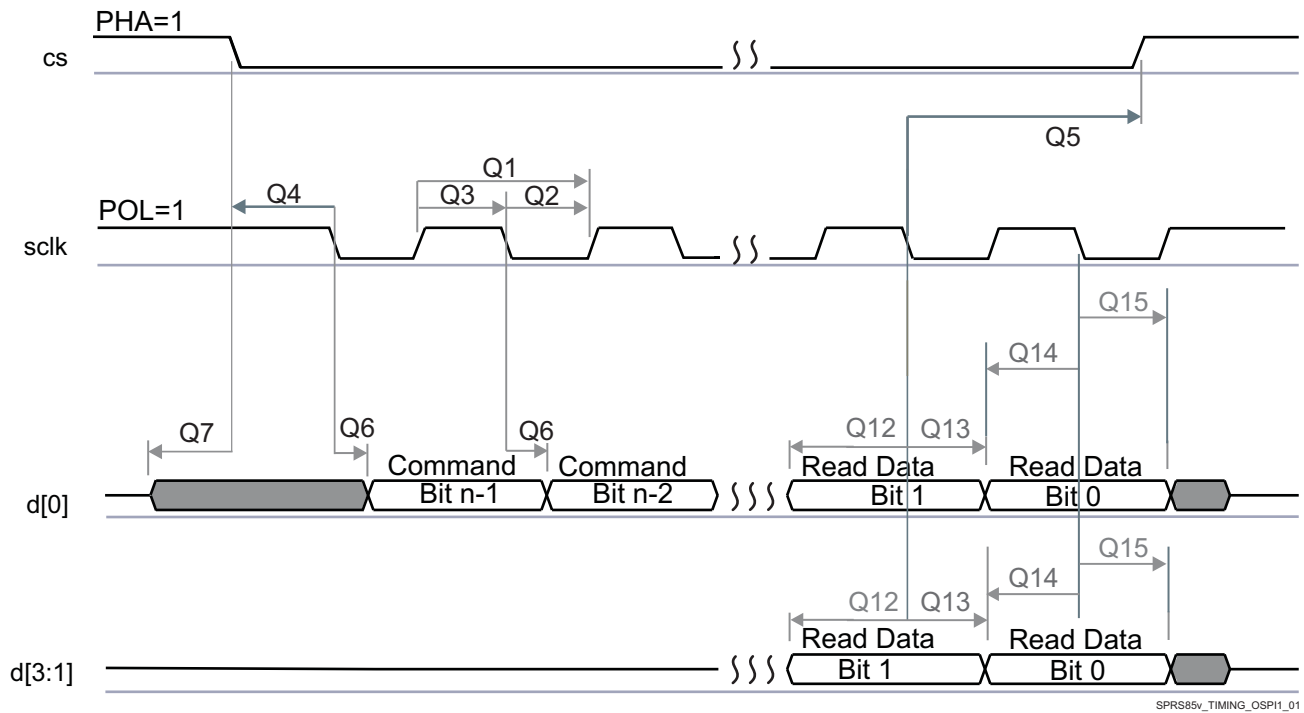


Figure 7-30. QSPI Read (Clock Mode 3)

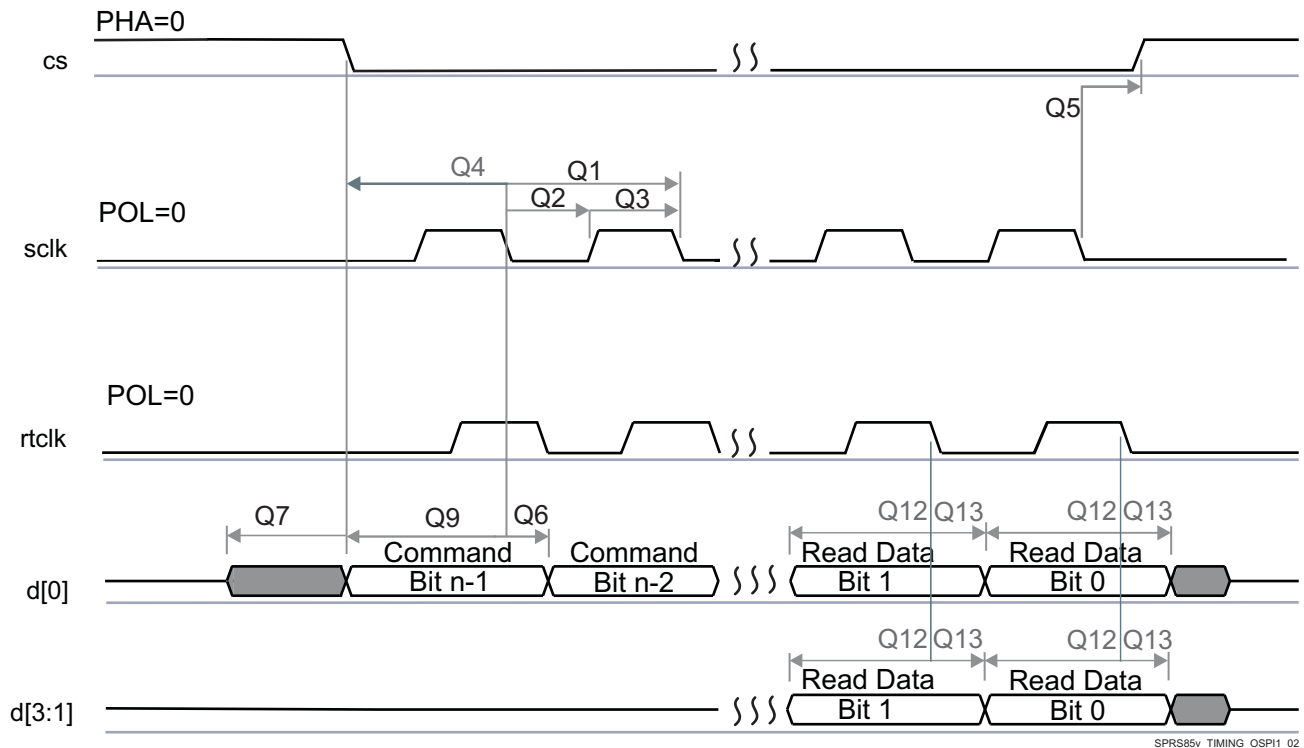


Figure 7-31. QSPI Read (Clock Mode 0)

CAUTION

The IO Timings provided in this section are only valid for some QSPI usage modes when the corresponding Virtual IO Timings or Manual IO Timings are configured as described in the tables found in this section.

Table 7-39. Timing Requirements for QSPI

No	PARAMETER	DESCRIPTION	Mode	MIN	MAX	UNIT
Q12	$t_{su}(D-RTCLK)$	Setup time, d[3:0] valid before falling rtclk edge	Default Timing Mode, Clock Mode 0	5.1		ns
	$t_{su}(D-SCLK)$	Setup time, d[3:0] valid before falling sclk edge	Default Timing Mode, Clock Mode 3	12.3		ns
Q13	$t_h(RTCLK-D)$	Hold time, d[3:0] valid after falling rtclk edge	Default Timing Mode, Clock Mode 0	-0.1		ns
	$t_h(SCLK-D)$	Hold time, d[3:0] valid after falling sclk edge	Default Timing Mode, Clock Mode 3	0		ns
Q14	$t_{su}(D-SCLK)$	Setup time, final d[3:0] bit valid before final falling sclk edge	Default Timing Mode, Clock Mode 3	12.3-P (1)		ns
Q15	$t_h(SCLK-D)$	Hold time, final d[3:0] bit valid after final falling sclk edge	Default Timing Mode, Clock Mode 3	0+P (1)		ns

- (1) P = SCLK period.
- (2) Clock Modes 1 and 2 are not supported.
- (3) The Device captures data on the falling clock edge in Clock Mode 0 and 3, as opposed to the traditional rising clock edge. Although nonstandard, the falling-edge-based setup and hold time timings have been designed to be compatible with standard SPI devices that launch data on the falling edge in Clock Modes 0 and 3.

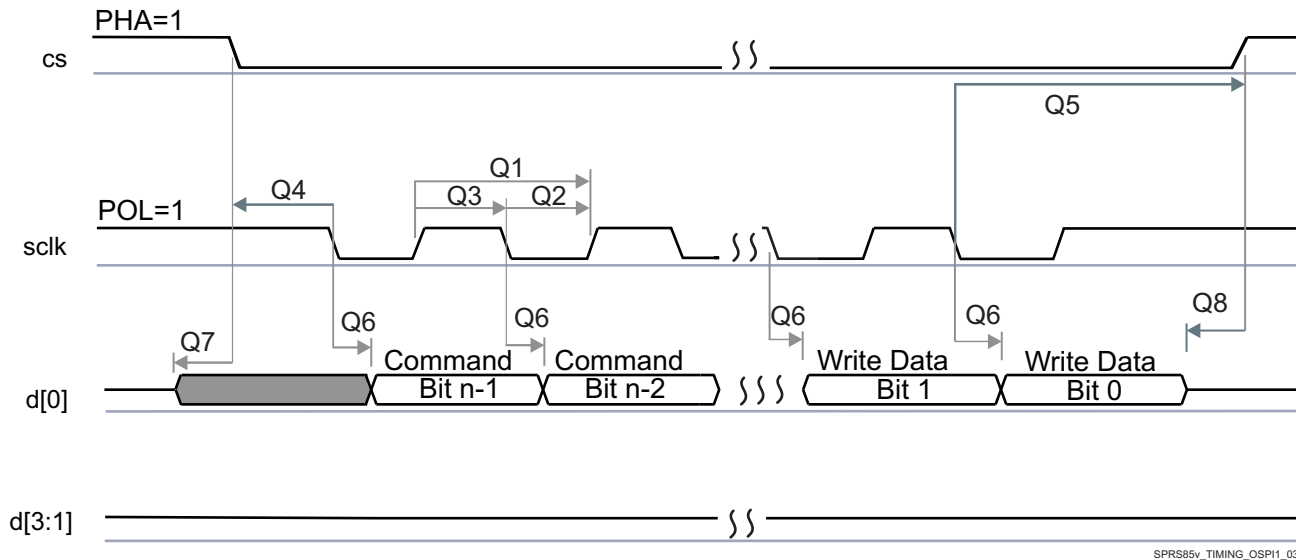


Figure 7-32. QSPI Write (Clock Mode 3)

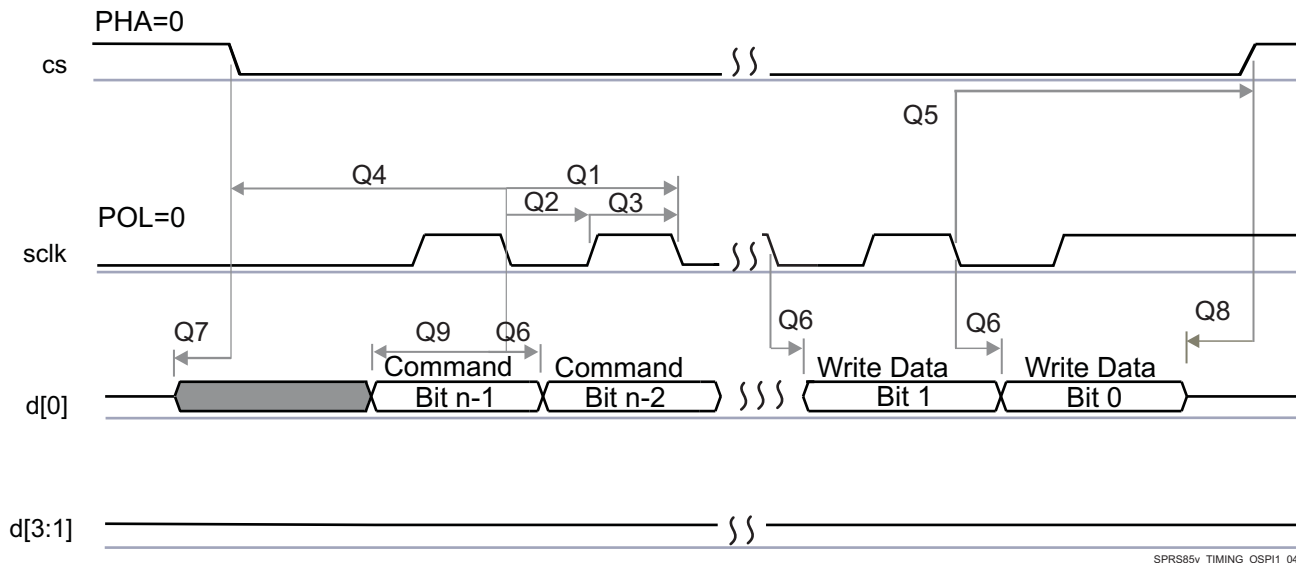


Figure 7-33. QSPI Write (Clock Mode 0)

NOTE

To configure the desired Manual IO Timing Mode the user must follow the steps described in section "Manual IO Timing Modes" of the Device TRM.

The associated registers to configure are listed in the CFG REGISTER column. For more information please see the *Control Module Chapter* in the Device TRM.

Manual IO Timings Modes must be used to guarantee some IO timings for QSPI. See [Table 7-2 Modes Summary](#) for a list of IO timings requiring the use of Manual IO Timings Modes. See [Table 7-40 Manual Functions Mapping for QSPI](#) for a definition of the Manual modes.

[Table 7-40](#) lists the A_DELAY and G_DELAY values needed to calculate the correct values to be set in the CFG_x registers.

Table 7-40. Manual Functions Mapping for QSPI

BALL	BALL NAME	QSPI_MODE0_MANUAL1		CFG REGISTER	MUXMODE 1
		A_DELAY (ps)	G_DELAY (ps)		
P2	gpmc_a3	114	0	CFG_GPMC_A3_OUT	qspi1_cs2
N2	gpmc_a4	91	0	CFG_GPMC_A4_OUT	qspi1_cs3
L4	gpmc_a13	0	0	CFG_GPMC_A13_IN	qspi1_rtcclk
L3	gpmc_a14	2575	966	CFG_GPMC_A14_IN	qspi1_d3
L2	gpmc_a15	2503	889	CFG_GPMC_A15_IN	qspi1_d2
L1	gpmc_a16	2528	1007	CFG_GPMC_A16_IN	qspi1_d0
L1	gpmc_a16	0	0	CFG_GPMC_A16_OUT	qspi1_d0
K6	gpmc_a17	2533	980	CFG_GPMC_A17_IN	qspi1_d1
K5	gpmc_a18	590	0	CFG_GPMC_A18_OUT	qspi1_sclk
K3	gpmc_cs2	0	0	CFG_GPMC_CS2_OUT	qspi1_cs0
K2	gpmc_cs3	70	0	CFG_GPMC_CS3_OUT	qspi1_cs1

7.16 Multichannel Audio Serial Port (McASP)

The multichannel audio serial port (McASP) functions as a general-purpose audio serial port optimized for the needs of multichannel audio applications. The McASP is useful for time-division multiplexed (TDM) stream, Inter-Integrated Sound (I2S) protocols, and inter-component digital audio interface transmission (DIT).

The device have integrated McASP module (McASP1-McASP7) with:

- McASP1 supporting 12 channels with independent TX/RX clock/sync domain
- McASP2 supporting 8 channels with independent TX/RX clock/sync domain
- McASP3 supporting 4 channels with independent TX/RX clock/sync domain
- McASP4 through McASP7 modules supporting 2 channels with independent TX/RX clock/sync domain

NOTE

For more information, see the Multichannel Audio Serial Port section of the Device TRM.

CAUTION

The IO Timings provided in this section are only valid for some McASP usage modes when the corresponding Virtual IO Timings or Manual IO Timings are configured as described in the tables found in this section.

Table 7-41, Table 7-42, Table 7-43 and Figure 7-34 present Timing Requirements for McASP1 to McASP7.

Table 7-41. Timing Requirements for McASP1 (1)

NO.	PARAMETER	DESCRIPTION	MODE	MIN	MAX	UNIT
1	$t_{c(AHCLKRX)}$	Cycle time, AHCLKR/X		20		ns
2	$t_{w(AHCLKRX)}$	Pulse duration, AHCLKR/X high or low		0.35P (2)		ns
3	$t_{c(ACLKRX)}$	Cycle time, ACLKR/X		20		ns
4	$t_{w(ACLKRX)}$	Pulse duration, ACLKR/X high or low		0.5R - 3 (3)		ns
5	$t_{su(AFSRX-ACLK)}$	Setup time, AFSR/X input valid before ACLKR/X	ACLKR/X int	20		ns
			ACLKR/X ext in ACLKR/X ext out	4		ns
6	$t_{h(ACLK-AFSRX)}$	Hold time, AFSR/X input valid after ACLKR/X	ACLKR/X int	-1		ns
			ACLKR/X ext in ACLKR/X ext out	2.21		ns
7	$t_{su(AXR-ACLK)}$	Setup time, AXR input valid before ACLKR/X	ACLKR/X int	21.9		ns
			ACLKR/X ext in ACLKR/X ext out	4.42		ns
8	$t_{h(ACLK-AXR)}$	Hold time, AXR input valid after ACLKR/X	ACLKR/X int	-1		ns
			ACLKR/X ext in ACLKR/X ext out	2.52		ns

(1) ACLKR internal: ACLKRCTL.CLKRM=1, PDIR.ACLKR = 1

ACLKR external input: ACLKRCTL.CLKRM=0, PDIR.ACLKR=0

ACLKR external output: ACLKRCTL.CLKRM=0, PDIR.ACLKR=1

ACLKX internal: ACLKXCTL.CLKXM=1, PDIR.ACLKX = 1

ACLKX external input: ACLKXCTL.CLKXM=0, PDIR.ACLKX=0

ACLKX external output: ACLKXCTL.CLKXM=0, PDIR.ACLKX=1

(2) P = AHCLKR/X period in ns.

(3) R = ACLKR/X period in ns.

Table 7-42. Timing Requirements for McASP2 (1)

NO.	PARAMETER	DESCRIPTION	MODE	MIN	MAX	UNIT
1	$t_{c(AHCLKRX)}$	Cycle time, AHCLKR/X		20		ns
2	$t_{w(AHCLKRX)}$	Pulse duration, AHCLKR/X high or low		0.35P (2)		ns
3	$t_{c(ACLKRX)}$	Cycle time, ACLKR/X	Any Other Conditions	20		ns
			ACLKX/AFSX (In Sync Mode), ACLKR/AFSR (In Async Mode), and AXR are all inputs "80M" Virtual IO Timing Mode	12.5		ns
4	$t_{w(ACLKRX)}$	Pulse duration, ACLKR/X high or low	Any Other Conditions	0.5R - 3 (3)		ns
			ACLKX/AFSX (In Sync Mode), ACLKR/AFSR (In Async Mode), and AXR are all inputs "80M" Virtual IO Timing Modes	0.38R (3)		ns
5	$t_{su(AFSRX-ACLK)}$	Setup time, AFSR/X input valid before ACLKR/X	ACLKR/X int	20.7		ns
			ACLKR/X ext in ACLKR/X ext out	3.9		ns
			ACLKR/X ext in ACLKR/X ext out "80M" Virtual IO Timing Modes	3		ns

Table 7-42. Timing Requirements for McASP2 ⁽¹⁾ (continued)

NO.	PARAMETER	DESCRIPTION	MODE	MIN	MAX	UNIT
6	$t_{h(ACLK-AFSRX)}$	Hold time, AFSRX input valid after ACLKR/X	ACLKR/X int	-1		ns
			ACLKR/X ext in ACLKR/X ext out	3.2		ns
			ACLKR/X ext in ACLKR/X ext out "80M" Virtual IO Timing Modes	3		ns
7	$t_{su(AXR-ACLK)}$	Setup time, AXR input valid before ACLKR/X	ACLKR/X int	21.4		ns
			ACLKR/X ext in ACLKR/X ext out	3.9		ns
			ACLKR/X ext in ACLKR/X ext out "80M" Virtual IO Timing Modes	3		ns
8	$t_{h(ACLK-AXR)}$	Hold time, AXR input valid after ACLKR/X	ACLKR/X int	-1		ns
			ACLKR/X ext in ACLKR/X ext out	3.2		ns
			ACLKR/X ext in ACLKR/X ext out "80M" Virtual IO Timing Modes	3		ns

(1) ACLKR internal: ACLKRCTL.CLKRM=1, PDIR.ACLKR = 1
 ACLKR external input: ACLKRCTL.CLKRM=0, PDIR.ACLKR=0
 ACLKR external output: ACLKRCTL.CLKRM=0, PDIR.ACLKR=1
 ACLKX internal: ACLKXCTL.CLKXM=1, PDIR.ACLKX = 1
 ACLKX external input: ACLKXCTL.CLKXM=0, PDIR.ACLKX=0
 ACLKX external output: ACLKXCTL.CLKXM=0, PDIR.ACLKX=1

(2) P = AHCLKR/X period in ns.

(3) R = ACLKR/X period in ns.

Table 7-43. Timing Requirements for McASP3/4/5/6/7 ⁽¹⁾

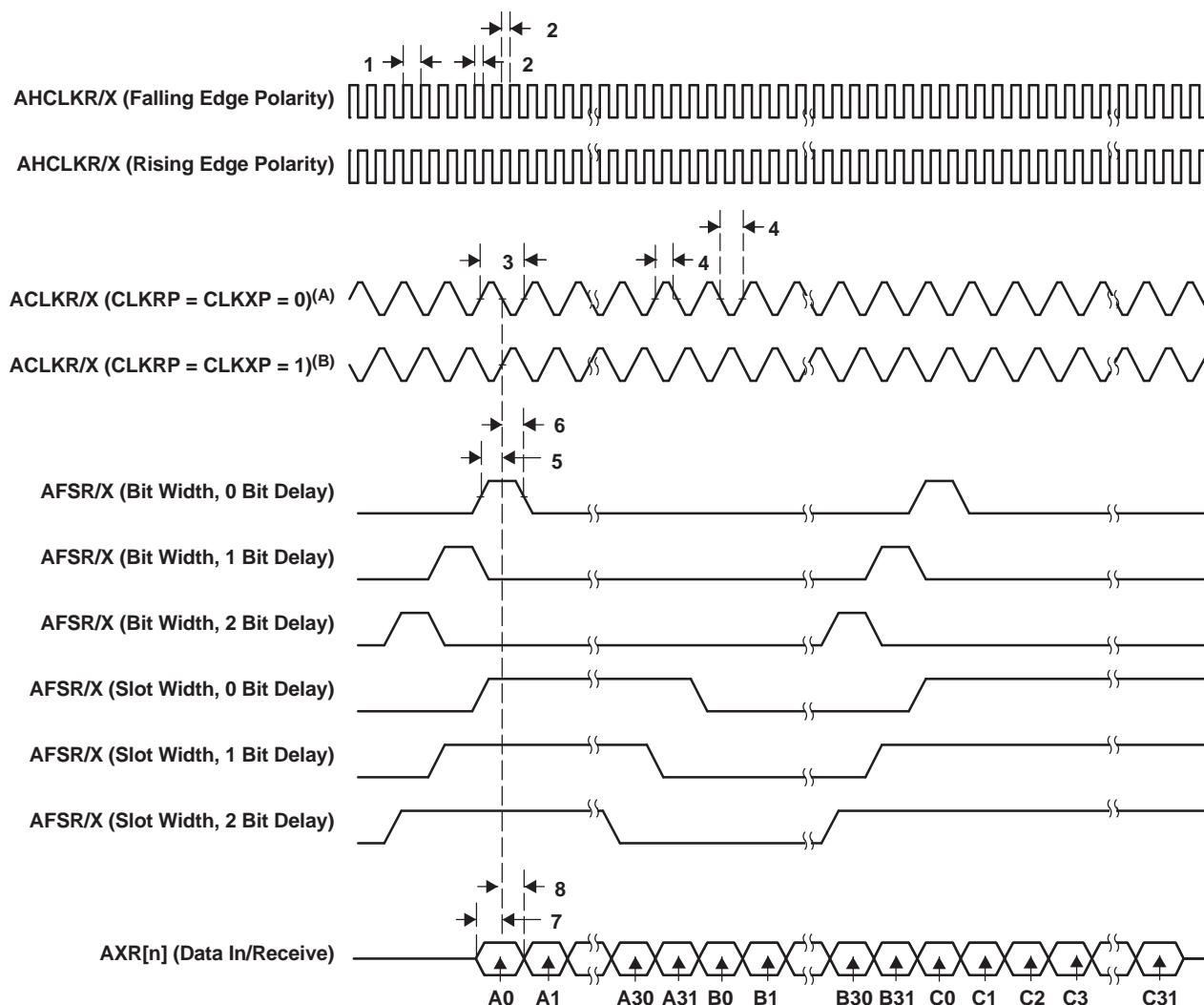
NO.	PARAMETER	DESCRIPTION	MODE	MIN	MAX	UNIT
1	$t_{c(AHCLKRX)}$	Cycle time, AHCLKR/X		20		ns
2	$t_{w(AHCLKRX)}$	Pulse duration, AHCLKR/X high or low		0.35P ⁽²⁾		ns
3	$t_{c(ACLKRX)}$	Cycle time, ACLKR/X		20		ns
4	$t_{w(ACLKRX)}$	Pulse duration, ACLKR/X high or low		0.5R - 3 ⁽³⁾		ns
5	$t_{su(AFSRX-ACLK)}$	Setup time, AFSRX input valid before ACLKR/X	ACLKR/X int	20.2		ns
			ACLKR/X ext in ACLKR/X ext out	4.9		ns
6	$t_{h(ACLK-AFSRX)}$	Hold time, AFSRX input valid after ACLKR/X	ACLKR/X int	-1		ns
			ACLKR/X ext in ACLKR/X ext out	2.26		ns
	$t_{su(AXR-ACLK)}$	Setup time, AXR input valid before ACLKX	ACLKX int (ASYNC=0)	20.8		ns
			ACLKR/X ext in ACLKR/X ext out	5.75		ns
8	$t_{h(ACLK-AXR)}$	Hold time, AXR input valid after ACLKX	ACLKX int (ASYNC=0)	-0.9		ns
			ACLKR/X ext in ACLKR/X ext out	2.87		ns

(1) ACLKR internal: ACLKRCTL.CLKRM=1, PDIR.ACLKR = 1 (NOT SUPPORTED)

ACLKR external input: ACLKRCTL.CLKRM=0, PDIR.ACLKR=0
 ACLKR external output: ACLKRCTL.CLKRM=0, PDIR.ACLKR=1
 ACLKX internal: ACLKXCTL.CLKXM=1, PDIR.ACLKX = 1
 ACLKX external input: ACLKXCTL.CLKXM=0, PDIR.ACLKX=0
 ACLKX external output: ACLKXCTL.CLKXM=0, PDIR.ACLKX=1

(2) P = AHCLKR/X period in ns.

(3) R = ACLKR/X period in ns.



- A. For CLKRP = CLKXP = 0, the McASP transmitter is configured for rising edge (to shift data out) and the McASP receiver is configured for falling edge (to shift data in).
- B. For CLKRP = CLKXP = 1, the McASP transmitter is configured for falling edge (to shift data out) and the McASP receiver is configured for rising edge (to shift data in).

Figure 7-34. McASP Input Timing

CAUTION

The IO Timings provided in this section are only valid for some McASP usage modes when the corresponding Virtual IO Timings or Manual IO Timings are configured as described in the tables found in this section.

Table 7-44, Table 7-45, Table 7-46 and Figure 7-35 present Switching Characteristics Over Recommended Operating Conditions for McASP1 to McASP7.

Table 7-44. Switching Characteristics Over Recommended Operating Conditions for McASP1 ⁽¹⁾

NO.	PARAMETER	DESCRIPTION	MODE	MIN	MAX	UNIT
9	t _c (AHCLKRX)	Cycle time, AHCLKR/X		20		ns

Table 7-44. Switching Characteristics Over Recommended Operating Conditions for McASP1⁽¹⁾ (continued)

NO.	PARAMETER	DESCRIPTION	MODE	MIN	MAX	UNIT
10	$t_{w(AHCLKRX)}$	Pulse duration, AHCLKR/X high or low		0.5P - 2.5 ⁽²⁾		ns
11	$t_{c(ACLKRX)}$	Cycle time, ACLKRX		20		ns
12	$t_{w(ACLKRX)}$	Pulse duration, ACLKRX high or low		0.5P - 2.5 ⁽³⁾		ns
13	$t_{d(ACLK-AFSXR)}$	Delay time, ACLKRX transmit edge to AFSX/R output valid	ACLKRX int	-0.21	6	ns
			ACLKRX ext in ACLKRX ext out	2	23.9	ns
14	$t_{d(ACLK-AXR)}$	Delay time, ACLKRX transmit edge to AXR output valid	ACLKRX int	-1.8	6.9	ns
			ACLKRX ext in ACLKRX ext out	2	25.6	ns

- (1) ACLKRX internal: ACLKRXCTL.CLKRM=1, PDIR.ACLKRX = 1
 ACLKRX external input: ACLKRXCTL.CLKRM=0, PDIR.ACLKRX=0
 ACLKRX external output: ACLKRXCTL.CLKRM=0, PDIR.ACLKRX=1
 ACLKX internal: ACLKXCTL.CLKXM=1, PDIR.ACLKX = 1
 ACLKX external input: ACLKXCTL.CLKXM=0, PDIR.ACLKX=0
 ACLKX external output: ACLKXCTL.CLKXM=0, PDIR.ACLKX=1

(2) P = AHCLKR/X period in ns.

(3) R = ACLKRX period in ns.

Table 7-45. Switching Characteristics Over Recommended Operating Conditions for McASP2⁽¹⁾

NO.	PARAMETER	DESCRIPTION	MODE	MIN	MAX	UNIT
9	$t_{c(AHCLKRX)}$	Cycle time, AHCLKR/X		20		ns
10	$t_{w(AHCLKRX)}$	Pulse duration, AHCLKR/X high or low		0.5P - 2.5 ⁽²⁾		ns
11	$t_{c(ACLKRX)}$	Cycle time, ACLKRX		20		ns
12	$t_{w(ACLKRX)}$	Pulse duration, ACLKRX high or low		0.5P - 2.5 ⁽³⁾		ns
13	$t_{d(ACLK-AFSXR)}$	Delay time, ACLKRX transmit edge to AFSX/R output valid	ACLKRX int	0	6	ns
			ACLKRX ext in ACLKRX ext out	2	25.2	ns
14	$t_{d(ACLK-AXR)}$	Delay time, ACLKRX transmit edge to AXR output valid	ACLKRX int	-1.29	6.11	ns
			ACLKRX ext in ACLKRX ext out	2	24.8	ns

- (1) ACLKRX internal: ACLKRXCTL.CLKRM=1, PDIR.ACLKRX = 1
 ACLKRX external input: ACLKRXCTL.CLKRM=0, PDIR.ACLKRX=0
 ACLKRX external output: ACLKRXCTL.CLKRM=0, PDIR.ACLKRX=1
 ACLKX internal: ACLKXCTL.CLKXM=1, PDIR.ACLKX = 1
 ACLKX external input: ACLKXCTL.CLKXM=0, PDIR.ACLKX=0
 ACLKX external output: ACLKXCTL.CLKXM=0, PDIR.ACLKX=1

(2) P = AHCLKR/X period in ns.

(3) R = ACLKRX period in ns.

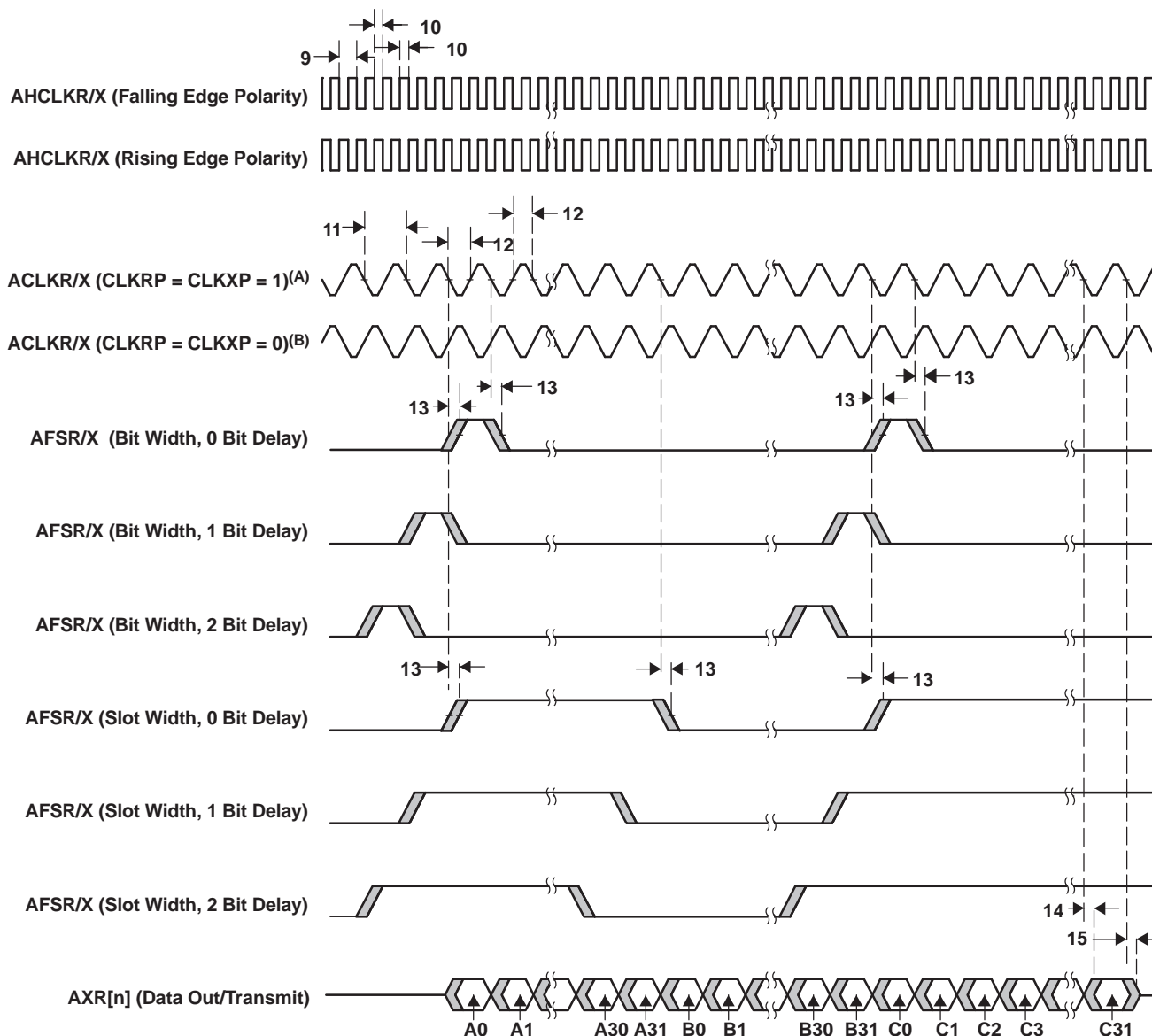
Table 7-46. Switching Characteristics Over Recommended Operating Conditions for McASP3/4/5/6/7⁽¹⁾

NO.	PARAMETER	DESCRIPTION	MODE	MIN	MAX	UNIT
9	$t_{c(AHCLKRX)}$	Cycle time, AHCLKR/X		20		ns
10	$t_{w(AHCLKRX)}$	Pulse duration, AHCLKR/X high or low		0.5P - 2.5 ⁽²⁾		ns
11	$t_{c(ACLKRX)}$	Cycle time, ACLKRX		20		ns
12	$t_{w(ACLKRX)}$	Pulse duration, ACLKRX high or low		0.5P - 2.5 ⁽³⁾		ns

Table 7-46. Switching Characteristics Over Recommended Operating Conditions for McASP3/4/5/6/7
(1) (continued)

NO.	PARAMETER	DESCRIPTION	MODE	MIN	MAX	UNIT
13	$t_{d(ACLK-AFSXR)}$	Delay time, ACLKR/X transmit edge to AFSX/R output valid	ACLKR/X int	-0.74	6	ns
			ACLKR/X ext in ACLKR/X ext out	2	26.4	ns
14	$t_{d(ACLK-AXR)}$	Delay time, ACLKR/X transmit edge to AXR output valid	ACLKR/X int	-1.68	6.97	ns
			ACLKR/X ext in ACLKR/X ext out	1.07	25.9	ns

- (1) ACLKR internal: ACLKRCTL.CLKRM=1, PDIR.ACLKR = 1
 ACLKR external input: ACLKRCTL.CLKRM=0, PDIR.ACLKR=0
 ACLKR external output: ACLKRCTL.CLKRM=0, PDIR.ACLKR=1
 ACLKX internal: ACLKXCTL.CLKXM=1, PDIR.ACLKX = 1
 ACLKX external input: ACLKXCTL.CLKXM=0, PDIR.ACLKX=0
 ACLKX external output: ACLKXCTL.CLKXM=0, PDIR.ACLKX=1
- (2) P = AHCLKR/X period in ns.
 (3) R = ACLKR/X period in ns.



- A. For CLKRP = CLKXP = 1, the McASP transmitter is configured for falling edge (to shift data out) and the McASP receiver is configured for rising edge (to shift data in).
- B. For CLKRP = CLKXP = 0, the McASP transmitter is configured for rising edge (to shift data out) and the McASP receiver is configured for falling edge (to shift data in).

Figure 7-35. McASP Output Timing

NOTE

To configure the desired virtual mode the user must set MODESELECT bit and DELAYMODE bitfield for each corresponding pad control register.

The pad control registers are presented in [Table 4-3](#) and described in Device TRM, *Control Module Chapter*.

[Table 7-47](#) through [Table 7-53](#) explain all cases with Virtual Mode Details for McASP1/2/3/4/5/6/7/8 (see [Figure 7-36](#) through [Figure 7-43](#)).

Table 7-47. Virtual Mode Case Details for McASP1

No.	CASE	CASE Description	Virtual Mode Settings		Notes
			Signals	Virtual Mode Value	
IP Mode : ASYNC					
1	COIFOI	CLKX / FSX: Output CLKR / FSR: Input	AXR(Outputs)/CLKX/FSX	Default (No Virtual Mode)	See Figure 7-36
			AXR(Inputs)/CLKR/FSR	MCASP1_VIRTUAL3_ASYNC_RX	
2	COIFIO	CLKX / FSR: Output CLKR / FSX: Input	AXR(Outputs)/CLKX/FSX	Default (No Virtual Mode)	See Figure 7-37
			AXR(Inputs)/CLKR/FSR	MCASP1_VIRTUAL3_ASYNC_RX	
3	CIOFIO	CLKR / FSR: Output CLKX / FSX: Input	AXR(Outputs)/CLKX/FSX	MCASP1_VIRTUAL3_ASYNC_RX	See Figure 7-38
			AXR(Inputs)/CLKR/FSR	MCASP1_VIRTUAL1_ASYNC_TX	
4	CIOFOI	CLKR / FSX: Output CLKX / FSR: Input	AXR(Outputs)/CLKX/FSX	MCASP1_VIRTUAL3_ASYNC_RX	See Figure 7-39
			AXR(Inputs)/CLKR/FSR	MCASP1_VIRTUAL1_ASYNC_TX	
IP Mode : SYNC (CLKR / FSR internally generated from CLKX / FSX)					
5	CO-FO-	CLKX / FSX: Output	AXR(Outputs)/CLKX/FSX	Default (No Virtual Mode)	See Figure 7-40
			AXR(Inputs)/CLKX/FSX	Default (No Virtual Mode)	
6	CI-FO-	FSX: Output CLKX: Input	AXR(Outputs)/CLKX/FSX	MCASP1_VIRTUAL2_SYNC_RX	See Figure 7-41
			AXR(Inputs)/CLKX/FSX	MCASP1_VIRTUAL2_SYNC_RX	
7	CI-FI-	CLKX / FSX: Input	AXR(Outputs)/CLKX/FSX	MCASP1_VIRTUAL2_SYNC_RX	See Figure 7-42
			AXR(Inputs)/CLKX/FSX	MCASP1_VIRTUAL2_SYNC_RX	
8	CO-FI-	CLKX: Output FSX: Input	AXR(Outputs)/CLKX/FSX	Default (No Virtual Mode)	See Figure 7-43
			AXR(Inputs)/CLKX/FSX	Default (No Virtual Mode)	

Table 7-48. Virtual Mode Case Details for McASP2

No.	CASE	CASE Description	Virtual Mode Settings		Notes
			Signals	Virtual Mode Value	
IP Mode : ASYNC					
1	COIFOI	CLKX / FSX: Output CLKR / FSR: Input	AXR(Outputs)/CLKX/FSX	Default (No Virtual Mode) ⁽¹⁾	See Figure 7-36
			AXR(Inputs)/CLKR/FSR	Default (No Virtual Mode) ⁽¹⁾	
			AXR(Inputs)/CLKR/FSR	MCASP2_VIRTUAL4_ASYNC_RX_80M ⁽²⁾	
2	COIFIO	CLKX / FSR: Output CLKR / FSX: Input	AXR(Outputs)/CLKX/FSX	Default (No Virtual Mode)	See Figure 7-37
			AXR(Inputs)/CLKR/FSR	MCASP2_VIRTUAL2_ASYNC_RX	
3	CIOFIO	CLKR / FSR: Output CLKX / FSX: Input	AXR(Outputs)/CLKX/FSX	MCASP2_VIRTUAL2_ASYNC_RX	See Figure 7-38
			AXR(Inputs)/CLKR/FSR	Default (No Virtual Mode)	
4	CIOFOI	CLKR / FSX: Output CLKX / FSR: Input	AXR(Outputs)/CLKX/FSX	MCASP2_VIRTUAL2_ASYNC_RX	See Figure 7-39
			AXR(Inputs)/CLKR/FSR	Default (No Virtual Mode)	
IP Mode : SYNC (CLKR / FSR internally generated from CLKX / FSX)					
5	CO-FO-	CLKX / FSX: Output	AXR(Outputs)/CLKX/FSX	Default (No Virtual Mode)	See Figure 7-40
			AXR(Inputs)/CLKX/FSX	Default (No Virtual Mode)	
6	CI-FO-	FSX: Output CLKX: Input	AXR(Outputs)/CLKX/FSX	MCASP2_VIRTUAL3_SYNC_RX	See Figure 7-41
			AXR(Inputs)/CLKX/FSX	MCASP2_VIRTUAL3_SYNC_RX	
7	CI-FI-	CLKX / FSX: Input	AXR(Outputs)/CLKX/FSX	MCASP2_VIRTUAL3_SYNC_RX ⁽¹⁾	See Figure 7-42
			AXR(Inputs)/CLKX/FSX	MCASP2_VIRTUAL3_SYNC_RX ⁽¹⁾	
			AXR(Inputs)/CLKX/FSX	MCASP2_VIRTUAL1_SYNC_RX_80M ⁽²⁾	
8	CO-FI-	CLKX: Output FSX: Input	AXR(Outputs)/CLKX/FSX	Default (No Virtual Mode)	See Figure 7-43
			AXR(Inputs)/CLKX/FSX	Default (No Virtual Mode)	

- (1) Used up to 50MHz. Should also be used in a CI-FI- mixed case where AXR operate as both inputs and outputs (that is, AXR are bidirectional).
- (2) Used in 80MHz input only mode when AXR, CLKX and FSX are all inputs.

Table 7-49. Virtual Mode Case Details for McASP3

No.	CASE	CASE Description	Virtual Mode Settings		Notes
			Signals	Virtual Mode Value	
IP Mode : ASYNC					
1	COIFOI	CLKX / FSX: Output CLKR / FSR: Input	AXR(Outputs)/CLKX/FSX	Default (No Virtual Mode)	See Figure 7-36
			AXR(Inputs)/CLKR/FSR	MCASP3_VIRTUAL2_SYNC_RX	
2	COIFIO	CLKX / FSR: Output CLKR / FSX: Input	AXR(Outputs)/CLKX/FSX	Default (No Virtual Mode)	See Figure 7-37
			AXR(Inputs)/CLKR/FSR	MCASP3_VIRTUAL2_SYNC_RX	
3	CIOFIO	CLKR / FSR: Output CLKX / FSX: Input	AXR(Outputs)/CLKX/FSX	MCASP3_VIRTUAL2_SYNC_RX	See Figure 7-38
			AXR(Inputs)/CLKR/FSR	MCASP3_VIRTUAL2_SYNC_RX	
4	CIOFOI	CLKR / FSX: Output CLKX / FSR: Input	AXR(Outputs)/CLKX/FSX	MCASP3_VIRTUAL2_SYNC_RX	See Figure 7-39
			AXR(Inputs)/CLKR/FSR	MCASP3_VIRTUAL2_SYNC_RX	
IP Mode : SYNC (CLKR / FSR internally generated from CLKX / FSX)					
5	CO-FO-	CLKX / FSX: Output	AXR(Outputs)/CLKX/FSX	Default (No Virtual Mode)	See Figure 7-40
			AXR(Inputs)/CLKX/FSX	Default (No Virtual Mode)	
6	CI-FO-	FSX: Output CLKX: Input	AXR(Outputs)/CLKX/FSX	MCASP3_VIRTUAL2_SYNC_RX	See Figure 7-41
			AXR(Inputs)/CLKX/FSX	MCASP3_VIRTUAL2_SYNC_RX	
7	CI-FI-	CLKX / FSX: Input	AXR(Outputs)/CLKX/FSX	MCASP3_VIRTUAL2_SYNC_RX	See Figure 7-42
			AXR(Inputs)/CLKX/FSX	MCASP3_VIRTUAL2_SYNC_RX	
8	CO-FI-	CLKX: Output FSX: Input	AXR(Outputs)/CLKX/FSX	Default (No Virtual Mode)	See Figure 7-43
			AXR(Inputs)/CLKX/FSX	Default (No Virtual Mode)	

Table 7-50. Virtual Mode Case Details for McASP4

No.	CASE	CASE Description	Virtual Mode Settings		Notes
			Signals	Virtual Mode Value	
IP Mode : ASYNC					
1	COIFOI	CLKX / FSX: Output CLKR / FSR: Input	AXR(Outputs)/CLKX/FSX	Default (No Virtual Mode)	See Figure 7-36
			AXR(Inputs)/CLKR/FSR	MCASP4_VIRTUAL1_SYNC_RX	
2	COIFIO	CLKX / FSR: Output CLKR / FSX: Input	AXR(Outputs)/CLKX/FSX	Default (No Virtual Mode)	See Figure 7-37
			AXR(Inputs)/CLKR/FSR	MCASP4_VIRTUAL1_SYNC_RX	
3	CIOFIO	CLKR / FSR: Output CLKX / FSX: Input	AXR(Outputs)/CLKX/FSX	MCASP4_VIRTUAL1_SYNC_RX	See Figure 7-38
			AXR(Inputs)/CLKR/FSR	MCASP4_VIRTUAL1_SYNC_RX	
4	CIOFOI	CLKR / FSX: Output CLKX / FSR: Input	AXR(Outputs)/CLKX/FSX	MCASP4_VIRTUAL1_SYNC_RX	See Figure 7-39
			AXR(Inputs)/CLKR/FSR	MCASP4_VIRTUAL1_SYNC_RX	
IP Mode : SYNC (CLKR / FSR internally generated from CLKX / FSX)					
5	CO-FO-	CLKX / FSX: Output	AXR(Outputs)/CLKX/FSX	Default (No Virtual Mode)	See Figure 7-40
			AXR(Inputs)/CLKX/FSX	Default (No Virtual Mode)	
6	CI-FO-	FSX: Output CLKX: Input	AXR(Outputs)/CLKX/FSX	MCASP4_VIRTUAL1_SYNC_RX	See Figure 7-41
			AXR(Inputs)/CLKX/FSX	MCASP4_VIRTUAL1_SYNC_RX	
7	CI-FI-	CLKX / FSX: Input	AXR(Outputs)/CLKX/FSX	MCASP4_VIRTUAL1_SYNC_RX	See Figure 7-42
			AXR(Inputs)/CLKX/FSX	MCASP4_VIRTUAL1_SYNC_RX	
8	CO-FI-	CLKX: Output FSX: Input	AXR(Outputs)/CLKX/FSX	Default (No Virtual Mode)	See Figure 7-43
			AXR(Inputs)/CLKX/FSX	Default (No Virtual Mode)	

Table 7-51. Virtual Mode Case Details for McASP5

No.	CASE	CASE Description	Virtual Mode Settings		Notes
			Signals	Virtual Mode Value	
IP Mode : ASYNC					
1	COIF OI	CLKX / FSX: Output CLKR / FSR: Input	AXR(Outputs)/CLKX/FSX	Default (No Virtual Mode)	See Figure 7-36
			AXR(Inputs)/CLKR/FSR	MCASP5_VIRTUAL1_SYNC_RX	
2	COIFI O	CLKX / FSR: Output CLKR / FSX: Input	AXR(Outputs)/CLKX/FSX	Default (No Virtual Mode)	See Figure 7-37
			AXR(Inputs)/CLKR/FSR	MCASP5_VIRTUAL1_SYNC_RX	
3	CIOFI O	CLKR / FSR: Output CLKX / FSX: Input	AXR(Outputs)/CLKX/FSX	MCASP5_VIRTUAL1_SYNC_RX	See Figure 7-38
			AXR(Inputs)/CLKR/FSR	MCASP5_VIRTUAL1_SYNC_RX	
4	CIOF OI	CLKR / FSX: Output CLKX / FSR: Input	AXR(Outputs)/CLKX/FSX	MCASP5_VIRTUAL1_SYNC_RX	See Figure 7-39
			AXR(Inputs)/CLKR/FSR	MCASP5_VIRTUAL1_SYNC_RX	
IP Mode : SYNC (CLKR / FSR internally generated from CLKX / FSX)					
5	CO- FO-	CLKX / FSX: Output	AXR(Outputs)/CLKX/FSX	Default (No Virtual Mode)	See Figure 7-40
			AXR(Inputs)/CLKX/FSX	Default (No Virtual Mode)	
6	CI- FO-	FSX: Output CLKX: Input	AXR(Outputs)/CLKX/FSX	MCASP5_VIRTUAL1_SYNC_RX	See Figure 7-41
			AXR(Inputs)/CLKX/FSX	MCASP5_VIRTUAL1_SYNC_RX	
7	CI-FI-	CLKX / FSX: Input	AXR(Outputs)/CLKX/FSX	MCASP5_VIRTUAL1_SYNC_RX	See Figure 7-42
			AXR(Inputs)/CLKX/FSX	MCASP5_VIRTUAL1_SYNC_RX	
8	CO- FI-	CLKX: Output FSX: Input	AXR(Outputs)/CLKX/FSX	Default (No Virtual Mode)	See Figure 7-43
			AXR(Inputs)/CLKX/FSX	Default (No Virtual Mode)	

Table 7-52. Virtual Mode Case Details for McASP6

No.	CASE	CASE Description	Virtual Mode Settings		Notes
			Signals	Virtual Mode Value	
IP Mode : ASYNC					
1	COIF OI	CLKX / FSX: Output CLKR / FSR: Input	AXR(Outputs)/CLKX/FSX	Default (No Virtual Mode)	See Figure 7-36
			AXR(Inputs)/CLKR/FSR	MCASP6_VIRTUAL1_SYNC_RX	
2	COIFI O	CLKX / FSR: Output CLKR / FSX: Input	AXR(Outputs)/CLKX/FSX	Default (No Virtual Mode)	See Figure 7-37
			AXR(Inputs)/CLKR/FSR	MCASP6_VIRTUAL1_SYNC_RX	
3	CIOFI O	CLKR / FSR: Output CLKX / FSX: Input	AXR(Outputs)/CLKX/FSX	MCASP6_VIRTUAL1_SYNC_RX	See Figure 7-38
			AXR(Inputs)/CLKR/FSR	MCASP6_VIRTUAL1_SYNC_RX	
4	CIOF OI	CLKR / FSX: Output CLKX / FSR: Input	AXR(Outputs)/CLKX/FSX	MCASP6_VIRTUAL1_SYNC_RX	See Figure 7-39
			AXR(Inputs)/CLKR/FSR	MCASP6_VIRTUAL1_SYNC_RX	
IP Mode : SYNC (CLKR / FSR internally generated from CLKX / FSX)					
5	CO- FO-	CLKX / FSX: Output	AXR(Outputs)/CLKX/FSX	Default (No Virtual Mode)	See Figure 7-40
			AXR(Inputs)/CLKX/FSX	Default (No Virtual Mode)	
6	CI-FO-	FSX: Output CLKX: Input	AXR(Outputs)/CLKX/FSX	MCASP6_VIRTUAL1_SYNC_RX	See Figure 7-41
			AXR(Inputs)/CLKX/FSX	MCASP6_VIRTUAL1_SYNC_RX	
7	CI-FI-	CLKX / FSX: Input	AXR(Outputs)/CLKX/FSX	MCASP6_VIRTUAL1_SYNC_RX	See Figure 7-42
			AXR(Inputs)/CLKX/FSX	MCASP6_VIRTUAL1_SYNC_RX	
8	CO-FI-	CLKX: Output FSX: Input	AXR(Outputs)/CLKX/FSX	Default (No Virtual Mode)	See Figure 7-43
			AXR(Inputs)/CLKX/FSX	Default (No Virtual Mode)	

Table 7-53. Virtual Mode Case Details for McASP7

No.	CASE	CASE Description	Virtual Mode Settings		Notes
			Signals	Virtual Mode Value	
IP Mode : ASYNC					
1	COIF OI	CLKX / FSX: Output CLKR / FSR: Input	AXR(Outputs)/CLKX/FSX	Default (No Virtual Mode)	See Figure 7-36
			AXR(Inputs)/CLKR/FSR	MCASP7_VIRTUAL2_SYNC_RX	
2	COIFI O	CLKX / FSR: Output CLKR / FSX: Input	AXR(Outputs)/CLKX/FSX	Default (No Virtual Mode)	See Figure 7-37
			AXR(Inputs)/CLKR/FSR	MCASP7_VIRTUAL2_SYNC_RX	
3	CIOFI O	CLKR / FSR: Output CLKX / FSX: Input	AXR(Outputs)/CLKX/FSX	MCASP7_VIRTUAL2_SYNC_RX	See Figure 7-38
			AXR(Inputs)/CLKR/FSR	MCASP7_VIRTUAL2_SYNC_RX	
4	CIOF OI	CLKR / FSX: Output CLKX / FSR: Input	AXR(Outputs)/CLKX/FSX	MCASP7_VIRTUAL2_SYNC_RX	See Figure 7-39
			AXR(Inputs)/CLKR/FSR	MCASP7_VIRTUAL2_SYNC_RX	
IP Mode : SYNC (CLKR / FSR internally generated from CLKX / FSX)					
5	CO-FO-	CLKX / FSX: Output	AXR(Outputs)/CLKX/FSX	Default (No Virtual Mode)	See Figure 7-40
			AXR(Inputs)/CLKX/FSX	Default (No Virtual Mode)	
6	CI-FO-	FSX: Output CLKX: Input	AXR(Outputs)/CLKX/FSX	MCASP7_VIRTUAL2_SYNC_RX	See Figure 7-41
			AXR(Inputs)/CLKX/FSX	MCASP7_VIRTUAL2_SYNC_RX	
7	CI-FI-	CLKX / FSX: Input	AXR(Outputs)/CLKX/FSX	MCASP7_VIRTUAL2_SYNC_RX	See Figure 7-42
			AXR(Inputs)/CLKX/FSX	MCASP7_VIRTUAL2_SYNC_RX	
8	CO-FI-	CLKX: Output FSX: Input	AXR(Outputs)/CLKX/FSX	Default (No Virtual Mode)	See Figure 7-43
			AXR(Inputs)/CLKX/FSX	Default (No Virtual Mode)	

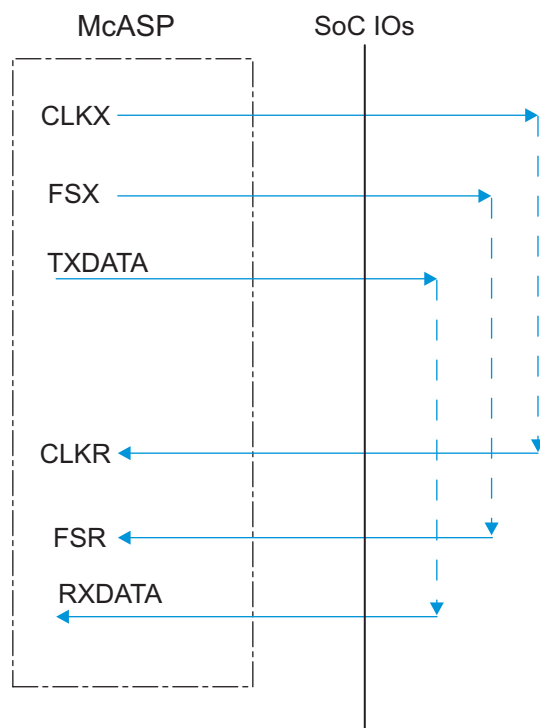


Figure 7-36. McASP1-7 COIFOI – ASYNC Mode

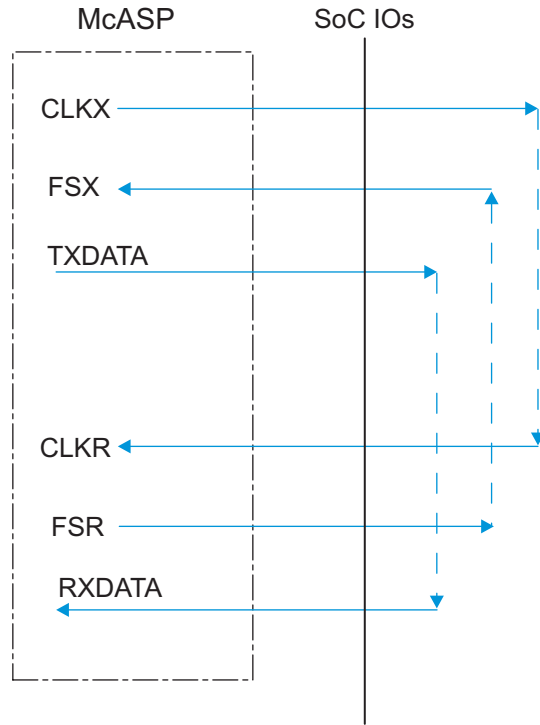


Figure 7-37. McASP1-7 COIFIO – ASYNC Mode

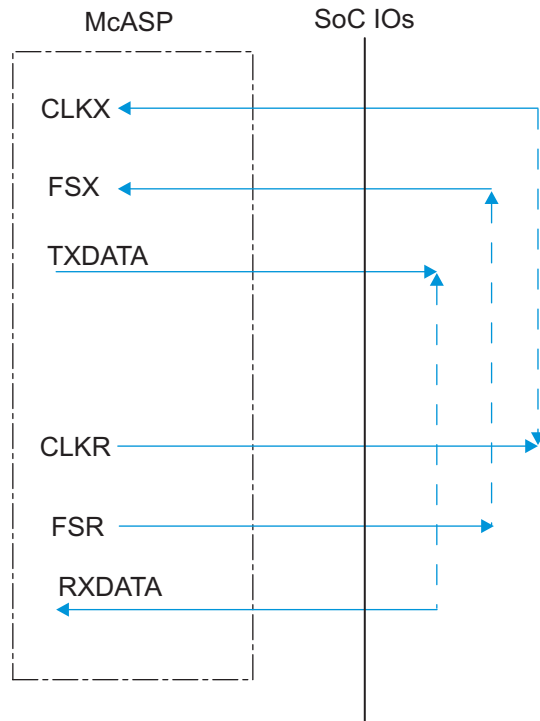


Figure 7-38. McASP1-7 CIOFIO – ASYNC Mode

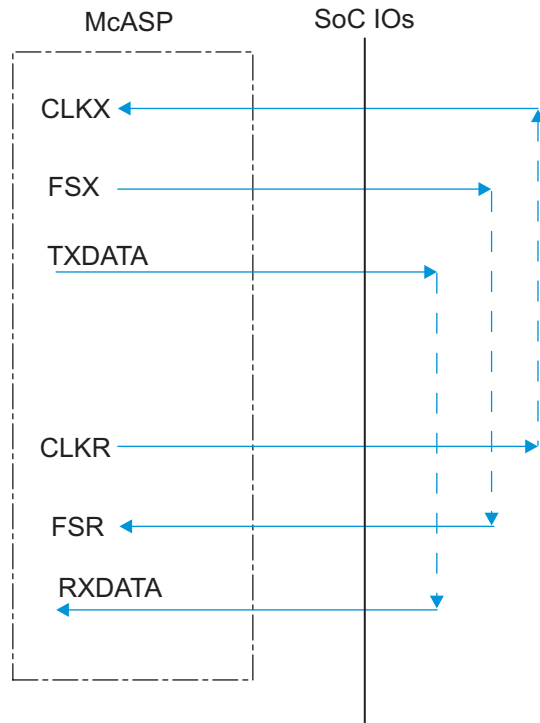


Figure 7-39. McASP1-7 CIOFOI – ASYNC Mode

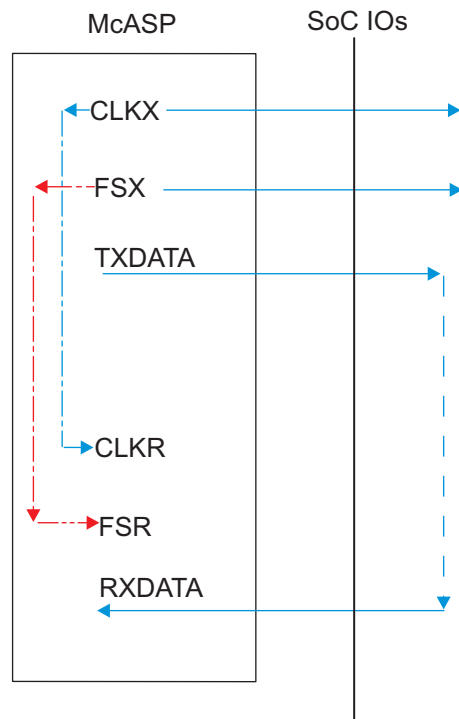


Figure 7-40. McASP1-7 CO-FO- – SYNC Mode

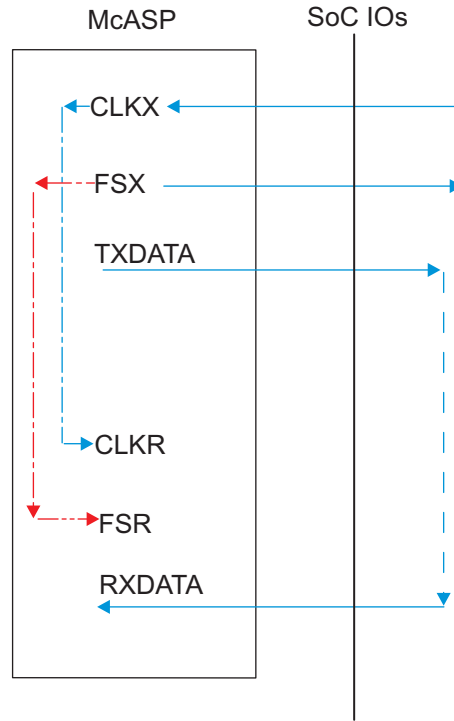


Figure 7-41. McASP1-7 CI-FO – SYNC Mode

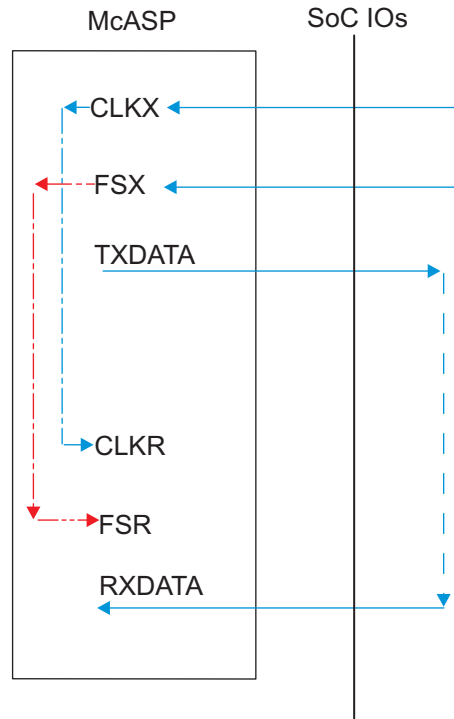


Figure 7-42. McASP1-7 CI-FI – SYNC Mode

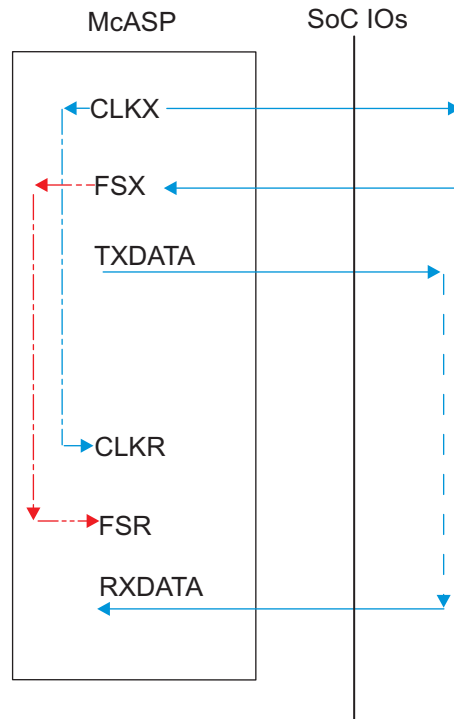


Figure 7-43. McASP1-7 CO-FI- – SYNC Mode

Virtual IO Timings Modes must be used to guarantee some IO timings for McASP1. See [Table 7-2 Modes Summary](#) for a list of IO timings requiring the use of Virtual IO Timings Modes. See [Table 7-54 Virtual Functions Mapping for McASP1](#) for a definition of the Virtual modes.

Table 7-54. Virtual Functions Mapping for McASP1

BALL	BALL NAME	Delay Mode Value			MUXMODE[15:0]	
		MCASP1_VIRTUAL1_ASYNC_TX	MCASP1_VIRTUAL2_SYNC_RX	MCASP1_VIRTUAL3_ASYNC_RX	0	2
C23	xref_clk0	0	15	14		mcasp1_axr4
C22	xref_clk1	0	15	14		mcasp1_axr5
C25	mcasp1_aclkx	8	15	14	mcasp1_aclkx	
B24	mcasp1_fsx	12	15	14	mcasp1_fsx	
B15	mcasp1_axr0	8	15	14	mcasp1_axr0	
A15	mcasp1_axr1	8	15	14	mcasp1_axr1	
A16	mcasp1_axr8	6	15	14	mcasp1_axr8	
A17	mcasp1_axr9	6	15	14	mcasp1_axr9	
A19	mcasp1_axr10	6	15	14	mcasp1_axr10	
A20	mcasp1_axr11	6	15	14	mcasp1_axr11	
A21	mcasp1_axr12	6	15	14	mcasp1_axr12	
A23	mcasp1_axr13	6	15	14	mcasp1_axr13	
C15	mcasp1_axr14	6	15	14	mcasp1_axr14	
B16	mcasp1_axr15	6	15	14	mcasp1_axr15	

1. NA in this table stands for Not Applicable.

Virtual IO Timings Modes must be used to guarantee some IO timings for McASP2. See [Table 7-2 Modes Summary](#) for a list of IO timings requiring the use of Virtual IO Timings Modes. See [Table 7-55 Virtual Functions Mapping for McASP2](#) for a definition of the Virtual modes.

[Table 7-55](#) presents the values for DELAYMODE bitfield.

Table 7-55. Virtual Functions Mapping for McASP2

BALL	BALL NAME	Delay Mode Value					MUXMODE[15:0]		
		MCASP2_VIRTUAL1_ASYNC_RX_80M	MCASP2_VIRTUAL2_ASYNC_RX	MCASP2_VIRTUAL3_ASYNC_TX	MCASP2_VIRTUAL4_SYNC_RX	MCASP2_VIRTUAL5_SYNC_RX_80M	0	1	2
C23	xref_clk0	10	9	4	8	6		mcasp2_axr8	
C22	xref_clk1	10	9	4	8	6		mcasp2_axr9	
B21	mcasp2_aclkr	15	14	10	N/A	N/A	mcasp2_aclkr		
B20	mcasp2_fsr	15	14	10	N/A	N/A	mcasp2_fsr		
B23	mcasp2_axr4	15	14	7	13	12	mcasp2_axr4		
B17	mcasp2_axr5	15	14	7	13	12	mcasp2_axr5		
B19	mcasp3_axr0	15	14	4	10	9			mcasp2_axr14
C16	mcasp3_axr1	15	14	3	10	8			mcasp2_axr15

1. NA in this table stands for Not Applicable.

Virtual IO Timings Modes must be used to guarantee some IO timings for McASP3/4/5/6/7. See [Table 7-2 Modes Summary](#) for a list of IO timings requiring the use of Virtual IO Timings Modes. See [Table 7-56 Virtual Functions Mapping for McASP3/4/5/6/7](#) for a definition of the Virtual modes.

[Table 7-56](#) presents the values for DELAYMODE bitfield.

Table 7-56. Virtual Functions Mapping for McASP3/4/5/6/7

BALL	BALL NAME	Delay Mode Value	MUXMODE[15:0]		
			0	1	2
MCASP3_VIRTUAL2_SYNC_RX					
B23	mcasp2_axr2	8		mcasp3_axr2	
B17	mcasp2_axr3	8		mcasp3_axr3	
B19	mcasp3_aclkx	8	mcasp3_aclkx	mcasp3_aclkr	
C16	mcasp3_fsx	8	mcasp3_fsx	mcasp3_fsr	
C17	mcasp3_axr0	8	mcasp3_axr0		
C20	mcasp3_axr1	6	mcasp3_axr1		
MCASP4_VIRTUAL1_SYNC_RX					
C23	mcasp1_axr4	13		mcasp4_axr2	
C22	mcasp1_axr5	13		mcasp4_axr3	
E24	mcasp4_aclkx	15	mcasp4_aclkx	mcasp4_aclkr	
D23	mcasp4_fsx	15	mcasp4_fsx	mcasp4_fsr	
E25	mcasp4_axr0	15	mcasp4_axr0		

Table 7-56. Virtual Functions Mapping for McASP3/4/5/6/7 (continued)

BALL	BALL NAME	Delay Mode Value	MUXMODE[15:0]		
			0	1	2
E23	mcasp4_axr1	15	mcasp4_axr1		
MCASP5_VIRTUAL1_SYNC_RX					
V1	mcasp5_aclkx	15	mcasp5_aclkx	mcasp5_aclkr	
W2	mcasp5_fsx	15	mcasp5_fsx	mcasp5_fsr	
V2	mcasp5_axr0	15	mcasp5_axr0		
U1	mcasp5_axr1	15	mcasp5_axr1		
MCASP6_VIRTUAL1_SYNC_RX					
A16	mcasp1_axr8	10		mcasp6_axr0	
A17	mcasp1_axr9	10		mcasp6_axr1	
A19	mcasp1_axr10	10		mcasp6_aclkx	mcasp6_aclkr
A20	mcasp1_axr11	10		mcasp6_fsx	mcasp6_fsr
MCASP7_VIRTUAL2_SYNC_RX					
A21	mcasp1_axr12	10		mcasp7_axr0	
A23	mcasp1_axr13	10		mcasp7_axr1	
C15	mcasp1_axr14	10		mcasp7_aclkx	mcasp7_aclkr
B16	mcasp1_axr15	10		mcasp7_fsx	mcasp7_fsr

7.17 Universal Serial Bus (USB)

SuperSpeed USB DRD Subsystem has four instances in the device providing the following functions:

- USB1: SuperSpeed (SS) USB 3.0 Dual-Role-Device (DRD) subsystem with integrated SS (USB3.0) PHY and HS/FS (USB2.0) PHY.
- USB2: High-Speed (HS) USB 2.0 Dual-Role-Device (DRD) subsystem with integrated HS/FS PHY.
- USB3: HS USB 2.0 Dual-Role-Device (DRD) subsystem with ULPI (SDR) interface to external HS/FS PHYs.
- USB4: HS USB 2.0 Dual-Role-Device (DRD) subsystem with ULPI (SDR) interface to external HS/FS PHYs.

NOTE

For more information, see the SuperSpeed USB DRD section of the Device TRM.

7.17.1 USB1 DRD PHY

The USB1 DRD interface supports the following applications:

- USB2.0 High-Speed PHY port (1.8 V and 3.3 V): this asynchronous high-speed interface is compliant with the USB2.0 PHY standard with an internal transceiver (USB2.0 standard v2.0), for a maximum data rate of 480 Mbps.
- USB3.0 Super-Speed PHY port (1.8 V): this asynchronous differential super-speed interface is compliant with the USB3.0 RX/TX PHY standard (USB3.0 standard v1.0) for a maximum data bit rate of 5Gbps.

7.17.2 USB2 PHY

The USB2 interface supports the following applications:

- USB2.0 High-Speed PHY port (1.8 V and 3.3 V): this asynchronous high-speed interface is compliant with the USB2.0 PHY standard with an internal transceiver (USB2.0 standard v2.0), for a maximum data rate of 480 Mbps.

7.17.3 USB3 and USB4 DRD ULPI—SDR—Slave Mode—12-pin Mode

The USB3 and USB4 DRD interfaces support the following application:

- USB ULPI port: this synchronous interface is compliant with the USB2.0 ULPI SDR standard (UTMI+ v1.22), for alternative off-chip USB2.0 PHY interface; that is, with external transceiver with a maximum frequency of 60 MHz (synchronous slave mode, SDR, 12-pin, 8-data-bit).

NOTE

The Universal Serial Bus k ULPI modules are also referred as USBk where k = 3, 4.

Table 7-57, Table 7-58 and Figure 7-44 assume testing over the recommended operating conditions and electrical characteristic conditions.

Table 7-57. Timing Requirements for ULPI SDR Slave Mode

NO.	PARAMETER	DESCRIPTION	MIN	MAX	UNIT
US1	$t_{c(\text{clk})}$	Cycle time, usb_ulpi_clk period	16.66		ns
US5	$t_{su(\text{ctrlV-clkH})}$	Setup time, usb_ulpi_dir/usb_ulpi_nxt valid before usb_ulpi_clk rising edge	6.73		ns
US6	$t_{h(\text{clkH-ctrlV})}$	Hold time, usb_ulpi_dir/usb_ulpi_nxt valid after usb_ulpi_clk rising edge	-0.41		ns

Table 7-57. Timing Requirements for ULPI SDR Slave Mode (continued)

NO.	PARAMETER	DESCRIPTION	MIN	MAX	UNIT
US7	$t_{su(dV-clkH)}$	Setup time, usb_ulpi_d[7:0] valid before usb_ulpi_clk rising edge	6.73		ns
US8	$t_{h(clkH-dV)}$	Hold time, usb_ulpi_d[7:0] valid after usb_ulpi_clk rising edge	-0.41		ns

Table 7-58. Switching Characteristics for ULPI SDR Slave Mode

NO.	PARAMETER	DESCRIPTION	MIN	MAX	UNIT
US4	$t_{d(clkH-stpV)}$	Delay time, usb_ulpi_clk rising edge high to output usb_ulpi_stp valid	0.44	8.35	ns
US9	$t_{d(clkL-dov)}$	Delay time, usb_ulpi_clk rising edge high to output usb_ulpi_d[7:0] valid	0.44	8.35	ns

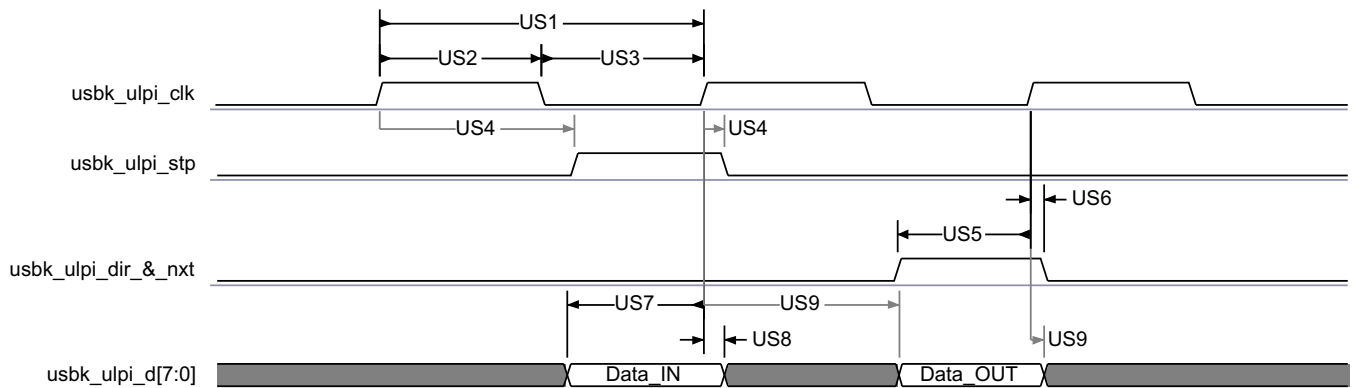


Figure 7-44. HS USB3 and USB4 ULPI —SDR—Slave Mode—12-pin Mode

In [Table 7-59](#) are presented the specific groupings of signals (IOSET) for use with USB3 and USB4 signals.

Table 7-59. USB3 and USB4 IOSETs

SIGNALS	IOSET1		IOSET2	
	BALL	MUX	BALL	MUX
USB3				
usb3_ulpi_d7	AD3	2	Y1	3
usb3_ulpi_d6	AC3	2	W1	3
usb3_ulpi_d5	AD2	2	W5	3
usb3_ulpi_d4	AB3	2	W4	3
usb3_ulpi_d3	AA2	2	U6	3
usb3_ulpi_d2	AC2	2	V6	3
usb3_ulpi_d1	Y3	2	U5	3
usb3_ulpi_d0	AB2	2	V3	3
usb3_ulpi_nxt	AB1	2	V5	3
usb3_ulpi_dir	AC1	2	W6	3
usb3_ulpi_stp	AA1	2	W3	3
usb3_ulpi_clk	Y2	2	V4	3
USB4				
usb4_ulpi_d7		5	R4	6
usb4_ulpi_d6		5	T3	6
usb4_ulpi_d5		5	U4	6
usb4_ulpi_d4		5	P5	6

Table 7-59. USB3 and USB4 IOSETs (continued)

SIGNALS	IOSET1		IOSET2	
	BALL	MUX	BALL	MUX
usb4_ulpi_d3		5	U3	6
usb4_ulpi_d2		5	U2	6
usb4_ulpi_d1		5	R5	6
usb4_ulpi_d0		5	T4	6
usb4_ulpi_stp		5	P6	6
usb4_ulpi_clk		5	R6	6
usb4_ulpi_dir		5	T5	6
usb4_ulpi_nxt		5	T6	6

7.18 Peripheral Component Interconnect Express (PCIe)

The device supports connections to PCIe-compliant devices via the integrated PCIe master/slave bus interface. The PCIe module is comprised of a dual-mode PCIe core and a SerDes PHY. Each PCIe subsystem controller has support for PCIe Gen-II mode (5.0 Gbps /lane) and Gen-I mode (2.5 Gbps/lane) (Single Lane and Flexible dual lane configuration).

The device PCIe supports the following features:

- 16-bit operation @250 MHz on PIPE interface (per 16-bit lane)
- Supports 1 ports x 1 lane configuration
- Single virtual channel (VC0), single traffic class (TC0)
- Single function in end-point mode
- Automatic width and speed negotiation
- Max payload: 128 byte outbound, 256 byte inbound
- Automatic credit management
- ECRC generation and checking
- Configurable BAR filtering
- Legacy interrupt reception (RC) and generation (EP)
- MSI generation and reception
- PCI Express Active State Power Management (ASPM) state L0s and L1 (with exceptions)
- All PCI Device Power Management D-states with the exception of D3_{cold} / L2 state

The PCIe controller on this device conforms to the PCI Express Base 3.0 Specification, revision 1.0 and the PCI Local Bus Specification, revision 3.0.

NOTE

For more information, see the PCIe Controller section of the Device TRM.

7.19 Controller Area Network Interface (DCAN)

The device provides two DCAN interfaces for supporting distributed realtime control with a high level of security. The DCAN interfaces implement the following features:

- Supports CAN protocol version 2.0 part A, B
- Bit rates up to 1 MBit/s
- 64 message objects
- Individual identifier mask for each message object
- Programmable FIFO mode for message objects
- Programmable loop-back modes for self-test operation

- Suspend mode for debug support
- Software module reset
- Automatic bus on after Bus-Off state by a programmable 32-bit timer
- Direct access to Message RAM during test mode
- CAN Rx/Tx pins are configurable as general-purpose IO pins
- Two interrupt lines (plus additional parity-error interrupts line)
- RAM initialization
- DMA support

NOTE

For more information, see the DCAN section of the Device TRM.

NOTE

The Controller Area Network Interface x (x = 1 to 2) is also referred to as DCANx.

NOTE

Refer to the CAN Specification for calculations necessary to validate timing compliance. Jitter tolerance calculations must be performed to validate the implementation.

Table 7-60 and Table 7-61 present timing and switching characteristics for DCANx Interface.

Table 7-60. Timing Requirements for DCANx Receive

NO.	PARAMETER	DESCRIPTION	MIN	NOM	MAX	UNIT
-	f(baud)	Maximum programmable baud rate			1	Mbps
-	t _{d(DCANRX)}	Delay time, DCANx_RX pin to receive shift register			15	ns

Table 7-61. Switching Characteristics Over Recommended Operating Conditions for DCANx Transmit

NO.	PARAMETER	DESCRIPTION	MIN	MAX	UNIT
-	f(baud)	Maximum programmable baud rate		1	Mbps
-	t _{d(DCANTX)}	Delay time, Transmit shift register to DCANx_TX pin ⁽¹⁾		15	ns

(1) These values do not include rise/fall times of the output buffer.

7.20 Ethernet Interface (GMAC_SW)

The three-port gigabit ethernet switch subsystem (GMAC_SW) provides ethernet packet communication and can be configured as an ethernet switch. It provides the Gigabit Media Independent Interface (G/MII) in MII mode, Reduced Gigabit Media Independent Interface (RGMII), Reduced Media Independent Interface (RMII), and the Management Data Input/Output (MDIO) for physical layer device (PHY) management.

NOTE

For more information, see the Ethernet Subsystem section of the Device TRM.

NOTE

The Gigabit, Reduced and Media Independent Interface n (n = 0 to 1) are also referred to as MII_n, RMII_n and RGMII_n

CAUTION

The IO timings provided in this section are only valid if signals within a single IOSET are used. The IOSETs are defined in the [Table 7-66](#), [Table 7-69](#), [Table 7-74](#) and [Table 7-81](#).

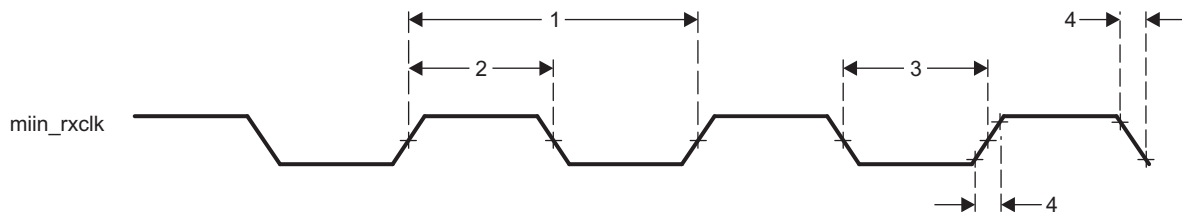
CAUTION

The IO Timings provided in this section are only valid for some GMAC usage modes when the corresponding Virtual IO Timings or Manual IO Timings are configured as described in the tables found in this section.

[Table 7-62](#) and [Figure 7-45](#) present timing requirements for MII in receive operation.

7.20.1 GMAC MII Timings**Table 7-62. Timing Requirements for miin_rxclk - MII Operation**

NO.	PARAMETER	DESCRIPTION	SPEED	MIN	MAX	UNIT
1	$t_{c(RX_CLK)}$	Cycle time, miin_rxclk	10 Mbps	400		ns
			100 Mbps	40		ns
2	$t_{w(RX_CLKH)}$	Pulse duration, miin_rxclk high	10 Mbps	140	260	ns
			100 Mbps	14	26	ns
3	$t_{w(RX_CLKL)}$	Pulse duration, miin_rxclk low	10 Mbps	140	260	ns
			100 Mbps	14	26	ns
4	$t_t(RX_CLK)$	Transition time, miin_rxclk	10 Mbps		3	ns
			100 Mbps		3	ns

**Figure 7-45. Clock Timing (GMAC Receive) - MII operation**

[Table 7-63](#) and [Figure 7-46](#) present timing requirements for MII in transmit operation.

Table 7-63. Timing Requirements for miin_txclk - MII Operation

NO.	PARAMETER	DESCRIPTION	SPEED	MIN	MAX	UNIT
1	$t_{c(TX_CLK)}$	Cycle time, miin_txclk	10 Mbps	400		ns
			100 Mbps	40		ns
2	$t_{w(TX_CLKH)}$	Pulse duration, miin_txclk high	10 Mbps	140	260	ns
			100 Mbps	14	26	ns
3	$t_{w(TX_CLKL)}$	Pulse duration, miin_txclk low	10 Mbps	140	260	ns
			100 Mbps	14	26	ns
4	$t_t(TX_CLK)$	Transition time, miin_txclk	10 Mbps		3	ns
			100 Mbps		3	ns

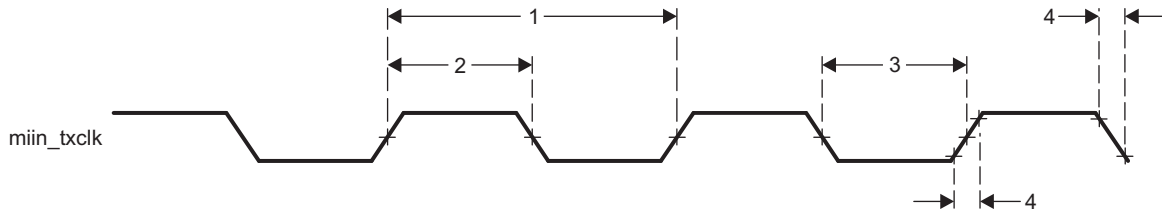


Figure 7-46. Clock Timing (GMAC Transmit) - MII operation

Table 7-64 and Figure 7-47 present timing requirements for GMAC MII Receive 10/100Mbit/s.

Table 7-64. Timing Requirements for GMAC MII Receive 10/100 Mbit/s

NO.	PARAMETER	DESCRIPTION	MIN	MAX	UNIT
1	$t_{su}(RXD-RX_CLK)$	Setup time, receive selected signals valid before miin_rxclk	8		ns
	$t_{su}(RX_DV-RX_CLK)$				
	$t_{su}(RX_ER-RX_CLK)$				
2	$t_h(RX_CLK-RXD)$	Hold time, receive selected signals valid after miin_rxclk	8		ns
	$t_h(RX_CLK-RX_DV)$				
	$t_h(RX_CLK-RX_ER)$				

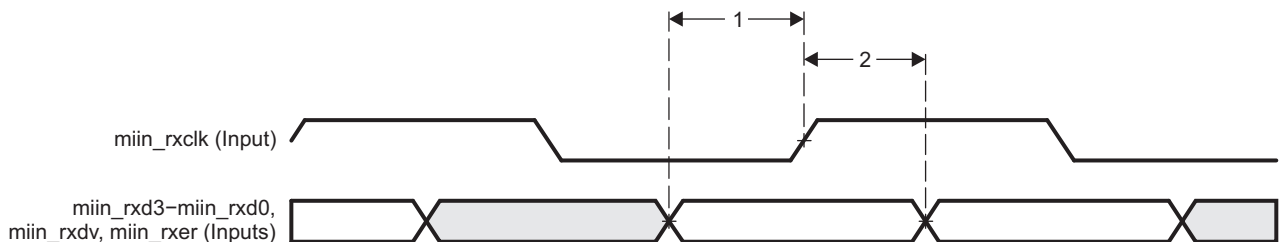


Figure 7-47. GMAC Receive Interface Timing MII operation

Table 7-65 and Figure 7-48 present timing requirements for GMAC MII Transmit 10/100Mbit/s.

Table 7-65. Switching Characteristics Over Recommended Operating Conditions for GMAC MII Transmit 10/100 Mbits/s

NO.	PARAMETER	DESCRIPTION	MIN	MAX	UNIT
1	$t_d(TX_CLK-TXD)$	Delay time, miin_txclk to transmit selected signals valid	0	25	ns
	$t_d(TX_CLK-TX_EN)$				

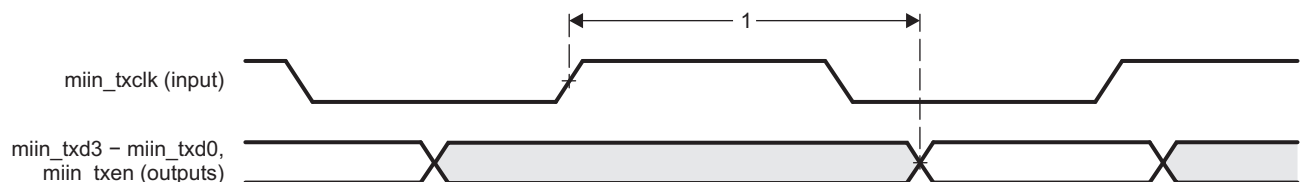


Figure 7-48. GMAC Transmit Interface Timing MII operation

In Table 7-66 are presented the specific groupings of signals (IOSET) for use with GMAC MII signals.

Table 7-66. GMAC MII IOSETS

SIGNALS	IOSET5		IOSET6	
	BALL	MUX	BALL	MUX
GMAC MII1				

Table 7-66. GMAC MII IOSETs (continued)

SIGNALS	IOSET5		IOSET6	
	BALL	MUX	BALL	MUX
mii1_txd3	A8	8		
mii1_txd2	B8	8		
mii1_txd1	B7	8		
mii1_txd0	D6	8		
mii1_rxd3	C5	8		
mii1_rxd2	B5	8		
mii1_rxd1	A4	8		
mii1_rxd0	A7	8		
mii1_col	D8	8		
mii1_rxer	C8	8		
mii1_txer	D7	8		
mii1_txen	E9	8		
mii1_crs	F8	8		
mii1_rxclk	E8	8		
mii1_txclk	C7	8		
mii1_rxdv	A6	8		
GMAC MII0				
mii0_txd3			U3	3
mii0_txd2			P5	3
mii0_txd1			T3	3
mii0_txd0			R4	3
mii0_rxd3			R6	3
mii0_rxd2			P6	3
mii0_rxd1			T4	3
mii0_rxd0			R5	3
mii0_txclk			U2	3
mii0_txer			T1	3
mii0_rxer			T6	3
mii0_rxdv			R1	3
mii0_crs			T5	3
mii0_col			R3	3
mii0_rxclk			T2	3
mii0_txen			U4	3

7.20.2 GMAC MDIO Interface Timings

CAUTION

The IO Timings provided in this section are only valid for some GMAC usage modes when the corresponding Virtual IO Timings or Manual IO Timings are configured as described in the tables found in this section.

Table 7-67, Table 7-67 and Figure 7-49 present timing requirements for MDIO.

Table 7-67. Timing Requirements for MDIO Input

No	PARAMETER	DESCRIPTION	MIN	MAX	UNIT
MDIO1	$t_{c(MDC)}$	Cycle time, MDC	400		ns
MDIO2	$t_{w(MDCH)}$	Pulse Duration, MDC High	160		ns
MDIO3	$t_{w(MDCL)}$	Pulse Duration, MDC Low	160		ns
MDIO4	$t_{su(MDIO-MDC)}$	Setup time, MDIO valid before MDC High	90		ns
MDIO5	$t_{h(MDIO_MDC)}$	Hold time, MDIO valid from MDC High	0		ns

Table 7-68. Switching Characteristics Over Recommended Operating Conditions for MDIO Output

NO	PARAMETER	DESCRIPTION	MIN	MAX	UNIT
MDIO6	$t_{t(MDC)}$	Transition time, MDC		5	ns
MDIO7	$t_{d(MDC-MDIO)}$	Delay time, MDC High to MDIO valid	10	390	ns

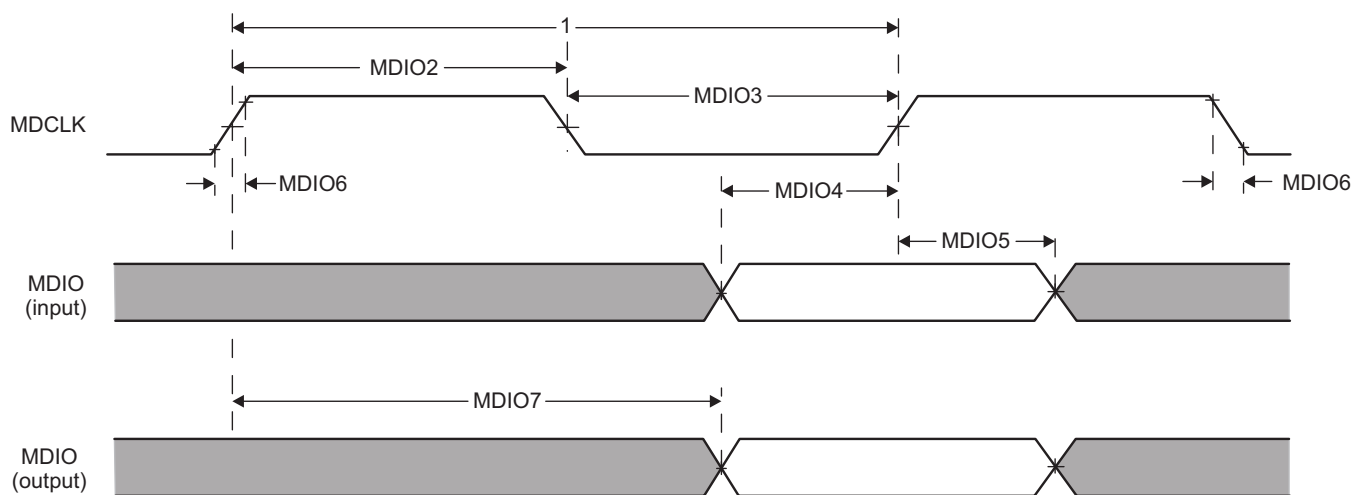


Figure 7-49. GMAC MDIO diagrams

In [Table 7-69](#) are presented the specific groupings of signals (IOSET) for use with GMAC MDIO signals.

Table 7-69. GMAC MDIO IOSETs

SIGNALS	IOSET7		IOSET8		IOSET9		IOSET10	
	BALL	MUX	BALL	MUX	BALL	MUX	BALL	MUX
mdio_d	B6	3	T1	0	W1	1	C24	5
mdio_mclk	A5	3	R3	0	Y1	1	C19	5

7.20.3 GMAC RMII Timings

The main reference clock REF_CLK (RMII_50MHZ_CLK) of RMII interface is internally supplied from PRCM. The source of this clock could be either externally sourced from the RMII_MHZ_50_CLK pin of the device or internally generated from DPLL_GMAC output clock GMAC_RMII_HS_CLK. Please see the PRCM chapter of the device TRM for full details about RMII reference clock.

CAUTION

The IO Timings provided in this section are only valid for some GMAC usage modes when the corresponding Virtual IO Timings or Manual IO Timings are configured as described in the tables found in this section.

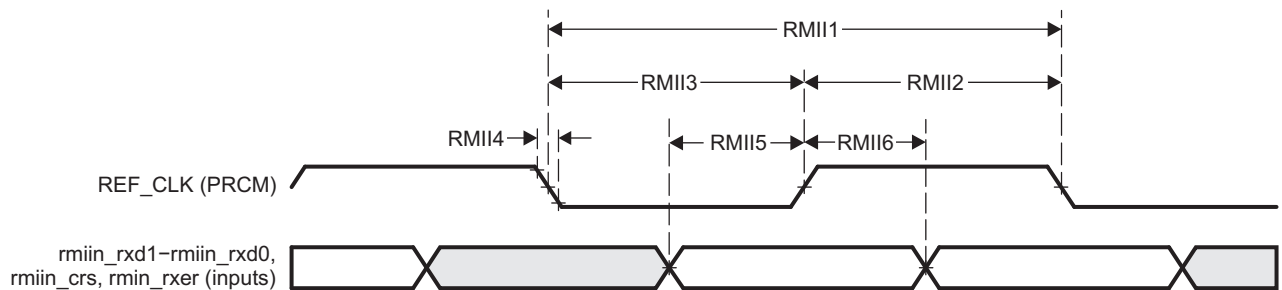
Table 7-70, Table 7-71 and Figure 7-50 present timing requirements for GMAC RMII In Receive.

Table 7-70. Timing Requirements for GMAC REF_CLK - RMII Operation

NO.	PARAMETER	DESCRIPTION	MIN	MAX	UNIT
RMII1	$t_{c(REF_CLK)}$	Cycle time, REF_CLK	20		ns
RMII2	$t_{w(REF_CLKH)}$	Pulse duration, REF_CLK high	7	13	ns
RMII3	$t_{w(REF_CLKL)}$	Pulse duration, REF_CLK low	7	13	ns
RMII4	$t_{tt(REF_CLK)}$	Transistion time, REF_CLK		3	ns

Table 7-71. Timing Requirements for GMAC RMII In Receive

NO.	PARAMETER	DESCRIPTION	MIN	MAX	UNIT
RMII5	$t_{su(RXD-REF_CLK)}$	Setup time, receive selected signals valid before REF_CLK	4		ns
	$t_{su(CRS_DV-REF_CLK)}$				
	$t_{su(RX_ER-REF_CLK)}$				
RMII6	$t_{h(REF_CLK-RXD)}$	Hold time, receive selected signals valid after REF_CLK	2		ns
	$t_{h(REF_CLK-CRS_DV)}$				
	$t_{h(REF_CLK-RX_ER)}$				



SPRS8xx_GMAC_RMII RX_05

Figure 7-50. GMAC Receive Interface Timing RMII In operation

Table 7-72, Table 7-72 and Figure 7-51 present switching characteristics for GMAC RMII In Transmit 10/100Mbit/s.

Table 7-72. Switching Characteristics Over Recommended Operating Conditions for GMAC REF_CLK - RMII Operation

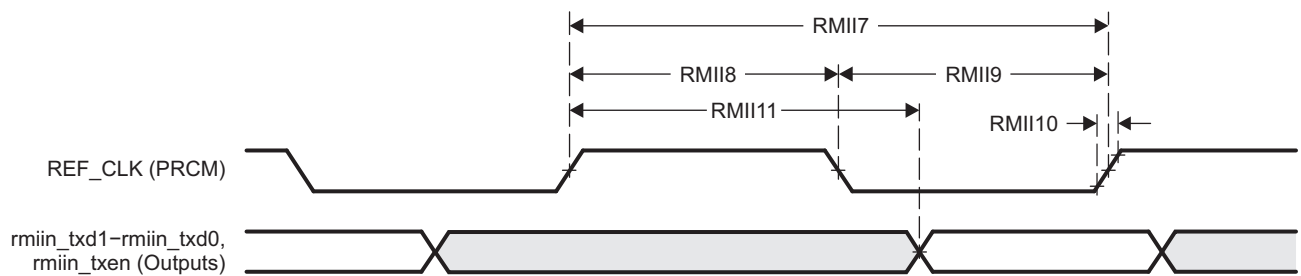
NO.	PARAMETER	DESCRIPTION	RMII In	MIN	MAX	UNIT
RMII7	$t_{c(REF_CLK)}$	Cycle time, REF_CLK		20		ns
RMII8	$t_{w(REF_CLKH)}$	Pulse duration, REF_CLK high		7	13	ns

Table 7-72. Switching Characteristics Over Recommended Operating Conditions for GMAC REF_CLK - RMIIO Operation (continued)

NO.	PARAMETER	DESCRIPTION	RMIIn	MIN	MAX	UNIT
RMIIO9	$t_w(\text{REF_CLKL})$	Pulse duration, REF_CLK low		7	13	ns
RMIIO10	$t_t(\text{REF_CLK})$	Transistion time, REF_CLK			3	ns

Table 7-73. Switching Characteristics Over Recommended Operating Conditions for GMAC RMIIn Transmit 10/100 Mbits/s

NO.	PARAMETER	DESCRIPTION	RMIIn	MIN	MAX	UNIT
RMIIO11	$t_d(\text{REF_CLK-TXD})$	Delay time, REF_CLK high to selected transmit signals valid	RMIIO	2	13.5	ns
	$t_{dd}(\text{REF_CLK-TXEN})$					
	$t_d(\text{REF_CLK-TXD})$		RMIIO1	2	13.8	ns
	$t_{dd}(\text{REF_CLK-TXEN})$					



SPRS952D_GMAC_RMIIOX_06

Figure 7-51. GMAC Transmit Interface Timing RMIIn Operation

In [Table 7-74](#) are presented the specific groupings of signals (IOSET) for use with GMAC RMIIO signals.

Table 7-74. GMAC RMIIO IOSETs

SIGNALS	IOSET1		IOSET2	
	BALL	MUX	BALL	MUX
GMAC RMIIO1				
RMIIO_MHZ_50_CLK	R2	0		
rmiio1_txd1	U3	2		
rmiio1_txd0	P5	2		
rmiio1_rxd1	R6	2		
rmiio1_rxd0	P6	2		
rmiio1_rxer	T2	2		
rmiio1_txen	U2	2		
rmiio1_crs	R1	2		
GMAC RMIIO0				
RMIIO_MHZ_50_CLK			R2	0
rmiio0_txd1			T3	1
rmiio0_txd0			R4	1
rmiio0_rxd1			T4	1
rmiio0_rxd0			R5	1
rmiio0_txen			U4	1
rmiio0_rxer			T6	1
rmiio0_crs			T5	1

Manual IO Timings Modes must be used to guarantee some IO timings for GMAC. See [Table 7-2 Modes Summary](#) for a list of IO timings requiring the use of Manual IO Timings Modes. See [Table 7-75 Manual Functions Mapping for GMAC RMII0](#) for a definition of the Manual modes.

[Table 7-75](#) lists the A_DELAY and G_DELAY values needed to calculate the correct values to be set in the CFG_x registers.

Table 7-75. Manual Functions Mapping for GMAC RMII0

BALL	BALL NAME	GMAC_RMII0_MANUAL1		CFG REGISTER	MUXMODE	
		A_DELAY (ps)	G_DELAY (ps)		0	1
R2	RMII_MHZ_50_CLK	0	0	CFG_RMII_MHZ_50_CLK_IN	RMII_MHZ_50_CLK	
R5	rgmii0_txd0	500	500	CFG_RGMII0_TXD0_IN		rmii0_rxd0
T4	rgmii0_txd1	840	1000	CFG_RGMII0_TXD1_IN		rmii0_rxd1
T6	rgmii0_txd2	360	840	CFG_RGMII0_TXD2_IN		rmii0_rxer
T5	rgmii0_txd3	600	1000	CFG_RGMII0_TXD3_IN		rmii0_crs

Manual IO Timings Modes must be used to guarantee some IO timings for GMAC. See [Table 7-2 Modes Summary](#) for a list of IO timings requiring the use of Manual IO Timings Modes. See [Table 7-76 Manual Functions Mapping for GMAC RMII1](#) for a definition of the Manual modes.

[Table 7-76](#) list the A_DELAY and G_DELAY values needed to calculate the correct values to be set in the CFG_x registers.

Table 7-76. Manual Functions Mapping for GMAC RMII1

BALL	BALL NAME	GMAC_RMII1_MANUAL1		CFG REGISTER	MUXMODE	
		A_DELAY (ps)	G_DELAY (ps)		0	2
R2	RMII_MHZ_50_CLK	0	0	CFG_RMII_MHZ_50_CLK_IN	RMII_MHZ_50_CLK	
P6	rgmii0_txctl	300	1000	CFG_RGMII0_TXCTL_IN		rmii1_rxd0
R6	rgmii0_txc	300	1200	CFG_RGMII0_TXC_IN		rmii1_rxd1
T2	uart3_txd	300	500	CFG_UART3_TXD_IN		rmii1_rxer
R1	uart3_rxd	400	700	CFG_UART3_RXD_IN		rmii1_crs

7.20.4 GMAC RGMII Timings

CAUTION

The IO Timings provided in this section are only valid for some GMAC usage modes when the corresponding Virtual IO Timings or Manual IO Timings are configured as described in the tables found in this section.

[Table 7-77](#), [Table 7-78](#) and [Figure 7-52](#) present timing requirements for receive RGMII operation.

Table 7-77. Timing Requirements for rgmiin_rxc - RGMII Operation

NO.	PARAMETER	DESCRIPTION	SPEED	MIN	MAX	UNIT
1	$t_{c(RXC)}$	Cycle time, rgmiin_rxc	10 Mbps	360	440	ns
			100 Mbps	36	44	ns
			1000 Mbps	7.2	8.8	ns
2	$t_{w(RXCH)}$	Pulse duration, rgmiin_rxc high	10 Mbps	160	240	ns
			100 Mbps	16	24	ns
			1000 Mbps	3.6	4.4	ns

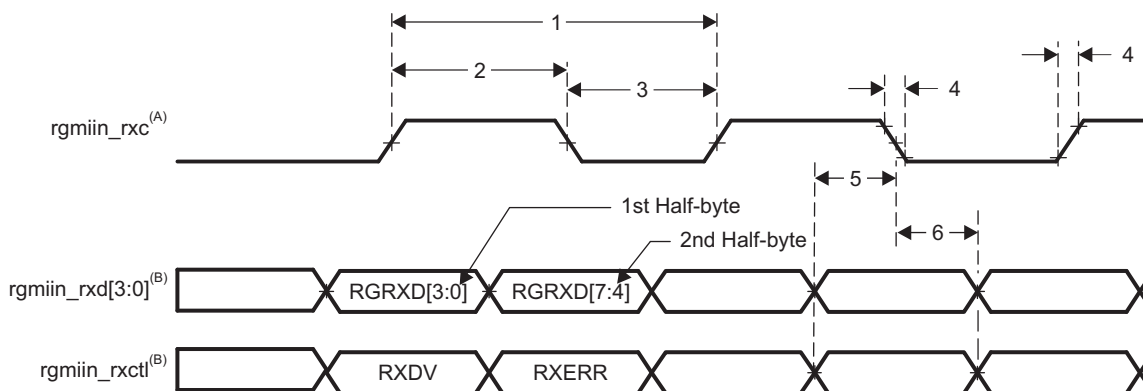
Table 7-77. Timing Requirements for rgmiin_rxc - RGMII Operation (continued)

NO.	PARAMETER	DESCRIPTION	SPEED	MIN	MAX	UNIT
3	$t_{w(RXCL)}$	Pulse duration, rgmiin_rxc low	10 Mbps	160	240	ns
			100 Mbps	16	24	ns
			1000 Mbps	3.6	4.4	ns
4	$t_{t(RXC)}$	Transition time, rgmiin_rxc	10 Mbps		0.75	ns
			100 Mbps		0.75	ns
			1000 Mbps		0.75	ns

Table 7-78. Timing Requirements for GMAC RGMII Input Receive for 10/100/1000 Mbps

NO.	PARAMETER	DESCRIPTION	MIN	MAX	UNIT
5	$t_{su(RXD-RXCH)}$	Setup time, receive selected signals valid before rgmiin_rxc high/low	1		ns
6	$t_{h(RXCH-RXD)}$	Hold time, receive selected signals valid after rgmiin_rxc high/low	1		ns

(1) For RGMII, receive selected signals include: rgmiin_rxd[3:0] and rgmiin_rxctl.



- A. $rgmiin_rxc$ must be externally delayed relative to the data and control pins.
- B. Data and control information is received using both edges of the clocks. $rgmiin_rxd[3:0]$ carries data bits 3-0 on the rising edge of $rgmiin_rxc$ and data bits 7-4 on the falling edge of $rgmiin_rxc$. Similarly, $rgmiin_rxctl$ carries RXDV on rising edge of $rgmiin_rxc$ and RXERR on falling edge of $rgmiin_rxc$.

Figure 7-52. GMAC Receive Interface Timing, RGMII operation

Table 7-79, Table 7-80 and Figure 7-53 present switching characteristics for transmit - RGMII for 10/100/1000Mbit/s.

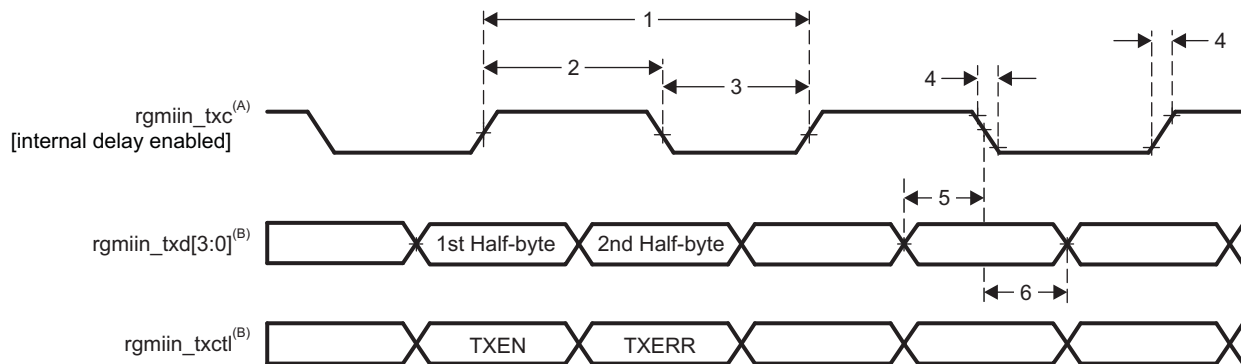
Table 7-79. Switching Characteristics Over Recommended Operating Conditions for rgmiin_txctl - RGMII Operation for 10/100/1000 Mbit/s

NO.	PARAMETER	DESCRIPTION	SPEED	MIN	MAX	UNIT
1	$t_c(TXC)$	Cycle time, rgmiin_txc	10 Mbps	360	440	ns
			100 Mbps	36	44	ns
			1000 Mbps	7.2	8.8	ns
2	$t_w(TXCH)$	Pulse duration, rgmiin_txc high	10 Mbps	160	240	ns
			100 Mbps	16	24	ns
			1000 Mbps	3.6	4.4	ns
3	$t_w(TXCL)$	Pulse duration, rgmiin_txc low	10 Mbps	160	240	ns
			100 Mbps	16	24	ns
			1000 Mbps	3.6	4.4	ns
4	$t_t(TXC)$	Transition time, rgmiin_txc	10 Mbps		0.75	ns
			100 Mbps		0.75	ns
			1000 Mbps		0.75	ns

Table 7-80. Switching Characteristics for GMAC RGMII Output Transmit for 10/100/1000 Mbps ⁽¹⁾

NO.	PARAMETER	DESCRIPTION	MODE	MIN	MAX	UNIT
5	$t_{osu}(TXD-TXC)$	Output Setup time, transmit selected signals valid to rgmiin_txc high/low	RGMII0, Internal Delay Enabled, 1000 Mbps	1.05 ⁽²⁾		ns
			RGMII0, Internal Delay Enabled, 10/100 Mbps	1.2		ns
			RGMII1, Internal Delay Enabled, 1000 Mbps	1.05 ⁽³⁾		ns
			RGMII1, Internal Delay Enabled, 10/100 Mbps	1.2		ns
6	$t_{oh}(TXC-TXD)$	Output Hold time, transmit selected signals valid after rgmiin_txc high/low	RGMII0, Internal Delay Enabled, 1000 Mbps	1.05 ⁽²⁾		ns
			RGMII0, Internal Delay Enabled, 10/100 Mbps	1.2		ns
			RGMII1, Internal Delay Enabled, 1000 Mbps	1.05 ⁽³⁾		ns
			RGMII1, Internal Delay Enabled, 10/100 Mbps	1.2		ns

- (1) For RGMII, transmit selected signals include: rgmiin_txd[3:0] and rgmiin_txctl.
- (2) RGMII0 1000Mbps operation requires that the 4 data pins rgmiio_txd[3:0] and rgmiio_txctl have their board propagation delays matched within 50pS of rgmiio_txc.
- (3) RGMII1 1000Mbps operation requires that the 4 data pins rgmii1_txd[3:0] and rgmii1_txctl have their board propagation delays matched within 50pS of rgmii1_txc.



- A. TxC is delayed internally before being driven to the rgmiin_txc pin. This internal delay is always enabled.
- B. Data and control information is transmitted using both edges of the clocks. rgmiin_txd[3:0] carries data bits 3-0 on the rising edge of rgmiin_txc and data bits 7-4 on the falling edge of rgmiin_txc. Similarly, rgmiin_txctl carries TXEN on rising edge of rgmiin_txc and TXERR of falling edge of rgmiin_txc.

Figure 7-53. GMAC Transmit Interface Timing RGMII operation

In [Table 7-81](#) are presented the specific groupings of signals (IOSET) for use with GMAC RGMII signals.

Table 7-81. GMAC RGMII IOSETs

SIGNALS	IOSET3		IOSET4	
	BALL	MUX	BALL	MUX
GMAC RGMII1				
rgmii1_txd3	C7	3		
rgmii1_txd2	D6	3		
rgmii1_txd1	B7	3		
rgmii1_txd0	B8	3		
rgmii1_rxd3	C8	3		
rgmii1_rxd2	D8	3		
rgmii1_rxd1	F8	3		

Table 7-81. GMAC RGMII IOSETs (continued)

SIGNALS	IOSET3		IOSET4	
	BALL	MUX	BALL	MUX
rgmii1_rxd0	E9	3		
rgmii1_rxctl	D7	3		
rgmii1_txc	E8	3		
rgmii1_txctl	A6	3		
rgmii1_rxc	A8	3		
GMAC RGMII0				
rgmii0_txd3			T5	0
rgmii0_txd2			T6	0
rgmii0_txd1			T4	0
rgmii0_txd0			R5	0
rgmii0_rxd3			P5	0
rgmii0_rxd2			U4	0
rgmii0_rxd1			T3	0
rgmii0_rxd0			R4	0
rgmii0_txc			R6	0
rgmii0_rxctl			U3	0
rgmii0_rxc			U2	0
rgmii0_txctl			P6	0

NOTE

To configure the desired Manual IO Timing Mode the user must follow the steps described in section "Manual IO Timing Modes" of the Device TRM.

The associated registers to configure are listed in the CFG REGISTER column. For more information please see the *Control Module Chapter* in the Device TRM.

Manual IO Timings Modes must be used to guarantee some IO timings for GMAC. See [Table 7-2 Modes Summary](#) for a list of IO timings requiring the use of Manual IO Timings Modes. See [Table 7-82 Manual Functions Mapping for GMAC RGMII0](#) for a definition of the Manual modes.

[Table 7-83](#) lists the A_DELAY and G_DELAY values needed to calculate the correct values to be set in the CFG_x registers. [Table 7-82](#)

Table 7-82. Manual Functions Mapping for GMAC RGMII0

BALL	BALL NAME	GMAC_RGMII0_MANUAL1		CFG REGISTER	MUXMODE
		A_DELAY (ps)	G_DELAY (ps)		0
U2	rgmii0_rxc	260	0	CFG_RGMII0_RXC_IN	rgmii0_rxc
U3	rgmii0_rxctl	0	1412	CFG_RGMII0_RXCTL_IN	rgmii0_rxctl
R4	rgmii0_rxd0	123	1047	CFG_RGMII0_RXD0_IN	rgmii0_rxd0
T3	rgmii0_rxd1	139	1081	CFG_RGMII0_RXD1_IN	rgmii0_rxd1
U4	rgmii0_rxd2	195	1100	CFG_RGMII0_RXD2_IN	rgmii0_rxd2
P5	rgmii0_rxd3	239	1216	CFG_RGMII0_RXD3_IN	rgmii0_rxd3
R6	rgmii0_txc	89	0	CFG_RGMII0_TXC_OUT	rgmii0_txc
P6	rgmii0_txctl	15	125	CFG_RGMII0_TXCTL_OUT	rgmii0_txctl
R5	rgmii0_txd0	339	162	CFG_RGMII0_TXD0_OUT	rgmii0_txd0
T4	rgmii0_txd1	146	94	CFG_RGMII0_TXD1_OUT	rgmii0_txd1
T6	rgmii0_txd2	0	27	CFG_RGMII0_TXD2_OUT	rgmii0_txd2
T5	rgmii0_txd3	291	205	CFG_RGMII0_TXD3_OUT	rgmii0_txd3

Manual IO Timings Modes must be used to guarantee some IO timings for GMAC. See [Table 7-2 Modes Summary](#) for a list of IO timings requiring the use of Manual IO Timings Modes. See [Table 7-82 Manual Functions Mapping for GMAC RGMII1](#) for a definition of the Manual modes.

[Table 7-83](#) lists the A_DELAY and G_DELAY values needed to calculate the correct values to be set in the CFG_x registers. [Table 7-83](#)

Table 7-83. Manual Functions Mapping for GMAC RGMII1

BALL	BALL NAME	GMAC_RGMII1_MANUAL1		CFG REGISTER	MUXMODE
		A_DELAY (ps)	G_DELAY (ps)		3
A8	vin2a_d18	411	0	CFG_VIN2A_D18_IN	rgmii1_rxc
D7	vin2a_d19	0	382	CFG_VIN2A_D19_IN	rgmii1_rxctl
C8	vin2a_d20	320	750	CFG_VIN2A_D20_IN	rgmii1_rxd3
D8	vin2a_d21	192	836	CFG_VIN2A_D21_IN	rgmii1_rxd2
F8	vin2a_d22	294	669	CFG_VIN2A_D22_IN	rgmii1_rxd1
E9	vin2a_d23	50	700	CFG_VIN2A_D23_IN	rgmii1_rxd0
E8	vin2a_d12	0	0	CFG_VIN2A_D12_OUT	rgmii1_txc
A6	vin2a_d13	219	101	CFG_VIN2A_D13_OUT	rgmii1_txctl
C7	vin2a_d14	92	58	CFG_VIN2A_D14_OUT	rgmii1_txd3
D6	vin2a_d15	135	100	CFG_VIN2A_D15_OUT	rgmii1_txd2
B7	vin2a_d16	154	101	CFG_VIN2A_D16_OUT	rgmii1_txd1
B8	vin2a_d17	78	27	CFG_VIN2A_D17_OUT	rgmii1_txd0

7.21 eMMC/SD/SDIO

The Device includes the following external memory interfaces 4 MultiMedia Card/Secure Digital/Secure Digital Input Output Interface (MMC/SD/SDIO).

NOTE

The eMMC/SD/SDIO_i (i = 2 to 4) controller is also referred to as MMC_i.

7.21.1 MMC2 — eMMC

MMC2 interface is compliant with the JC64 eMMC Standard v4.5 and it supports the following eMMC applications:

- Standard JC64 SDR, 8-bit data, half cycle
- High-speed JC64 SDR, 8-bit data, half cycle
- High-speed JC64 DDR, 8-bit data

NOTE

For more information, see the eMMC/SD/SDIO chapter of the Device TRM.

7.21.1.1 Standard JC64 SDR, 8-bit data, half cycle

[Table 7-84](#) and [Table 7-85](#) present Timing requirements and Switching characteristics for MMC2 - Standard SDR in receiver and Transmitter mode (see [Figure 7-54](#) and [Figure 7-55](#)).

Table 7-84. Timing Requirements for MMC2 - JC64 Standard SDR Mode

NO.	PARAMETER	DESCRIPTION	MIN	MAX	UNIT
SSDR5	$t_{su}(cmdV-clkH)$	Setup time, mmc2_cmd valid before mmc2_clk rising clock edge	13.19		ns
SSDR6	$t_h(clkH-cmdV)$	Hold time, mmc2_cmd valid after mmc2_clk rising clock edge	8.4		ns

Table 7-84. Timing Requirements for MMC2 - JC64 Standard SDR Mode (continued)

NO.	PARAMETER	DESCRIPTION	MIN	MAX	UNIT
SSDR7	$t_{su}(dV-clkH)$	Setup time, mmc2_dat[7:0] valid before mmc2_clk rising clock edge	13.19		ns
SSDR8	$t_{h}(clkH-dV)$	Hold time, mmc2_dat[7:0] valid after mmc2_clk rising clock edge	8.4		ns

Table 7-85. Switching Characteristics for MMC2 - JC64 Standard SDR Mode

NO.	PARAMETER	DESCRIPTION	MIN	MAX	UNIT
SSDR1	$f_{op}(clk)$	Operating frequency, mmc2_clk		24	MHz
SSDR2H	$t_w(clkH)$	Pulse duration, mmc2_clk high	0.5*P-0.172 (1)		ns
SSDR2L	$t_w(clkL)$	Pulse duration, mmc2_clk low	0.5*P-0.172 (1)		ns
SSDR3	$t_d(clkL-cmdV)$	Delay time, mmc2_clk falling clock edge to mmc2_cmd transition	-16.96	16.96	ns
SSDR4	$t_d(clkL-dV)$	Delay time, mmc2_clk falling clock edge to mmc2_dat[7:0] transition	-16.96	16.96	ns

(1) P = output mmc2_clk period in ns

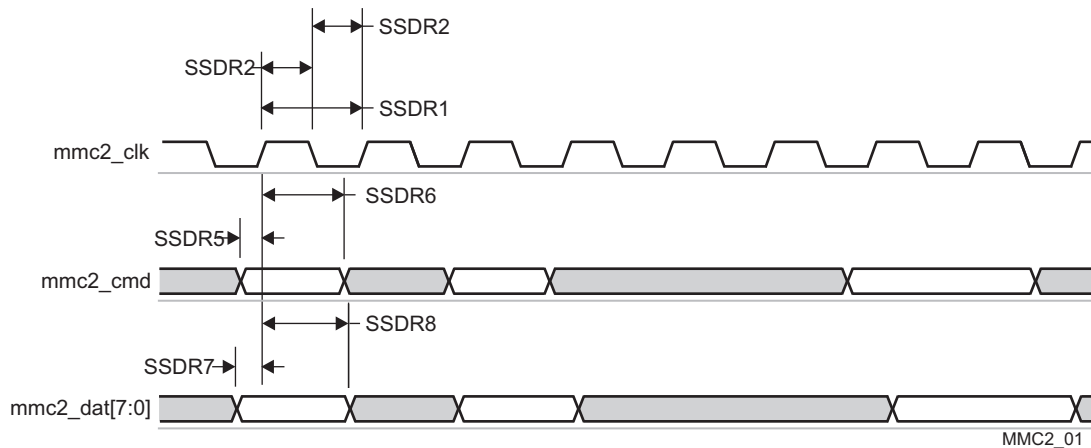


Figure 7-54. MMC/SD/SDIO in - Standard JC64 - Receiver Mode

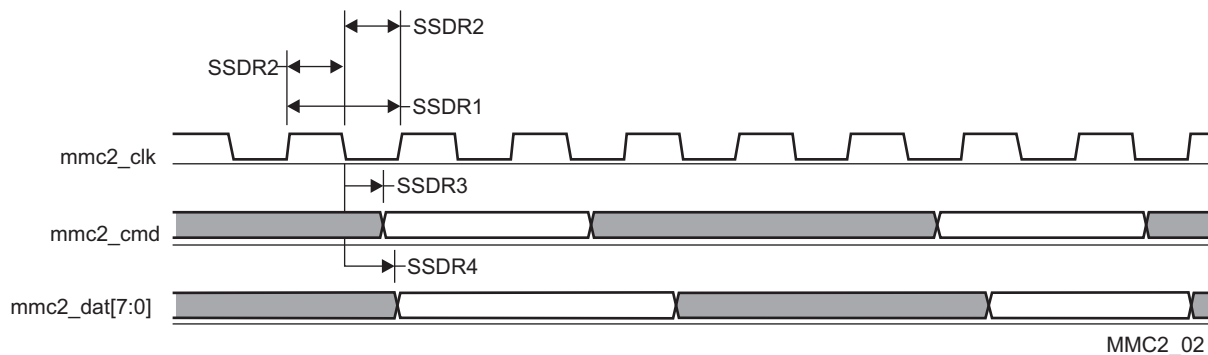


Figure 7-55. MMC/SD/SDIO in - Standard JC64 - Transmitter Mode

7.21.1.2 High-speed JC64 SDR, 8-bit data, half cycle

Table 7-86 and Table 7-87 present Timing requirements and Switching characteristics for MMC2 - High speed SDR in receiver and transmitter mode (see Figure 7-56 and Figure 7-57).

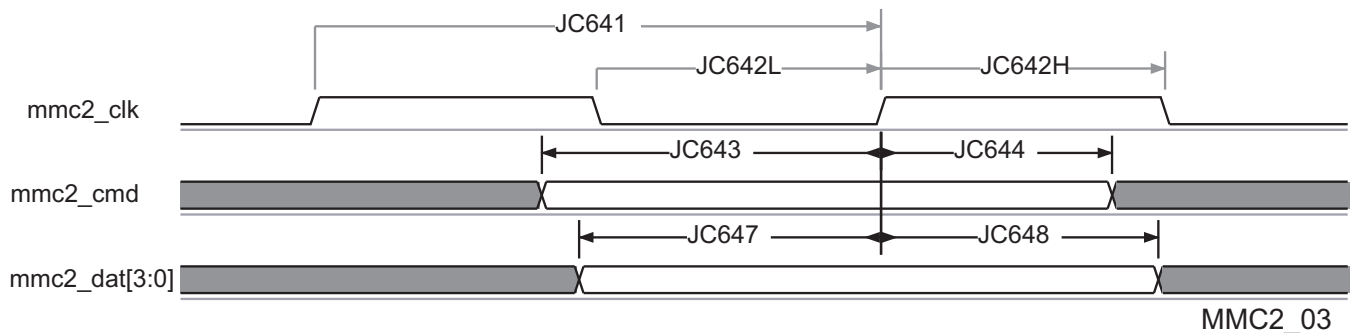
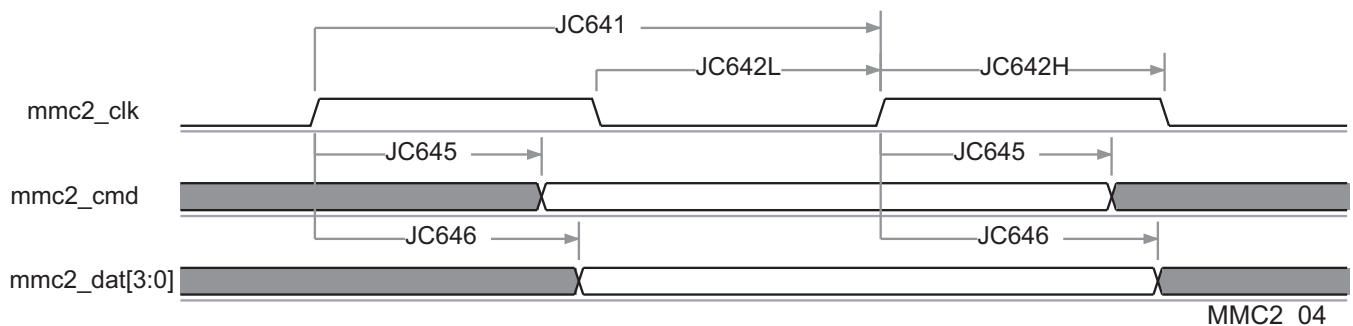
Table 7-86. Timing Requirements for MMC2 - JC64 High Speed SDR Mode

NO.	PARAMETER	DESCRIPTION	MIN	MAX	UNIT
JC643	$t_{su(cmdV-clkH)}$	Setup time, mmc2_cmd valid before mmc2_clk rising clock edge	5.6		ns
JC644	$t_{h(clkH-cmdV)}$	Hold time, mmc2_cmd valid after mmc2_clk rising clock edge	2.6		ns
JC647	$t_{su(dV-clkH)}$	Setup time, mmc2_dat[7:0] valid before mmc2_clk rising clock edge	5.6		ns
JC648	$t_{h(clkH-dV)}$	Hold time, mmc2_dat[7:0] valid after mmc2_clk rising clock edge	2.6		ns

Table 7-87. Switching Characteristics for MMC2 - JC64 High Speed SDR Mode

NO.	PARAMETER	DESCRIPTION	MIN	MAX	UNIT
JC641	$f_{op(clk)}$	Operating frequency, mmc2_clk		48	MHz
JC642H	$t_{w(clkH)}$	Pulse duration, mmc2_clk high	0.5*P- 0.172 (1)		ns
JC642L	$t_{w(clkL)}$	Pulse duration, mmc2_clk low	0.5*P- 0.172 (1)		ns
JC645	$t_{d(clkL-cmdV)}$	Delay time, mmc2_clk falling clock edge to mmc2_cmd transition	-6.64	6.64	ns
JC646	$t_{d(clkL-dV)}$	Delay time, mmc2_clk falling clock edge to mmc2_dat[7:0] transition	-6.64	6.64	ns

(1) P = output mmc2_clk period in ns

**Figure 7-56. MMC/SD/SDIO in - High Speed JC64 - Receiver Mode****Figure 7-57. MMC/SD/SDIO in - High Speed JC64 - Transmitter Mode**

7.21.1.3 High-speed JC64 DDR, 8-bit data

Table 7-88 and Table 7-89 present Timing requirements and Switching characteristics for MMC2 - High speed DDR in receiver and transmitter mode (see Figure 7-58 and Figure 7-59).

Table 7-88. Timing Requirements for MMC2 - JC64 High Speed DDR Mode

NO.	PARAMETER	DESCRIPTION	MODE	MIN	MAX	UNIT
DDR3	$t_{su(cmdV-clk)}$	Setup time, mmc2_cmd valid before mmc2_clk transition		1.8		ns

Table 7-88. Timing Requirements for MMC2 - JC64 High Speed DDR Mode (continued)

NO.	PARAMETER	DESCRIPTION	MODE	MIN	MAX	UNIT
DDR4	$t_{h(\text{clk-cmdV})}$	Hold time, mmc2_cmd valid after mmc2_clk transition		1.8		ns
DDR7	$t_{su(\text{dV-clk})}$	Setup time, mmc2_dat[7:0] valid before mmc2_clk transition		1.8		ns
DDR8	$t_{h(\text{clk-dV})}$	Hold time, mmc2_dat[7:0] valid after mmc2_clk transition	Pad Loopback (1.8V)	1.8 (1)		ns
			Pad Loopback (3.3V)	1.8		ns
			Internal Loopback	1.8 (1)		ns

(1) This Hold time requirement is larger than the Hold time provided by a typical eMMC component. Therefore, the trace length between the Device and eMMC component must be sufficiently long enough to ensure that the Hold time is met at the Device.

Table 7-89. Switching Characteristics for MMC2 - JC64 High Speed DDR Mode

NO.	PARAMETER	DESCRIPTION	MIN	MAX	UNIT
DDR1	$f_{op(\text{clk})}$	Operating frequency, mmc2_clk		48	MHz
DDR2H	$t_{w(\text{clkH})}$	Pulse duration, mmc2_clk high	0.5*P- 0.172 (1)		ns
DDR2L	$t_{w(\text{clkL})}$	Pulse duration, mmc2_clk low	0.5*P- 0.172 (1)		ns
DDR5	$t_{d(\text{clk-cmdV})}$	Delay time, mmc2_clk transition to mmc2_cmd transition	2.9	7.14	ns
DDR6	$t_{d(\text{clk-dV})}$	Delay time, mmc2_clk transition to mmc2_dat[7:0] transition	2.9	7.14	ns

(1) P = output mmc2_clk period in ns

Table 7-90 and Table 7-91 present Timing requirements and Switching characteristics for MMC2 - High speed DDR in receiver and transmitter mode During Boot (see Figure 7-58 and Figure 7-59).

Table 7-90. Timing Requirements for MMC2 - JC64 High Speed DDR Mode During Boot

NO.	PARAMETER	DESCRIPTION	MODE	MIN	MAX	UNIT
DDR3	$t_{su(\text{cmdV-clk})}$	Setup time, mmc2_cmd valid before mmc2_clk transition	Boot (1.8V)	1.8		ns
			Boot (3.3V)	1.8		ns
DDR4	$t_{h(\text{clk-cmdV})}$	Hold time, mmc2_cmd valid after mmc2_clk transition	Boot (1.8V)	1.8 (1)		ns
			Boot (3.3V)	1.8 (1)		ns
DDR7	$t_{su(\text{dV-clk})}$	Setup time, mmc2_dat[7:0] valid before mmc2_clk transition	Boot (1.8V)	1.8		ns
			Boot (3.3V)	1.8		ns
DDR8	$t_{h(\text{clk-dV})}$	Hold time, mmc2_dat[7:0] valid after mmc2_clk transition	Boot (1.8V)	1.8 (1)		ns
			Boot (3.3V)	1.8 (1)		ns

(1) This Hold time requirement is larger than the Hold time provided by a typical eMMC component. Therefore, the trace length between the Device and eMMC component must be sufficiently long enough to ensure that the Hold time is met at the Device.

Table 7-91. Switching Characteristics for MMC2 - JC64 High Speed DDR Mode During Boot

NO.	PARAMETER	DESCRIPTION	MODE	MIN	MAX	UNIT
DDR1	$f_{op(\text{clk})}$	Operating frequency, mmc2_clk			48	MHz
DDR2H	$t_{w(\text{clkH})}$	Pulse duration, mmc2_clk high		0.5*P- 0.172 (1)		ns
DDR2L	$t_{w(\text{clkL})}$	Pulse duration, mmc2_clk low		0.5*P- 0.172 (1)		ns
DDR5	$t_{d(\text{clk-cmdV})}$	Delay time, mmc2_clk transition to mmc2_cmd transition	Boot (1.8V)	2.9	7.14	ns
			Boot (3.3V)	2.9	7.14	ns
DDR6	$t_{d(\text{clk-dV})}$	Delay time, mmc2_clk transition to mmc2_dat[7:0] transition	Boot (1.8V)	2.9	7.14	ns
			Boot (3.3V)	2.9	7.14	ns

(1) P = output mmc2_clk period in ns

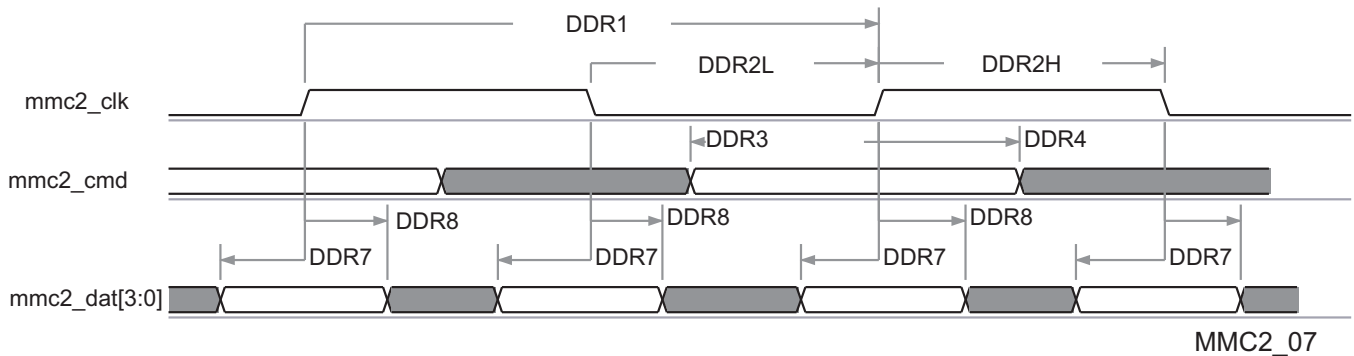


Figure 7-58. MMC/SD/SDIO in - High Speed DDR JC64 - Receiver Mode

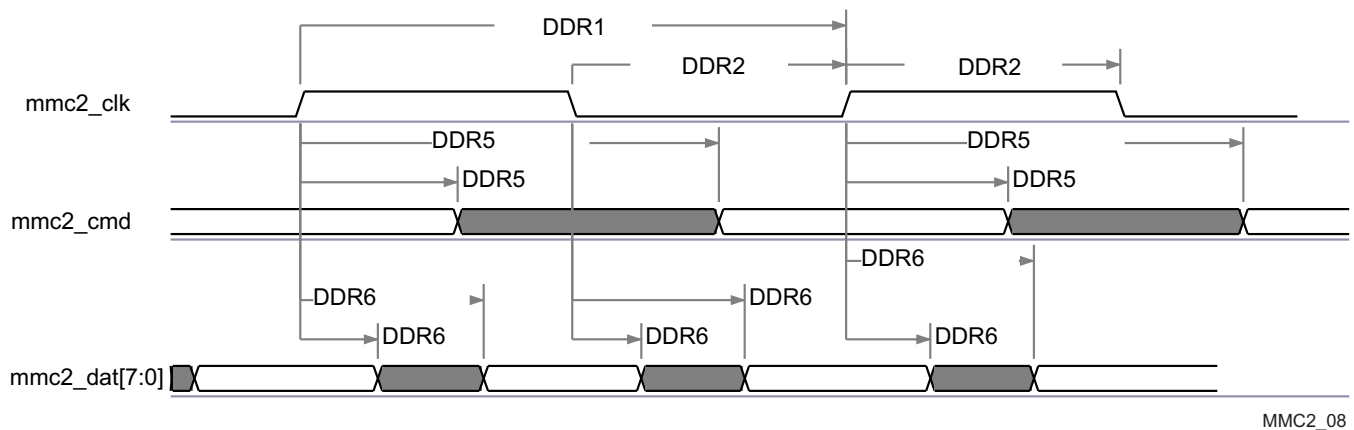


Figure 7-59. MMC/SD/SDIO in - High Speed DDR JC64 - Transmitter Mode

NOTE

To configure the desired Manual IO Timing Mode the user must follow the steps described in section Manual IO Timing Modes of the Device TRM.

The associated registers to configure are listed in the **CFG REGISTER** column. For more information see the Control Module chapter in the Device TRM.

Manual IO Timings Modes must be used to guarantee some IO timings for MMC2. See [Table 7-2 Modes Summary](#) for a list of IO timings requiring the use of Manual IO Timings Modes. See [Table 7-92 Manual Functions Mapping for MMC2 with Internal Loopback Clock](#) for a definition of the Manual modes.

[Table 7-92](#) lists the A_DELAY and G_DELAY values needed to calculate the correct values to be set in the CFG_x registers.

Table 7-92. Manual Functions Mapping for MMC2 With Internal Loopback Clock

BALL	BALL NAME	MMC2_DDR_LB_MANUAL1		MMC2_STD_HS_LB_MANUAL 1		CFG REGISTER	MUXMODE
		A_DELAY (ps)	G_DELAY (ps)	A_DELAY (ps)	G_DELAY (ps)		1
C2	gpmc_a19	49	0	850	0	CFG_GPMC_A19_IN	mmc2_dat4
C2	gpmc_a19	0	0	0	0	CFG_GPMC_A19_OEN	mmc2_dat4
C2	gpmc_a19	170	0	0	0	CFG_GPMC_A19_OUT	mmc2_dat4
D3	gpmc_a20	463	0	1264	0	CFG_GPMC_A20_IN	mmc2_dat5

Table 7-92. Manual Functions Mapping for MMC2 With Internal Loopback Clock (continued)

BALL	BALL NAME	MMC2_DDR_LB_MANUAL1		MMC2_STD_HS_LB_MANUAL 1		CFG REGISTER	MUXMODE
		A_DELAY (ps)	G_DELAY (ps)	A_DELAY (ps)	G_DELAY (ps)		1
D3	gpmc_a20	0	0	0	0	CFG_GPMC_A20_OEN	mmc2_dat5
D3	gpmc_a20	81	0	0	0	CFG_GPMC_A20_OUT	mmc2_dat5
D2	gpmc_a21	8	0	786	0	CFG_GPMC_A21_IN	mmc2_dat6
D2	gpmc_a21	0	0	0	0	CFG_GPMC_A21_OEN	mmc2_dat6
D2	gpmc_a21	123	0	0	0	CFG_GPMC_A21_OUT	mmc2_dat6
D1	gpmc_a22	0	102	902	0	CFG_GPMC_A22_IN	mmc2_dat7
D1	gpmc_a22	0	0	0	0	CFG_GPMC_A22_OEN	mmc2_dat7
D1	gpmc_a22	55	0	0	0	CFG_GPMC_A22_OUT	mmc2_dat7
E1	gpmc_a23	592	2815	0	2764	CFG_GPMC_A23_IN	mmc2_clk
E1	gpmc_a23	422	0	0	0	CFG_GPMC_A23_OUT	mmc2_clk
E2	gpmc_a24	384	0	1185	0	CFG_GPMC_A24_IN	mmc2_dat0
E2	gpmc_a24	0	0	0	0	CFG_GPMC_A24_OEN	mmc2_dat0
E2	gpmc_a24	0	0	0	0	CFG_GPMC_A24_OUT	mmc2_dat0
E3	gpmc_a25	0	0	670	0	CFG_GPMC_A25_IN	mmc2_dat1
E3	gpmc_a25	0	0	0	0	CFG_GPMC_A25_OEN	mmc2_dat1
E3	gpmc_a25	0	0	0	0	CFG_GPMC_A25_OUT	mmc2_dat1
E4	gpmc_a26	171	0	972	0	CFG_GPMC_A26_IN	mmc2_dat2
E4	gpmc_a26	0	0	0	0	CFG_GPMC_A26_OEN	mmc2_dat2
E4	gpmc_a26	0	0	0	0	CFG_GPMC_A26_OUT	mmc2_dat2
F3	gpmc_a27	315	0	1116	0	CFG_GPMC_A27_IN	mmc2_dat3
F3	gpmc_a27	0	0	0	0	CFG_GPMC_A27_OEN	mmc2_dat3
F3	gpmc_a27	54	0	0	0	CFG_GPMC_A27_OUT	mmc2_dat3
C1	gpmc_cs1	0	0	250	0	CFG_GPMC_CS1_IN	mmc2_cmd
C1	gpmc_cs1	0	0	0	0	CFG_GPMC_CS1_OEN	mmc2_cmd
C1	gpmc_cs1	0	0	0	0	CFG_GPMC_CS1_OUT	mmc2_cmd

7.21.2 MMC3 and MMC4—SDIO/SD

MMC3 and MMC4 interfaces are compliant with the SDIO3.0 standard v1.0, SD Part E1 and for generic SDIO devices, it supports the following applications:

- MMC3 8-bit data and MMC4 4-bit data, SD Default speed, SDR
- MMC3 8-bit data and MMC4 4-bit data, SD High speed, SDR
- MMC3 8-bit data and MMC4 4-bit data, UHS-1 SDR12 (SD Standard v3.01), 4-bit data, SDR, half cycle
- MMC3 8-bit data and MMC4 4-bit data, UHS-I SDR25 (SD Standard v3.01), 4-bit data, SDR, half cycle
- MMC3 8-bit data, UHS-I SDR50

NOTE

The eMMC/SD/SDIO_j (j = 3 to 4) controller is also referred to as MMC_j.

NOTE

For more information, see the MMC/SDIO chapter of the Device TRM.

7.21.2.1 MMC3 and MMC4, SD Default Speed

Figure 7-60, Figure 7-61, and Table 7-93 through Table 7-96 present Timing requirements and Switching characteristics for MMC3 and MMC4 - SD Default speed in receiver and transmitter mode.

Table 7-93. Timing Requirements for MMC3 - Default Speed Mode ⁽¹⁾

NO.	PARAMETER	DESCRIPTION	MIN	MAX	UNIT
DS5	$t_{su(cmdV-clkH)}$	Setup time, mmc3_cmd valid before mmc3_clk rising clock edge	5.11		ns
DS6	$t_h(clkH-cmdV)$	Hold time, mmc3_cmd valid after mmc3_clk rising clock edge	20.46		ns
DS7	$t_{su(dV-clkH)}$	Setup time, mmc3_dat[i:0] valid before mmc3_clk rising clock edge	5.11		ns
DS8	$t_h(clkH-dV)$	Hold time, mmc3_dat[i:0] valid after mmc3_clk rising clock edge	20.46		ns

(1) i in [i:0] = 7

Table 7-94. Switching Characteristics for MMC3 - SD/SDIO Default Speed Mode ⁽²⁾

NO.	PARAMETER	DESCRIPTION	MIN	MAX	UNIT
DS0	fop(clk)	Operating frequency, mmc3_clk		24	MHz
DS1	$t_w(clkH)$	Pulse duration, mmc3_clk high	0.5*P- 0.270 ⁽¹⁾		ns
DS2	$t_w(clkL)$	Pulse duration, mmc3_clk low	0.5*P- 0.270 ⁽¹⁾		ns
DS3	$t_d(clkL-cmdV)$	Delay time, mmc3_clk falling clock edge to mmc3_cmd transition	-14.93	14.93	ns
DS4	$t_d(clkL-dV)$	Delay time, mmc3_clk falling clock edge to mmc3_dat[i:0] transition	-14.93	14.93	ns

(1) P = output mmc3_clk period in ns

(2) i in [i:0] = 7

Table 7-95. Timing Requirements for MMC4 - Default Speed Mode ⁽¹⁾

NO.	PARAMETER	DESCRIPTION	MIN	MAX	UNIT
DS5	$t_{su(cmdV-clkH)}$	Setup time, mmc4_cmd valid before mmc4_clk rising clock edge	5.11		ns
DS6	$t_h(clkH-cmdV)$	Hold time, mmc4_cmd valid after mmc4_clk rising clock edge	20.46		ns
DS7	$t_{su(dV-clkH)}$	Setup time, mmc4_dat[i:0] valid before mmc4_clk rising clock edge	5.11		ns
DS8	$t_h(clkH-dV)$	Hold time, mmc4_dat[i:0] valid after mmc4_clk rising clock edge	20.46		ns

(1) i in [i:0] = 3

Table 7-96. Switching Characteristics for MMC4 - Default Speed Mode ⁽²⁾

NO.	PARAMETER	DESCRIPTION	MIN	MAX	UNIT
DS0	fop(clk)	Operating frequency, mmc4_clk		24	MHz
DS1	$t_w(clkH)$	Pulse duration, mmc4_clk high	0.5*P- 0.270 ⁽¹⁾		ns
DS2	$t_w(clkL)$	Pulse duration, mmc4_clk low	0.5*P- 0.270 ⁽¹⁾		ns
DS3	$t_d(clkL-cmdV)$	Delay time, mmc4_clk falling clock edge to mmc4_cmd transition	-14.93	14.93	ns
DS4	$t_d(clkL-dV)$	Delay time, mmc4_clk falling clock edge to mmc4_dat[i:0] transition	-14.93	14.93	ns

- (1) P = output mmc4_clk period in ns
- (2) i in [i:0] = 3

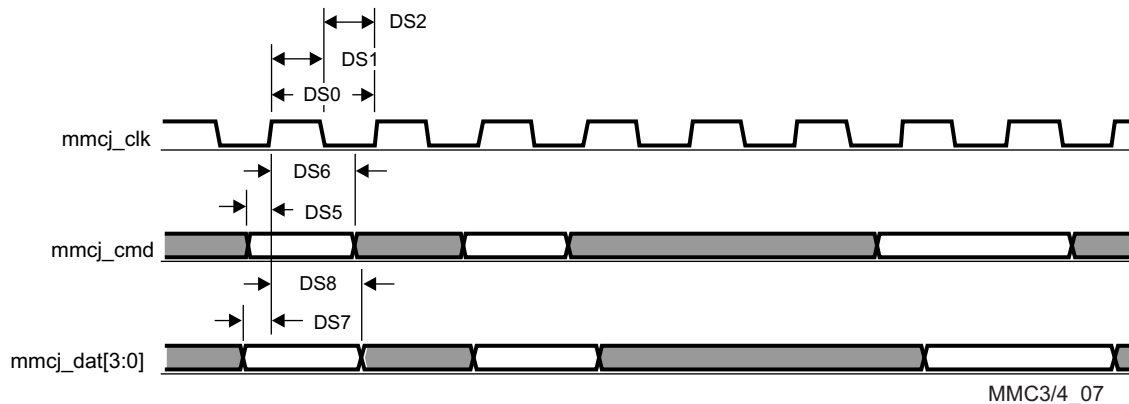


Figure 7-60. MMC/SD/SDIOj in - Default Speed - Receiver Mode

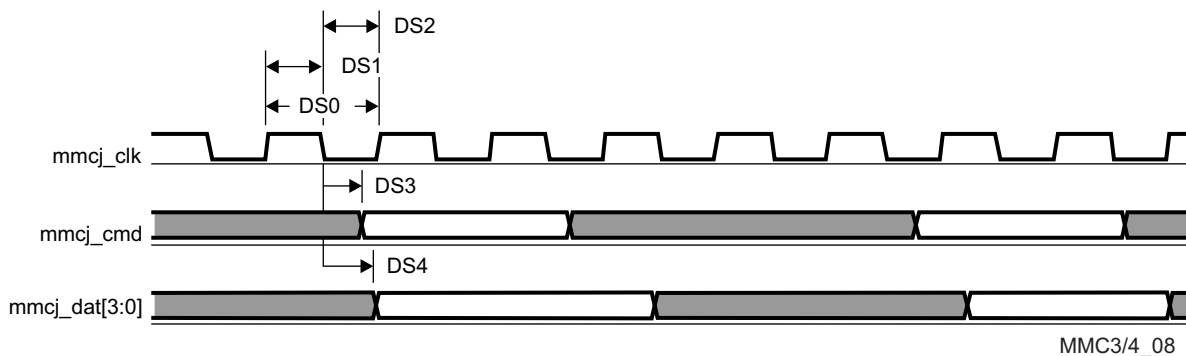


Figure 7-61. MMC/SD/SDIOj in - Default Speed - Transmitter Mode

7.21.2.2 MMC3 and MMC4, SD High Speed

Figure 7-62, Figure 7-63, and Table 7-97 through Table 7-100 present Timing requirements and Switching characteristics for MMC3 and MMC4 - SD and SDIO High speed in receiver and transmitter mode.

Table 7-97. Timing Requirements for MMC3 - SD/SDIO High Speed Mode ⁽¹⁾

NO.	PARAMETER	DESCRIPTION	MIN	MAX	UNIT
HS3	$t_{su(cmdV-clkH)}$	Setup time, mmc3_cmd valid before mmc3_clk rising clock edge	5.3		ns
HS4	$t_{h(clkH-cmdV)}$	Hold time, mmc3_cmd valid after mmc3_clk rising clock edge	2.6		ns
HS7	$t_{su(dV-clkH)}$	Setup time, mmc3_dat[i:0] valid before mmc3_clk rising clock edge	5.3		ns
HS8	$t_{h(clkH-dV)}$	Hold time, mmc3_dat[i:0] valid after mmc3_clk rising clock edge	2.6		ns

(1) i in [i:0] = 7

Table 7-98. Switching Characteristics for MMC3 - SD/SDIO High Speed Mode ⁽²⁾

NO.	PARAMETER	DESCRIPTION	MIN	MAX	UNIT
HS1	fop(clk)	Operating frequency, mmc3_clk		48	MHz
HS2H	$t_w(clkH)$	Pulse duration, mmc3_clk high	0.5*P-0.270 ⁽¹⁾		ns
HS2L	$t_w(clkL)$	Pulse duration, mmc3_clk low	0.5*P-0.270 ⁽¹⁾		ns
HS5	$t_d(clkL-cmdV)$	Delay time, mmc3_clk falling clock edge to mmc3_cmd transition	-7.6	3.6	ns
HS6	$t_d(clkL-dV)$	Delay time, mmc3_clk falling clock edge to mmc3_dat[i:0] transition	-7.6	3.6	ns

- (1) P = output mmc3_clk period in ns
- (2) i in [i:0] = 7

Table 7-99. Timing Requirements for MMC4 - High Speed Mode ⁽¹⁾

NO.	PARAMETER	DESCRIPTION	MIN	MAX	UNIT
HS3	$t_{su(cmdV-clkH)}$	Setup time, mmc4_cmd valid before mmc4_clk rising clock edge	5.3		ns
HS4	$t_h(clkH-cmdV)$	Hold time, mmc4_cmd valid after mmc4_clk rising clock edge	1.6		ns
HS7	$t_{su(dV-clkH)}$	Setup time, mmc4_dat[i:0] valid before mmc4_clk rising clock edge	5.3		ns
HS8	$t_h(clkH-dV)$	Hold time, mmc4_dat[i:0] valid after mmc4_clk rising clock edge	1.6		ns

(1) i in [i:0] = 3

Table 7-100. Switching Characteristics for MMC4 - High Speed Mode ⁽²⁾

NO.	PARAMETER	DESCRIPTION	MIN	MAX	UNIT
HS1	fop(clk)	Operating frequency, mmc4_clk		48	MHz
HS2H	$t_w(clkH)$	Pulse duration, mmc4_clk high	0.5*P-0.270 ⁽¹⁾		ns
HS2L	$t_w(clkL)$	Pulse duration, mmc4_clk low	0.5*P-0.270 ⁽¹⁾		ns
HS5	$t_d(clkL-cmdV)$	Delay time, mmc4_clk falling clock edge to mmc4_cmd transition	-8.8	6.6	ns
HS6	$t_d(clkL-dV)$	Delay time, mmc4_clk falling clock edge to mmc4_dat[i:0] transition	-8.8	6.6	ns

(1) P = output mmc4_clk period in ns

(2) i in [i:0] = 3

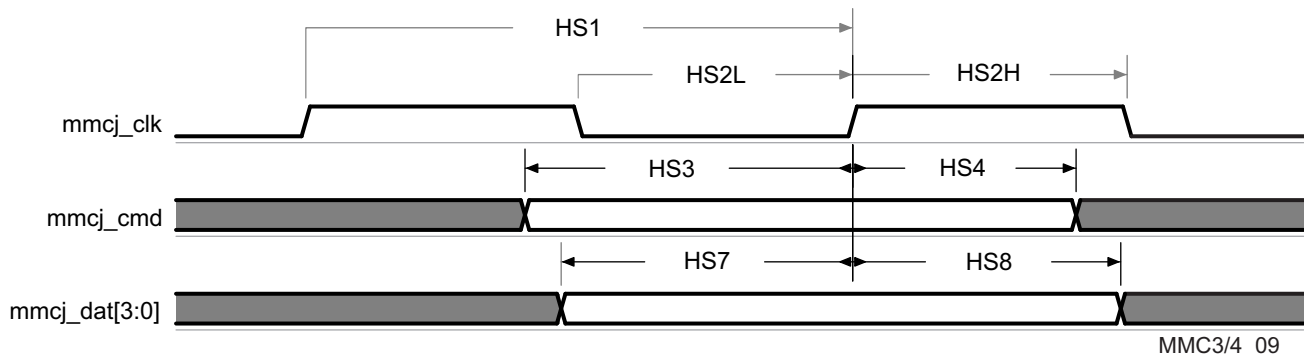


Figure 7-62. MMC/SD/SDIOj in - High Speed - Receiver Mode

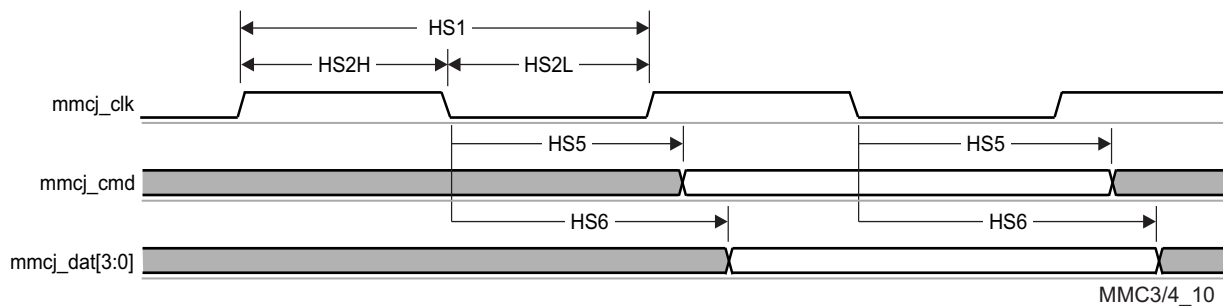


Figure 7-63. MMC/SD/SDIOj in - High Speed - Transmitter Mode

7.21.2.3 MMC3 and MMC4, SD and SDIO SDR12 Mode

Figure 7-64, Figure 7-65, and Table 7-101, through Table 7-104 present Timing requirements and Switching characteristics for MMC3 and MMC4 - SD and SDIO SDR12 in receiver and transmitter mode.

Table 7-101. Timing Requirements for MMC3 - SDR12 Mode ⁽¹⁾

NO.	PARAMETER	DESCRIPTION	MIN	MAX	UNIT
SDR125	$t_{su(cmdV-clkH)}$	Setup time, mmc3_cmd valid before mmc3_clk rising clock edge	25.99		ns
SDR126	$t_h(clkH-cmdV)$	Hold time, mmc3_cmd valid after mmc3_clk rising clock edge	1.6		ns
SDR127	$t_{su(dV-clkH)}$	Setup time, mmc3_dat[i:0] valid before mmc3_clk rising clock edge	25.99		ns
SDR128	$t_h(clkH-dV)$	Hold time, mmc3_dat[i:0] valid after mmc3_clk rising clock edge	1.6		ns

(1) i in [i:0] = 7

Table 7-102. Switching Characteristics for MMC3 - SDR12 Mode ⁽²⁾

NO.	PARAMETER	DESCRIPTION	MIN	MAX	UNIT
SDR120	fop(clk)	Operating frequency, mmc3_clk		24	MHz
SDR121	$t_w(clkH)$	Pulse duration, mmc3_clk high	0.5*P-0.270 ⁽¹⁾		ns
SDR122	$t_w(clkL)$	Pulse duration, mmc3_clk low	0.5*P-0.270 ⁽¹⁾		ns
SDR123	$t_d(clkL-cmdV)$	Delay time, mmc3_clk falling clock edge to mmc3_cmd transition	-19.13	16.93	ns
SDR124	$t_d(clkL-dV)$	Delay time, mmc3_clk falling clock edge to mmc3_dat[i:0] transition	-19.13	16.93	ns

(1) P = output mmc3_clk period in ns

(2) i in [i:0] = 7

Table 7-103. Timing Requirements for MMC4 - SDR12 Mode ⁽¹⁾

NO.	PARAMETER	DESCRIPTION	MIN	MAX	UNIT
SDR125	$t_{su(cmdV-clkH)}$	Setup time, mmc4_cmd valid before mmc4_clk rising clock edge	25.99		ns
SDR126	$t_h(clkH-cmdV)$	Hold time, mmc4_cmd valid after mmc4_clk rising clock edge	1.6		ns
SDR127	$t_{su(dV-clkH)}$	Setup time, mmc4_dat[i:0] valid before mmc4_clk rising clock edge	25.99		ns
SDR128	$t_h(clkH-dV)$	Hold time, mmc4_dat[i:0] valid after mmc4_clk rising clock edge	1.6		ns

(1) j in [i:0] = 3

Table 7-104. Switching Characteristics for MMC4 - SDR12 Mode ⁽²⁾

NO.	PARAMETER	DESCRIPTION	MIN	MAX	UNIT
SDR120	fop(clk)	Operating frequency, mmc4_clk		24	MHz
SDR121	$t_w(clkH)$	Pulse duration, mmc4_clk high	0.5*P-0.270 ⁽¹⁾		ns
SDR122	$t_w(clkL)$	Pulse duration, mmc4_clk low	0.5*P-0.270 ⁽¹⁾		ns
SDR125	$t_d(clkL-cmdV)$	Delay time, mmc4_clk falling clock edge to mmc4_cmd transition	-19.13	16.93	ns
SDR126	$t_d(clkL-dV)$	Delay time, mmc4_clk falling clock edge to mmc4_dat[i:0] transition	-19.13	16.93	ns

(1) P = output mmc4_clk period in ns

(2) j in [i:0] = 3

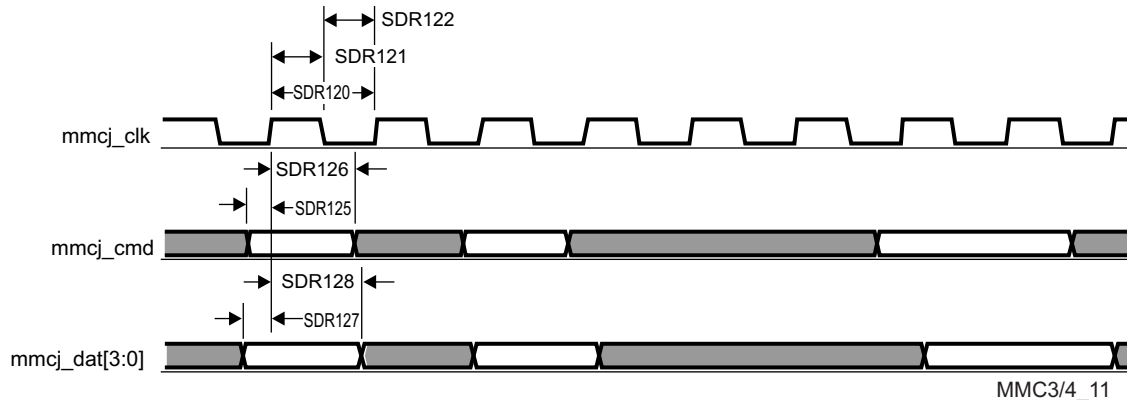
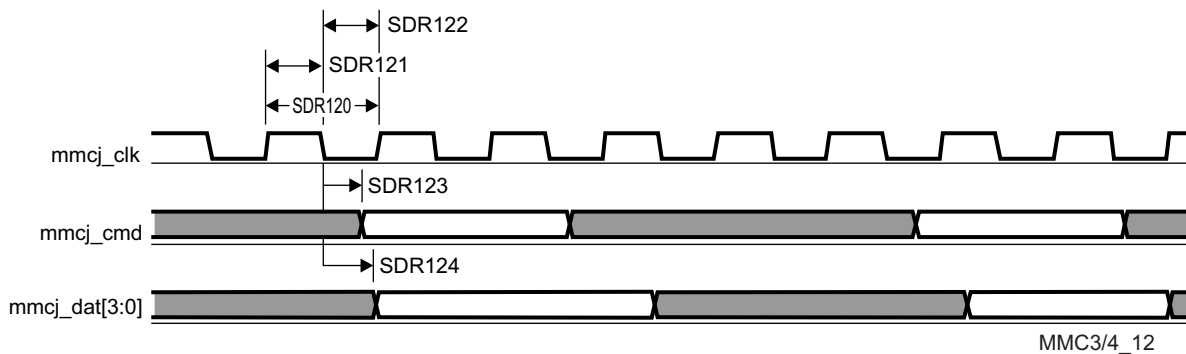
**Figure 7-64. MMC/SD/SDIOj in - SDR12 - Receiver Mode****Figure 7-65. MMC/SD/SDIOj in - SDR12 - Transmitter Mode****7.21.2.4 MMC3 and MMC4, SD SDR25 Mode**

Figure 7-66, Figure 7-67, and Table 7-105 through Table 7-108 present Timing requirements and Switching characteristics for MMC3 and MMC4 - SD and SDIO SDR25 in receiver and transmitter mode.

Table 7-105. Timing Requirements for MMC3 - SDR25 Mode ⁽¹⁾

NO.	PARAMETER	DESCRIPTION	MIN	MAX	UNIT
SDR253	$t_{su}(cmdV-clkH)$	Setup time, mmc3_cmd valid before mmc3_clk rising clock edge	5.3		ns
SDR254	$t_h(clkH-cmdV)$	Hold time, mmc3_cmd valid after mmc3_clk rising clock edge	1.6		ns
SDR257	$t_{su}(dV-clkH)$	Setup time, mmc3_dat[i:0] valid before mmc3_clk rising clock edge	5.3		ns
SDR258	$t_h(clkH-dV)$	Hold time, mmc3_dat[i:0] valid after mmc3_clk rising clock edge	1.6		ns

(1) i in [i:0] = 7

Table 7-106. Switching Characteristics for MMC3 - SDR25 Mode ⁽²⁾

NO.	PARAMETER	DESCRIPTION	MIN	MAX	UNIT
SDR251	fop(clk)	Operating frequency, mmc3_clk		48	MHz
SDR252 H	$t_w(clkH)$	Pulse duration, mmc3_clk high	0.5*P- 0.270	⁽¹⁾	ns
SDR252L	$t_w(clkL)$	Pulse duration, mmc3_clk low	0.5*P- 0.270	⁽¹⁾	ns
SDR255	$t_d(clkL-cmdV)$	Delay time, mmc3_clk falling clock edge to mmc3_cmd transition	-8.8	6.6	ns
SDR256	$t_d(clkL-dV)$	Delay time, mmc3_clk falling clock edge to mmc3_dat[i:0] transition	-8.8	6.6	ns

- (1) P = output mmc3_clk period in ns
- (2) i in [i:0] = 7

Table 7-107. Timing Requirements for MMC4 - SDR25 Mode ⁽¹⁾

NO.	PARAMETER	DESCRIPTION	MIN	MAX	UNIT
SDR255	$t_{su}(cmdV-clkH)$	Setup time, mmc4_cmd valid before mmc4_clk rising clock edge	5.3		ns
SDR256	$t_h(clkH-cmdV)$	Hold time, mmc4_cmd valid after mmc4_clk rising clock edge	1.6		ns
SDR257	$t_{su}(dV-clkH)$	Setup time, mmc4_dat[i:0] valid before mmc4_clk rising clock edge	5.3		ns
SDR258	$t_h(clkH-dV)$	Hold time, mmc4_dat[i:0] valid after mmc4_clk rising clock edge	1.6		ns

- (1) i in [i:0] = 3

Table 7-108. Switching Characteristics for MMC4 - SDR25 Mode ⁽²⁾

NO.	PARAMETER	DESCRIPTION	MIN	MAX	UNIT
SDR251	fop(clk)	Operating frequency, mmc4_clk		48	MHz
SDR252 H	$t_w(clkH)$	Pulse duration, mmc4_clk high	0.5*P-0.270 ⁽¹⁾		ns
SDR252L	$t_w(clkL)$	Pulse duration, mmc4_clk low	0.5*P-0.270 ⁽¹⁾		ns
SDR255	$t_d(clkL-cmdV)$	Delay time, mmc4_clk falling clock edge to mmc4_cmd transition	-8.8	6.6	ns
SDR256	$t_d(clkL-dV)$	Delay time, mmc4_clk falling clock edge to mmc4_dat[i:0] transition	-8.8	6.6	ns

- (1) P = output mmc4_clk period in ns
- (2) i in [i:0] = 3

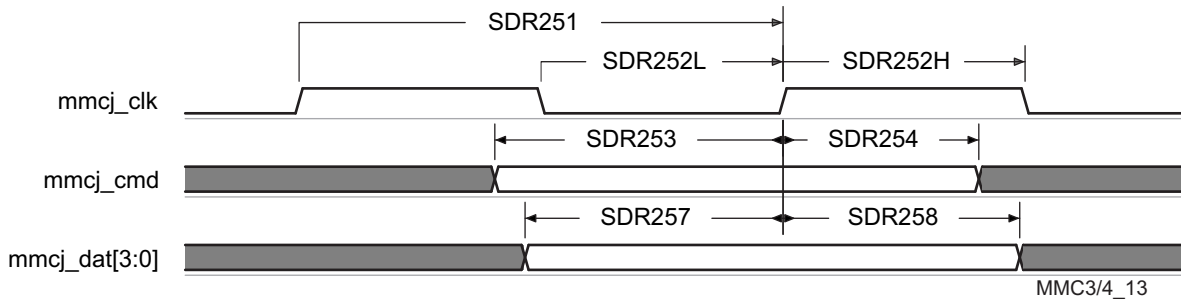


Figure 7-66. MMC/SD/SDIOj in - SDR25 - Receiver Mode

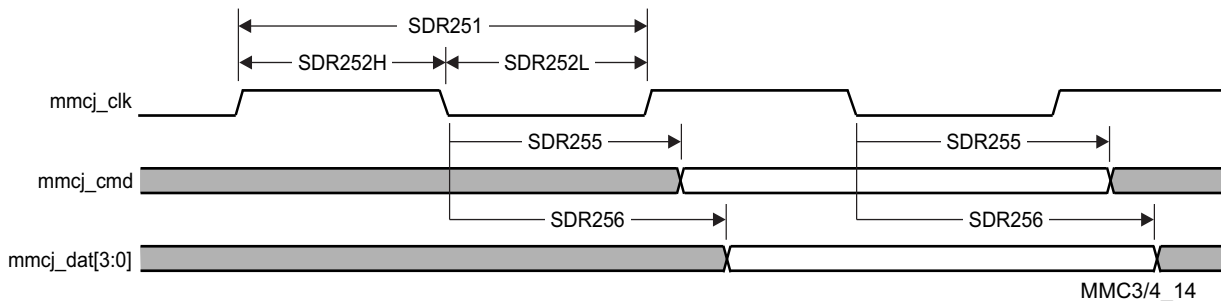


Figure 7-67. .MMC/SD/SDIOj in - SDR25 - Transmitter Mode

7.21.2.5 MMC3 SDIO High-Speed UHS-I SDR50 Mode, Half Cycle

Figure 7-68, Figure 7-69, Table 7-109, and Table 7-110 present Timing requirements and Switching characteristics for MMC3 - SDIO High speed SDR50 in receiver and transmitter mode.

Table 7-109. Timing Requirements for MMC3 - SDR50 Mode ⁽¹⁾

NO.	PARAMETER	DESCRIPTION	MIN	MAX	UNIT
SDR503	$t_{su}(cmdV-clkH)$	Setup time, mmc3_cmd valid before mmc3_clk rising clock edge	1.48		ns
SDR504	$t_h(clkH-cmdV)$	Hold time, mmc3_cmd valid after mmc3_clk rising clock edge	1.6		ns
SDR507	$t_{su}(dV-clkH)$	Setup time, mmc3_dat[i:0] valid before mmc3_clk rising clock edge	1.48		ns
SDR508	$t_h(clkH-dV)$	Hold time, mmc3_dat[i:0] valid after mmc3_clk rising clock edge	1.6		ns

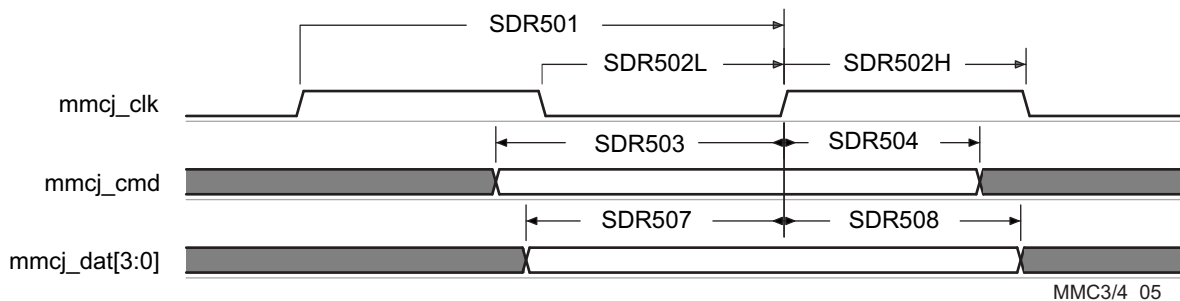
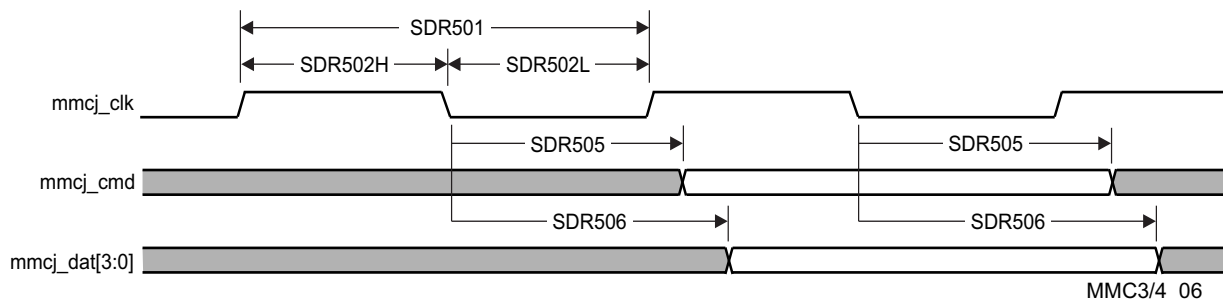
(1) i in [i:0] = 7

Table 7-110. Switching Characteristics for MMC3 - SDR50 Mode ⁽²⁾

NO.	PARAMETER	DESCRIPTION	MIN	MAX	UNIT
SDR501	fop(clk)	Operating frequency, mmc3_clk		64	MHz
SDR502H	$t_w(clkH)$	Pulse duration, mmc3_clk high	0.5*P-0.270 ⁽¹⁾		ns
SDR502L	$t_w(clkL)$	Pulse duration, mmc3_clk low	0.5*P-0.270 ⁽¹⁾		ns
SDR505	$t_d(clkL-cmdV)$	Delay time, mmc3_clk falling clock edge to mmc3_cmd transition	-3.66	1.46	ns
SDR506	$t_d(clkL-dV)$	Delay time, mmc3_clk falling clock edge to mmc3_dat[i:0] transition	-3.66	1.46	ns

(1) P = output mmc3_clk period in ns

(2) i in [i:0] = 7

**Figure 7-68. MMC/SD/SDIOj in - High Speed SDR50 - Receiver Mode****Figure 7-69. MMC/SD/SDIOj in - High Speed SDR50 - Transmitter Mode****NOTE**

To configure the desired Manual IO Timing Mode the user must follow the steps described in section Manual IO Timing Modes of the Device TRM.

The associated registers to configure are listed in the **CFG REGISTER** column. For more information see the Control Module chapter in the Device TRM.

Manual IO Timings Modes must be used to guarantee some IO timings for MMC3. See [Table 7-2 Modes Summary](#) for a list of IO timings requiring the use of Manual IO Timings Modes. See [Table 7-111 Manual Functions Mapping for MMC3](#) for a definition of the Manual modes.

Table 7-111 lists the A_DELAY and G_DELAY values needed to calculate the correct values to be set in the CFG_x registers.

Table 7-111. Manual Functions Mapping for MMC3

BALL	BALL NAME	MMC3_MANUAL1		CFG REGISTER	MUXMODE
		A_DELAY (ps)	G_DELAY (ps)		0
W5	mmc3_clk	0	386	CFG_MMC3_CLK_IN	mmc3_clk
W5	mmc3_clk	605	0	CFG_MMC3_CLK_OUT	mmc3_clk
W4	mmc3_cmd	0	0	CFG_MMC3_CMD_IN	mmc3_cmd
W4	mmc3_cmd	0	0	CFG_MMC3_CMD_OEN	mmc3_cmd
W4	mmc3_cmd	0	0	CFG_MMC3_CMD_OUT	mmc3_cmd
U6	mmc3_dat0	171	0	CFG_MMC3_DAT0_IN	mmc3_dat0
U6	mmc3_dat0	0	0	CFG_MMC3_DAT0_OEN	mmc3_dat0
U6	mmc3_dat0	0	0	CFG_MMC3_DAT0_OUT	mmc3_dat0
V6	mmc3_dat1	221	0	CFG_MMC3_DAT1_IN	mmc3_dat1
V6	mmc3_dat1	0	0	CFG_MMC3_DAT1_OEN	mmc3_dat1
V6	mmc3_dat1	0	0	CFG_MMC3_DAT1_OUT	mmc3_dat1
U5	mmc3_dat2	0	0	CFG_MMC3_DAT2_IN	mmc3_dat2
U5	mmc3_dat2	0	0	CFG_MMC3_DAT2_OEN	mmc3_dat2
U5	mmc3_dat2	0	0	CFG_MMC3_DAT2_OUT	mmc3_dat2
V3	mmc3_dat3	474	0	CFG_MMC3_DAT3_IN	mmc3_dat3
V3	mmc3_dat3	0	0	CFG_MMC3_DAT3_OEN	mmc3_dat3
V3	mmc3_dat3	0	0	CFG_MMC3_DAT3_OUT	mmc3_dat3
V5	mmc3_dat4	792	0	CFG_MMC3_DAT4_IN	mmc3_dat4
V5	mmc3_dat4	0	0	CFG_MMC3_DAT4_OEN	mmc3_dat4
V5	mmc3_dat4	0	0	CFG_MMC3_DAT4_OUT	mmc3_dat4
W6	mmc3_dat5	782	0	CFG_MMC3_DAT5_IN	mmc3_dat5
W6	mmc3_dat5	0	0	CFG_MMC3_DAT5_OEN	mmc3_dat5
W6	mmc3_dat5	0	0	CFG_MMC3_DAT5_OUT	mmc3_dat5
W3	mmc3_dat6	942	0	CFG_MMC3_DAT6_IN	mmc3_dat6
W3	mmc3_dat6	0	0	CFG_MMC3_DAT6_OEN	mmc3_dat6
W3	mmc3_dat6	0	0	CFG_MMC3_DAT6_OUT	mmc3_dat6
V4	mmc3_dat7	636	0	CFG_MMC3_DAT7_IN	mmc3_dat7
V4	mmc3_dat7	0	0	CFG_MMC3_DAT7_OEN	mmc3_dat7
V4	mmc3_dat7	0	0	CFG_MMC3_DAT7_OUT	mmc3_dat7

Manual IO Timings Modes must be used to guarantee some IO timings for MMC4. See [Table 7-2 Modes Summary](#) for a list of IO timings requiring the use of Manual IO Timings Modes. See [Table 7-112 Manual Functions Mapping for MMC4](#) for a definition of the Manual modes.

Table 7-112 lists the A_DELAY and G_DELAY values needed to calculate the correct values to be set in the CFG_x registers.

Table 7-112. Manual Functions Mapping for MMC4

BALL	BALL NAME	MMC4_MANUAL1		MMC4_DS_MANUAL1		CFG REGISTER	MUXMODE
		A_DELAY (ps)	G_DELAY (ps)	A_DELAY (ps)	G_DELAY (ps)		3
H25	uart1_ctsn	0	0	0	0	CFG_UART1_CTSN_IN	mmc4_clk
H25	uart1_ctsn	1147	0	0	0	CFG_UART1_CTSN_OUT	mmc4_clk
H24	uart1_rtsn	1834	0	307	0	CFG_UART1_RTSN_IN	mmc4_cmd
H24	uart1_rtsn	0	0	0	0	CFG_UART1_RTSN_OEN	mmc4_cmd

Table 7-112. Manual Functions Mapping for MMC4 (continued)

BALL	BALL NAME	MMC4_MANUAL1		MMC4_DS_MANUAL1		CFG REGISTER	MUXMODE
		A_DELAY (ps)	G_DELAY (ps)	A_DELAY (ps)	G_DELAY (ps)		3
H24	uart1_rtsn	0	0	0	0	CFG_UART1_RTSN_OUT	mmc4_cmd
J22	uart2_ctsn	2165	0	785	0	CFG_UART2_CTSN_IN	mmc4_dat2
J22	uart2_ctsn	0	0	0	0	CFG_UART2_CTSN_OEN	mmc4_dat2
J22	uart2_ctsn	0	0	0	0	CFG_UART2_CTSN_OUT	mmc4_dat2
J24	uart2_rtsn	1929	64	613	0	CFG_UART2_RTSN_IN	mmc4_dat3
J24	uart2_rtsn	0	0	0	0	CFG_UART2_RTSN_OEN	mmc4_dat3
J24	uart2_rtsn	0	0	0	0	CFG_UART2_RTSN_OUT	mmc4_dat3
H23	uart2_rxd	1935	128	683	0	CFG_UART2_RXD_IN	mmc4_dat0
H23	uart2_rxd	0	0	0	0	CFG_UART2_RXD_OEN	mmc4_dat0
H23	uart2_rxd	0	0	0	0	CFG_UART2_RXD_OUT	mmc4_dat0
J25	uart2_txd	2172	44	835	0	CFG_UART2_TXD_IN	mmc4_dat1
J25	uart2_txd	0	0	0	0	CFG_UART2_TXD_OEN	mmc4_dat1
J25	uart2_txd	0	0	0	0	CFG_UART2_TXD_OUT	mmc4_dat1

7.22 General-Purpose Interface (GPIO)

The general-purpose interface combines eight general-purpose input/output (GPIO) banks. Each GPIO module provides 32 dedicated general-purpose pins with input and output capabilities; thus, the general-purpose interface supports up to 247 pins.

These pins can be configured for the following applications:

- Data input (capture)/output (drive)
- Keyboard interface with a debounce cell
- Interrupt generation in active mode upon the detection of external events. Detected events are processed by two parallel independent interrupt-generation submodules to support biprocessor operations
- Wake-up request generation in idle mode upon the detection of external events

NOTE

For more information, see the General-Purpose Interface chapter of the Device TRM.

NOTE

The general-purpose input/output i ($i = 1$ to 8) bank is also referred to as GPIO i .

7.23 System and Miscellaneous interfaces

The Device includes the following System and Miscellaneous interfaces:

- Sysboot Interface
- Enhanced DMA Interface
- Interrupt Controllers (INTC) Interface
- Observability Signal (OBS) Interface

7.24 Test Interfaces

The Device includes the following Test interfaces:

- IEEE 1149.1 Standard-Test-Access Port (JTAG)
- Trace Port Interface Unit (TPIU)

- Advanced Event Triggering Interface (AET)

7.24.1 IEEE 1149.1 Standard-Test-Access Port (JTAG)

The JTAG (IEEE Standard 1149.1-1990 Standard-Test-Access Port and Boundary Scan Architecture) interface is used for BSDL testing and emulation of the device. The $\overline{\text{TRST}}$ pin only needs to be released when it is necessary to use a JTAG controller to debug the device or exercise the device's boundary scan functionality. For maximum reliability, the device includes an internal Pulldown (IPD) on the $\overline{\text{TRST}}$ pin to ensure that $\overline{\text{TRST}}$ is always asserted upon power up and the device's internal emulation logic is always properly initialized. JTAG controllers from Texas Instruments actively drive $\overline{\text{TRST}}$ high. However, some third-party JTAG controllers may not drive $\overline{\text{TRST}}$ high but expect the use of a Pullup resistor on $\overline{\text{TRST}}$. When using this type of JTAG controller, assert $\overline{\text{TRST}}$ to initialize the device after powerup and externally drive $\overline{\text{TRST}}$ high before attempting any emulation or boundary-scan operations.

The main JTAG features include:

- 32KB embedded trace buffer (ETB™)
- 5-pin system trace interface for debug
- Supports Advanced Event Triggering (AET)
- All processors can be emulated via JTAG ports
- All functions on EMU pins of the device:
 - EMU[1:0] - cross-triggering, boot mode (WIR), STM trace
 - EMU[4:2] - STM trace only (single direction)

7.24.1.1 JTAG Electrical Data/Timing

Table 7-113, Table 7-114 and Figure 7-70 assume testing over the recommended operating conditions and electrical characteristic conditions below.

Table 7-113. Timing Requirements for IEEE 1149.1 JTAG

NO.	PARAMETER	DESCRIPTION	MIN	MAX	UNIT
1	$t_c(\text{TCK})$	Cycle time, TCK	62.29		ns
1a	$t_w(\text{TCKH})$	Pulse duration, TCK high (40% of t_c)	24.92		ns
1b	$t_w(\text{TCKL})$	Pulse duration, TCK low (40% of t_c)	24.92		ns
3	$t_{su}(\text{TDI-TCK})$	Input setup time, TDI valid to TCK high	6.23		ns
	$t_{su}(\text{TMS-TCK})$	Input setup time, TMS valid to TCK high	6.23		ns
4	$t_h(\text{TCK-TDI})$	Input hold time, TDI valid from TCK high	31.15		ns
	$t_h(\text{TCK-TMS})$	Input hold time, TMS valid from TCK high	31.15		ns

Table 7-114. Switching Characteristics Over Recommended Operating Conditions for IEEE 1149.1 JTAG

NO.	PARAMETER	DESCRIPTION	MIN	MAX	UNIT
2	$t_d(\text{TCKL-TDOV})$	Delay time, TCK low to TDO valid	0	30.5	ns

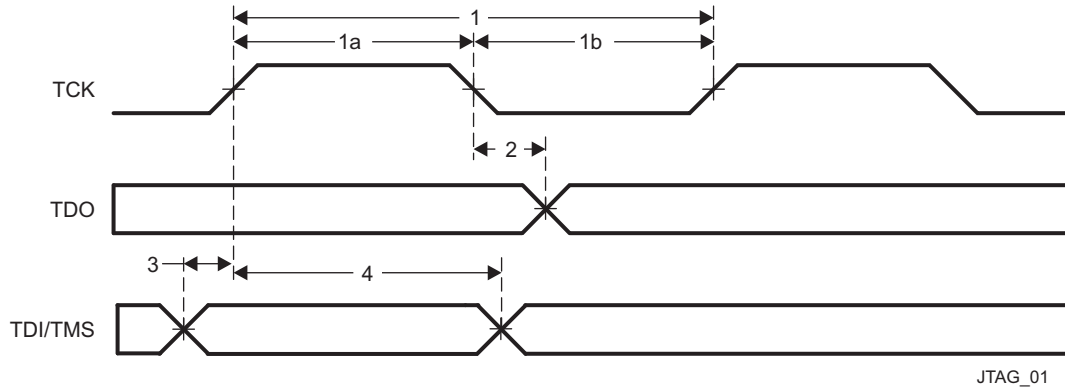


Figure 7-70. JTAG Timing

Table 7-115, Table 7-116 and Figure 7-71 assume testing over the recommended operating conditions and electrical characteristic conditions below.

Table 7-115. Timing Requirements for IEEE 1149.1 JTAG With RTCK

NO.	PARAMETER	DESCRIPTION	MIN	MAX	UNIT
1	$t_c(\text{TCK})$	Cycle time, TCK	62.29		ns
1a	$t_w(\text{TCKH})$	Pulse duration, TCK high (40% of t_c)	24.92		ns
1b	$t_w(\text{TCKL})$	Pulse duration, TCK low (40% of t_c)	24.92		ns
3	$t_{su}(\text{TDI-TCK})$	Input setup time, TDI valid to TCK high	6.23		ns
	$t_{su}(\text{TMS-TCK})$	Input setup time, TMS valid to TCK high	6.23		ns
4	$t_h(\text{TCK-TDI})$	Input hold time, TDI valid from TCK high	31.15		ns
	$t_h(\text{TCK-TMS})$	Input hold time, TMS valid from TCK high	31.15		ns

Table 7-116. Switching Characteristics Over Recommended Operating Conditions for IEEE 1149.1 JTAG With RTCK

NO.	PARAMETER	DESCRIPTION	MIN	MAX	UNIT
5	$t_d(\text{TCK-RTCK})$	Delay time, TCK to RTCK with no selected subpaths (i.e. ICEPick™ is the only tap selected - when the ARM is in the scan chain, the delay time is a function of the ARM functional clock).	0	27	ns
6	$t_c(\text{RTCK})$	Cycle time, RTCK	62.29		ns
7	$t_w(\text{RTCKH})$	Pulse duration, RTCK high (40% of t_c)	24.92		ns
8	$t_w(\text{RTCKL})$	Pulse duration, RTCK low (40% of t_c)	24.92		ns

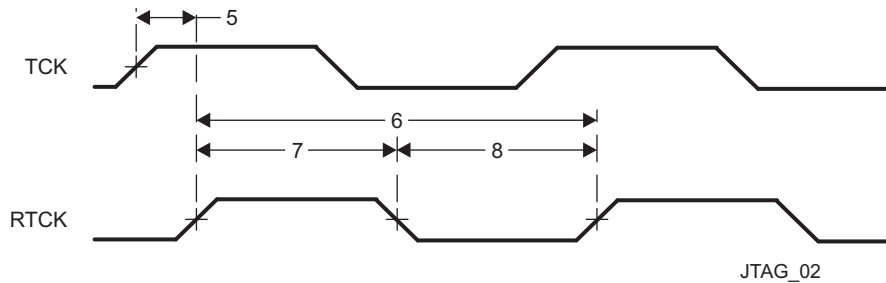


Figure 7-71. JTAG With RTCK Timing

7.24.2 Trace Port Interface Unit (TPIU)

CAUTION

The I/O timings provided in this section are valid only if signals within a single IOSET are used. The IOSETs are defined in [Table 7-118](#).

7.24.2.1 TPIU PLL DDR Mode

[Table 7-117](#) and [Figure 7-72](#) assume testing over the recommended operating conditions and electrical characteristic conditions below.

Table 7-117. Switching Characteristics for TPIU

NO.	PARAMETER	DESCRIPTION	MIN	MAX	UNIT
TPIU1	$t_{c(\text{clk})}$	Cycle time, TRACECLK period	5.56		ns
TPIU4	$t_{d(\text{clk-ctlV})}$	Skew time, TRACECLK transition to TRACECTL transition	-0.96	0.96	ns
TPIU5	$t_{d(\text{clk-dataV})}$	Skew time, TRACECLK transition to TRACEDATA[17:0]	-0.96	0.96	ns

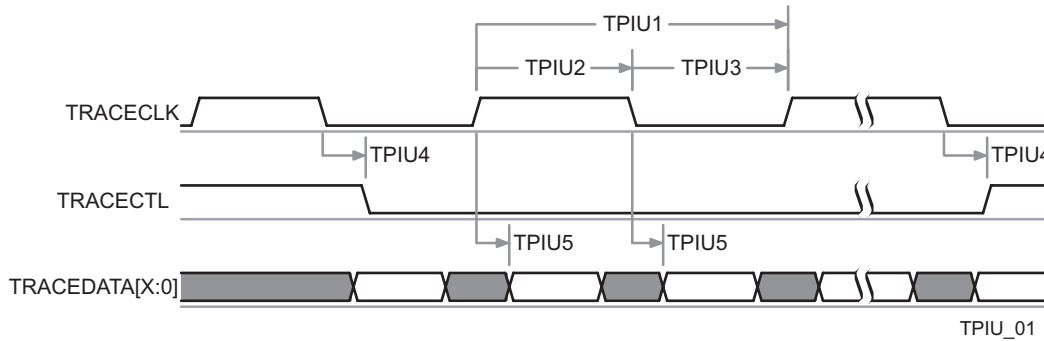


Figure 7-72. TPIU—PLL DDR Transmit Mode⁽¹⁾

(1) In d[X:0], X is equal to 15 or 17.

In [Table 7-118](#) are presented the specific groupings of signals (IOSET) for use with TPIU signals.

Table 7-118. TPIU IOSETs

SIGNALS	IOSET1		IOSET2	
	BALL	MUX	BALL	MUX
emu0	E20	0	E20	0
emu1	D21	0	D21	0
emu2	A11	2	A11	2
emu3	B12	2	B12	2
emu4	D15	2	D15	2
emu5	D4	5	C9	2
emu6	B4	5	A13	2
emu7	E6	5	A12	2
emu8	D5	5	B14	2
emu9	C4	5	B13	2
emu10	C3	5	B10	2
emu11	B2	5	C14	2
emu12	E7	5	C10	2
emu13	B3	5	A10	2

Table 7-118. TPIU IOSETs (continued)

SIGNALS	IOSET1		IOSET2	
	BALL	MUX	BALL	MUX
emu14	A3	5	C13	2
emu15	C6	5	E15	2
emu16	A4	5	D9	2
emu17	B5	5	E14	2
emu18	C5	5	D14	2
emu19	A7	5	D11	2

8 Applications, Implementation, and Layout

NOTE

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test design implementation to confirm system functionality.

8.1 Introduction

This chapter is intended to communicate, guide and illustrate a PCB design strategy resulting in a PCB that can support TI's latest Application Processor. This Processor is a high-performance processor designed for automotive Infotainment and Advanced Driver Assistance Systems based on enhanced OMAP™ architecture integrated on a 28-nm CMOS process technology.

These guidelines first focus on designing a robust Power Delivery Network (PDN) which is essential to achieve the desirable high performance processing available on Device. The general principles and step-by-step approach for implementing good power integrity (PI) with specific requirements will be described for the key Device power domains.

TI strongly believes that simulating a PCB's proposed PDN is required for first pass PCB design success. Key Device processor high-current power domains need to be evaluated for Power Rail IR Drop, Decoupling Capacitor Loop-Inductance and Power Rail Target Impedance. Only then can a PCB's PDN performance be truly accessed by comparing these model PI parameters vs. TI's recommended values. Ultimately for any high-volume product, TI recommends conducting a "Processor PDN Validation" test on prototype PCBs across processor "split lots" to verify PDN robustness meets desired performance goals for each customer's worst-case scenario. Please contact your TI representative to receive guidance on PDN PI modeling and validation testing.

Likewise, the methodology and requirements needed to route Device high-speed, differential interfaces (i.e. USB2.0, USB3.0, HDMI, PCI, SATA), single-ended interfaces (i.e. DDR2/DDR3, QSPI) and general purpose interfaces using LVCMOS drivers that meet timing requirements while minimizing signal integrity (SI) distortions on the PCB's signaling traces. Signal trace lengths and flight times are aligned with FR-4 standard specification for PCBs.

Several different PCB layout stack-up examples have been presented to illustrate a typical number of layers, signal assignments and controlled impedance requirements. Different Device interface signals demand more or less complexity for routing and controlled impedance stack-ups. Optimizing the PCB's PDN stack-up needs with all of these different types of signal interfaces will ultimately determine the final layer count and layer assignments in each customer's PCB design.

This guideline must be used as a supplement in complement to TI's Application Processor, Power Management IC (PMIC) and Audio Companion components along with other TI component technical documentation (i.e. Technical Reference Manual, Data Manual, Data Sheets, Silicon Errata, Pin-Out Spreadsheet, Application Notes, etc.).

NOTE

Notwithstanding any provision to the contrary, TI makes no warranty expressed, implied, or statutory, including any implied warranty of merchantability of fitness for a specific purpose, for customer boards. The data described in this appendix are intended as guidelines only.

NOTE

These PCB guidelines are in a draft maturity and consequently, are subject to change depending on design verification testing conducted during IC development and validation. Note also that any references to Application Processor's ballout or pin muxing are subject to change following the processor's ballout maturity.

8.1.1 Initial Requirements and Guidelines

Unless otherwise specified, the characteristic impedance for single-ended interfaces is recommended to be between 35 Ω and 65 Ω to minimize the overshoot or undershoot on far-end loads.

Characteristic impedance for differential interfaces must be routed as differential traces on the same layer. The trace width and spacing must be chosen to yield the recommended differential impedance. For more information see [Section 8.5.1](#).

The PDN must be optimized for low trace resistance and low trace inductance for all high-current power nets from PMIC to the device.

An external interface using a connector must be protected following the IEC61000-4-2 level 4 system ESD.

8.2 Power Optimizations

This section describes the necessary steps for designing a robust Power Distribution Network (PDN):

- [Section 8.2.1, Step 1](#): PCB Stack-up
- [Section 8.2.2, Step 2](#): Physical Placement
- [Section 8.2.3, Step 3](#): Static Analysis
- [Section 8.2.4, Step 4](#): Frequency Analysis

8.2.1 Step 1: PCB Stack-up

The PCB stack-up (layer assignment) is an important factor in determining the optimal performance of the power distribution system. An optimized PCB stack-up for higher power integrity performance can be achieved by following these recommendations:

- Power and ground plane pairs must be closely coupled together. The capacitance formed between the planes can decouple the power supply at high frequencies. Whenever possible, the power and ground planes must be solid to provide continuous return path for return current.
- Use a thin dielectric between the power and ground plane pair. Capacitance is inversely proportional to the separation of the plane pair. Minimizing the separation distance (the dielectric thickness) maximizes the capacitance.
- Optimize the power and ground plane pair carrying high current supplies to key component power domains as close as possible to the same surface where these components are placed (see [Figure 8-1](#)). This will help to minimize "loop inductance" encountered between supply decoupling capacitors and component supply inputs and between power and ground plane pairs.

NOTE

1-2oz Cu weight for power / ground plane is preferred to enable better PCB heat spreading, helping to reduce Processor junction temperatures. In addition, it is preferable to have the power / ground planes be adjacent to the PCB surface on which the Processor is mounted.

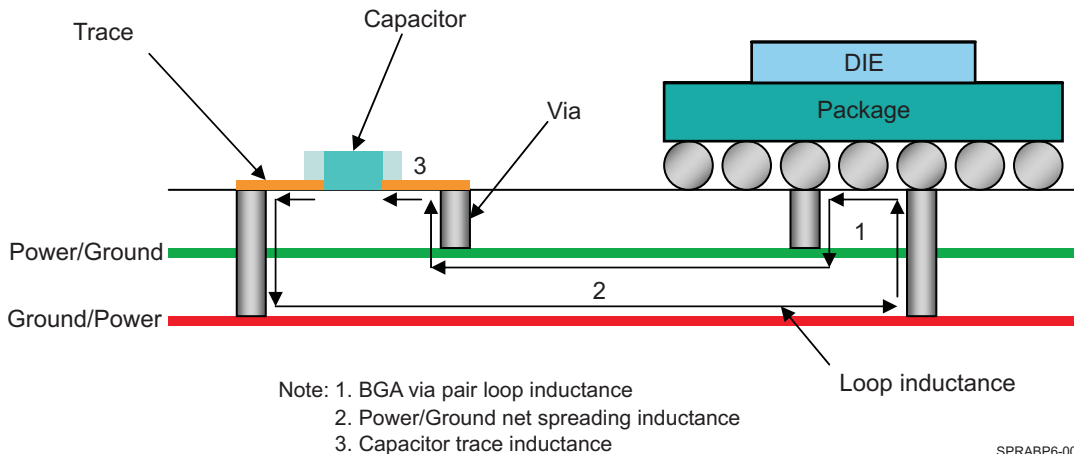


Figure 8-1. Minimize Loop Inductance With Proper Layer Assignment

The placement of power and ground planes in the PCB stackup (determined by layer assignment) has a significant impact on the parasitic inductances of power current path as shown in Figure 8-1. For this reason, it is recommended to consider layer order in the early stages of the PCB PDN design cycle, putting high-priority supplies in the top half of the stackup (assuming high load and priority components are mounted on the top-side of PCB) and low-priority supplies in the bottom half of the stackup as shown in the examples below (vias have parasitic inductances which impact the bottom layers more, so it is advised to put the sensitive and high-priority power supplies on the top/same layers).

Two PCB stack-ups with layer assignments and via types that can enable an optimize PDN are shown in Figure 8-2 and Figure 8-3.

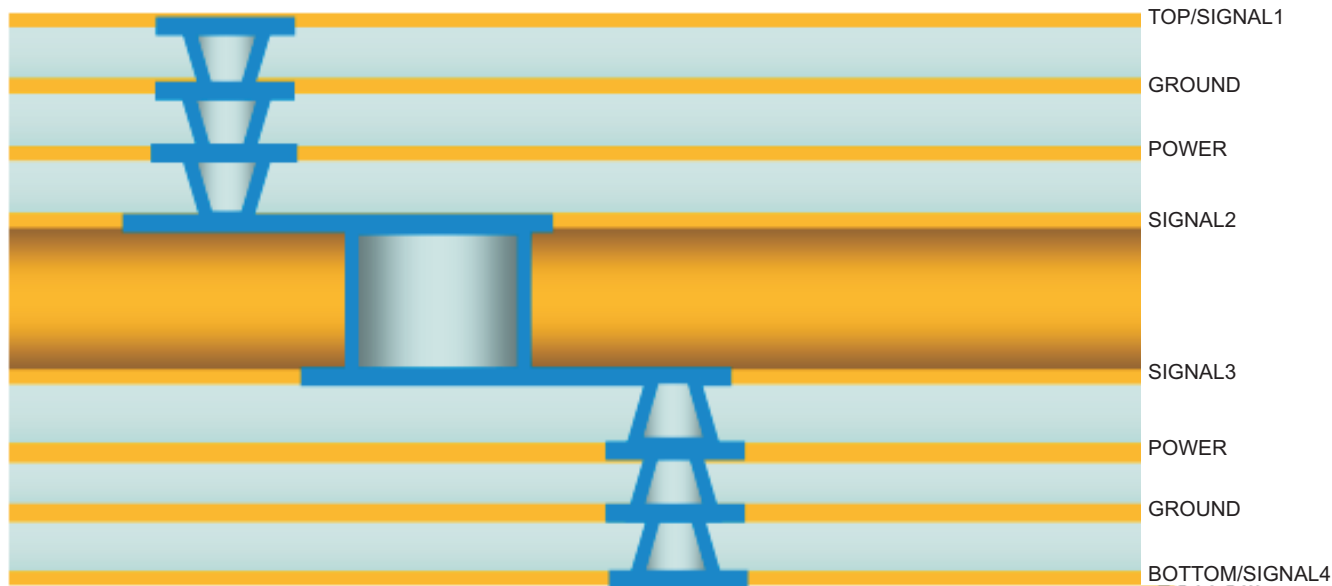
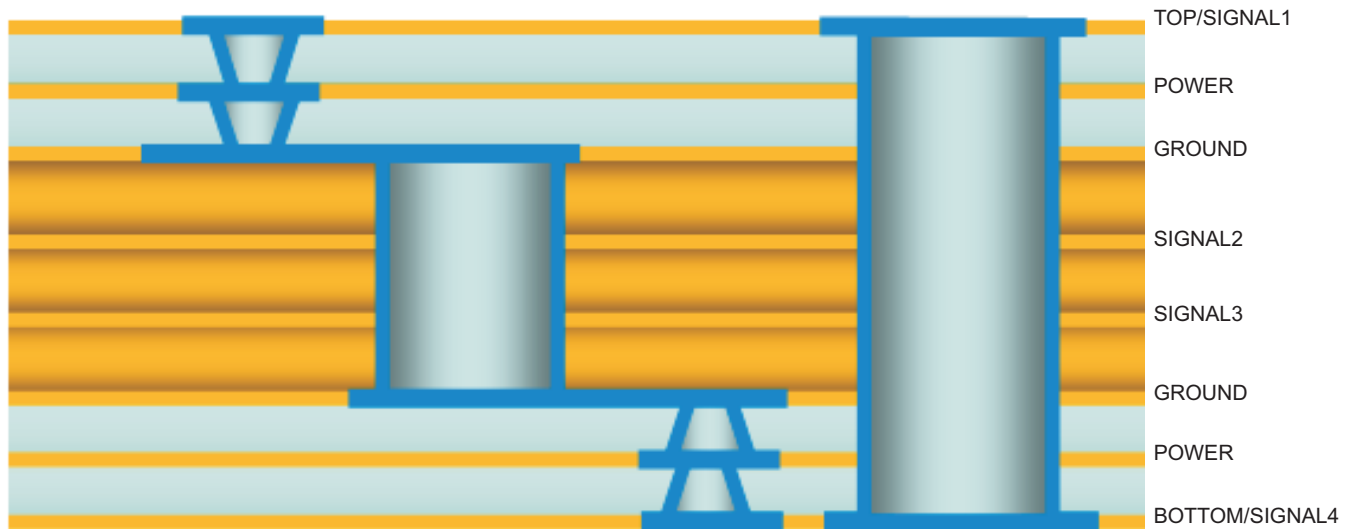


Figure 8-2. Layer PCB With High Density Interconnect (HDI) Vias



SPRABP6-003

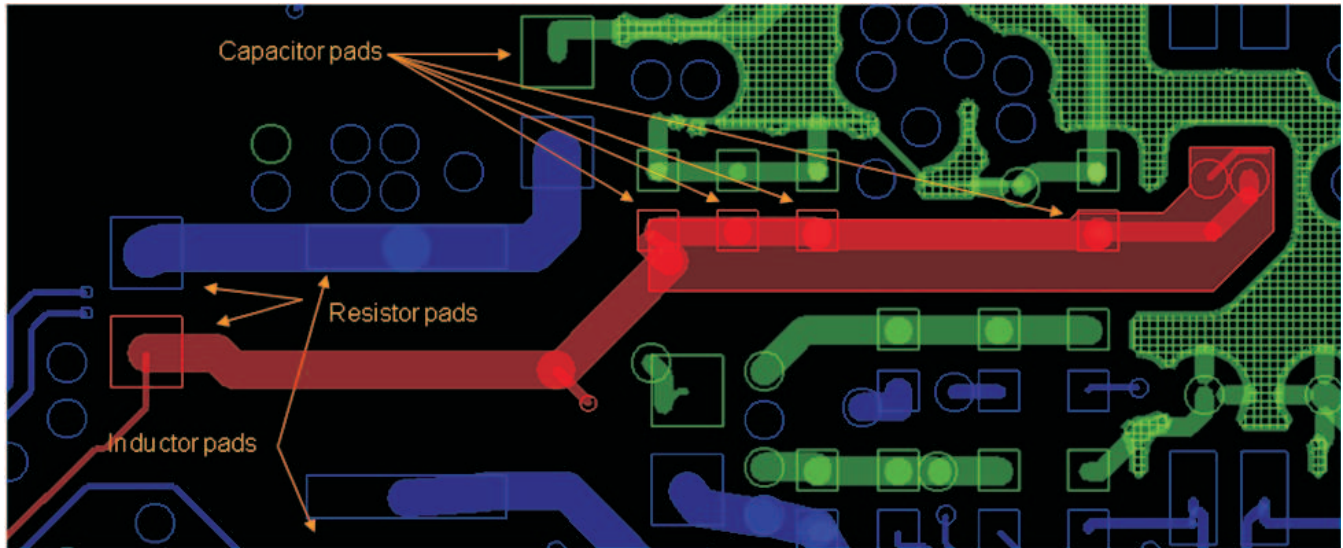
Figure 8-3. Layer PCB With Plated Through Holes (PTH) Vias

8.2.2 Step 2: Physical Placement

A critical step in designing an optimized PDN is that proper care must be taken to making sure that the initial floor planning of the PCB layout is done with good power integrity design guidelines in mind. The following points are important for optimizing a PCB's PDN:

- Minimizing the physical distance between power sources and key high load components is the first step toward optimization. Placing source and load components on the same side of the PCB is desirable. This will minimize via inductance impact for high current loads and steps
- External trace routing between components must be as wide as possible. The wider the traces, the lower the DC resistance and consequently the lower the static IR drop.
- Whenever possible for the internal layers (routing and plane), wide traces and copper area fills are preferred for PDN layout. The routing of power nets in plane provide for more interplane capacitance and improved high frequency performance of the PDN.
- Whenever possible, use a via to component pin/pad ratio of 1:1 or better (i.e. especially decoupling capacitors, power inductors and current sensing resistors). Do not share vias among multiple capacitors for connecting power supply and ground planes.
- Placement of vias must be as close as possible or even within a component's solder pad if the PCB technology you are using provides this capability.

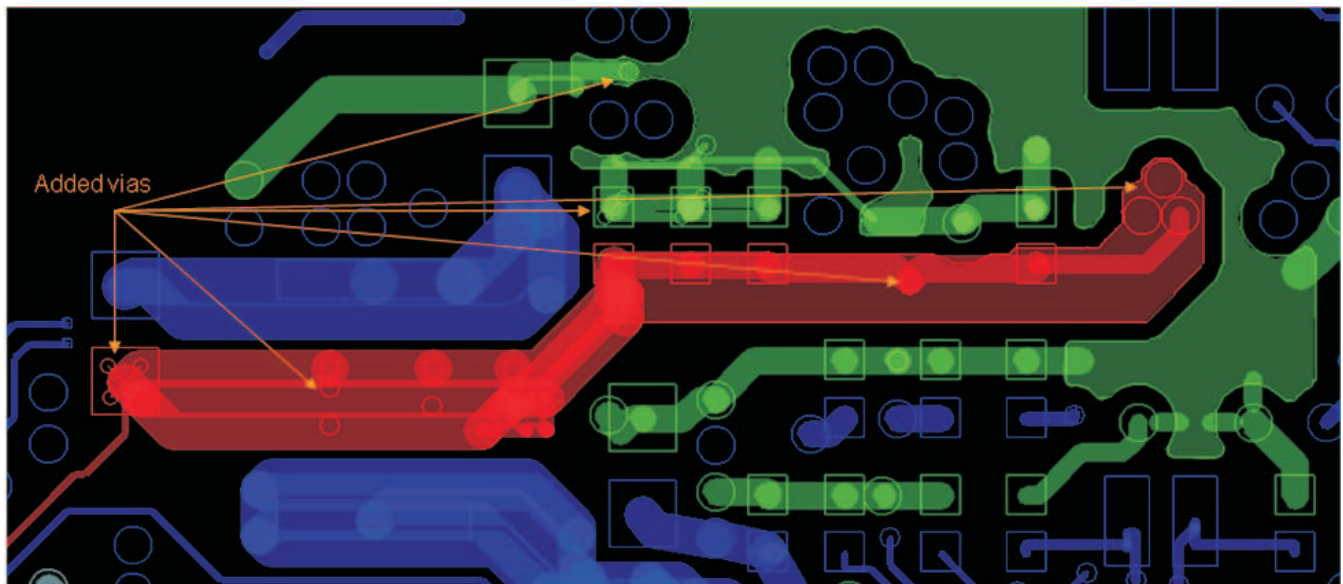
[Figure 8-4](#) shows an example of acceptable width for power net routing but with poor via placement.



SWPS040-211

Figure 8-4. Poor Via Assignment for PDN

Figure 8-5 shows an improved power net routing with better via assignment and placement, respectively.



SWPS040-212

Figure 8-5. Improved Via Assignment for PDN

- To avoid any “ampacity” issue – maximum current-carrying capacity of each transitional via should be evaluated to determine the appropriate number of vias required to connect components.

Figure 8-6 and Figure 8-7 show examples of “via starvation” on a power net transitioning from top routing layer to internal layers and the improved layout, respectively. Adding vias to bring the “via-to-pad” ratio to 1:1 will improve PDN performance.



SWPS040-213

One via for 5 capacitor pads is NOT good practice

Figure 8-6. Via Starvation



SWPS040-214

Added vias

Figure 8-7. Improved Layout With More Transitional Vias

- For noise sensitive power supplies (i.e. Phase Lock-Loops, analog signals like audio and video), a Gnd shield can be used to isolate coplanar supplies that may have high step currents or high frequency switching transitions from coupling into low-noise supplies.

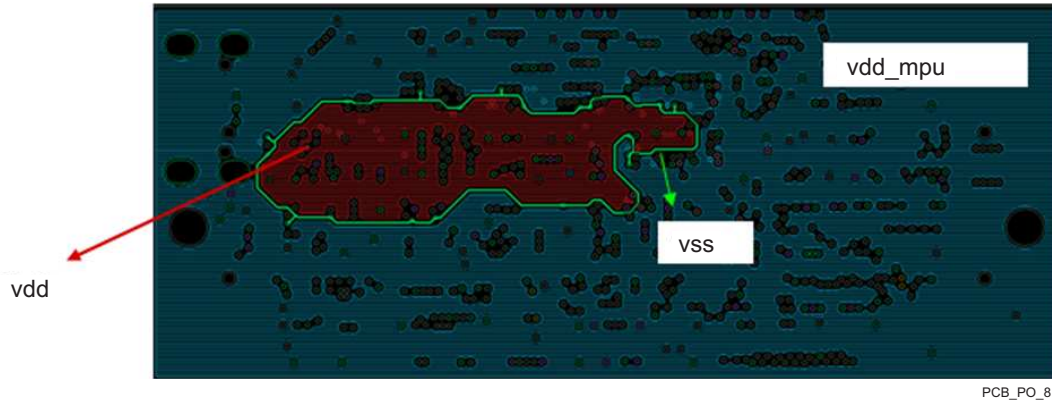


Figure 8-8. Coplanar Shielding of Power Net Using Ground Guard-band

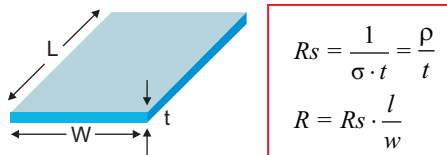
8.2.3 Step 3: Static Analysis

Delivering reliable power to circuits is always of critical importance because voltage drops (also known as IR drops) can happen at every level within an electronic system, on-chip, within a package, and across the board. Robust system performance can only be ensured by understanding how the system elements will perform under typical stressful Use Cases. Therefore, it is a good practice to perform a Static or DC Analysis.

Static or DC analysis and design methodology results in a PDN design that minimizes voltage or IR drops across power and ground planes, traces and vias. This ensures the application processor’s internal transistors will be operating within their specified voltage ranges for proper functionality. The amount of IR drop that will be encountered is based upon amount power drawn for a desired Use Case and PCB trace (widths, geometry and number of parallel traces) and via (size, type and number) characteristics.

Components that are distant from their power source are particularly susceptible to IR drop. Designs that rely on battery power must minimize voltage drops to avoid unacceptable power loss that can negatively impact system performance. Early assessments a PDN’s static (DC) performance helps to determine basic power distribution parameters such as best system input power point, optimal PCB layer stackup, and copper area needed for load currents.

The resistance R_s of a plane conductor for a unit length and unit width is called the **surface resistivity** (ohms per square).



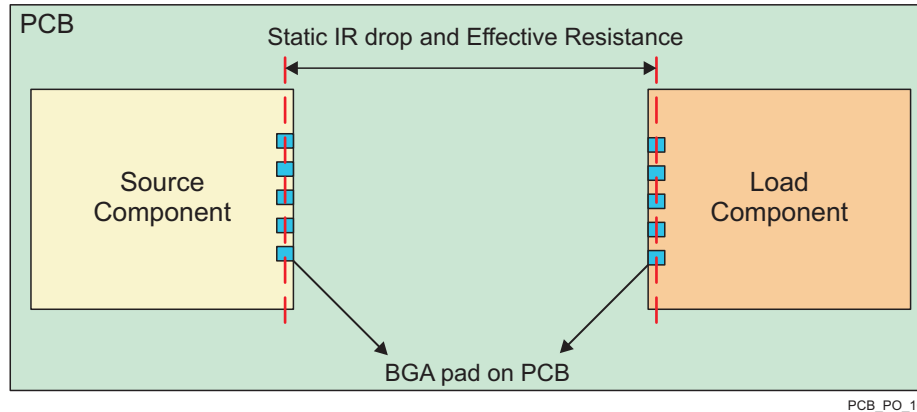
SWPS040-178

Figure 8-9. Depiction of Sheet Resistivity and Resistance

Ohm’s Law ($V = I \times R$) relates conduction current to voltage drop. At DC, the relation coefficient is a constant and represents the resistance of the conductor. Even current carrying conductors will dissipate power at high currents even though their resistance may be very small. Both voltage drop and power dissipation are proportional to the resistance of the conductor.

Figure 8-10 shows a PCB-level static IR drop budget defined between the power management device (PMIC) pins and the application processor’s balls when the PMIC is supplying power.

- It is highly recommended to physically place the PMIC as close as possible to the processor and on the same side. The orientation of the PMIC vs. processor should be aligned to minimize distance for the highest current rail.



PCB_PO_10

Figure 8-10. Static IR Drop Budget for PCB Only

The system-level IR drop budget is made up of three portions: on-chip, package, and PCB board. Static IR or DC analysis/design methodology consists of designing the PDN such that the voltage drop (under DC operating conditions) across power and ground pads of the transistors of the application processor device is within a specified value of the nominal voltage for proper functionality of the device.

A PCB system-level voltage drop budget for proper device functionality is typically 1.5% of nominal voltage. For a 1.35-V supply, this would be ≤ 20 mV.

To accurately analyze PCB static IR drop, the actual geometry of the PDN must be modeled properly and simulated to accurately characterize long distribution paths, copper weight impacts, electro-migration violations of current-carrying vias, and “Swiss-cheese” effects via placement has on power rails. It is recommended to perform the following analyses:

- Lumped resistance/IR drop analysis
- Distributed resistance/IR drop analysis

NOTE

The PMIC companion device supporting Processor has been designed with voltage sensing feedback loop capabilities that enable a remote sense of the SMPS output voltage at the point of use.

The NOTE above means the SMPS feedback signals and returns must be routed across PCB and connected to the Device input power ball for which a particular SMPS is supplying power. This feedback loop provides compensation for some of the voltage drop encountered across the PDN within limits. As such, the effective resistance of the PDN within this loop should be determined in order to optimize voltage compensation loop performance. The resistance of two PDN segments are of interest: one from the power inductor/bulk power filtering capacitor node to the Processor's input power and second is the entire PDN route from SMPS output pin/ball to the Processor input power.

In the following sections each methodology is described in detail and an example has been provided of analysis flow that can be used by the PCB designer to validate compliance to the requirements on their PCB PDN design.

8.2.3.1 PDN Resistance and IR Drop

Lumped methodology consists of grouping all of the power pins on both the PMIC (voltage source) and processor (current sink) devices. Then the PMIC source is set to an expected Use Case voltage level and the processor load has its Use Case current sink value set as well. Now the lumped/effective resistance for the power rail trace/plane routes can be determine based upon the actual layout's power rail etch wide, shape, length, via count and placement [Figure 8-11](#) illustrates the pin-grouping/lumped concept.

The lumped methodology consists of importing the PCB layout database (from Cadence Allegro tool or any other layout design tool) into the static IR drop modeling and simulation tool of preference for the PCB designer. This is followed by applying the correct PCB stack-up information (thickness, material properties) of the PCB dielectric and metallization layers. The material properties of dielectric consist of permittivity (Dk) and loss tangent (Df).

For the conductor layers, the correct conductivity needs to be programmed into the simulation tool. This is followed by pin-grouping of the power and ground nets, and applying appropriate voltage/current sources. The current and voltage information can be obtained from the power and voltage specifications of the device under different operating conditions / Use Cases.

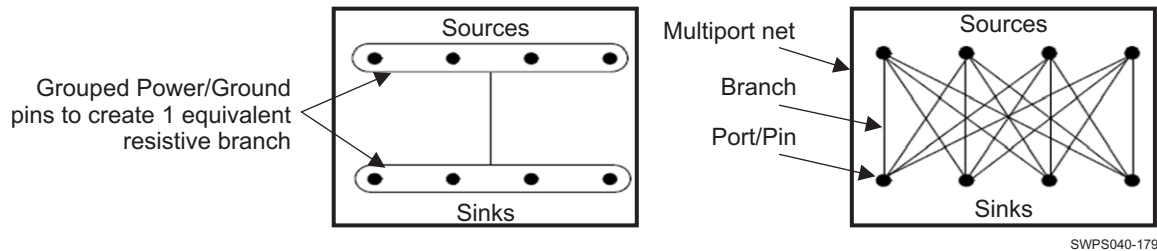


Figure 8-11. Pin-grouping concept: Lumped and Distributed Methodologies

8.2.4 Step 4: Frequency Analysis

Delivering low noise voltage sources are very important to allowing a system to operate at the lowest possible Operational Performance Point (OPP) for any one Use Case. An OPP is a combination of the supply voltage level and clocking rate for key internal processor domains. A SCH and PCB designed to provide low noise voltage supplies will then enable the processor to enter optimal OPPs for each Use Case that in turn will minimize power dissipation and junction temperatures on-die. Therefore, it is a good engineering practice to perform a Frequency Analysis over the key power domains.

Frequency analysis and design methodology results in a PDN design that minimizes transient noise voltages at the processor's input power balls. This allows the processor's internal transistors to operate near the minimum specified operating supply voltage levels. To accomplish this one must evaluate how a voltage supply will change due to impedance variations over frequency. This analysis will focus on the decoupling capacitor network (VDD_xxx and VSS/Gnd rails) at the load. Sufficient capacitance with a distribution of self-resonant points will provide for an overall lower impedance vs frequency response for each power domain.

Decoupling components that are distant from their load's input power are susceptible to encountering spreading loop inductance from the PCB design. Early analysis of each key power domain's frequency response helps to determine basic decoupling capacitor placement, optimal footprint, layer assignment, and types needed for minimizing supply voltage noise/fluctuations due to switching and load current transients.

NOTE

Evaluation of loop inductance values for decoupling capacitors placed ~300mils closer to the load's input power balls has shown an 18% reduction in loop inductance due to reduced distance.

- Decoupling capacitors must be carefully placed in order to minimize loop inductance impact on supply voltage transients. A real capacitor has characteristics not only of capacitance but also inductance and resistance.

Figure 8-12 shows the parasitic model of a real capacitor. A real capacitor must be treated as an RLC circuit with effective series resistance (ESR) and effective series inductance (ESL).

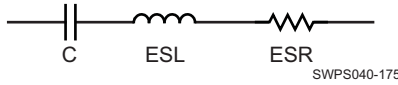


Figure 8-12. Characteristics of a Real Capacitor With ESL and ESR

The magnitude of the impedance of this series model is given as:

$$|Z| = \sqrt{ESR^2 + \left(\omega ESL - \frac{1}{\omega C} \right)^2}$$

where: $\omega = 2\pi f$

SWPS040-e002

Figure 8-13. Series Model Impedance Equation

Figure 8-14 shows the resonant frequency response of a typical capacitor with a self-resonant frequency of 55 MHz. The impedance of the capacitor is a combination of its series resistance and reactive capacitance and inductance as shown in the equation above.

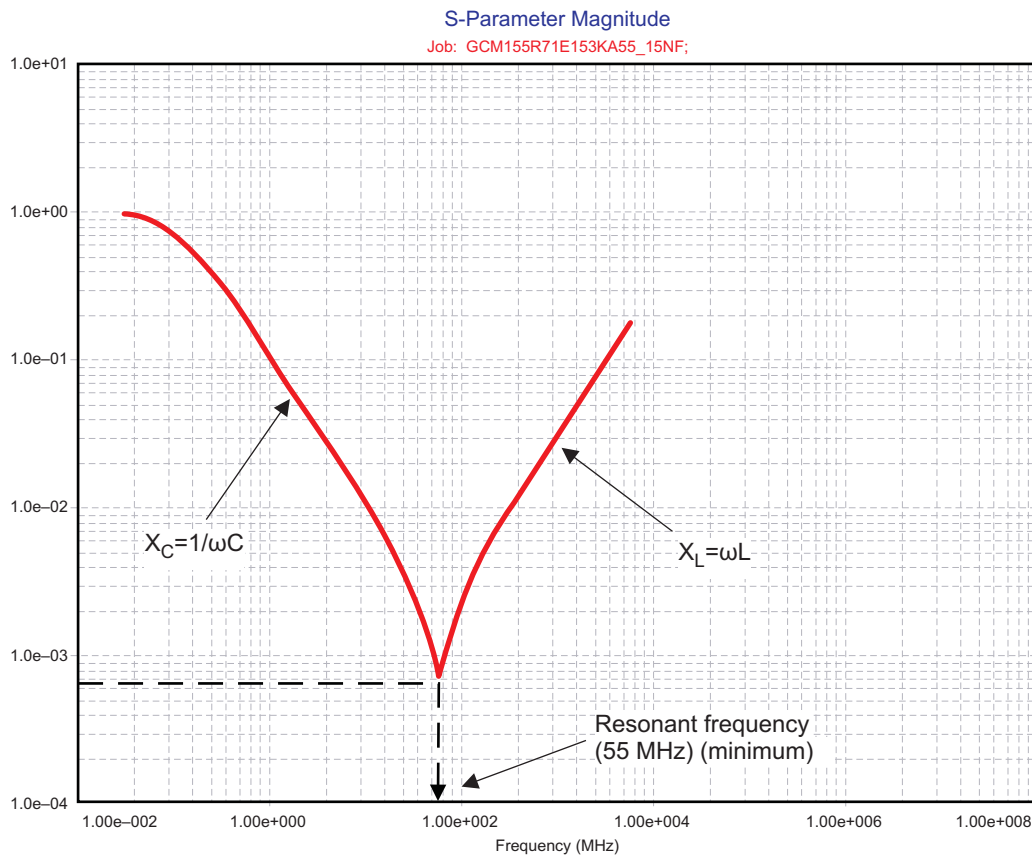


Figure 8-14. Typical Impedance Profile of a Capacitor

Because a capacitor has series inductance and resistance that impacts its effectiveness, it is important that the following recommendations are adopted in placing capacitors on the PDN.

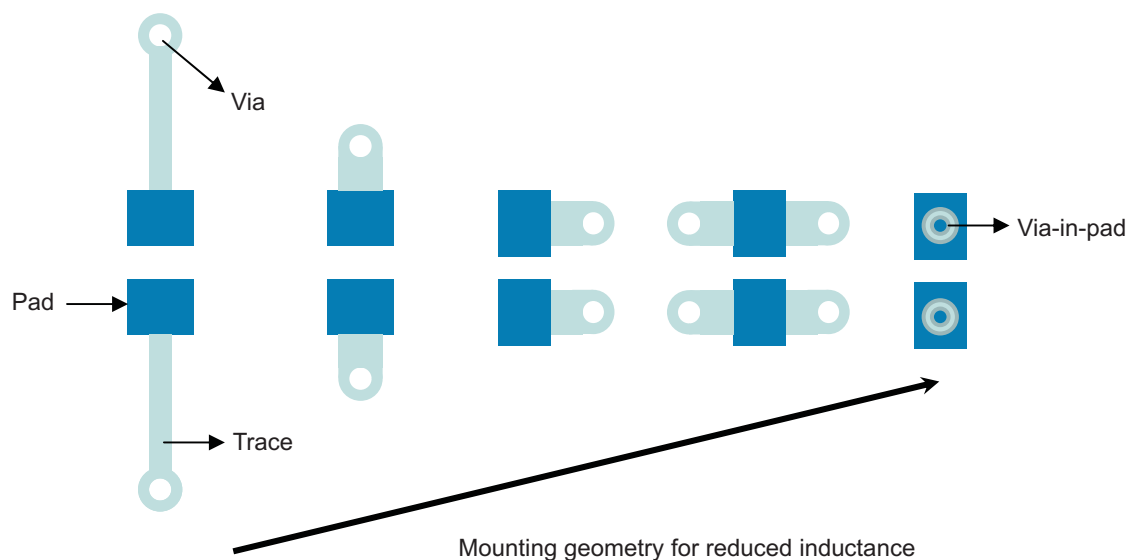
Wherever possible, mount the capacitor with the geometry that minimizes the mounting inductance and resistance. This was shown earlier in Figure 8-1. The capacitor mounting inductance and resistance values include the inductance and resistance of the pads, trace, and vias. Whenever possible, use footprints that have the lowest inductance configuration as shown in Figure 8-15

The length of a trace used to connect a capacitor has a big impact on parasitic inductance and resistance of the mounting. This trace must be as short and as wide as possible. Wherever possible, minimize distance to supply and Gnd vias by locating vias nearby or within the capacitor's solder pad landing. Further improvements can be made to the mounting by placing vias to the side of capacitor lands or doubling the number of vias as shown in Figure 8-15. If the PCB manufacturing processes allow it and if cost-effective, via-in-pad (VIP) geometries are strongly recommended.

In addition to mounting inductance and resistance associated with placing a capacitor on the PCB, the effectiveness of a decoupling capacitor also depends on the spreading inductance and resistance that the capacitor sees with respect to the load. The spreading inductance and resistance is strongly dependent on the layer assignment in the PCB stack-up. Therefore, try to minimize X, Y and Z dimensions where the Z is due to PCB thickness (as shown in Figure 8-2).

From left (highest inductance) to right (lowest inductance) the capacitor footprint types shown in Figure 8-15 are known as:

- 2-via, Skinny End Exit (2vSEE)
- 2-via, Wide End Exit (2vWEE)
- 2-via, Wide Side Exit (2vWSE)
- 4-via, Wide Side Exit (4vWSE)
- 2-via, In-Pad (2vVIP)



SWPS040-177

Figure 8-15. Capacitor Placement Geometry for Improved Mounting Inductance

NOTE

Evaluation of loop inductance values for decoupling capacitor footprints 2vSEE (worst case) vs 4vWSE (2nd best) has shown a 30% reduction in inductance when 4vWSE footprint was used in place of 2vSEE.

Decoupling Capacitor (Dcap) Strategy:

1. Use lowest inductance footprint and trace connection scheme possible for given PCB technology and layout area in order to minimize Dcap loop inductance to power pin as much as possible (see Figure 8-15).
2. Place Dcaps on “same-side” as component within their power plane outline to minimize “decoupling loop inductance”. Target distance to power pin should be less than ~500mils depending upon PCB layout characteristics (plane's layer assignment and solid nature). Use PI modeling CAD tool to verify

minimum inductance for top vs bottom-side placement.

3. Place Dcaps on “opposite-side” as component within their power plane outline if “same-side” is not feasible or if distance to power pin is greater than ~500mils for top-side location. Use PI modeling CAD tool to verify minimum inductance for top vs bottom-side placement.
4. Use minimum 10mil trace width for all voltage and gnd planes connections (i.e. Dcap pads, component power pins, etc.).
5. Place all voltage and gnd plane vias “as close as possible” to point of use (i.e. Dcap pads, component power pins, etc.).
6. Use a “Power/Gnd pad/pin to via” ratio of 1:1 whenever possible. Do not exceed 2:1 ratio for small number of vias within restricted PCB areas (i.e. underneath BGA components).

Frequency analysis for the MPU power domain has yielded the vdd_mpu Impedance vs Frequency response shown in [Section 8.3.7.2](#), vdd_mpu Example Analysis. As the example shows the overall MPU PDN R_{eff} meets the maximum recommended PDN resistance of 10m Ω .

8.2.5 System ESD Generic Guidelines

8.2.5.1 System ESD Generic PCB Guideline

Protection devices must be placed close to the ESD source which means close to the connector. This allows the device to subtract the energy associated with an ESD strike before it reaches the internal circuitry of the application board.

To help minimize the residual voltage pulse that will be built-up at the protection device due to its nonzero turn-on impedance, it is mandatory to route the ESD device with minimum stub length so that the low-resistive, low-inductive path from the signal to the ground is granted and not increasing the impedance between signal and ground.

For ESD protection array being railed to a power supply when no decoupling capacitor is available in close vicinity, consider using a decoupling capacitor ($\geq 0.1 \mu\text{F}$) tight to the VCC pin of the ESD protection. A positive strike will be partially diverted to this capacitance resulting in a lower residual voltage pulse.

Ensure that there is sufficient metallization for the supply of signals at the interconnect side (VCC and GND in [Figure 8-16](#)) from connector to external protection because the interconnect may see between 15-A to 30-A current in a short period of time during the ESD event.

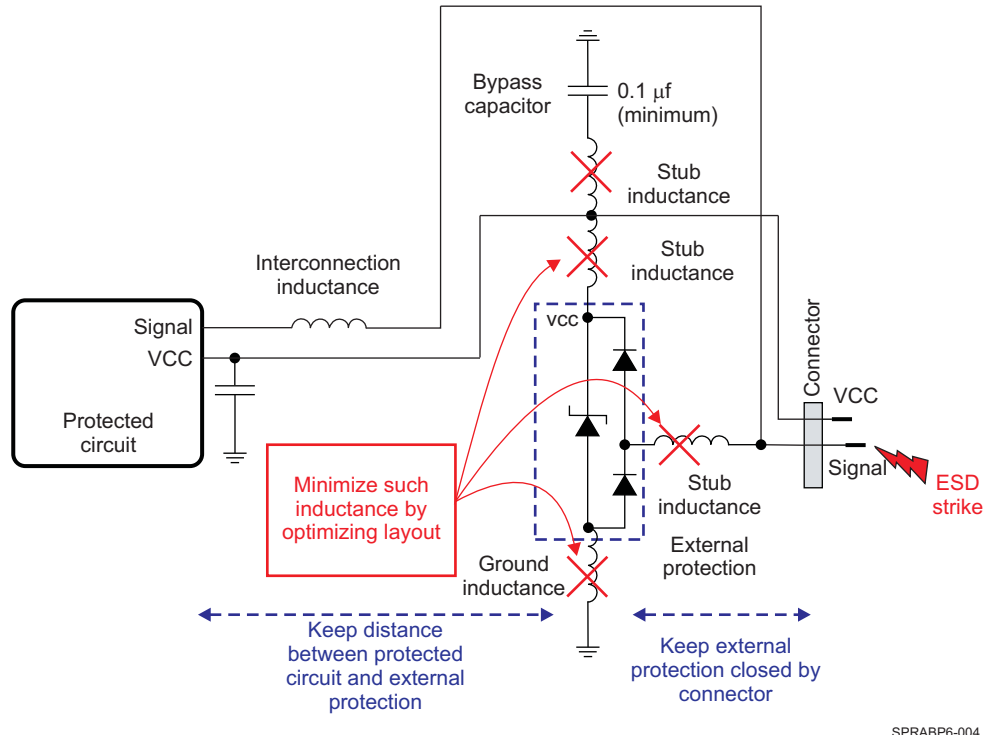


Figure 8-16. Placement Recommendation for an ESD External Protection

NOTE

To ensure normal behavior of the ESD protection (unwanted leakage), it is better to ground the ESD protection to the board ground rather than any local ground (example isolated shield or audio ground).

8.2.5.2 Miscellaneous EMC Guidelines to Mitigate ESD Immunity

- Avoid running critical signal traces (clocks, resets, interrupts, control signals, and so forth) near PCB edges.
- Add high frequency filtering: Decoupling capacitors close to the receivers rather than close to the drivers to minimize ESD coupling.
- Put a ground (guard) ring around the entire periphery of the PCB to act as a lightning rod.
- Connect the guard ring to the PCB ground plane to provide a low impedance path for ESD-coupled current on the ring.
- Fill unused portions of the PCB with ground plane.
- Minimize circuit loops between power and ground by using multilayer PCB with dedicated power and ground planes.
- Shield long line length (strip lines) to minimize radiated ESD.
- Avoid running traces over split ground planes. It is better to use a bridge connecting the two planes in one area.

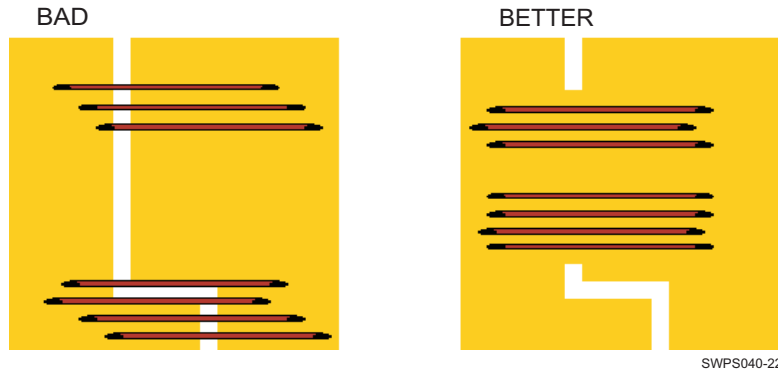


Figure 8-17. Trace Examples

- Always route signal traces and their associated ground returns as close to one another as possible to minimize the loop area enclosed by current flow:
 - At high frequencies current follows the path of least inductance.
 - At low frequencies current flows through the path of least resistance.

8.2.6 EMI / EMC Issues Prevention

All high-speed digital integrated circuits can be sources of unwanted radiation, which can affect nearby sensitive circuitry and cause the final product to have radiated emissions levels above the limits allowed by the EMC regulations if some preventative steps are not taken.

Likewise, analog and digital circuits can be susceptible to interference from the outside world and picked up by the circuitry interconnections.

To minimize the potential for EMI/EMC issues, the following guidelines are recommended to be followed.

8.2.6.1 Signal Bandwidth

To evaluate the frequency of a digital signal, an estimated rule of thumb is to consider its bandwidth f_{BW} with respect to its rise time, t_R :

$$f_{BW} \approx 0.35 / t_R$$

This frequency actually corresponds to the break point in the signal spectrum, where the harmonics start to decay at 40 dB per decade instead of 20 dB per decade.

8.2.6.2 Signal Routing

8.2.6.2.1 Signal Routing—Sensitive Signals and Shielding

Keep radio frequency (RF) sensitive circuitry (like GPS receivers, GSM/WCDMA, Bluetooth/WLAN transceivers, frequency modulation (FM) radio) away from high-speed ICs (the device, power and audio manager, chargers, memories, and so forth) and ideally on the opposite side of the PCB. For improved protection it is recommended to place these emission sources in a shield can. If the shield can have a removable lid (two-piece shield), ensure there is low contact impedance between the fence and the lid. Leave some space between the lid and the components under it to limit the high-frequency currents induced in the lid. Limit the shield size to put any potential shield resonances above the frequencies of interest; see [Figure 8-14, Typical Impedance Profile of a Capacitor](#).

8.2.6.2.2 Signal Routing—Outer Layer Routing

In case there is a need to use the outer layers for routing outside of shielded areas, it is recommended to route only static signals and ensure that these static signals do not carry any high-frequency components (due to parasitic coupling with other signals). In case of long traces, make provision for a bypass capacitor near the signal source.

Routing of high-frequency clock signals on outer layers, even for a short distance, is discouraged, because their emissions energy is concentrated at the discrete harmonics and can become significant even with poor radiators.

Coplanar shielding of traces on outer layers (placing ground near the sides of a track along its length) is effective only if the distance between the trace sides and the ground is smaller than the trace height above the ground reference plane. For modern multilayer PCBs this is often not possible, so coplanar shielding will not be effective. Do not route high-frequency traces near the periphery of the PCB, as the lack of a ground reference near the trace edges can increase EMI: see [Section 8.2.6.3, Ground Guidelines](#).

8.2.6.3 Ground Guidelines

8.2.6.3.1 PCB Outer Layers

Ideally the areas on the top and bottom layers of the PCB that are not enclosed by a shield should be filled with ground after the routing is completed and connected with an adequate number of vias to the ground on the inner ground planes.

8.2.6.3.2 Metallic Frames

Ensure that all metallic parts are well connected to the PCB ground (like LCD screens metallic frames, antennas reference planes, connector cages, flex cables grounds, and so forth). If using flex PCB ribbon cables to bring high-frequency signals off the PCB, ensure they are adequately shielded (coaxial cables or flex ribbons with a solid reference ground).

8.2.6.3.3 Connectors

For high-frequency signals going to connectors choose a fully shielded connector, if possible (for example, SD card connectors). For signals going to external connectors or which are routed over long distances, it is recommended to reduce their bandwidth by using low-pass filters (resistor, capacitor (RC) combinations or lossy ferrite inductors). These filters will help to prevent emissions from the board and can also improve the immunity from external disturbances.

8.2.6.3.4 Guard Ring on PCB Edges

The major advantage of a multilayer PCB with ground-plane is the ground return path below each and every signal or power trace.

As shown in [Figure 8-18](#) the field lines of the signal return to PCB ground as long as an infinite ground is available.

Traces near the PCB-edges do not have this infinite ground and therefore may radiate more than the others. Thus, signals (clocks) or power traces (core power) identified to be critical must not be routed in the vicinity of PCB edges, or, if not avoidable, must be accompanied by a guard ring on the PCB edge.

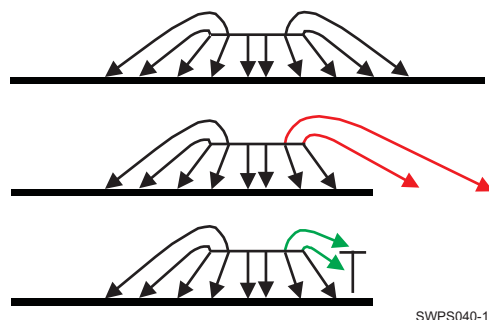


Figure 8-18. Field Lines of a Signal Above Ground



Figure 8-19. Guard Ring Routing

The intention of the guard ring is that HF-energy, that otherwise would have been emitted from the PCB edge, is reflected back into the board where it partially will be absorbed. For this purpose ground traces on the borders of all layers (including power layer) must be applied as shown in [Figure 8-19](#).

As these traces must have the same (HF-) potential as the ground plane they must be connected to the ground plane at least every 10 mm.

8.2.6.3.5 Analog and Digital Ground

For the optimum solution, the AGND and the DGND planes must be connected together at the power supply source in a same point. This ensures that both planes are at the same potential, while the transfer of noise from the digital to the analog domain is minimized.

8.3 Core Power Domains

This section provides boundary conditions and theoretical background to be applied as a guide for optimizing a PCB design. The decoupling capacitor and PDN characteristics tables shown below give recommended capacitors and PCB parameters to be followed for schematic and PCB designs. Board designs that meet the static and dynamic PDN characteristics shown in tables below will be aligned to the expected PDN performance needed to optimize SoC performance.

8.3.1 General Constraints and Theory

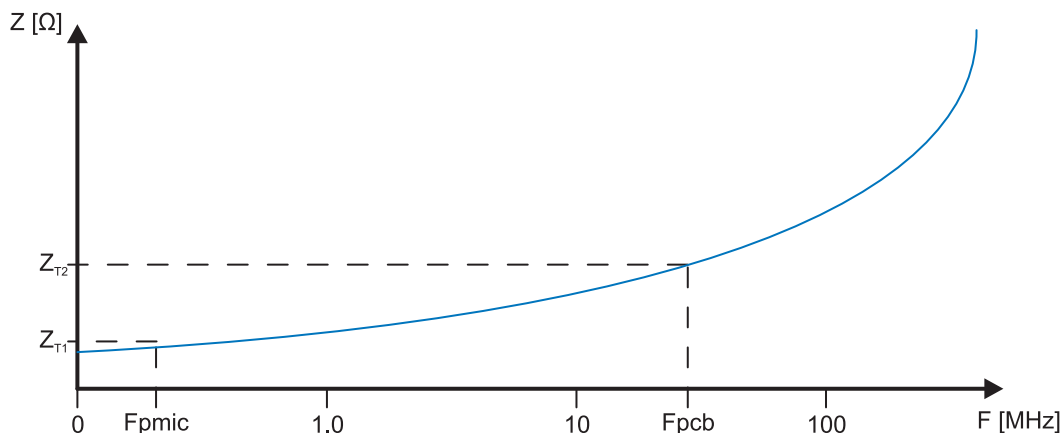
- Max PCB static/DC voltage drop (IRd) budget of **1.5% of supply voltage** when using PMICs **without remote sensing** as measured from PMIC's power inductor and filter capacitor node to Processor input including any ground return losses.
- Max PCB static/DC voltage drop (IRd) budget can be relaxed to **5% of supply voltage** when using PMICs **with remote sensing at the load** as measured from PMIC's power inductor and filter capacitor node to Device's supply input including any ground return losses.
- PMIC component DM and guidelines should be referenced for the following:
 - Routing remote feedback sensing to optimize per each SMPS's implementation
 - Selecting power filtering capacitor values and PCB placement.
- Max Effective Resistance (R_{eff}) budget can range from **4 – 50mΩ** for key Device power rails not including ground returns depending upon maximum load currents and maximum DC voltage drop budget (as discussed above).
- Max Device supply input voltage difference budget of **5mV** under max current loading shall be maintained across all balls connected to a common power rail. This represents any voltage difference that may exist between a remote sense point to any power input.
- Max PCB Loop Inductance (LL) budget between Device's power inputs and local bulk and high frequency decoupling capacitors including ground returns should range from **0.4 – 2.5nH depending upon maximum transient load currents**.
- Max PCB dynamic/AC peak-to-peak transient noise voltage budgets between PMIC and Device including ground returns are as follows:
 - **+/-3% of nominal supply voltage** for frequencies below the PMIC bandwidth (typ F_{pmic} ~ 200kHz)
 - **+/-5% of nominal supply voltage** for frequencies between F_{pmic} to F_{pcb} (typ 20 – 100MHz)

- Max PCB Impedance (Z) vs Frequency (F) budget between Device's power inputs and PMIC's output power filter node including ground return is determined by applying the Frequency Domain Target Impedance Method to determine the PCB's maximum frequency of interest (Fpcb). Ideally a properly designed and decoupled PDN will exhibit smoothly increasing Z vs. F curve. There are 2 general regions of interest as can be seen in [Figure 8-20](#).
 - 1st area is from DC (0Hz) up to Fpmic (typ a few 100 kHz) where a PMIC's transient response characteristic (i.e. Switching Freq, Compensation Loop BW) dominate. A PDN's Z is typically very low due to power filtering & bulk capacitor values when PDN has very low trace resistance (i.e. good Reff performance). The goal is to maintain a smoothly increasing Z that is less than Zt1 over this low frequency range. This will ensure that a max transient current event will not cause a voltage drop more than the PMIC's current step response can support (typ 3%).
 - 2nd area is from Fpmic up to Fpcb (typ 20-100MHz) where a PCB's inherent characteristics (i.e. parasitic capacitance, planar spreading inductances) dominate. A PDN's Z will naturally increase with frequency. At frequencies between Fpmic up to Fpcb, the goal is to maintain a smoothly increasing Z to be less than Zt2. This will ensure that the high frequency content of a max transient current event will not cause a voltage drop to be more than 5% of the min supply voltage.

$$Z_T = \frac{\text{Max Voltage Rail Drop}^{\text{Note1}}}{\text{Max Transient Current}^{\text{Note2}}}$$

$$Z_{T1} = \frac{(\text{Min Voltage}) \times (\text{PMIC's Step Responce})}{(\sim 50\% \text{ of Max DC Current})} = \frac{V_{\text{min}} \times 3\%(\text{typ})}{I_{\text{max}} \times \sim 50\%}$$

$$Z_{T2} = \frac{(\text{Min Voltage}) \times (\text{High-Freq Transient Noise})}{(\sim 50\% \text{ of Max DC Current})} = \frac{V_{\text{min}} \times 5\%(\text{typ})}{I_{\text{max}} \times \sim 50\%}$$



PCB_CPD_8

Figure 8-20. PDN's Target impedance

1.Voltage Rail Drop includes regulation accuracy, voltage distribution drops, and all dynamic events such as transient noise, AC ripple, voltage dips etc.

2. Typical max transient current is defined as 50% of max current draw possible.

8.3.2 Voltage Decoupling

Recommended power supply decoupling capacitors main characteristics for commercial products whose ambient temperature is not to exceed +85C are shown in table below:

Table 8-1. Commercial Applications Recommended Decoupling Capacitors Characteristics⁽¹⁾⁽²⁾⁽³⁾

Value	Voltage [V]	Package	Stability	Dielectric	Capacitance Tolerance	Temp Range [°C]	Temp Sensitivity [%]	REFERENCE
22μF	6,3	0603	Class 2	X5R	- / + 20%	-55 to + 85	- / + 15	GRM188R60J226MEA0L
10μF	4,0	0402	Class 2	X5R	- / + 20%	-55 to + 85	- / + 15	GRM155R60G106ME44
4.7μF	6,3	0402	Class 2	X5R	- / + 20%	-55 to + 85	- / + 15	GRM155R60J475ME95
2.2μF	6,3	0402	Class 2	X5R	- / + 20%	-55 to + 85	- / + 15	GRM155R60J225ME95
1μF	6,3	0201	Class 2	X5R	- / + 20%	-55 to + 85	- / + 15	GRM033R60J105MEA2
470nF	6,3	0201	Class 2	X5R	- / + 20%	-55 to + 85	- / + 15	GRM033R60G474ME90
220nF	6,3	0201	Class 2	X5R	- / + 20%	-55 to + 85	- / + 15	GRM033R60J224ME90
100nF	6,3	0201	Class 2	X5R	- / + 20%	-55 to + 85	- / + 15	GRM033R60J104ME19

(1) Minimum value for each PCB capacitor: 100 nF.

(2) Among the different capacitors, 470 nF is recommended (not required) to filter at 5-MHz to 10-MHz frequency range.

(3) In comparison with the EIA Class 1 dielectrics, Class 2 dielectric capacitors tend to have severe temperature drift, high dependence of capacitance on applied voltage, high voltage coefficient of dissipation factor, high frequency coefficient of dissipation, and problems with aging due to gradual change of crystal structure. Aging causes gradual exponential loss of capacitance and decrease of dissipation factor.

Recommended power supply decoupling capacitors main characteristics for automotive products are shown in table below:

Table 8-2. Automotive Applications Recommended Decoupling Capacitors Characteristics⁽¹⁾⁽²⁾

Value	Voltage [V]	Package	Stability	Dielectric	Capacitance Tolerance	Temp Range [°C]	Temp Sensitivity [%]	REFERENCE
22μF	6,3	1206	Class 2	X7R	- / + 20%	-55 to + 125	- / + 15	GCM31CR70J226ME23
10μF	6,3	0805	Class 2	X7R	- / + 20%	-55 to + 125	- / + 15	GCM21BR70J106ME22
4.7μF	10	0805	Class 2	X7R	- / + 20%	-55 to + 125	- / + 15	GCM21BC71A475MA73
2.2μF	6,3	0603	Class 2	X7R	- / + 20%	-55 to + 125	- / + 15	GCM188R70J225ME22
1μF	16	0603	Class 2	X7R	- / + 20%	-55 to + 125	- / + 15	GCM188R71C105MA64
470nF	16	0603	Class 2	X7R	- / + 20%	-55 to + 125	- / + 15	GCM188R71C474MA55
220nF	25	0603	Class 2	X7R	- / + 20%	-55 to + 125	- / + 15	GCM188L81C224MA37
100nF	16	0402	Class 2	X7R	- / + 20%	-55 to + 125	- / + 15	GCM155R71C104MA55

(1) Minimum value for each PCB capacitor: 100 nF.

(2) Among the different capacitors, 470 nF is recommended (not required) to filter at 5-MHz to 10-MHz frequency range.

8.3.3 Static PDN Analysis

One power net parameter derived from a PCB's PDN static analysis is the Effective Resistance (R_{eff}). This is the total PCB power net routing resistance that is the sum of all the individual power net segments used to deliver a supply voltage to the point of load and includes any series resistive elements (i.e. current sensing resistor) that may be installed between the PMIC outputs and Processor inputs

8.3.4 Dynamic PDN Analysis

Three power net parameters derived from a PCB's PDN dynamic analysis are the Loop Inductance (LL), Impedance (Z) and PCB Frequency of Interest (F_{pcb}).

- LL values shown are the recommended max PCB trace inductance between a decoupling capacitor's power supply and ground reference terminals when viewed from the decoupling capacitor with a "theoretical shorted" applied across the Processor's supply inputs to ground reference.
- Z values shown are the recommended max PCB trace impedances allowed between Fpmic up to Fpcb frequency range that limits transient noise drops to no more than 5% of min supply voltage during max transient current events.
- Fpcb (Frequency of Interest) is defined to be a power rail's max frequency after which adding a reasonable number of decoupling capacitors no longer significantly reduces the power rail impedance below the desired impedance target (Zt2). This is due to the dominance of the PCB's parasitic planar spreading and internal package inductances.

Table 8-3. Recommended PDN and Decoupling Characteristics ⁽¹⁾⁽²⁾⁽³⁾⁽⁴⁾⁽⁵⁾

PDN Analysis: Supply	Static Max R _{eff} ⁽⁷⁾ [mΩ]	Dynamic			Number of Recommended Decoupling Capacitors per Supply							
		Dec. Cap. Max LL ⁽⁸⁾⁽⁶⁾ [nH]	Impedance [mΩ]	Frequency of Interest [MHz]	100 nF ⁽⁶⁾	220 nF	470 nF	1 μF	2.2 μF	4.7 μF	10 μF	22 μF
vdd_mpu	10	2	57	20	12	2	2	3	1	1		1
vdd_dspeve	13	2.5	54	20	8	1	1	2	1	1	1	
vdd	27	2	87	50	6	1	1	1	1	1		
vdd_gpu	18	2.5	207	50	6	1	1	1	1	1		
vdd_iva	48	2	800	100	5		1			1		
vdds_ddr1	10	2.5	200	100	8	4		2		2		1
cap_vbldo_dspeve	N/A	6	N/A	N/A				1				
cap_vbldo_gpu	N/A	6	N/A	N/A				1				
cap_vbldo_iva	N/A	6	N/A	N/A				1				
cap_vbldo_mpu	N/A	6	N/A	N/A				1				
cap_vddram_core1	N/A	6	N/A	N/A				1				
cap_vddram_core2	N/A	6	N/A	N/A				1				
cap_vddram_core3	N/A	6	N/A	N/A				1				
cap_vddram_core4	N/A	6	N/A	N/A				1				
cap_vddram_core5	N/A	6	N/A	N/A				1				
cap_vddram_dspeve1	N/A	6	N/A	N/A				1				
cap_vddram_dspeve2	N/A	6	N/A	N/A				1				
cap_vddram_gpu	N/A	6	N/A	N/A				1				
cap_vddram_iva	N/A	6	N/A	N/A				1				
cap_vddram_mpu1	N/A	6	N/A	N/A				1				
cap_vddram_mpu2	N/A	6	N/A	N/A				1				

(1) For more information on peak-to-peak noise values, see the Recommended Operating Conditions table of the Specifications chapter.

(2) ESL must be as low as possible and must not exceed 0.5 nH.

(3) The PDN (Power Delivery Network) impedance characteristics are defined versus the device activity (that runs at different frequency) based on the Recommended Operating Conditions table of the Specifications chapter.

(4) The static drop requirement drives the maximum acceptable PCB resistance between the PMIC or the external SMPS and the processor power balls.

(5) Assuming that the external SMPS (power IC) feedback sense is taken close to processor power balls.

(6) High-frequency (30 to 70MHz) PCB decoupling capacitors

(7) Maximum R_{eff} from SMPS to Processor.

(8) Maximum Loop Inductance for decoupling capacitor.

NOTE

For power IC which can support more than 10uF close to processor, a bulk capacitor of at least 22uF is strongly recommended for VDD_MPU power domains.

8.3.5 Power Supply Mapping

TPS65917 or TPS659039 are the Power Management ICs (PMICs) that should be used for the Device designs. TI requires use of these PMICs for the following reasons:

- TI has validated their use with the Device
- Board level margins including transient response and output accuracy are analyzed and optimized for the entire system
- Support for power sequencing requirements (refer to [Section 5.9 Power Supply Sequences](#))
- Support for Adaptive Voltage Scaling (AVS) Class 0 requirements, including TI provided software

Whenever we allow for combining of rails mapped on any of the SMPSes, the PDN guidelines that are the most stringent of the rails combined should be implemented for the particular supply rail.

It is possible that some voltage domains on the device are unused in some systems. In such cases, to ensure device reliability, it is still required that the supply pins for the specific voltage domains are connected to some core power supply output.

These unused supplies though can be combined with any of the core supplies that are used (active) in the system. e.g. if IVA and GPU domains are not used, they can be combined with the CORE domain, thereby having a single power supply driving the combined CORE, IVA and GPU domains.

For the combined rail, the following relaxations do apply:

- The AVS voltage of active rail in the combined rail needs to be used to set the power supply
- The decoupling capacitance should be set according to the active rail in the combined rail

[Table 8-4](#) illustrates the approved and validated power supply connections to the Device for the SMPS outputs of the TPS659039 PMIC.

Table 8-4. TPS659039 Power Supply Connections

SMPS	Valid Combination 1: Reference Platform	Valid Combination 2: MPU Centric	Valid Combination 3: DSPEVE Centric ⁽³⁾	Valid Combination 4: IVA Centric	TPS659039 Current Rating Limitation ⁽⁴⁾ ⁽⁵⁾
SMPS1/2/3 ⁽²⁾	vdd_mpu	vdd_mpu	vdd_mpu, vdd_gpu, vdd_iva	vdd_mpu	SMPS1/2: 6A SMPS1/2/3: 9A
SMPS3 ⁽²⁾	vdds_dds1	vdds_dds1	vdds_dds1	vdds_dds1	SMPS3: 3A
SMPS4/5	vdd_dspeve	vdd_dspeve, vdd_gpu, vdd_iva	vdd_dspeve	vdd_dspeve, vdd_gpu	SMPS4/5: 4A
SMPS6	vdd_gpu	vdd	vdd	vdd	SMPS6: 2-3A (BOOST_CURRENT =0/1)
SMPS7	vdd	Free	Free	Free	2A
SMPS8	vdd_iva	Free	Free	vdd_iva	1A
SMPS9	vdds18v	vdds18v	vdds18v	vdds18v	1A

- (1) Power consumption is highly application-specific. Separate analysis must be performed to ensure output current ratings (average and peak) is within the limits of the PMIC for all rails of the device.
- (2) Dual phase (SMPS1/2) can be used as long as the peak power consumption is maintained below the SMPS1/2 capacity
- For the latest rated output current specifications for the TPS659039 device, please refer to the PMIC data manual.
 - MPU power consumption is highly system dependent. A detailed power consumption estimate must be performed to confirm compatibility. Example: Single vs Dual MPU, OPP_NOM vs OPP_OD vs OPP_HIGH, TPS659039 configured with $V_I \geq 3V$ vs $V_I < 3V$, etc. Contact your TI representative for details.
- (3) Combination 3 must only be used in systems where the MPU frequency is 1 GHz or lower. If greater than 1 GHz MPU is required, then the vdd_mpu domain must be powered independently.

- (4) Refer to the PMIC data manual for the latest TPS659039 specifications.
- (5) A product's maximum ambient temperature, thermal system design & heat spreading performance could limit the maximum power dissipation below the full PMIC capacity in order to not exceed recommended SoC max Tj.

[Table 8-5](#) illustrates the approved and validated power supply connections to the Device for the SMPS outputs of the TPS65917 PMIC.

Table 8-5. TPS65917 Power Supply Connections

TPS65917	Valid Combination 1:	Valid Combination 2	TPS65917 Current Rating Limitation ^{(1) (3)}
SMPS1	vdd_mpu	vdd_mpu	SMPS1: $3.5A \leq OPP_NOM$ (dual or single) OR $\leq OPP_OD$ (single ONLY)
SMPS2 ⁽²⁾	vdd_dspeve, vdd_gpu, vdd_iva	vdd	3.5A
SMPS3 ⁽²⁾	vdd	vdd_dspeve, vdd_gpu, vdd_iva	3A
SMPS4 ⁽³⁾	vdds18v	vdds18v	1.5A
SMPS5 ⁽⁴⁾	vdds_ddr1	vdds_ddr1	2A

- (1) Refer to the TPS65917 Data Manual for exact current rating limitations, including assumed V_{IN} and other parameters. Values provided in this table are for comparison purposes.
- (2) DSP, EVE, GPU, and IVAHD power consumption is highly application-specific. Separate analysis must be performed to ensure output current ratings (average and peak) is within the limits of the PMIC. VDD only supports OPP_NOM.
- (3) Highly application-specific. Separate analysis must be performed to ensure average and peak power is within the limits of the PMIC.
- (4) Furthermore, if SMPS5 is used for DDR power, both total memory + SoC power must be within the PMIC limits.

8.3.6 DPLL Voltage Requirement

The voltage input to the DPLLs has a low noise requirement. Board designs should supply these voltage inputs with a low noise LDO to ensure they are isolated from any potential digital switching noise. The TPS65917 and TPS659039 PMIC LDOLN outputs are specifically designed to meet this low noise requirement.

NOTE

For more information about Input Voltage Sources, see [Section 6.3 DPLLs, DLLs Specifications](#).

[Table 8-4](#) present the voltage inputs that supply the DPLLs.

Table 8-6. Input Voltage Power Supplies for the DPLLs

POWER SUPPLY	DPLLs
vdda_abe_per	DPLL_PER, DPLL_ABE and PER HSDIVIDER analog power supply
vdda_ddr	DPLL_DDR and DDR HSDIVIDER analog power supply
vdda_debug	DPLL_DEBUG analog power supply
vdda_dsp_eve	DPLL_DSP and DPLL_EVE analog power supply
vdda_gmac_core	DPLL_CORE and HSDIVIDER analog power supply
vdda_gpu	DPLL_GPU analog power supply
vdda_iva	DPLL_IVA analog power supply
vdda_video	DPLL_VIDEO1 and DPLL_VIDEO2 analog power supply
vdda_mpu	DPLL_MPU analog power supply
vdda_osc	not DPLL input but is required to be supplied by low noise input voltage

8.3.7 Example PCB Design

The following sections describe an example PCB design and its resulting PDN performance for the vdd_mpu key processor power domain.

8.3.7.1 Example Stack-up

Layer Assignments:

- Layer Top: Signal and Segmented Power Plane
 - Processor and PMIC components placed on Top-side
- Layer 2: Gnd Plane1
- Layer 3: Signals
- Layer n: Power Plane1
- Layer n+1: Power Plane 2
- Layer n+2: Signal
- Layer n+3: Gnd Plane2
- Layer Bottom: Signal and Segmented Power Planes
 - Decoupling caps, etc.

Via Technology: Through-hole

Copper Weight:

- ½ oz for all signal layers.
- 1-2oz for all power plane for improved PCB heat spreading.
- Total PCB Thickness 0.080inches.

8.3.7.2 vdd_mpu Example Analysis

Maximum acceptable PCB resistance (R_{eff}) between the PMIC and Processor input power balls should not exceed 10m Ω .

Maximum decoupling capacitance loop inductance (LL) between Processor input power balls and decoupling capacitances should not exceed 2.0nH (ESL NOT included)

Impedance target for key frequency of interest between Processor input power balls and PMIC's SMPS output power balls should not exceed 57m Ω at 20MHz.

Table 8-7. Example PCB vdd_mpu PI Analysis Summary

Parameter	Recommendation	Example PCB
Processor OPP	High	
Clocking Rate	1.5 GHz	
Voltage Level	1.22V	1.22V
Max Current Draw	5.12 A	5.12 A
Max Effective Resistance: Power Inductor Segment Total R_{eff}	10m Ω	9.0m Ω
Max Loop Inductance	2.0nH	1.0 – 1.4nH
Impedance Target	57m Ω F<20Mhz	57m Ω F<20Mhz

Figure 8-21, Figure 8-22, Figure 8-23, and Figure 8-24 show a PCB layout example and the resulting PI analysis results.

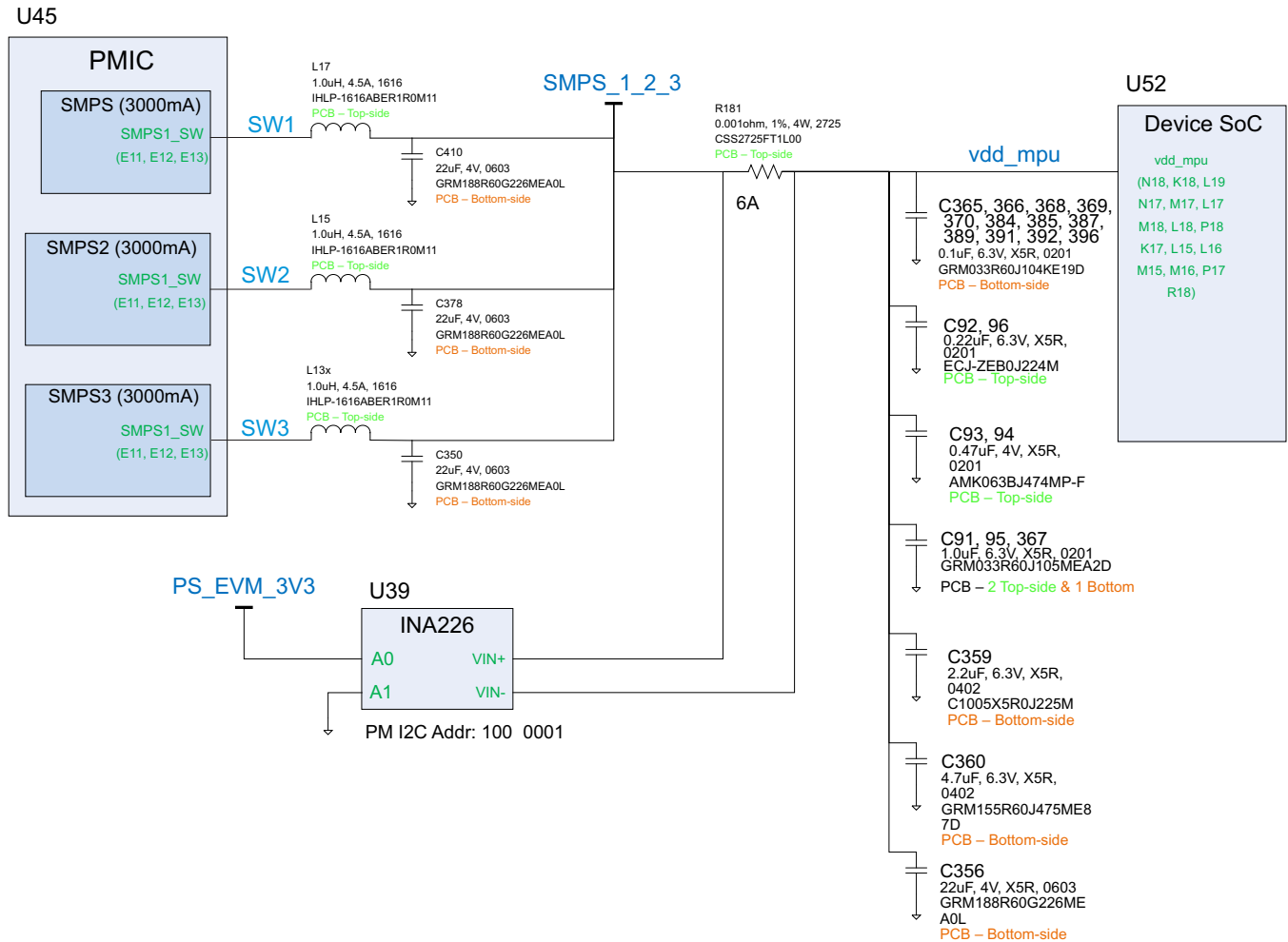


Figure 8-21. vdd_mpu Simplified SCH Diagram

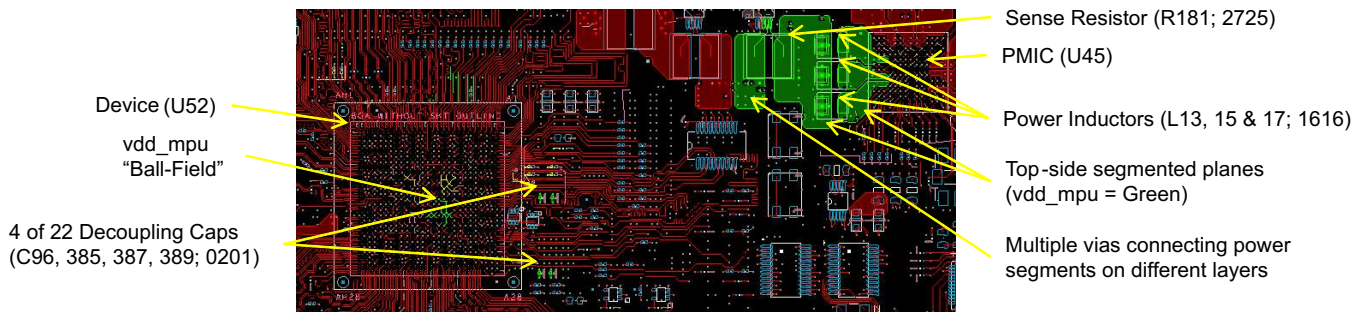


Figure 8-22. vdd_mpu routing [Top Layer]

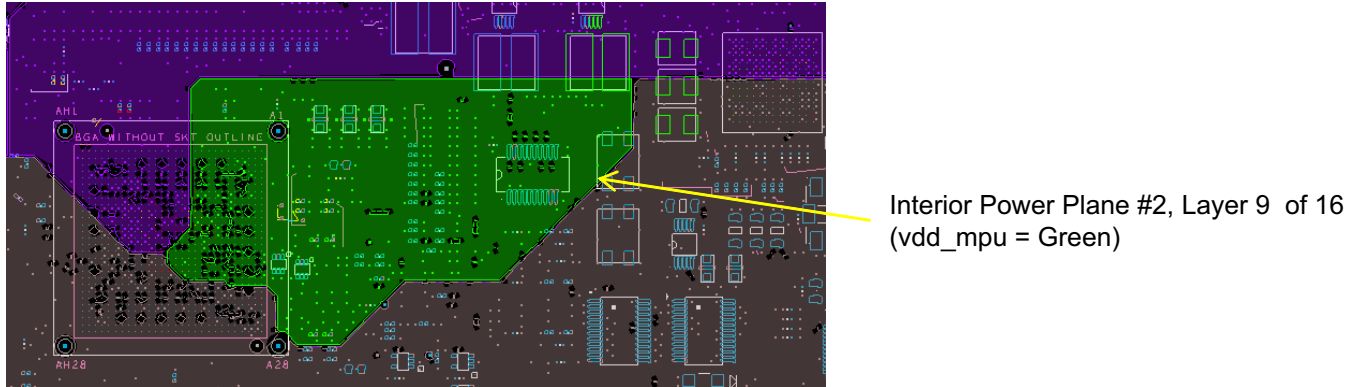


Figure 8-23. vdd_mpu routing [Internal Power Plane #2]

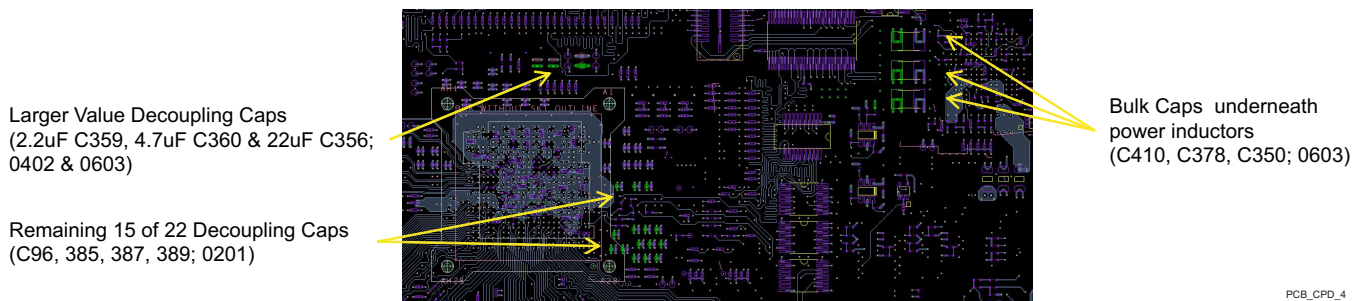


Figure 8-24. vdd_mpu routing and cap placements [Bottom Layer]

Table 8-8. PCB Etch Resistance Breakdown - From PMIC Source to Device Load

Net[from]	Component [from]:	Net[to]	Component [to]:	Etch Resistance (Ω)	% of Total Etch Resistance
SW1	L17	SW1	U45	0,001038	13%
SW2	L15	SW2	U45	0,000898	12%
SW3	L13	SW3	U45	0,000861	11%
SW1	L17	SMPS_1_2_3	R181	0,000696	9%
SW2	L15	SMPS_1_2_3	R181	0,000541	7%
SW3	L13	SMPS_1_2_3	R181	0,000526	7%
vdd_mpu	R181	vdd_mpu	U52	0,006311	78%
vdd_mpu	R181	vdd_mpu	U52	0,006311	81%
vdd_mpu	R181	vdd_mpu	U52	0,006311	82%
Total Etch Resistance from SW1 =				0,008045	100%
Total Etch Resistance from SW2 =				0,00775	100%
Total Etch Resistance from SW3 =				0,007698	100%
Max Value =				0,008045	

Table 8-9. PCB Etch Resistance Breakdown - From Power Inductor to Device Load

Net[from]	Component [from]:	Net[to]	Component [to]:	Etch Resistance (Ω)	% of Total Etch Resistance
SMPS_1_2_3	L17	SMPS_1_2_3	R181	0,000696	10%
SMPS_1_2_3	L15	SMPS_1_2_3	R181	0,000541	8%
SMPS_1_2_3	L13	SMPS_1_2_3	R181	0,000526	8%

Table 8-9. PCB Etch Resistance Breakdown - From Power Inductor to Device Load (continued)

Net[from]	Component [from]:	Net[to]	Component [to]:	Etch Resistance (Ω)	% of Total Etch Resistance
vdd_mpu	R181	vdd_mpu	U52	0,006311	90%
vdd_mpu	R181	vdd_mpu	U52	0,006311	92%
vdd_mpu	R181	vdd_mpu	U52	0,006311	92%
Total Etch Resistance =				0,007007	100%
Total Etch Resistance =				0,006852	100%
Total Etch Resistance =				0,006837	100%
Max Value =				0,007007	

Table 8-10. PDN Effective Resistance - From PMIC Source to Device Load

PDN Elements	PDN Effective Resistance (Ω)	% of Total Etch Resistance
Etch	0,008045	89%
Inductor	0	0%
Sense Resistor	0,001	11%
Max PDN Effectiv Resistance from Source	0,009045	100%

IR Drop: vdd_mpu (PCB RevJan14, Sentinel PSI)

- Source Conditions: 1.22V @ 5,12A
- Recommended $R_{eff} < 10m\Omega$
- $R_{eff} = \text{Total Trace Resistance} + \text{Sence Resistor} = 8,04m\Omega + 1m\Omega = 9,04m\Omega$
- Voltage / IR Drop: 1,22 - 1,179 = 52,6 mV

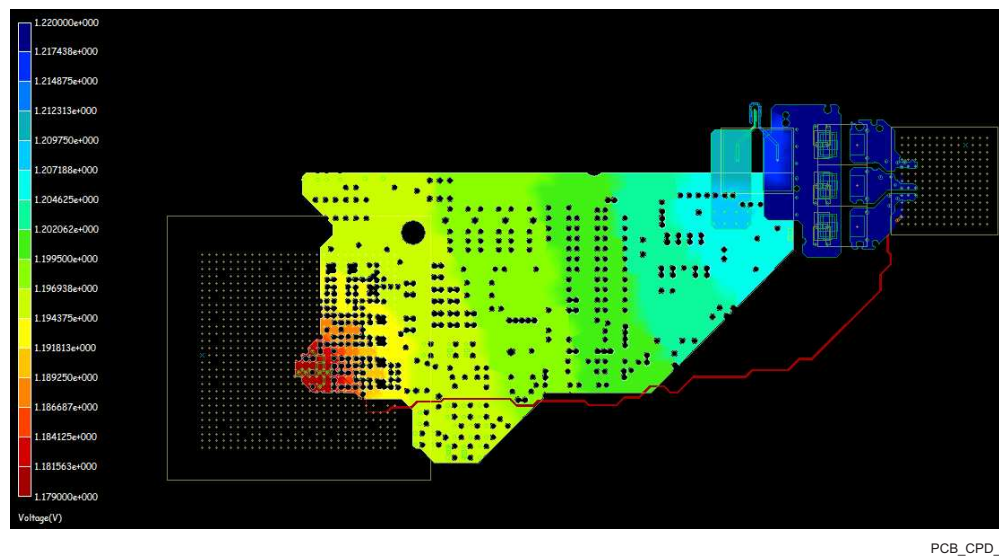


Figure 8-25. vdd_mpu Voltage/IR Drop [All Layers]

Dynamic analysis of this PCB design for the MPU power domain determined the vdd_mpu decoupling capacitor loop inductance and impedance vs frequency analysis shown below. As you can see, the loop inductance values ranged from 1.0 to 1.4nH and were less than maximum 2.0nH recommended.

NOTE

Comparing loop inductances for capacitors at different distances from the processor's input power balls shows an 18% reduction for caps placed closer. This was derived by averaging the inductances for the 3 caps with distances over 800mils (Avg LL = 1.33nH) vs the 3 caps with distances less than 600mils (Avg LL = 1.096nH).

Table 8-11. Rail - vdd_mpu

Cap Ref Des	Model Port #	Loop Inductance [nH]	Footprint Types	PCB Side	Distance to Ball-Field [mils]	Value [μ F]	Size
C356	1	1,4	4vWSE	Bottom	897	22	0603
C359	2	1,26	4vWSE	Bottom	855	2,2	0402
C360	3	1,33	4vWSE	Bottom	850	4,7	0402
C365	4	1,14	4vWSE	Bottom	817	0,1	0201
C366	5	1,13	4vWSE	Bottom	755	0,1	0201
C367	6	1,07	4vWSE	Bottom	758	1	0201
C368	7	1,12	4vWSE	Bottom	811	0,1	0201
C369	8	1,06	4vWSE	Bottom	690	0,1	0201
C370	9	1,12	4vWSE	Bottom	680	0,1	0201
C384	10	1,04	4vWSE	Bottom	686	0,1	0201
C385	11	1,07	4vWSE	Top	686	0,1	0201
C387	12	1,16	4vWSE	Top	755	0,1	0201
C389	13	1,18	4vWSE	Top	693	0,1	0201
C391	14	1,14	4vWSE	Bottom	693	0,1	0201
C392	15	1,18	4vWSE	Bottom	542	0,1	0201
C396	16	1,11	4vWSE	Bottom	745	0,1	0201
C91	17	1,1	4vWSE	Bottom	515	1	0201
C92	18	1,09	4vWSE	Bottom	622	0,22	0201
C93	19	1,01	4vWSE	Bottom	504	0,47	0201
C94	20	1,13	4vWSE	Bottom	604	0,47	0201
C95	21	1,04	4vWSE	Bottom	612	1	0201
C96	22	1,08	4vWSE	Top	612	0,22	0201

Loop Inductance range: 1,01 - 1,40 nH



Figure 8-26. vdd_mpu Decoupling Cap Loop Inductances

Figure 8-27 shows vdd_mpu Impedance vs Frequency characteristics.

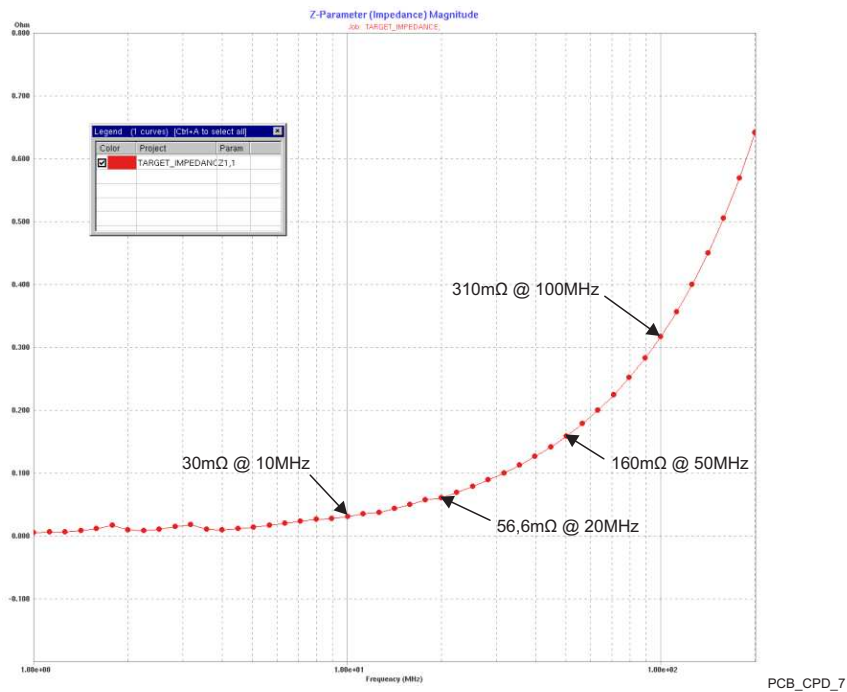


Figure 8-27. vdd_mpu Impedance vs Frequency

8.4 Single-Ended Interfaces

8.4.1 General Routing Guidelines

The following paragraphs detail the routing guidelines that must be observed when routing the various functional LVCMOS interfaces.

- Line spacing:
 - For a line width equal to W , the spacing between two lines must be $2W$, at least. This minimizes the crosstalk between switching signals between the different lines. On the PCB, this is not achievable everywhere (for example, when breaking signals out from the device package), but it is recommended to follow this rule as much as possible. When violating this guideline, minimize the length of the traces running parallel to each other (see [Figure 8-28](#)).

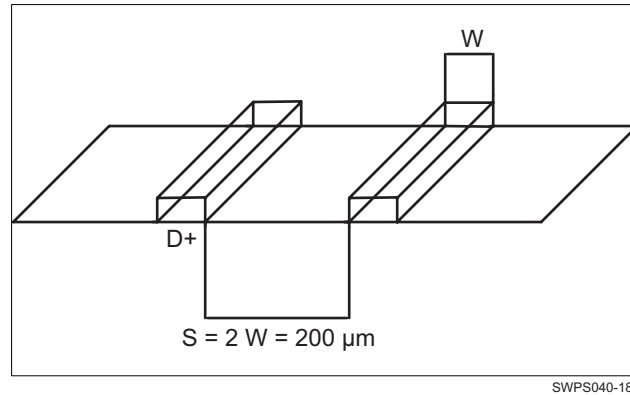


Figure 8-28. Ground Guard Illustration

- Length matching (unless otherwise specified):
 - For bus or traces at frequencies less than 10 MHz, the trace length matching (maximum length difference between the longest and the shortest lines) must be less than 25 mm.
 - For bus or traces at frequencies greater than 10 MHz, the trace length matching (maximum length difference between the longest and the shortest lines) must be less than 2.5 mm.
- Characteristic impedance
 - Unless otherwise specified, the characteristic impedance for single-ended interfaces is recommended to be between 35- Ω and 65- Ω .
- Multiple peripheral support
 - For interfaces where multiple peripherals have to be supported in the star topology, the length of each branch has to be balanced. Before closing the PCB design, it is highly recommended to verify signal integrity based on simulations including actual PCB extraction.

8.4.2 QSPI Board Design and Layout Guidelines

The following section details the routing guidelines that must be observed when routing the QSPI interfaces.

- The `qspi1_sclk` output signal must be looped back into the `qspi1_rtclk` input.
- The signal propagation delay from the `qspi1_sclk` ball to the QSPI device CLK input pin (A to C) must be approximately equal to the signal propagation delay from the QSPI device CLK pin to the `qspi1_rtclk` ball (C to D).
- The signal propagation delay from the QSPI device CLK pin to the `qspi1_rtclk` ball (C to D) must be approximately equal to the signal propagation delay of the control and data signals between the QSPI device and the SoC device (E to F, or F to E).
- The signal propagation delay from the `qspi1_sclk` signal to the series terminators ($R2 = 10 \Omega$) near the QSPI device must be $< 450\text{pS}$ ($\sim 7\text{cm}$ as stripline or $\sim 8\text{cm}$ as microstrip)
- 50 Ω PCB routing is recommended along with series terminations, as shown in [Figure 8-29](#).

- Propagation delays and matching:
 - A to C = C to D = E to F.
 - Matching skew: < 60pS
 - A to B < 450pS
 - B to C = as small as possible (<60pS)

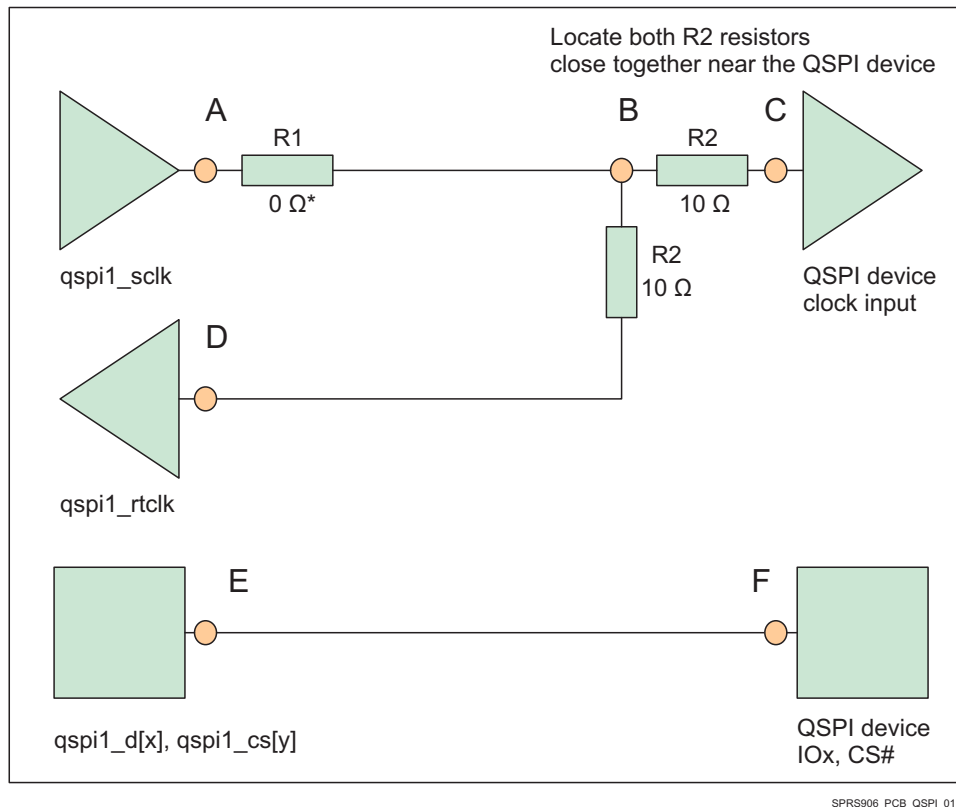


Figure 8-29. QSPI Interface High Level Schematic

NOTE

*0 Ω resistor (R1), located as close as possible to the qspi1_sclk pin, is placeholder for fine-tuning if needed.

8.5 Differential Interfaces

8.5.1 General Routing Guidelines

To maximize signal integrity, proper routing techniques for differential signals are important for high-speed designs. The following general routing guidelines describe the routing guidelines for differential lanes and differential signals.

- As much as possible, no other high-frequency signals must be routed in close proximity to the differential pair.
- Must be routed as differential traces on the same layer. The trace width and spacing must be chosen to yield the differential impedance value recommended.
- Minimize external components on differential lanes (like external ESD, probe points).
- Through-hole pins are not recommended.
- Differential lanes mustn't cross image planes (ground planes).
- No sharp bend on differential lanes.

- Number of vias on the differential pairs must be minimized, and identical on each line of the differential pair. In case of multiple differential lanes in the same interface, all lines should have the same number of vias.
- Shielded routing is to be promoted as much as possible (for instance, signals must be routed on internal layers that are inside power and/or ground planes).

8.5.2 USB 2.0 Board Design and Layout Guidelines

This section discusses schematic guidelines when designing a universal serial bus (USB) system.

8.5.2.1 Background

Clock frequencies generate the main source of energy in a USB design. The USB differential DP/DM pairs operate in high-speed mode at 480 Mbps. System clocks can operate at 12 MHz, 48 MHz, and 60 MHz. The USB cable can behave as a monopole antenna; take care to prevent RF currents from coupling onto the cable.

When designing a USB board, the signals of most interest are:

- Device interface signals: Clocks and other signal/data lines that run between devices on the PCB.
- Power going into and out of the cable: The USB connector socket pin 1 (VBUS) may be heavily filtered and need only pass low frequency signals of less than ~100 KHz. The USB socket pin 4 (analog ground) must be able to return the current during data transmission, and must be filtered sparingly.
- Differential twisted pair signals going out on cable, DP and DM: Depending upon the data transfer rate, these device terminals can have signals with fundamental frequencies of 240 MHz (high speed), 6 MHz (full speed), and 750 kHz (low speed).
- External crystal circuit (device terminals XI and X0): 12 MHz, 19.2 MHz, 24 MHz, and 48 MHz fundamental. When using an external crystal as a reference clock, a 24 MHz and higher crystal is highly recommended.

8.5.2.2 USB PHY Layout Guide

The following sections describe in detail the specific guidelines for USB PHY Layout.

8.5.2.2.1 General Routing and Placement

Use the following routing and placement guidelines when laying out a new design for the USB physical layer (PHY). These guidelines help minimize signal quality and electromagnetic interference (EMI) problems on a four-or-more layer evaluation module (EVM).

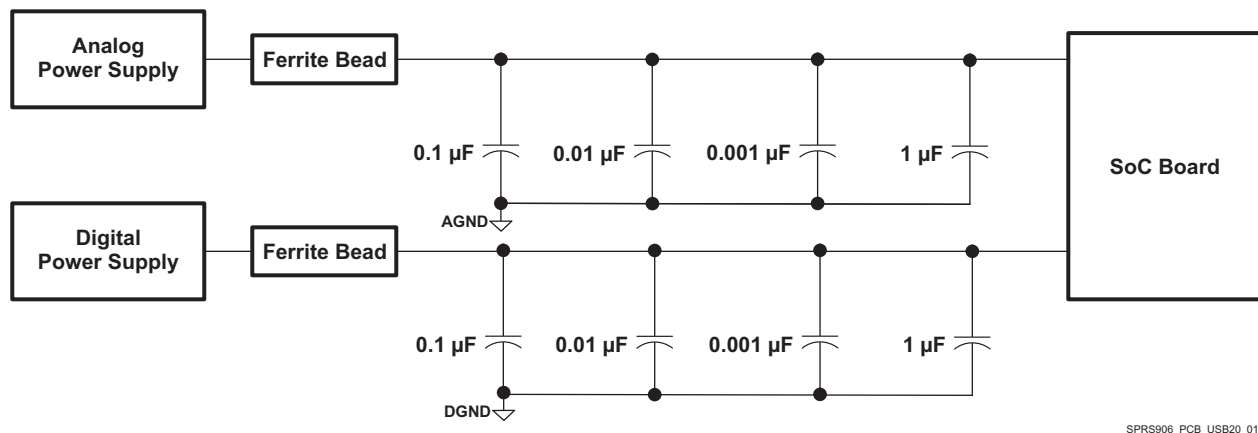
- Place the USB PHY and major components on the un-routed board first. For more details, see [Section 8.5.2.2.3](#).
- Route the high-speed clock and high-speed USB differential signals with minimum trace lengths.
- Route the high-speed USB signals on the plane closest to the ground plane, whenever possible.
- Route the high-speed USB signals using a minimum of vias and corners. This reduces signal reflections and impedance changes.
- When it becomes necessary to turn 90°, use two 45° turns or an arc instead of making a single 90° turn. This reduces reflections on the signal traces by minimizing impedance discontinuities.
- Do not route USB traces under or near crystals, oscillators, clock signal generators, switching regulators, mounting holes, magnetic devices or IC's that use or duplicate clock signals.
- Avoid stubs on the high-speed USB signals because they cause signal reflections. If a stub is unavoidable, then the stub should be less than 200 mils.
- Route all high-speed USB signal traces over continuous planes (V_{CC} or GND), with no interruptions. Avoid crossing over anti-etch, commonly found with plane splits.

8.5.2.2.2 Specific Guidelines for USB PHY Layout

The following sections describe in detail the specific guidelines for USB PHY Layout.

8.5.2.2.2.1 Analog, PLL, and Digital Power Supply Filtering

To minimize EMI emissions, add decoupling capacitors with a ferrite bead at power supply terminals for the analog, phase-locked loop (PLL), and digital portions of the chip. Place this array as close to the chip as possible to minimize the inductance of the line and noise contributions to the system. An analog and digital supply example is shown in [Figure 8-30](#). In case of multiple power supply pins with the same function, tie them up to a single low-impedance point in the board and then add the decoupling capacitors, in addition to the ferrite bead. This array of caps and ferrite bead improve EMI and jitter performance. Take both EMI and jitter into account before altering the configuration.



SPRS906_PCB_USB20_01

Figure 8-30. Suggested Array Capacitors and a Ferrite Bead to Minimize EMI

Consider the recommendations listed below to achieve proper ESD/EMI performance:

- Use a 0.01 μF cap on each cable power VBUS line to chassis GND close to the USB connector pin.
- Use a 0.01 μF cap on each cable ground line to chassis GND next to the USB connector pin.
- If voltage regulators are used, place a 0.01 μF cap on both input and output. This is to increase the immunity to ESD and reduce EMI. For other requirements, see the device-specific datasheet.

8.5.2.2.2 Analog, Digital, and PLL Partitioning

If separate power planes are used, they must be tied together at one point through a low-impedance bridge or preferably through a ferrite bead. Care must be taken to capacitively decouple each power rail close to the device. The analog ground, digital ground, and PLL ground must be tied together to the low-impedance circuit board ground plane.

8.5.2.2.3 Board Stackup

Because of the high frequencies associated with the USB, a printed circuit board with at least four layers is recommended; two signal layers separated by a ground and power layer as shown in [Figure 8-31](#).

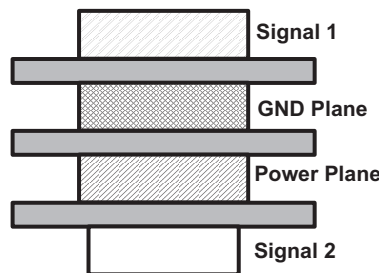


Figure 8-31. Four-Layer Board Stack-Up

The majority of signal traces should run on a single layer, preferably SIGNAL1. Immediately next to this layer should be the GND plane, which is solid with no cuts. Avoid running signal traces across a split in the ground or power plane. When running across split planes is unavoidable, sufficient decoupling must be used. Minimizing the number of signal vias reduces EMI by reducing inductance at high frequencies.

8.5.2.2.4 Cable Connector Socket

Short the cable connector sockets directly to a small chassis ground plane (GND *strap*) that exists immediately underneath the connector sockets. This shorts EMI (and ESD) directly to the chassis ground before it gets onto the USB cable. This etch plane should be as large as possible, but all the conductors coming off connector pins 1 through 6 must have the board signal GND plane run under. If needed, scoop out the chassis GND strap etch to allow for the signal ground to extend under the connector pins. Note that the etches coming from pins 1 and 4 (VBUS power and GND) should be wide and via-ed to their respective planes as soon as possible, respecting the filtering that may be in place between the connector pin and the plane. See [Figure 8-32](#) for a schematic example.

Place a ferrite in series with the cable shield pins near the USB connector socket to keep EMI from getting onto the cable shield. The ferrite bead between the cable shield and ground may be valued between 10 Ω and 50 Ω at 100 MHz; it should be resistive to approximately 1 GHz. To keep EMI from getting onto the cable bus power wire (a very large antenna) a ferrite may be placed in series with cable bus power, VBUS, near the USB connector pin 1. The ferrite bead between connector pin 1 and bus power may be valued between 47 Ω and approximately 1000 Ω at 100 MHz. It should continue being resistive out to approximately 1 GHz, as shown in [Figure 8-32](#).

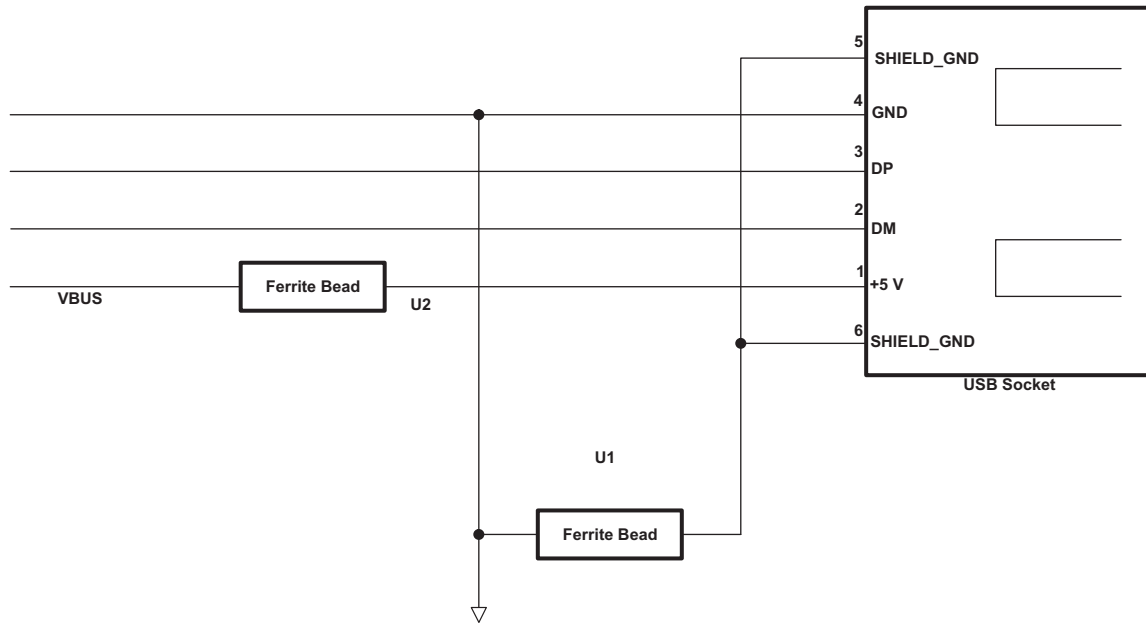


Figure 8-32. USB Connector

8.5.2.2.5 Clock Routings

To address the system clock emissions between devices, place a ~10 to 130 Ω resistor in series with the clock signal. Use a trial and error method of looking at the shape of the clock waveform on a high-speed oscilloscope and of tuning the value of the resistance to minimize waveform distortion. The value on this resistor should be as small as possible to get the desired effect. Place the resistor close to the device generating the clock signal. If an external crystal is used, follow the guidelines detailed in the *Selection and Specification of Crystals for Texas Instruments USB 2.0 Devices (SLLA122)*.

When routing the clock traces from one device to another, try to use the 3W spacing rule. The distance from the center of the clock trace to the center of any adjacent signal trace should be at least three times the width of the clock trace. Many clocks, including slow frequency clocks, can have fast rise and fall times. Using the 3W rule cuts down on crosstalk between traces. In general, leave space between each of the traces running parallel between the devices. Avoid using right angles when routing traces to minimize the routing distance and impedance discontinuities. For further protection from crosstalk, run guard traces beside the clock signals (GND pin to GND pin), if possible. This lessens clock signal coupling, as shown in Figure 8-33.

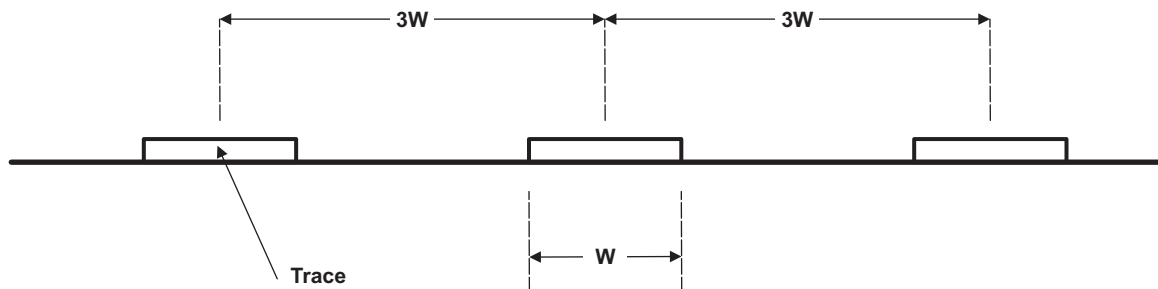


Figure 8-33. 3W Spacing Rule

8.5.2.2.2.6 Crystals/Oscillator

Keep the crystal and its load capacitors close to the USB PHY pins, XI and XO (see [Figure 8-34](#)). Note that frequencies from power sources or large capacitors can cause modulations within the clock and should not be placed near the crystal. In these instances, errors such as dropped packets occur. A placeholder for a resistor, in parallel with the crystal, can be incorporated in the design to assist oscillator startup.

Power is proportional to the current squared. The current is $I = C \cdot dv/dt$, because dv/dt is a function of the PHY, current is proportional to the capacitive load. Cutting the load to 1/2 decreases the current by 1/2 and the power to 1/4 of the original value. For more details on crystal selection, see the *Selection and Specification of Crystals for Texas Instruments USB 2.0 Devices* ([SLLA122](#)).

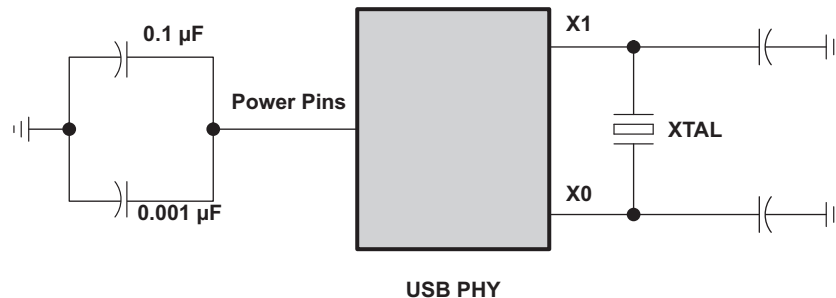


Figure 8-34. Power Supply and Clock Connection to the USB PHY

8.5.2.2.2.7 DP/DM Trace

Place the USB PHY as close as possible to the USB 2.0 connector. The signal swing during high-speed operation on the DP/DM lines is relatively small ($400 \text{ mV} \pm 10\%$), so any differential noise picked up on the twisted pair can affect the received signal. When the DP/DM traces do not have any shielding, the traces tend to behave like an antenna and picks up noise generated by the surrounding components in the environment. To minimize the effect of this behavior:

- DP/DM traces should always be matched lengths and must be no more than 4 inches in length; otherwise, the eye opening may be degraded (see [Figure 8-35](#)).
- Route DP/DM traces close together for noise rejection on differential signals, parallel to each other and within two mils in length of each other. The measurement for trace length must be started from device's balls.
- A high-speed USB connection is made through a shielded, twisted pair cable with a differential characteristic impedance of $90 \Omega \pm 15\%$. In layout, the impedance of DP and DM should each be $45 \Omega \pm 10\%$.
- DP/DM traces should not have any extra components to maintain signal integrity. For example, traces cannot be routed to two USB connectors.

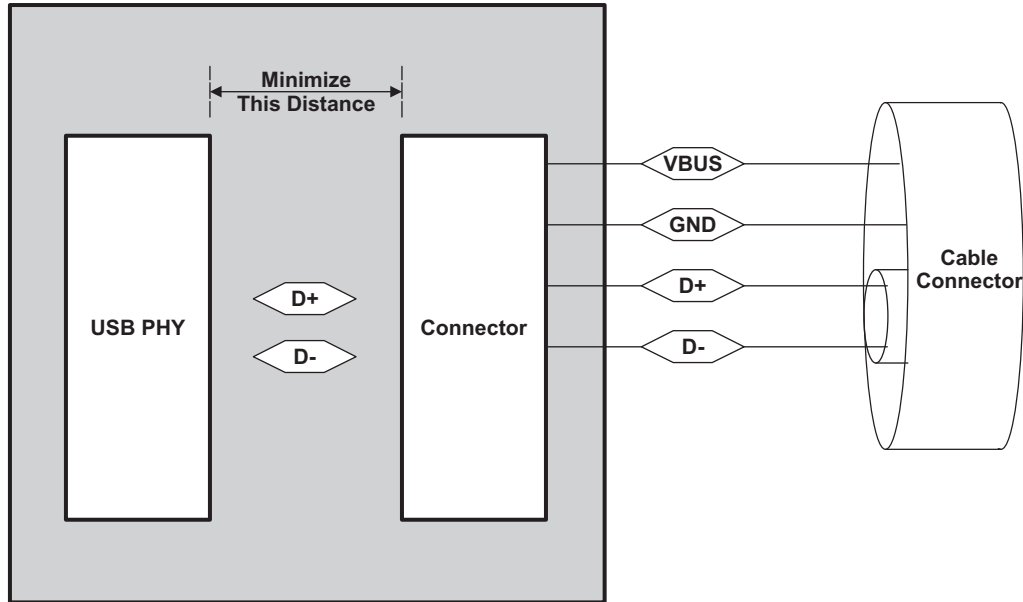


Figure 8-35. USB PHY Connector and Cable Connector

8.5.2.2.8 DP/DM Vias

When a via must be used, increase the clearance size around it to minimize its capacitance. Each via introduces discontinuities in the signal's transmission line and increases the chance of picking up interference from the other layers of the board. Be careful when designing test points on twisted pair lines; through-hole pins are not recommended.

8.5.2.2.9 Image Planes

An image plane is a layer of copper (voltage plane or ground plane), physically adjacent to a signal routing plane. Use of image planes provides a low impedance, shortest possible return path for RF currents. For a USB board, the best image plane is the ground plane because it can be used for both analog and digital circuits.

- Do not route traces so they cross from one plane to the other. This can cause a broken RF return path resulting in an EMI radiating loop as shown in [Figure 8-36](#). This is important for higher frequency or repetitive signals. Therefore, on a multi-layer board, it is best to run all clock signals on the signal plane above a solid ground plane.
- Avoid crossing the image power or ground plane boundaries with high-speed clock signal traces immediately above or below the separated planes. This also holds true for the twisted pair signals (DP, DM). Any unused area of the top and bottom signal layers of the PCB can be filled with copper that is connected to the ground plane through vias.

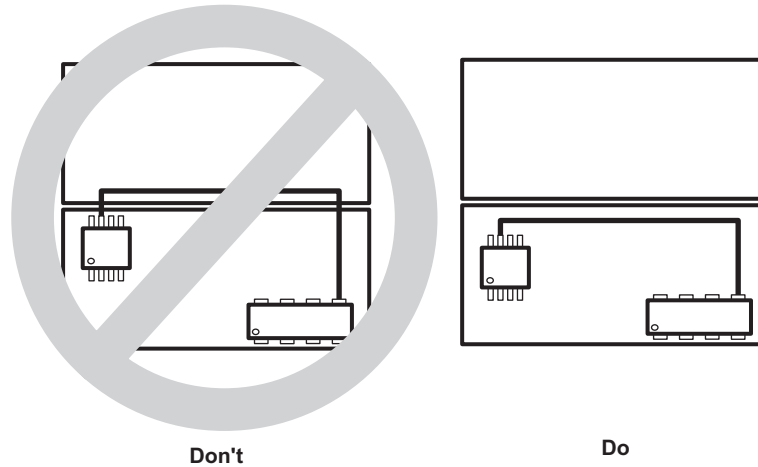


Figure 8-36. Do Not Cross Plane Boundaries

- Do not overlap planes that do not reference each other. For example, do not overlap a digital power plane with an analog power plane as this produces a capacitance between the overlapping areas that could pass RF emissions from one plane to the other, as shown in [Figure 8-37](#).

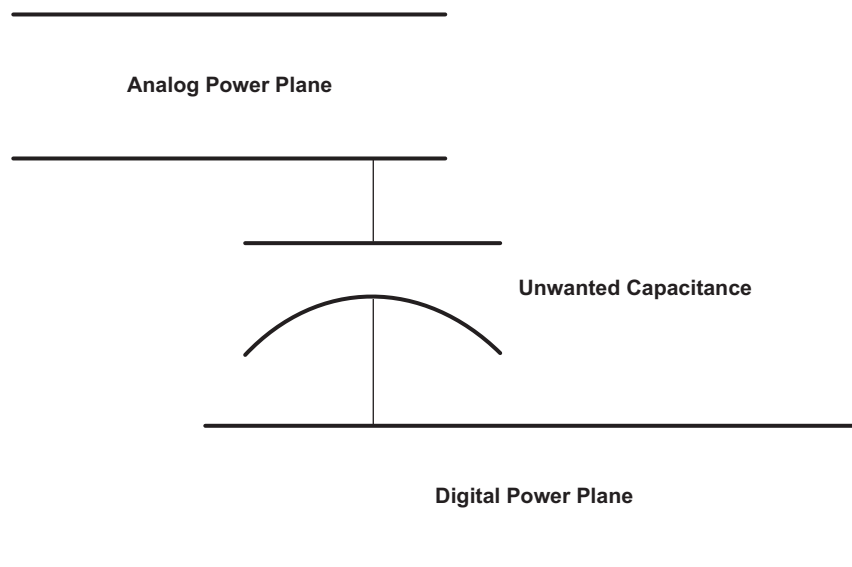


Figure 8-37. Do Not Overlap Planes

- Avoid image plane violations. Traces that route over a slot in an image plane results in a possible RF return loop, as shown in [Figure 8-38](#).

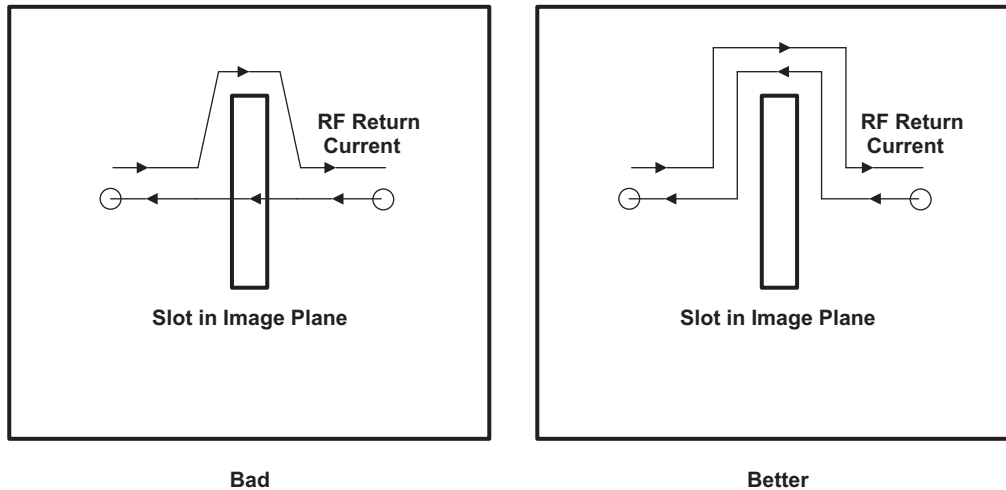


Figure 8-38. Do Not Violate Image Planes

8.5.2.2.2.10 JTAG Interface

For test and debug of the USB PHY only, an IEEE Standard 1149.1-1990, IEEE Standard Test Access Port and Boundary-Scan Architecture (JTAG) and Serial Test and Configuration Interface (STCI) may be available on the System-on-Chip (SoC). If available, keep the USB PHY JTAG interface less than six inches; keeping this distance short reduces noise coupling from other devices and signal loss due to resistance.

8.5.2.2.2.11 Power Regulators

Switching power regulators are a source of noise and can cause noise coupling if placed close to sensitive areas on a circuit board. Therefore, the switching power regulator should be kept away from the DP/DM signals, the external clock crystal (or clock oscillator), and the USB PHY.

8.5.2.3 Electrostatic Discharge (ESD)

International Electronic Commission (IEC) 61000-4-xx is a set of about 25 testing specifications from the IEC. IEC ESD Stressing is done both un-powered and with power applied, and with the device functioning. There must be no physical damage, and the device must keep working normally after the conclusion of the stressing. Typically, equipment has to pass IEC stressing at 8 kV contact and 15 kV air discharge, or higher. To market products/systems in the European community, all products/systems must be CE compliant and have the CE Mark. To obtain the CE Mark, all products/systems need to go through and pass IEC standard requirements; for ESD, it is 61000-4-2. 61000-4-2 requires that the products/systems pass contact discharge at 8 kV and air discharge at 15 kV. When performing an IEC ESD Stressing, only pins accessible to the *outside world* need to pass the test. The system into which the integrated circuit (IC) is placed makes a difference in how well the IC does. For example:

- Cable between the zap point and the IC attenuate the high frequencies in the waveform.
- Series inductance on the PCB board attenuates the high frequencies.
- Unless the capacitor's ground connection is inductive, capacitance to ground shunts away high frequencies.

8.5.2.3.1 IEC ESD Stressing Test

The following sections describe in detail the IEC ESD Stressing Test modes and test types.

8.5.2.3.1.1 Test Mode

The IEC ESD Stressing test is done through two modes: contact discharge mode and air discharge mode.

For the contact discharge test mode, the preferred way is direct contact applied to the conductive surfaces of the equipment under test (EUT). In the case of the USB system, the conductive surface is the outer casing of the USB connector. The electrode of the ESD generator is held in contact with the EUT or a coupling plane prior to discharge. The arc formation is created under controlled conditions, inside a relay, resulting in repeatable waveforms; however, this arc does not accurately recreate the characteristic unique to the arc of an actual ESD event.

8.5.2.3.1.2 Air Discharge Mode

The air discharge usually applies to a non-conductive surface of the EUT. Instead of a direct contact with the EUT, the charged electrode of the ESD generator is brought close to the EUT, and a spark in the air to the EUT actuates the discharge. Compared to the contact discharge mode, the air discharge is more realistic to the actual ESD occurrence. However, due to the variations of the arc length, it may not be able to produce repeatable waveform.

8.5.2.3.1.3 Test Type

The IEC ESD Stressing test has two test types: direct discharge and indirect discharge. Direct discharge is applied directly to the surface or the structure of the EUT. It includes both contact discharge and air discharge modes. Indirect discharge applies to a coupling plane in the vicinity of the EUT. The indirect discharge is used to simulate personal discharge to objects which are adjacent to the EUT. It includes contact discharge mode only.

8.5.2.3.2 TI Component Level IEC ESD Test

TI Component Level IEC ESD Test tests only the IC terminals that are exposed in system level applications. It can be used to determine the robustness of on-chip protection and the latch-up immunity. The IC can only pass the TI Component Level IEC ESD test when there is no latch-up and IC is fully functional after the test.

8.5.2.3.3 Construction of a Custom USB Connector

A standard USB connector, either type A or type B, provides good ESD protection. However, if a custom USB connector is desired, the following guidelines should be observed to ensure good ESD protection.

- There should be an easily accessible shield plate next to the connector for air-discharge mode purpose.
- Tie the outer shield of the connector to GND. When a cable is inserted into the connector, the shield of the cable should first make contact with the outer shield.
- If the connector includes power and GND, the lead of power and GND need to be longer than the leads of signal.
- The connector needs to have a key to ensure proper insertion of the cable.
- See the standard USB connector for reference.

8.5.2.3.4 ESD Protection System Design Consideration

ESD protection system design consideration is covered in [Section 8.5.2.2](#) of this document. The following are additional considerations for ESD protection in a system.

- Metallic shielding for both ESD and EMI
- Chassis GND isolation from the board GND
- Air gap designed on board to absorb ESD energy
- Clamping diodes to absorb ESD energy
- Capacitors to divert ESD energy
- The use of external ESD components on the DP/DM lines may affect signal quality and are not recommended.

8.5.2.4 References

- *USB 2.0 Specification*, Intel, 2000, <http://www.usb.org/developers/docs/>
- *High Speed USB Platform Design Guidelines*, Intel, 2000, http://www.intel.com/technology/usb/download/usb2dg_R1_0.pdf
- *Selection and Specification of Crystals for Texas Instruments USB 2.0 Devices* ([SLLA122](#))

8.5.3 HDMI Board Design and Layout Guidelines

This section provides the timing specification for the HDMI interface as a PCB design and manufacturing specification. The design rules constrain PCB trace length, PCB trace skew, signal integrity, cross-talk, and signal timing. TI has performed the simulation and system design work to ensure the HDMI interface requirements are met. The design rules stated within this document are targeted at resolutions less than or equal to 1080p60 with 8-bit color; deep color (10-bit) requires further signal integrity optimization.

8.5.3.1 HDMI Interface Schematic

The HDMI bus is separated into three main sections (HDMI Ethernet and the optional Audio Return Channel are not specifically supported by this Device):

1. Transition Minimized Differential Signaling (TMDS) high speed digital video interface
2. Display Data Channel (I2C bus for configuration and status exchange between two devices)
3. Consumer Electronics Control (optional) for remote control of connected devices.

The DDC and CEC are low speed interfaces, so nothing special is required for PCB layout of these signals.

The TMDS channels are high speed differential pairs and therefore require the most care in layout. Specifications for TMDS layout are below.

[Figure 8-39](#) shows the HDMI interface schematic.

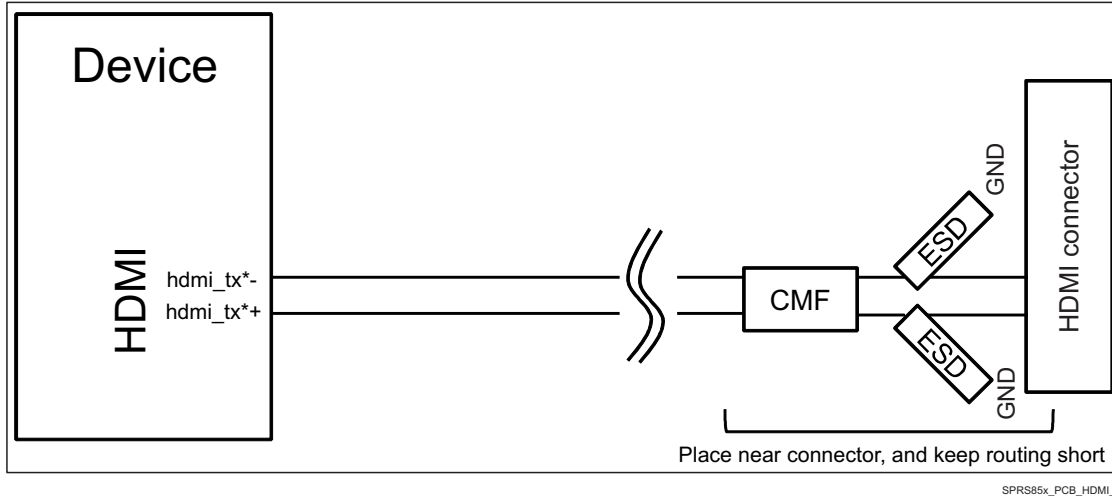


Figure 8-39. HDMI Interface High Level Schematic

Figure 8-40 presents placement diagram for HDMI interface.

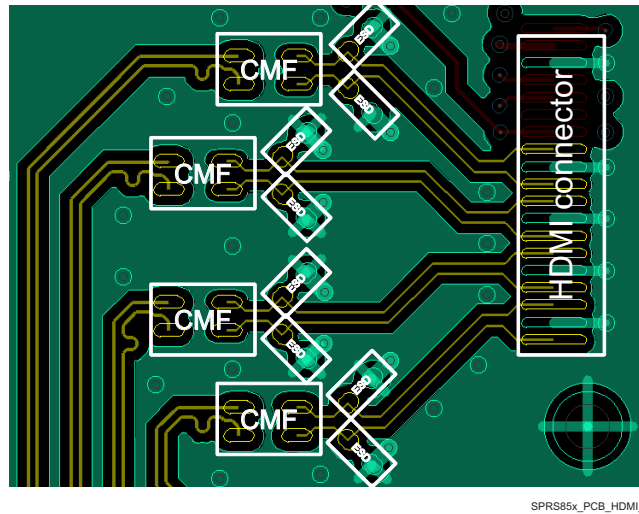


Figure 8-40. HDMI Placement Diagram

Table 8-12. HDMI Component Reference

INTERFACE	DEVICE	SUPPLIER	PART NUMBER
HDMI	ESD	TI	TPD1E05U06
	CMF	Murata	DLW21SN900HQ2

8.5.3.2 TMDS General Routing Guidelines

The TMDS signals are high speed differential pairs. Care must be taken in the PCB layout of these signals to ensure good signal integrity.

The TMDS differential signal traces must be routed to achieve 100 Ohms (+/- 10%) differential impedance and 60 ohms (+/-10%) single ended impedance. Single ended impedance control is required because differential signals can't be closely coupled on PCBs and therefore single ended impedance becomes important.

These impedances are impacted by trace width, trace spacing, distance to reference planes, and dielectric material. Verify with a PCB design tool that the trace geometry for both data signal pairs results in as close to 60 ohms impedance traces as possible. For best accuracy, work with your PCB fabricator to ensure this impedance is met.

In general, closely coupled differential signal traces are not an advantage on PCBs. When differential signals are closely coupled, tight spacing and width control is necessary. Very small width and spacing variations affect impedance dramatically, so tight impedance control can be more problematic to maintain in production.

Loosely coupled PCB differential signals make impedance control much easier. Wider traces and spacing make obstacle avoidance easier, and trace width variations don't affect impedance as much, therefore it's easier to maintain accurate impedance over the length of the signal. The wider traces also show reduced skin effect and therefore often result in better signal integrity.

Some general routing guidelines regarding TMDS:

- Avoid crossing splits reference plane(s).
- Shorter trace length is preferred.
- Distance between common mode filter (CMF) and ESD protection device should be as short as possible
- Distance between ESD protection device and HDMI connector should be as short as possible.

Table 8-13 shows the routing specifications for the TMDS signals.

Table 8-13. TMDS Routing Specifications

PARAMETER	MIN	TYP	MAX	UNIT
Device balls to HDMI header trace length			4000	Mills
Skew within a differential pair		3	5	Mils
Number of stubs allowed on TMDS traces			0	stubs
TMDS pair differential impedance	90	100	110	Ω
TMDS single-ended impedance	54	60	66	Ω
Number of vias on each TMDS trace			0	Vias
TMDS differential pair to any other trace spacing ⁽¹⁾ ⁽²⁾ ⁽³⁾	2xDS	3xDS		Mils
Number of ground plane cuts allowed within HDMI routing region (except for specific ground carving as explained in this document)			0	Cuts
Number of layers between HDMI routing region and reference ground plane			0	Layers
PCB trace width		4.4		Mils

(1) DS = differential spacing of the traces.

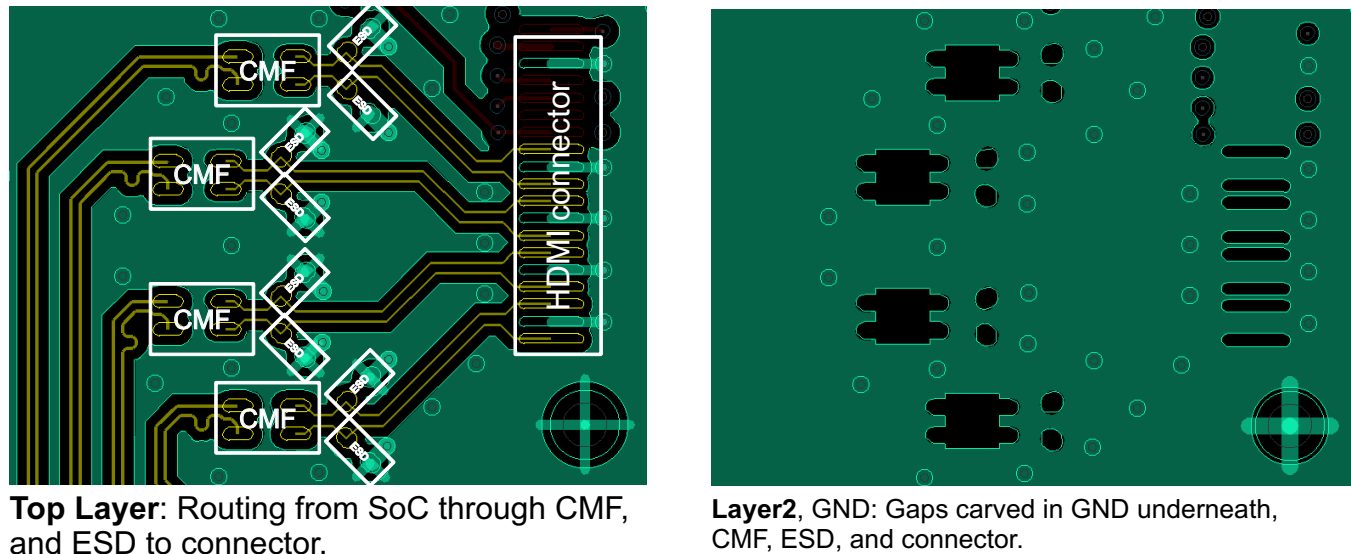
(2) Exceptions may be necessary in the SoC package BGA area.

(3) GND guard-bands may be closer, but should not be allowed to affect the impedance of the differential pair routing. GND guard-bands to isolate HDMI differential pairs from all other signals is recommended.

Table 8-14. TDMS Routing Recommendations

Item	Description	Reason
ESD part number	TPD1E05U06	Minimize capacitance (0.42pF)
Carve Ground	Carve GND underneath ESD and CMF	Minimize capacitance under ESD and CMF
Round pads	Reduce pad size and round the corners of the pads for the ESD and CMF components	Minimize capacitance
Routing layer	Route all signals only on the same layer as SoC	Minimize reflection loss

Figure 8-41 presents an example layout, demonstrating the “carve GND” concept.



SPRS85x_PCB_HDMI_3

Figure 8-41. HDMI Example “carve GND” layout

8.5.3.3 TPD5S115

The TPD5S115 is an integrated HDMI companion chip solution. The device provides a regulated 5 V output (5VOUT) for sourcing the HDMI power line. The TPD5S115 exceeds the IEC61000-4-2 (Level 4) ESD protection level.

8.5.3.4 HDMI ESD Protection Device (Required)

Interfaces that connect to a cable such as HDMI generally require more ESD protection than can be built into the processor’s outputs. Therefore this HDMI interface requires the use of an ESD protection chip to provide adequate ESD.

When selecting an ESD protection chip, choose the lowest capacitance ESD protection available to minimize signal degradation. In no case should be ESD protection circuit capacitance be more than 5pF.

TI manufactures these devices that provide ESD protection for HDMI signals such as the TPDxE05U06. For more information see the www.ti.com website.

8.5.3.5 PCB Stackup Specifications

Table 8-15 shows the stackup and feature sizes required for HDMI.

Table 8-15. HDMI PCB Stackup Specifications

PARAMETER	MIN	TYP	MAX	UNIT
PCB Routing/Plane Layers	4	6	-	Layers
Signal Routing Layers	2	3	-	Layers
Number of ground plane cuts allowed within HDMI routing region	-	-	0	Cuts
Number of layers between HDMI routing region and reference ground plane	-	-	0	Layers
PCB Trace width		4		Mils

8.5.3.6 Grounding

Each TMDS channel has its own shield pin and they should be grounded to provide a return current path for the TMDS signal.

8.5.4 SATA Board Design and Layout Guidelines

The device provides one SATA port. This section provides the timing specification for the SATA interface as a PCB design and manufacturing specification. The design rules constrain PCB trace length, PCB trace skew, signal integrity, cross-talk, and signal timing. TI has performed the simulation and system design work to ensure the SATA interface requirements are met.

8.5.4.1 SATA Interface Schematic

Figure 8-42 shows the data portion of the SATA interface schematic.

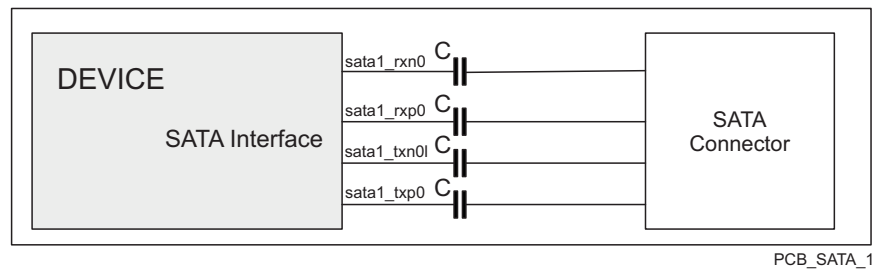


Figure 8-42. SATA Interface High Level Schematic

NOTE

AC coupling capacitors (C) are required on the receive and transmit data pairs. Table 8-16 shows the requirements for these capacitors.

Table 8-16. SATA AC Coupling Capacitors Requirements

PARAMETER	MIN	TYP	MAX	UNIT
SATA AC coupling capacitor value	0.3	10	12	nF
SATA AC coupling capacitor package size		0402	0603	EIA ⁽¹⁾⁽²⁾

(1) EIA LxW units, i.e., a 0402 is a 40x20 mils surface mount capacitor.

(2) The physical size of the capacitor should be as small as practical. Use the same size on both lines in each pair placed side by side.

8.5.4.2 Compatible SATA Components and Modes

Table 8-17 shows the compatible SATA components and supported modes. Note that the only supported configuration is an internal cable from the processor host to the SATA device.

Table 8-17. Compatible SATA Components and Modes

PARAMETER	MIN	MAX	UNIT	SUPPORTED
Transfer Rates	1.5	3	Gbps	
Internal Cable	-	-	-	YES

8.5.4.3 PCB Stackup Specifications

Table 8-18 shows the stackup and feature sizes required for these types of SATA connections.

Table 8-18. SATA PCB Stackup Specifications

PARAMETER	MIN	TYP	MAX	UNIT
Number of ground plane cuts allowed within SATA routing region	-	-	0	Cuts
Number of layers between SATA routing area and reference plane	-	-	0	Layers
PCB Routing clearance		4		Mils
PCB Trace width		4		Mils

8.5.4.4 Routing Specifications

The SATA data signal traces must be routed to achieve 100 Ohms (+/-10%) differential impedance and 60 ohms (+/-10%) single ended impedance. The signal ended impedance is required because differential signals can't be closely coupled on PCBs and therefore single ended impedance becomes important. 60 ohms is chosen for the single ended impedance to minimize problems caused by too low an impedance.

These impedances are impacted by trace width, trace spacing, distance to reference planes, and dielectric material. Verify with a PCB design tool that the trace geometry for both data signal pairs results in as close to 100 ohms differential and 60 ohms single ended impedance traces as possible. For best accuracy, work with your PCB fabricator to ensure this impedance is met.

Table 8-19 shows the routing specifications for the SATA data signals.

Table 8-19. SATA Routing Specifications

PARAMETER	MIN	TYP	MAX	UNIT
SATA signal trace length (device balls to SATA connector)			3050 ⁽¹⁾	Mils
Differential pair trace skew matching			5	Mils
Number of stubs allowed on SATA traces ⁽²⁾			0	stubs
TX/RX pair differential impedance	90	100	110	Ω
TX/RX single-ended impedance	54	60	66	Ω
Number of vias on each SATA trace			0	Vias
SATA differential pair to any other trace spacing	2xDS ⁽³⁾			

(1) Beyond this, signal integrity may suffer.

(2) Inline pads may be used for probing.

(3) DS = differential spacing of the SATA traces.

Table 8-20. SATA Routing Recommendations

Item	Description	Reason
ESD part number	None	ESD suppression generally not used on SATA

8.5.5 PCIe Board Design and Layout Guidelines

The PCIe interface on the device provides support for a 5.0 Gbps lane with polarity inversion.

8.5.5.1 PCIe Connections and Interface Compliance

The PCIe interface on the device is compliant with the PCIe revision 3.0 specification. Please refer to the PCIe specifications for all connections that are described in it. Those recommendations are more descriptive and exhaustive than what is possible here.

The use of PCIe compatible bridges and switches is allowed for interfacing with more than one other processor or PCIe device.

8.5.5.1.1 Coupling Capacitors

AC coupling capacitors are required on the transmit data pair. [Table 8-21](#) shows the requirements for these capacitors.

Table 8-21. PCIe AC Coupling Capacitors Requirements

PARAMETER	MIN	TYP	MAX	UNIT
PCIe AC coupling capacitor value	90	100	110	nF
PCIe AC coupling capacitor package size		0402	0603	EIA ⁽¹⁾⁽²⁾

(1) EIA LxW units, i.e., a 0402 is a 40x20 mils surface mount capacitor.

(2) The physical size of the capacitor should be as small as practical. Use the same size on both lines in each pair placed side by side.

8.5.5.1.2 Polarity Inversion

The PCIe specification requires polarity inversion support. This means for layout purposes, polarity is unimportant because each signal can change its polarity on die inside the chip. This means polarity within a lane is unimportant for layout.

8.5.5.2 Non-standard PCIe connections

The following sections contain suggestions for any PCIe connection that is NOT described in the official PCIe specification, such as an on-board Device to Device or Device to other PCIe compliant processor connection.

8.5.5.2.1 PCB Stackup Specifications

[Table 8-22](#) shows the stackup and feature sizes required for these types of PCIe connections.

Table 8-22. PCIe PCB Stackup Specifications

PARAMETER	MIN	TYP	MAX	UNIT
Number of ground plane cuts allowed within PCIe routing region	-	-	0	Cuts
Number of layers between PCIe routing area and reference plane ⁽¹⁾	-	-	0	Layers
PCB Routing clearance		4		Mils
PCB Trace width		4		Mils

(1) A reference plane may be a ground plane or the power plane referencing the PCIe signals.

8.5.5.2.2 Routing Specifications

8.5.5.2.2.1 Impedance

The PCIe data signal traces must be routed to achieve 100-Ω (±10%) differential impedance and 60-Ω (±10%) single-ended impedance. The single-ended impedance is required because differential signals are extremely difficult to closely couple on PCBs and, therefore, single-ended impedance becomes important. These requirements are the same as those recommended in the PCIe Motherboard Checklist 1.0 document, available from PCI-SIG (www.pcisig.com).

These impedances are impacted by trace width, trace spacing, distance between signals and referencing planes, and dielectric material. Verify with a PCB design tool that the trace geometry for both data signal pairs result in as close to 100-Ω differential impedance and 60-Ω single-ended impedance as possible. For best accuracy, work with your PCB fabricator to ensure this impedance is met. See [Table 8-23](#) below.

8.5.5.2.2.2 Differential Coupling

In general, closely coupled differential signal traces are not an advantage on PCBs. When differential signals are closely coupled, tight spacing and width control is necessary. Very small width and spacing variations affect impedance dramatically, so tight impedance control can be more problematic to maintain in production. For PCBs with very tight space limitations (which are usually small) this can work, but for most PCBs, the loosely coupled option is probably best.

Loosely coupled PCB differential signals make impedance control much easier. Wider traces and spacing make obstacle avoidance easier (because each trace is not so fixed in position relative to the other), and trace width variations don't affect impedance as much, therefore it's easier to maintain an accurate impedance over the length of the signal. For longer routes, the wider traces also show reduced skin effect and therefore often result in better signal integrity with a larger eye diagram opening.

Table 8-23 shows the routing specifications for the PCIe data signals.

Table 8-23. PCI-E Routing Specifications

PARAMETER	MIN	TYP	MAX	UNIT
PCIe signal trace length (device balls to PCIe connector)			4700 ⁽¹⁾	Mills
Differential pair trace matching			5 ⁽²⁾	Mils
Number of stubs allowed on PCIe traces ⁽³⁾			0	stubs
TX/RX pair differential impedance	90	100	110	Ω
TX/RX single-ended impedance	54	60	66	Ω
Pad size of vias on PCIe trace			25 ⁽⁴⁾	Mils
Hole size of vias on PCIe trace			14	Mils
Number of vias on each PCIe trace			0	Vias
PCIe differential pair to any other trace spacing	2xDS ⁽⁵⁾			

(1) Beyond this, signal integrity may suffer.

(2) For example, RXP0 within 5 Mils of RXN0.

(3) Inline pads may be used for probing.

(4) 35-Mil antipad maximum recommended.

(5) DS = differential spacing of the PCIe traces.

Table 8-24. PCI-E Routing Recommendations

Item	Description	Reason
ESD part number	None	ESD suppression generally not used on PCIe

8.5.5.2.2.3 Pair Length Matching

Each signal in the differential pair should be matched to within 5 mils of its matching differential signal. Length matching should be done as close to the mismatch as possible.

8.5.5.3 LJCB_REFNP Connections

A Common Refclk Rx Architecture is required to be used for the device PCIe interface. Specifically, two modes of Common Refclk Rx Architecture are supported:

- **External REFCLK Mode:** An common external 100MHz clock source is distributed to both the Device and the link partner
- **Output REFCLK Mode:** A 100MHz HCSL clock source is output by the device and used by the link partner

In **External REFCLK Mode**, a high-quality, low-jitter, differential HCSL 100MHz clock source compliant to the PCIe REFCLK AC Specifications should be provided on the Device's ljcb_clkn / ljcb_clkp inputs. Alternatively, an LVDS clock source can be used with the following additional requirements:

- External AC coupling capacitors described in [Table 8-25](#) should be populated at the ljcb_clk / ljcb_clkp inputs.
- All termination requirements (ex. parallel 100ohm termination) from the clock source manufacturer should be followed.

In **Output REFCLK Mode**, the 100MHz clock from the Device's DPLL_PCIE_REF should be output on the Device's ljcb_clk / ljcb_clkp pins and used as the HCSL REFCLK by the link partner. External near-side termination to ground described in [Table 8-26](#) is required on both of the ljcb_clk / ljcb_clkp outputs in this mode.

Table 8-25. LJCB_REFN/P Requirements in External LVDS REFCLK Mode

PARAMETER	MIN	TYP	MAX	UNIT
ljcb_clk / ljcb_clkp AC coupling capacitor value		100		nF
ljcb_clk / ljcb_clkp AC coupling capacitor package size		0402	0603	EIA ⁽¹⁾⁽²⁾

(1) EIA LxW units, i.e., a 0402 is a 40x20 mils surface mount capacitor.

(2) The physical size of the capacitor should be as small as practical. Use the same size on both lines in each pair placed side by side.

Table 8-26. LJCB_REFN/P Requirements in Output REFCLK Mode

PARAMETER	MIN	TYP	MAX	UNIT
ljcb_clk / ljcb_clkp near-side termination to ground value	47.5	50	52.5	Ohms

8.6 Clock Routing Guidelines

8.6.1 32-kHz Oscillator Routing

When designing the printed-circuit board:

- Keep the crystal as close as possible to the crystal pins X1 and X2.
- Keep the trace lengths short and small to reduce capacitor loading and prevent unwanted noise pickup.
- Place a guard ring around the crystal and tie the ring to ground to help isolate the crystal from unwanted noise pickup.
- Keep all signals out from beneath the crystal and the X1 and X2 pins to prevent noise coupling.
- Finally, an additional local ground plane on an adjacent PCB layer can be added under the crystal to shield it from unwanted pickup from traces on other layers of the board. This plane must be isolated from the regular PCB ground plane and tied to the GND pin of the RTC. The plane must not be any larger than the perimeter of the guard ring. Make sure that this ground plane does not contribute to significant capacitance (a few pF) between the signal line and ground on the connections that run from X1 and X2 to the crystal.

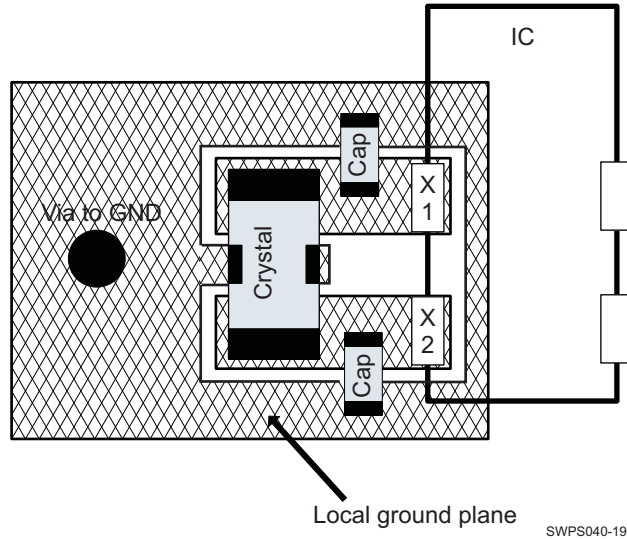


Figure 8-43. Slow Clock PCB Requirements

8.6.2 Oscillator Ground Connection

Although the impedance of a ground plane is low it is, of course, not zero. Therefore, any noise current in the ground plane causes a voltage drop in the ground. Figure 8-44 shows the grounding scheme for slow (low frequency) clock generated from the internal oscillator.

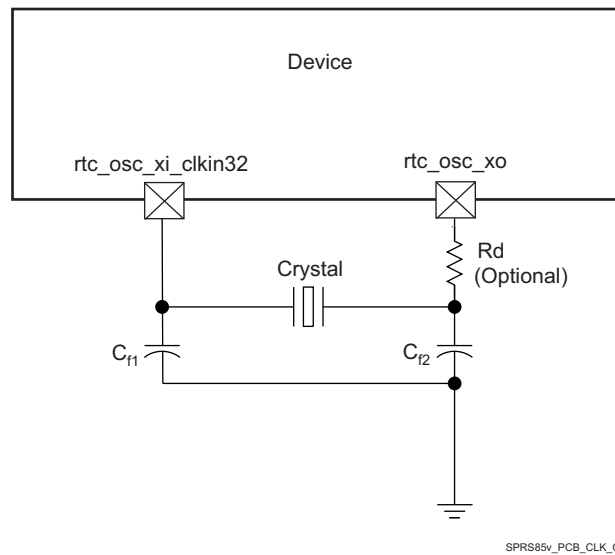
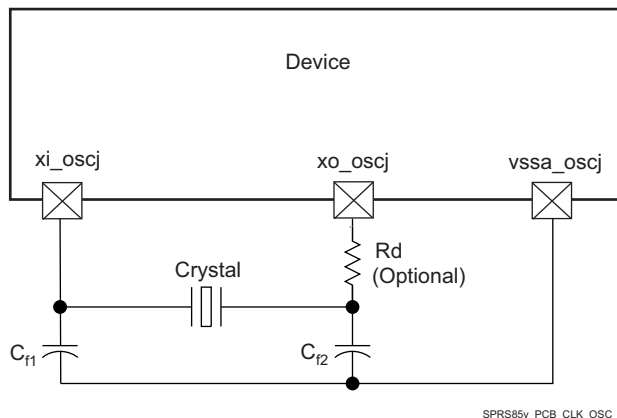


Figure 8-44. Grounding Scheme for Low-Frequency Clock

Figure 8-45 shows the grounding scheme for high-frequency clock.



(1) j in *_osc = 0 or 1

Figure 8-45. Grounding Scheme for High-Frequency Clock

8.7 DDR2/DDR3 Board Design and Layout Guidelines

8.7.1 DDR2/DDR3 General Board Layout Guidelines

To help ensure good signaling performance, consider the following board design guidelines:

- Avoid crossing splits in the power plane.
- Minimize Vref noise.
- Use the widest trace that is practical between decoupling capacitors and memory module.
- Maintain a single reference.
- Minimize ISI by keeping impedances matched.
- Minimize crosstalk by isolating sensitive bits, such as strobes, and avoiding return path discontinuities.
- Use proper low-pass filtering on the Vref pins.
- Keep the stub length as short as possible.
- Add additional spacing for on-clock and strobe nets to eliminate crosstalk.
- Maintain a common ground reference for all bypass and decoupling capacitors.
- Take into account the differences in propagation delays between microstrip and stripline nets when evaluating timing constraints.

8.7.2 DDR2 Board Design and Layout Guidelines

8.7.2.1 Board Designs

TI only supports board designs that follow the guidelines outlined in this document. The switching characteristics and the timing diagram for the DDR2 memory controller are shown in [Table 8-27](#) and [Figure 8-46](#).

Table 8-27. Switching Characteristics Over Recommended Operating Conditions for DDR2 Memory Controller

NO.	PARAMETER	DESCRIPTION	MIN	MAX	UNIT
DDR21	$t_c(\text{DDR_CLK})$	Cycle time, DDR_CLK	2.5	8	ns

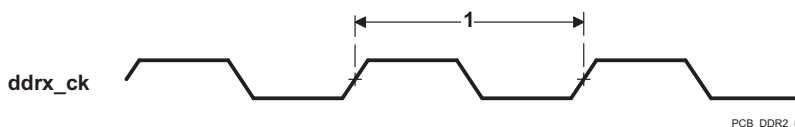


Figure 8-46. DDR2 Memory Controller Clock Timing

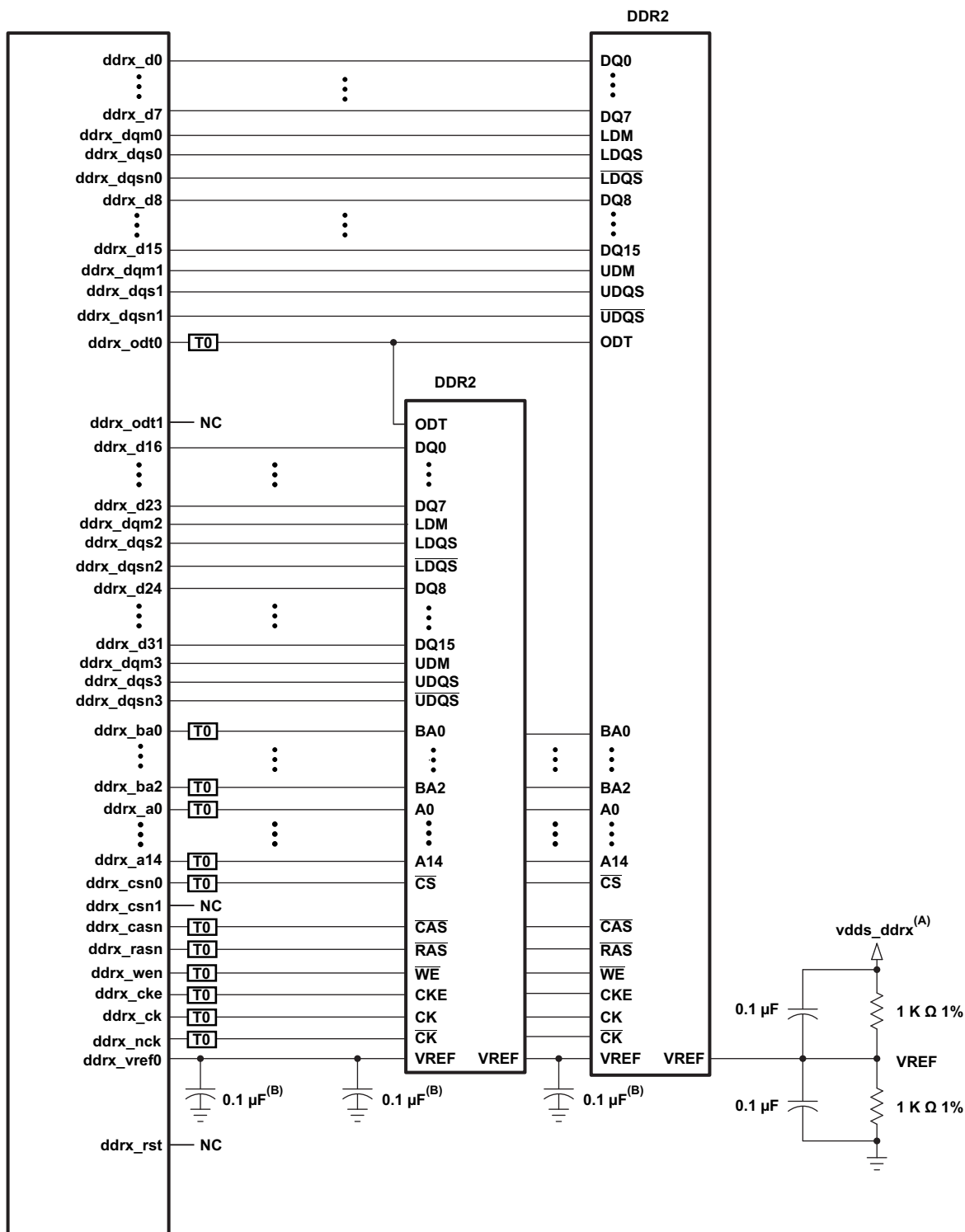
8.7.2.2 DDR2 Interface

This section provides the timing specification for the DDR2 interface as a PCB design and manufacturing specification. The design rules constrain PCB trace length, PCB trace skew, signal integrity, cross-talk, and signal timing. These rules, when followed, result in a reliable DDR2 memory system without the need for a complex timing closure process. For more information regarding the guidelines for using this DDR2 specification, see the *Understanding TI's PCB Routing Rule-Based DDR Timing Specification* Application Report (Literature Number: [SPRAAV0](#)).

8.7.2.2.1 DDR2 Interface Schematic

[Figure 8-47](#) shows the DDR2 interface schematic for a x32 DDR2 memory system. In [Figure 8-48](#) the x16 DDR2 system schematic is identical except that the high-word DDR2 device is deleted.

When not using all or part of a DDR2 interface, the proper method of handling the unused pins is to tie off the `ddrx_dqsi` pins to ground via a 1k- Ω resistor and to tie off the `ddrx_dqsn` pins to the corresponding `vdds_ddrx` supply via a 1k- Ω resistor. This needs to be done for each byte not used. The `vdds_ddrx` and `ddrx_vref0` power supply pins need to be connected to their respective power supplies even if DDRx is not being used. All other DDR interface pins can be left unconnected. Note that the supported modes for use of the DDR EMIF are 32-bits wide, 16-bits wide, or not used.

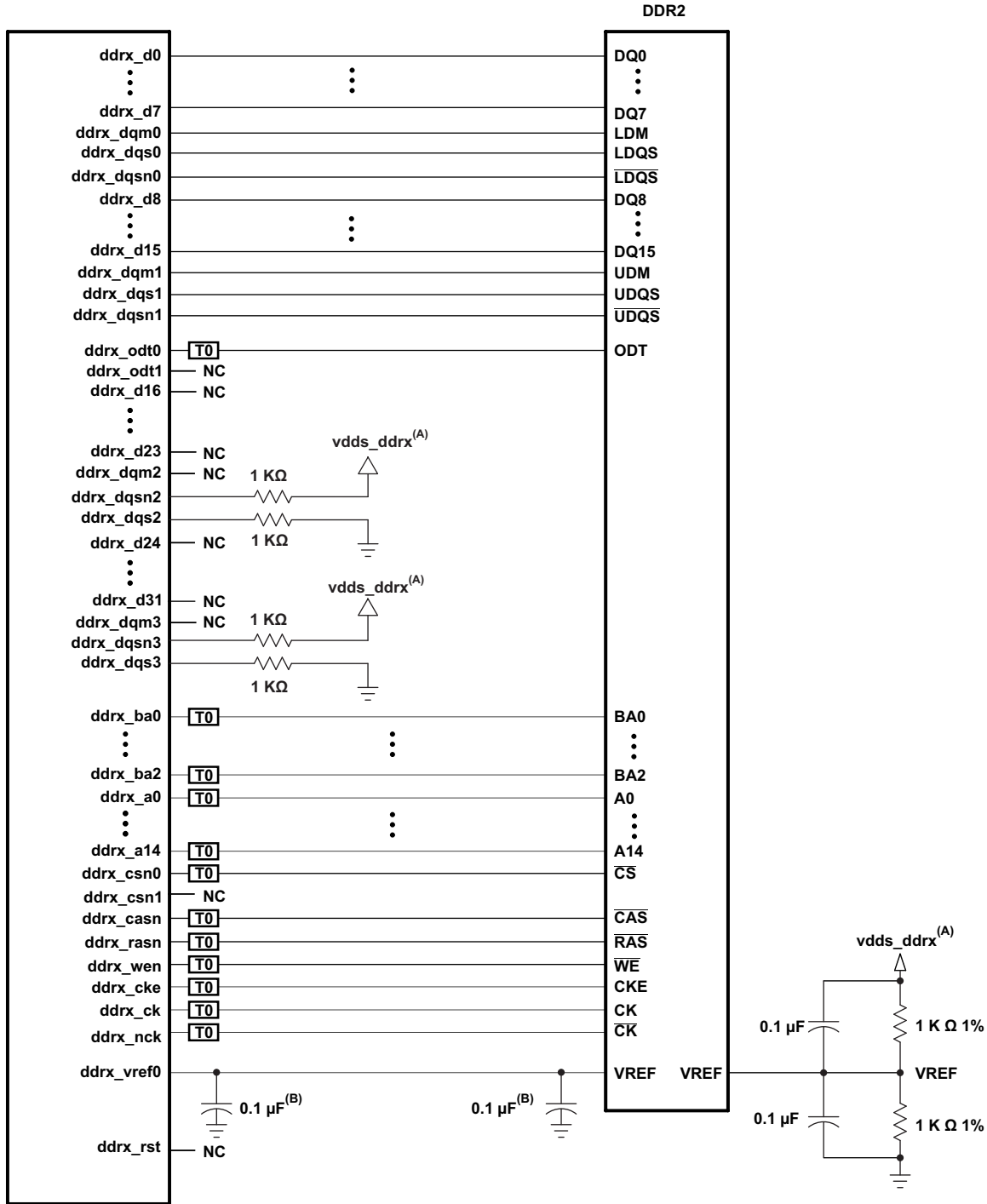


T0 Termination is required. See terminator comments.

PCB_DDR2_1

- A. vdds_ddrx is the power supply for the DDR2 memories and the Device DDR2 interface.
- B. One of these capacitors can be eliminated if the divider and its capacitors are placed near a VREF pin.

Figure 8-47. 32-Bit DDR2 High-Level Schematic



T0 Termination is required. See terminator comments.

PCB_DDR2_2

- A. vdds_ddrx is the power supply for the DDR2 memories and the Device DDR2 interface.
- B. One of these capacitors can be eliminated if the divider and its capacitors are placed near a VREF pin.

Figure 8-48. 16-Bit DDR2 High-Level Schematic

8.7.2.2.2 Compatible JEDEC DDR2 Devices

Table 8-28 shows the parameters of the JEDEC DDR2 devices that are compatible with this interface. Generally, the DDR2 interface is compatible with x16 DDR2-800 speed grade DDR2 devices.

Table 8-28. Compatible JEDEC DDR2 Devices (Per Interface)

NO.	PARAMETER	MIN	MAX	UNIT
CJ21	JEDEC DDR2 device speed grade ⁽¹⁾	DDR2-800		
CJ22	JEDEC DDR2 device bit width	x16	x16	Bits
CJ23	JEDEC DDR2 device count ⁽²⁾	1	2	Devices
CJ24	JEDEC DDR2 device ball count ⁽³⁾	84	92	Balls

(1) Higher DDR2 speed grades are supported due to inherent JEDEC DDR2 backwards compatibility.

(2) One DDR2 device is used for a 16-bit DDR2 memory system. Two DDR2 devices are used for a 32-bit DDR2 memory system.

(3) The 92-ball devices are retained for legacy support. New designs will migrate to 84-ball DDR2 devices. Electrically, the 92- and 84-ball DDR2 devices are the same.

8.7.2.2.3 PCB Stackup

The minimum stackup required for routing the Device is a six-layer stackup as shown in Table 8-29. Additional layers may be added to the PCB stackup to accommodate other circuitry or to reduce the size of the PCB footprint.

Table 8-29. Minimum PCB Stackup

LAYER	TYPE	DESCRIPTION
1	Signal	Top routing mostly horizontal
2	Plane	Ground
3	Plane	Power
4	Signal	Internal routing
5	Plane	Ground
6	Signal	Bottom routing mostly vertical

Complete stackup specifications are provided in [Table 8-30](#).

Table 8-30. PCB Stackup Specifications

NO.	PARAMETER	MIN	TYP	MAX	UNIT
PS21	PCB routing/plane layers	6			
PS22	Signal routing layers	3			
PS23	Full ground reference layers under DDR2 routing region ⁽¹⁾	1			
PS24	Full vdds_ddrx power reference layers under the DDR2 routing region ⁽¹⁾	1			
PS25	Number of reference plane cuts allowed within DDR routing region ⁽²⁾			0	
PS26	Number of layers between DDR2 routing layer and reference plane ⁽³⁾			0	
PS27	PCB routing feature size		4		Mils
PS28	PCB trace width, w		4		Mils
PS29	Single-ended impedance, Z_0	50		75	Ω
PS210	Impedance control ⁽⁵⁾	Z-5	Z	Z+5	Ω

(1) Ground reference layers are preferred over power reference layers. Be sure to include bypass caps to accommodate reference layer return current as the trace routes switch routing layers. A full ground reference layer should be placed adjacent to each DDR routing layer in PCB stack up.

(2) No traces should cross reference plane cuts within the DDR routing region. High-speed signal traces crossing reference plane cuts create large return current paths which can lead to excessive crosstalk and EMI radiation.

(3) Reference planes are to be directly adjacent to the signal plane to minimize the size of the return current loop.

(4) An 18-mil pad assumes Via Channel is the most economical BGA escape. A 20-mil pad may be used if additional layers are available for power routing. An 18-mil pad is required for minimum layer count escape.

(5) Z is the nominal singled-ended impedance selected for the PCB specified by PS29.

8.7.2.2.4 Placement

Figure 8-49 shows the required placement for the Device as well as the DDR2 devices. The dimensions for this figure are defined in Table 8-31. The placement does not restrict the side of the PCB on which the devices are mounted. The ultimate purpose of the placement is to limit the maximum trace lengths and allow for proper routing space. For a 16-bit DDR memory system, the high-word DDR2 device is omitted from the placement.

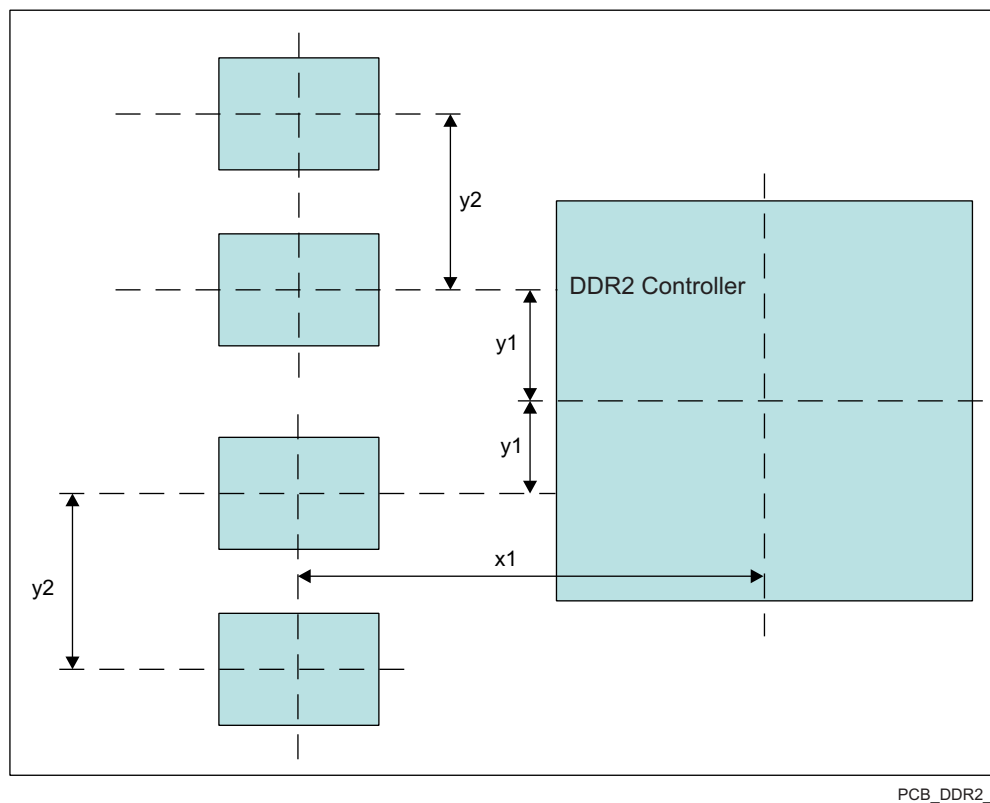


Figure 8-49. Device and DDR2 Device Placement

Table 8-31. Placement Specifications DDR2

NO.	PARAMETER	MIN	MAX	UNIT
KOD21	X1		2000	Mils
KOD22	Y1		500	Mils
KOD23	Y2		1300	Mils
KOD24	DDR2 keepout region ⁽¹⁾			
KOD25	Clearance from non-DDR2 signal to DDR2 keepout region ^{(2) (3)}	4		W

- (1) DDR2 keepout region to encompass entire DDR2 routing area.
- (2) Non-DDR2 signals allowed within DDR2 keepout region provided they are separated from DDR2 routing layers by a ground plane.
- (3) If a device has more than one DDR controller, the signals from the other controller(s) are considered non-DDR2 and should be separated by this specification.

8.7.2.2.5 DDR2 Keepout Region

The region of the PCB used for the DDR2 circuitry must be isolated from other signals. The DDR2 keepout region is defined for this purpose and is shown in [Figure 8-50](#). The size of this region varies with the placement and DDR routing. Additional clearances required for the keepout region are shown in [Table 8-31](#).

The region shown in [Table 8-31](#) should encompass all the DDR2 circuitry and varies depending on placement. Non-DDR2 signals should not be routed on the DDR signal layers within the DDR2 keepout region. Non-DDR2 signals may be routed in the region, provided they are routed on layers separated from DDR2 signal layers by a ground layer. No breaks should be allowed in the reference ground layers in this region. In addition, the vdds_ddrx power plane should cover the entire keepout region. Routes for the two DDR interfaces must be separated by at least 4x; the more separation, the better.

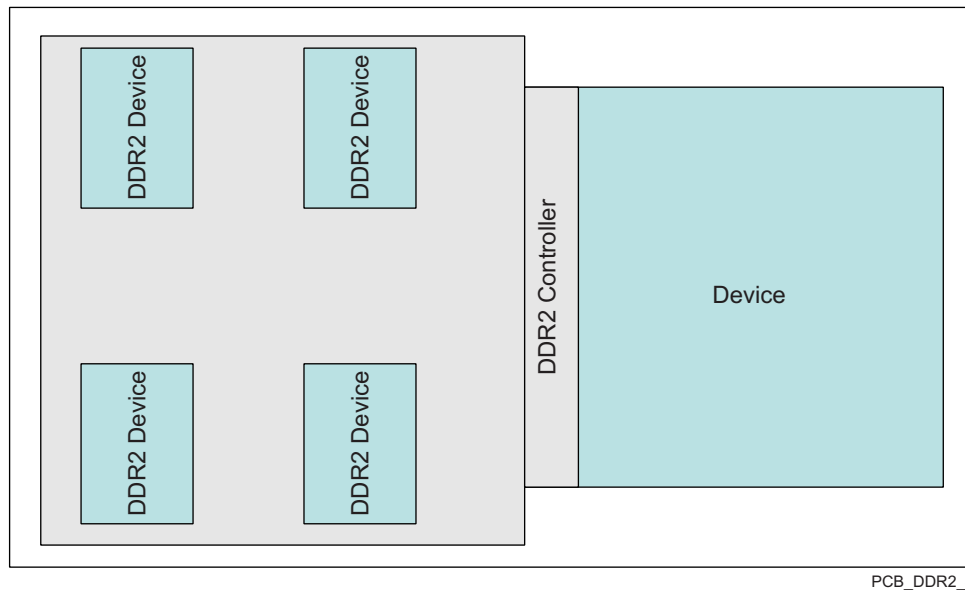


Figure 8-50. DDR2 Keepout Region

8.7.2.2.6 Bulk Bypass Capacitors

Bulk bypass capacitors are required for moderate speed bypassing of the DDR2 and other circuitry. [Table 8-32](#) contains the minimum numbers and capacitance required for the bulk bypass capacitors. Note that this table only covers the bypass needs of the DDR2 interfaces and DDR2 device. Additional bulk bypass capacitance may be needed for other circuitry.

Table 8-32. Bulk Bypass Capacitors

NO.	PARAMETER	MIN	TYP	MAX	UNIT
BC21	vdds_ddrx bulk bypass capacitor ($\geq 1\mu\text{F}$) count ⁽¹⁾		1		Devices
BC22	vdds_ddrx bulk bypass total capacitance		22		μF

(1) These devices should be placed near the devices they are bypassing, but preference should be given to the placement of the high-speed (HS) bypass capacitors and DDR2 signal routing.

8.7.2.2.7 High-Speed Bypass Capacitors

TI recommends that a PDN/power integrity analysis is performed to ensure that capacitor selection and placement is optimal for a given implementation. This section provides guidelines that can serve as a good starting point.

High-speed (HS) bypass capacitors are critical for proper DDR2 interface operation. It is particularly important to minimize the parasitic series inductance of the HS bypass capacitors, processor/DDR power, and processor/DDR ground connections. [Table 8-33](#) contains the specification for the HS bypass capacitors as well as for the power connections on the PCB. Generally speaking, it is good to:

1. Fit as many HS bypass capacitors as possible.
2. HS bypass capacitor value is < 1µF
3. Minimize the distance from the bypass cap to the pins/balls being bypassed.
4. Use the smallest physical sized capacitors possible with the highest capacitance readily available.
5. Connect the bypass capacitor pads to their vias using the widest traces possible and using the largest hole size via possible.
6. Minimize via sharing. Note the limites on via sharing shown in [Table 8-33](#).

Table 8-33. High-Speed Bypass Capacitors

NO.	PARAMETER	MIN	TYP	MAX	UNIT
HS21	HS bypass capacitor package size ⁽¹⁾		0201	0402	10 Mils
HS22	Distance, HS bypass capacitor to processor being bypassed ⁽²⁾⁽³⁾⁽⁴⁾			400 ⁽¹²⁾	Mils
HS23	processor HS bypass capacitor count per vdds_ddrx rail ⁽¹²⁾	See Table 8-3 and ⁽¹¹⁾			Devices
HS24	processor HS bypass capacitor total capacitance per vdds_ddrx rail ⁽¹²⁾	See Table 8-3 and ⁽¹¹⁾			µF
HS25	Number of connection vias for each device power/ground ball ⁽⁵⁾	1			Vias
HS26	Trace length from device power/ground ball to connection via ⁽²⁾		35	70	Mils
HS27	Distance, HS bypass capacitor to DDR device being bypassed ⁽⁶⁾			150	Mils
HS28	Number of connection vias for each HS capacitor ⁽⁸⁾⁽⁹⁾		4 ⁽¹⁴⁾		Vias
HS29	DDR2 device HS bypass capacitor count ⁽⁷⁾		12 ⁽¹³⁾		Devices
HS210	DDR2 device HS bypass capacitor total capacitance ⁽⁷⁾	0.85			µF
HS211	Trace length from bypass capacitor connect to connection via ⁽²⁾⁽⁹⁾		35	100	Mils
HS212	Number of connection vias for each DDR2 device power/ground ball ⁽¹⁰⁾	1			Vias
HS213	Trace length from DDR2 device power/ground ball to connection via ⁽²⁾⁽⁸⁾		35	60	Mils

(1) LxW, 10-mil units, that is, a 0402 is a 40x20-mil surface-mount capacitor.

(2) Closer/shorter is better.

(3) Measured from the nearest processor power/ground ball to the center of the capacitor package.

(4) Three of these capacitors should be located underneath the processor, between the cluster of vdds_ddrx balls and ground balls, between the DDR interfaces on the package.

(5) See the Via Channel™ escape for the processor package.

(6) Measured from the DDR2 device power/ground ball to the center of the capacitor package.

(7) Per DDR2 device.

(8) An additional HS bypass capacitor can share the connection vias only if it is mounted on the opposite side of the board. No sharing of vias is permitted on the same side of the board.

(9) An HS bypass capacitor may share a via with a DDR device mounted on the same side of the PCB. A wide trace should be used for the connection and the length from the capacitor pad to the DDR device pad should be less than 150 mils.

(10) Up to a total of two pairs of DDR power/ground balls may share a via.

(11) The capacitor recommendations in this data manual reflect only the needs of this processor. Please see the memory vendor's guidelines for determining the appropriate decoupling capacitor arrangement for the memory device itself.

(12) For more information, see [Section 8.3, Core Power Domains](#)

(13) For more information refer to DDR2 specification.

(14) Preferred configuration is 4 vias: 2 to power and 2 to ground.

8.7.2.2.8 Net Classes

Table 8-34 lists the clock net classes for the DDR2 interface. Table 8-35 lists the signal net classes, and associated clock net classes, for the signals in the DDR2 interface. These net classes are used for the termination and routing rules that follow.

Table 8-34. Clock Net Class Definitions

CLOCK NET CLASS	PIN NAMES
CK	ddrx_ck / ddrx_nck
DQS0	ddrx_dqs0 / ddrx_dqsn0
DQS1	ddrx_dqs1 / ddrx_dqsn1
DQS2 ⁽¹⁾	ddrx_dqs2 / ddrx_dqsn2
DQS3 ⁽¹⁾	ddrx_dqs3 / ddrx_dqsn3

(1) Only used on 32-bit wide DDR2 memory systems.

Table 8-35. Signal Net Class Definitions

SIGNAL NET CLASS	ASSOCIATED CLOCK NET CLASS	PIN NAMES
ADDR_CTRL	CK	ddrx_ba[2:0], ddrx_a[14:0], ddrx_csnj, ddrx_casn, ddrx_rasn, ddrx_wen, ddrx_cke, ddrx_odti
DQ0	DQS0	ddrx_d[7:0], ddrx_dqm0
DQ1	DQS1	ddrx_d[15:8], ddrx_dqm1
DQ2 ⁽¹⁾	DQS2	ddrx_d[23:16], ddrx_dqm2
DQ3 ⁽¹⁾	DQS3	ddrx_d[31:24], ddrx_dqm3

(1) Only used on 32-bit wide DDR2 memory systems.

8.7.2.2.9 DDR2 Signal Termination

Signal terminators are required in CK and ADDR_CTRL net classes. Serial terminators may be used on data lines to reduce EMI risk; however, serial terminations are the only type permitted. ODTs are integrated on the data byte net classes. They should be enabled to ensure signal integrity. Table 8-36 shows the specifications for the series terminators.

Table 8-36. DDR2 Signal Terminations

NO.	PARAMETER	MIN	TYP	MAX	UNIT
ST21	CK net class ⁽¹⁾⁽²⁾	0		10	Ω
ST22	ADDR_CTRL net class ⁽¹⁾⁽²⁾⁽³⁾⁽⁴⁾	0	22	Z _o	Ω
ST23	Data byte net classes (DQS0-DQS3, DQ0-DQ3) ⁽⁵⁾	0		Z _o	Ω

(1) Only series termination is permitted, parallel or SST specifically disallowed on board.

(2) Only required for EMI reduction.

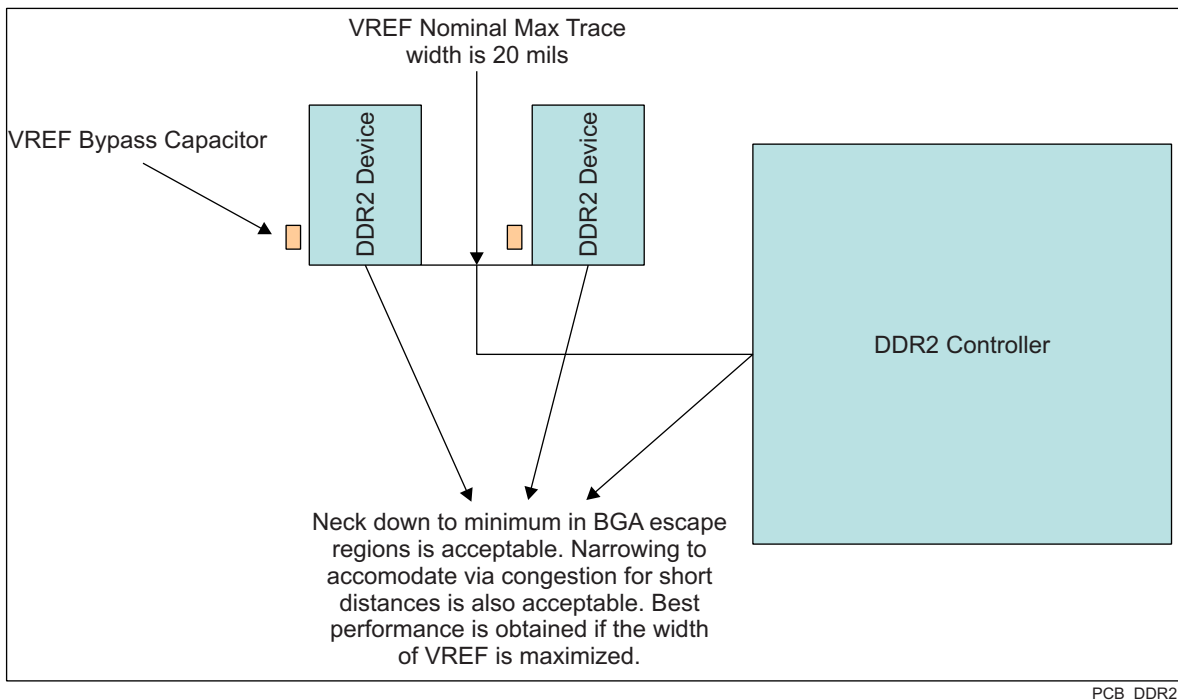
(3) Terminator values larger than typical only recommended to address EMI issues.

(4) Termination value should be uniform across net class.

(5) No external terminations allowed for data byte net classes. ODT is to be used.

8.7.2.2.10 VREF Routing

VREF (ddrx_vref0) is used as a reference by the input buffers of the DDR2 memories as well as the processor. VREF is intended to be half the DDR2 power supply voltage and should be created using a resistive divider as shown in Figure 8-48. Other methods of creating VREF are not recommended. Figure 8-51 shows the layout guidelines for VREF.

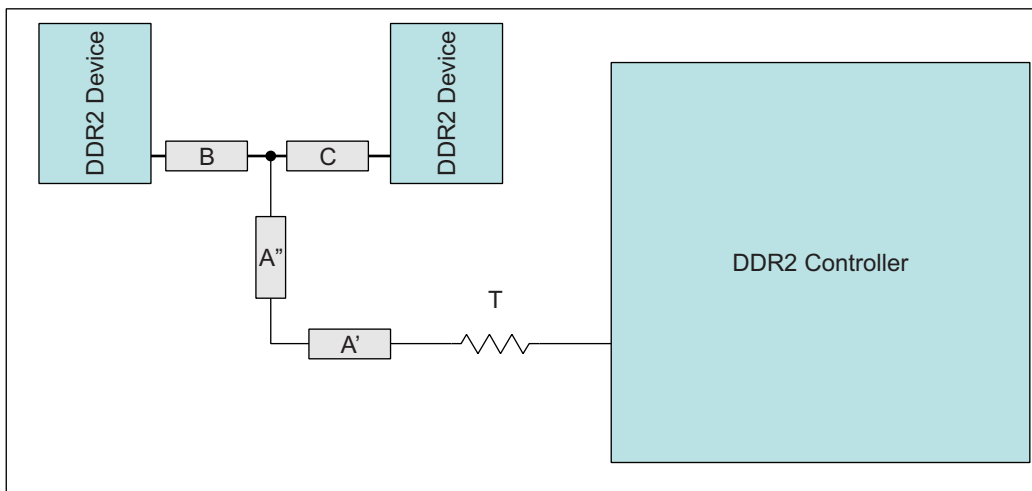


PCB_DDR2_5

Figure 8-51. VREF Routing and Topology

8.7.2.3 DDR2 CK and ADDR_CTRL Routing

Figure 8-52 shows the topology of the routing for the CK and ADDR_CTRL net classes. The route is a balanced T as it is intended that the length of segments B and C be equal. In addition, the length of A = (A'+A'') should be maximized.



PCB_DDR2_6

Figure 8-52. CK and ADDR_CTRL Routing and Topology

Table 8-37. CK and ADDR_CTRL Routing Specification ⁽¹⁾

NO.	PARAMETER	MIN	MAX	UNIT
RSC21	Center-to-center ddrx_ck - ddrx_nck spacing		2w	
RSC22	ddrx_ck / ddrx_nck skew ⁽¹⁾		5	ps
RSC23	CK A-to-B/A-to-C skew mismatch ⁽²⁾		10	ps

Table 8-37. CK and ADDR_CTRL Routing Specification ⁽¹⁾ (continued)

NO.	PARAMETER	MIN	MAX	UNIT
RSC24	CK B-to-C skew mismatch		10	ps
RSC25	Center-to-center CK to other DDR2 trace spacing ⁽³⁾	4w		
RSC26	CK/ADDR_CTRL trace length ⁽⁴⁾		680	ps
RSC27	ADDR_CTRL-to-CK skew mismatch		25	ps
RSC28	ADDR_CTRL-to-ADDR_CTRL skew mismatch		25	ps
RSC29	Center-to-center ADDR_CTRL to other DDR2 trace spacing ⁽³⁾	4w		
RSC210	Center-to-center ADDR_CTRL to other ADDR_CTRL trace spacing ⁽³⁾	3w		
RSC211	ADDR_CTRL A-to-B/A-to-C skew mismatch ⁽²⁾		25	ps
RSC212	ADDR_CTRL B-to-C skew mismatch		25	ps

(1) The length of segment A = A' + A'' as shown in [Figure 8-52](#).

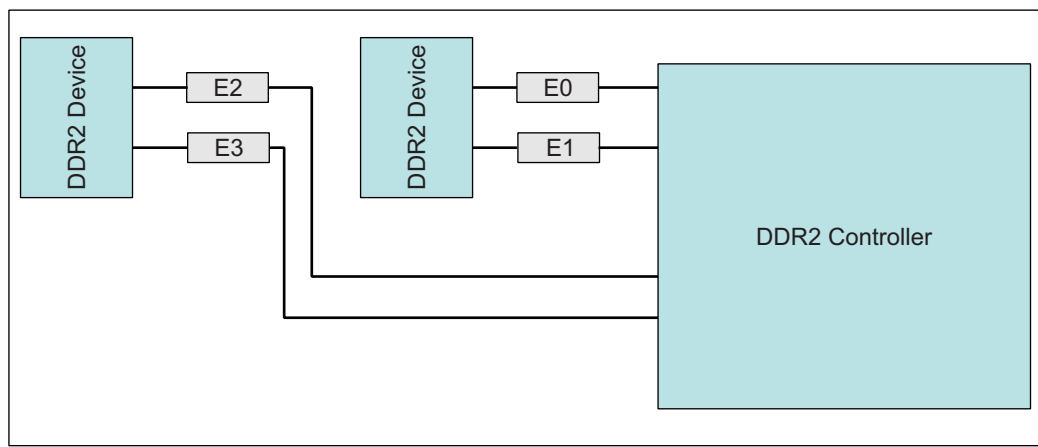
(2) Series terminator, if used, should be located closest to the Device.

(3) Center-to-center spacing is allowed to fall to minimum 2w for up to 500 mils of routed length to accommodate BGA escape and routing congestion.

(4) This is the longest routing length of the CK and ADDR_CTRL net classes.

(5) Length of A should be maximized.

[Figure 8-53](#) shows the topology and routing for the DQS and DQ net classes; the routes are point to point. Skew matching across bytes is not needed nor recommended.



PCB_DDR2_7

Figure 8-53. DQS and DQ Routing and Topology**Table 8-38. DQS and DQ Routing Specification**

NO.	PARAMETER	MIN	MAX	UNIT
RSDQ21	Center-to-center DQS-DQSn spacing in E0 E1 E2 E3	2w		
RSDQ22	DQS-DQSn skew in E0 E1 E2 E3		5	ps
RSDQ23	Center-to-center DQS to other DDR2 trace spacing ⁽¹⁾	4w		
RSDQ24	DQS/DQ trace length ⁽²⁾⁽³⁾⁽⁴⁾		325	ps
RSDQ25	DQ-to-DQS skew mismatch ⁽²⁾⁽³⁾⁽⁴⁾		10	ps
RSDQ26	DQ-to-DQ skew mismatch ⁽²⁾⁽³⁾⁽⁴⁾		10	ps
RSDQ27	DQ-to-DQ/DQS via count mismatch ⁽²⁾⁽³⁾⁽⁴⁾		1	Vias
RSDQ28	Center-to-center DQ to other DDR2 trace spacing ⁽¹⁾⁽⁵⁾	4w		
RSDQ29	Center-to-center DQ to other DQ trace spacing ⁽¹⁾⁽⁶⁾⁽⁷⁾	3w		
RSDQ210	DQ/DQS E skew mismatch ⁽²⁾⁽³⁾⁽⁴⁾		25	ps

- (1) Center-to-center spacing is allowed to fall to minimum 2w for up to 500 mils of routed length to accommodate BGA escape and routing congestion.
- (2) A 16-bit DDR memory system has two sets of data net classes; one for data byte 0, and one for data byte 1, each with an associated DQS (2 DQSs) per DDR EMIF used.
- (3) A 32-bit DDR memory system has four sets of data net classes; one each for data bytes 0 through 3, and each associated with a DQS (4 DQSs) per DDR EMIF used.
- (4) There is no need, and it is not recommended, to skew match across data bytes; that is, from DQS0 and data byte 0 to DQS1 and data byte 1.
- (5) DQs from other DQS domains are considered *other DDR2 trace*.
- (6) DQs from other data bytes are considered *other DDR2 trace*.
- (7) This is the longest routing distance of each of the DQS and DQ net classes.

8.7.3 DDR3 Board Design and Layout Guidelines

8.7.3.1 Board Designs

TI only supports board designs using DDR3 memory that follow the guidelines in this document. The switching characteristics and timing diagram for the DDR3 memory controller are shown in [Table 8-39](#) and [Figure 8-54](#).

Table 8-39. Switching Characteristics Over Recommended Operating Conditions for DDR3 Memory Controller

NO.	PARAMETER		-1G		UNIT
			MIN	MAX	
1	t _{c(DDR_CLK)}	Cycle time, DDR_CLK	1.875	2.5 ⁽¹⁾	ns

(1) This is the absolute maximum the clock period can be. Actual maximum clock period may be limited by DDR3 speed grade and operating frequency (see the DDR3 memory device data sheet).

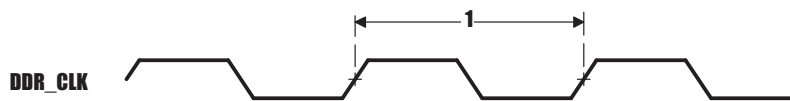


Figure 8-54. DDR3 Memory Controller Clock Timing

8.7.3.1.1 DDR3 versus DDR2

This specification only covers device PCB designs that use DDR3 memory. Designs using DDR2 memory should use the PCB design specifications for DDR2 memory. While similar, the two memory systems have different requirements. It is currently not possible to design one PCB that covers both DDR2 and DDR3.

8.7.3.2 DDR3 EMIFs

The processor contains two separate DDR3 EMIFs. This specification covers one of these EMIFs (ddr1_*) and, thus, needs to be implemented twice, once for each EMIF. The PCB layout generally turns out to be a semi-mirror with ddr2_* being a flipped version of ddr1_*; the only exception being the DDR3 devices themselves are not flipped unless mounted on opposite sides of the PCB. Requirements are identical between the two EMIFs.

8.7.3.3 DDR3 Device Combinations

Because there are several possible combinations of device counts and single- or dual-side mounting, [Table 8-40](#) summarizes the supported device configurations.

Table 8-40. Supported DDR3 Device Combinations⁽¹⁾

NUMBER OF DDR3 DEVICES	DDR3 DEVICE WIDTH (BITS)	MIRRORED?	DDR3 EMIF WIDTH (BITS)
1	16	N	16
2	8	Y ⁽²⁾	16

Table 8-40. Supported DDR3 Device Combinations⁽¹⁾ (continued)

NUMBER OF DDR3 DEVICES	DDR3 DEVICE WIDTH (BITS)	MIRRORED?	DDR3 EMIF WIDTH (BITS)
2	16	N	32
2	16	Y ⁽²⁾	32
3	16	N	32
4	8	N	32
4	8	Y ⁽³⁾	32
5	8	N	32

(1) This table is per EMIF.

(2) Two DDR3 devices are mirrored when one device is placed on the top of the board and the second device is placed on the bottom of the board.

(3) This is two mirrored pairs of DDR3 devices.

8.7.3.4 DDR3 Interface Schematic

8.7.3.4.1 32-Bit DDR3 Interface

The DDR3 interface schematic varies, depending upon the width of the DDR3 devices used and the width of the bus used (16 or 32 bits). General connectivity is straightforward and very similar. 16-bit DDR devices look like two 8-bit devices. [Figure 8-55](#) and [Figure 8-56](#) show the schematic connections for 32-bit interfaces using x16 devices.

8.7.3.4.2 16-Bit DDR3 Interface

Note that the 16-bit wide interface schematic is practically identical to the 32-bit interface (see [Figure 8-55](#) and [Figure 8-56](#)); only the high-word DDR memories are removed and the unused DQS inputs are tied off.

When not using all or part of a DDR interface, the proper method of handling the unused pins is to tie off the `ddrx_dqsi` pins to ground via a 1k-Ω resistor, and to tie off the `ddrx_dqsn` pins to the corresponding `vdds_ddrx` supply via a 1k-Ω resistor. This needs to be done for each byte not used. Although these signals have internal pullups and pulldowns, external pullups and pulldowns provide additional protection against external electrical noise causing activity on the signals.

The `vdds_ddrx` and `ddrx_vref0` power supply pins need to be connected to their respective power supplies even if `ddrx` is not being used. All other DDR interface pins can be left unconnected. Note that the supported modes for use of the DDR EMIF are 32-bits wide, 16-bits wide, or not used.

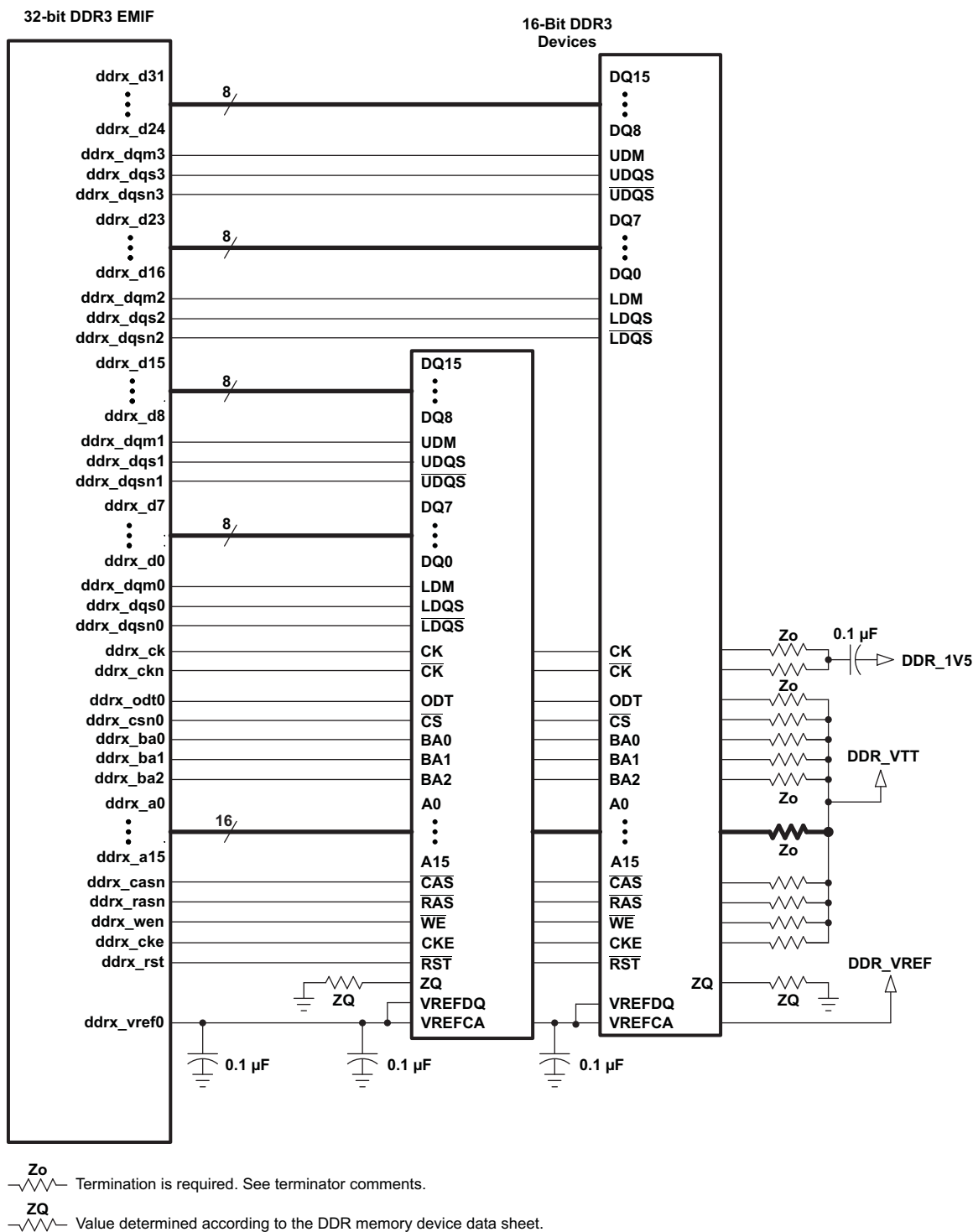
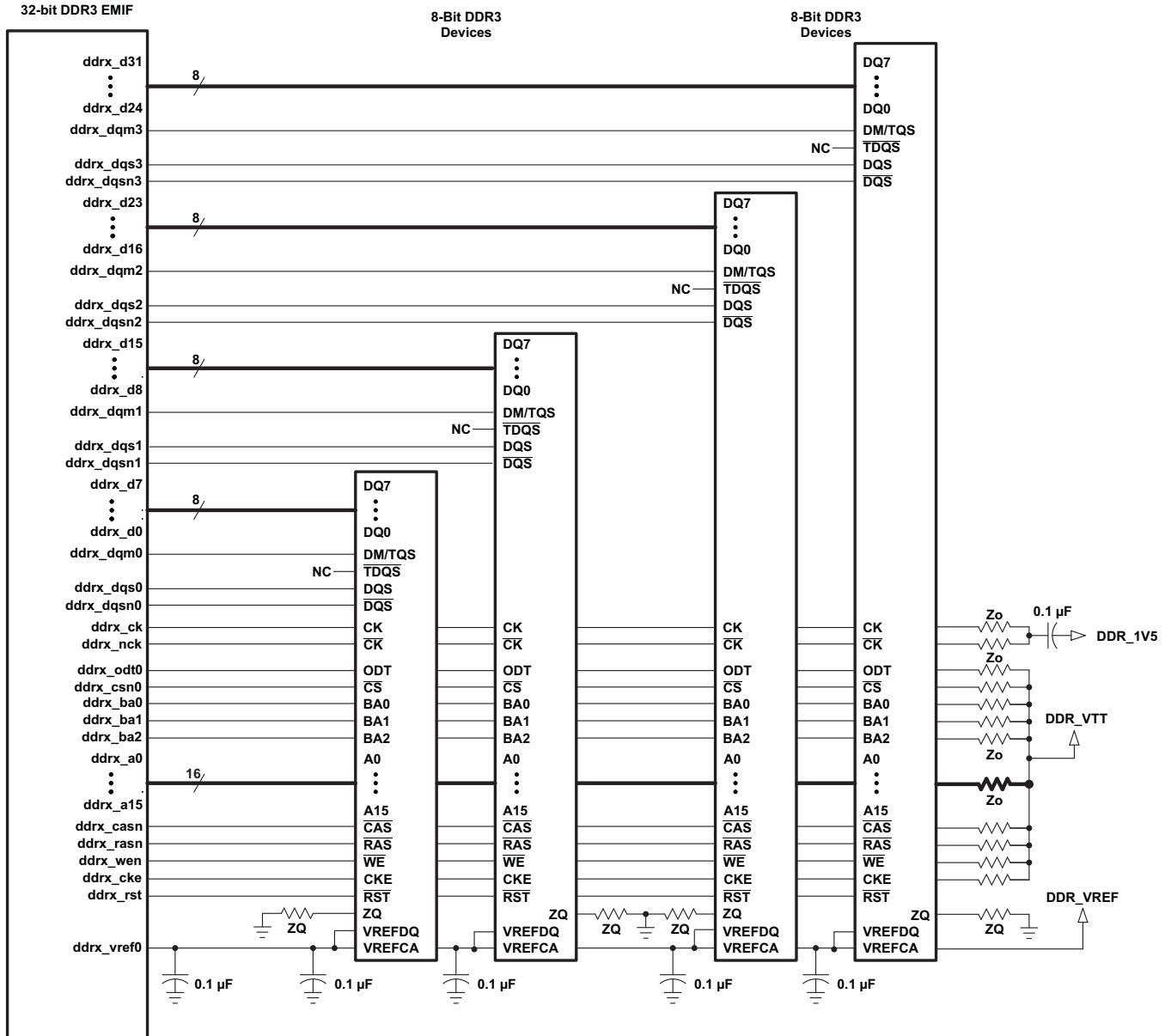


Figure 8-55. 32-Bit, One-Bank DDR3 Interface Schematic Using Two 16-Bit DDR3 Devices



Z_o Termination is required. See terminator comments.
 Z_Q Value determined according to the DDR memory device data sheet.

Figure 8-56. 32-Bit, One-Bank DDR3 Interface Schematic Using Four 8-Bit DDR3 Devices

8.7.3.5 Compatible JEDEC DDR3 Devices

Table 8-41 shows the parameters of the JEDEC DDR3 devices that are compatible with this interface. Generally, the DDR3 interface is compatible with DDR3-1066 devices in the x8 or x16 widths.

Table 8-41. Compatible JEDEC DDR3 Devices (Per Interface)

N O.	PARAMETER	CONDITION	MIN	MAX	UNIT
1	JEDEC DDR3 device speed grade ⁽¹⁾	DDR clock rate = 400MHz	DDR3-800	DDR3-1600	
		400MHz < DDR clock rate ≤ 533MHz	DDR3-1066	DDR3-1600	
2	JEDEC DDR3 device bit width		x8	x16	Bits
3	JEDEC DDR3 device count ⁽²⁾		2	4	Devices

(1) Refer to Table 8-39 Switching Characteristics Over Recommended Operating Conditions for DDR3 Memory Controller for the range of supported DDR clock rates.

(2) For valid DDR3 device configurations and device counts, see Section 8.7.3.4, Figure 8-55, and Figure 8-56.

8.7.3.6 PCB Stackup

The minimum stackup for routing the DDR3 interface is a six-layer stack up as shown in Table 8-42. Additional layers may be added to the PCB stackup to accommodate other circuitry, enhance SI/EMI performance, or to reduce the size of the PCB footprint. Complete stackup specifications are provided in Table 8-43.

Table 8-42. Six-Layer PCB Stackup Suggestion

LAYER	TYPE	DESCRIPTION
1	Signal	Top routing mostly vertical
2	Plane	Ground
3	Plane	Split power plane
4	Plane	Split power plane or Internal routing
5	Plane	Ground
6	Signal	Bottom routing mostly horizontal

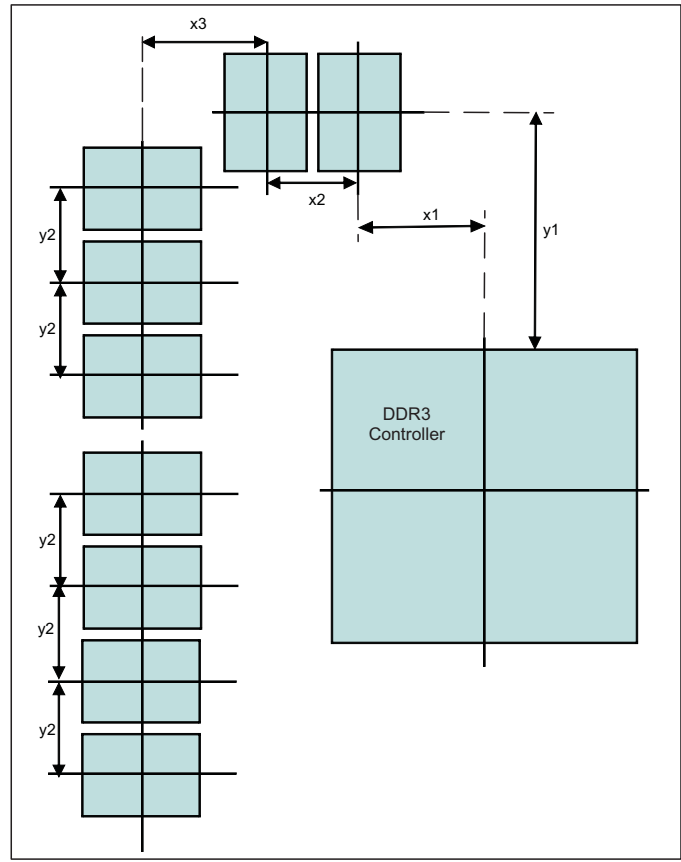
Table 8-43. PCB Stackup Specifications

NO.	PARAMETER	MIN	TYP	MAX	UNIT
PS1	PCB routing/plane layers	6			
PS2	Signal routing layers	3			
PS3	Full ground reference layers under DDR3 routing region ⁽¹⁾	1			
PS4	Full 1.5-V power reference layers under the DDR3 routing region ⁽¹⁾	1			
PS5	Number of reference plane cuts allowed within DDR routing region ⁽²⁾			0	
PS6	Number of layers between DDR3 routing layer and reference plane ⁽³⁾			0	
PS7	PCB routing feature size		4		Mils
PS8	PCB trace width, w		4		Mils
PS9	Single-ended impedance, Z ₀	50		75	Ω
PS10	Impedance control ⁽⁵⁾	Z-5	Z	Z+5	Ω

- (1) Ground reference layers are preferred over power reference layers. Be sure to include bypass caps to accommodate reference layer return current as the trace routes switch routing layers.
- (2) No traces should cross reference plane cuts within the DDR routing region. High-speed signal traces crossing reference plane cuts create large return current paths which can lead to excessive crosstalk and EMI radiation.
- (3) Reference planes are to be directly adjacent to the signal plane to minimize the size of the return current loop.
- (4) An 18-mil pad assumes Via Channel is the most economical BGA escape. A 20-mil pad may be used if additional layers are available for power routing. An 18-mil pad is required for minimum layer count escape.
- (5) Z is the nominal singled-ended impedance selected for the PCB specified by PS9.

8.7.3.7 Placement

Figure 8-57 shows the required placement for the processor as well as the DDR3 devices. The dimensions for this figure are defined in Table 8-44. The placement does not restrict the side of the PCB on which the devices are mounted. The ultimate purpose of the placement is to limit the maximum trace lengths and allow for proper routing space. For a 16-bit DDR memory system, the high-word DDR3 devices are omitted from the placement.



PCB_DDR3_3

Figure 8-57. Placement Specifications

Table 8-44. Placement Specifications DDR3

NO.	PARAMETER	MIN	MAX	UNIT
KOD31	X1		500	Mils
KOD32	X2		600	Mils
KOD33	X3		600	Mils
KOD34	Y1		1800	Mils
KOD35	Y2		600	Mils
KOD36	DDR3 keepout region ⁽¹⁾			
KOD37	Clearance from non-DDR3 signal to DDR3 keepout region ^{(2) (3)}	4		W

- (1) DDR3 keepout region to encompass entire DDR3 routing area.
- (2) Non-DDR3 signals allowed within DDR3 keepout region provided they are separated from DDR3 routing layers by a ground plane.
- (3) If a device has more than one DDR controller, the signals from the other controller(s) are considered non-DDR3 and should be separated by this specification.

8.7.3.8 DDR3 Keepout Region

The region of the PCB used for DDR3 circuitry must be isolated from other signals. The DDR3 keepout region is defined for this purpose and is shown in [Figure 8-58](#). The size of this region varies with the placement and DDR routing. Additional clearances required for the keepout region are shown in [Table 8-44](#). Non-DDR3 signals should not be routed on the DDR signal layers within the DDR3 keepout region. Non-DDR3 signals may be routed in the region, provided they are routed on layers separated from the DDR signal layers by a ground layer. No breaks should be allowed in the reference ground layers in this region. In addition, the 1.5-V DDR3 power plane should cover the entire keepout region. Also note that the two signals from the DDR3 controller should be separated from each other by the specification in [Table 8-44](#), (see [KOD37](#)).

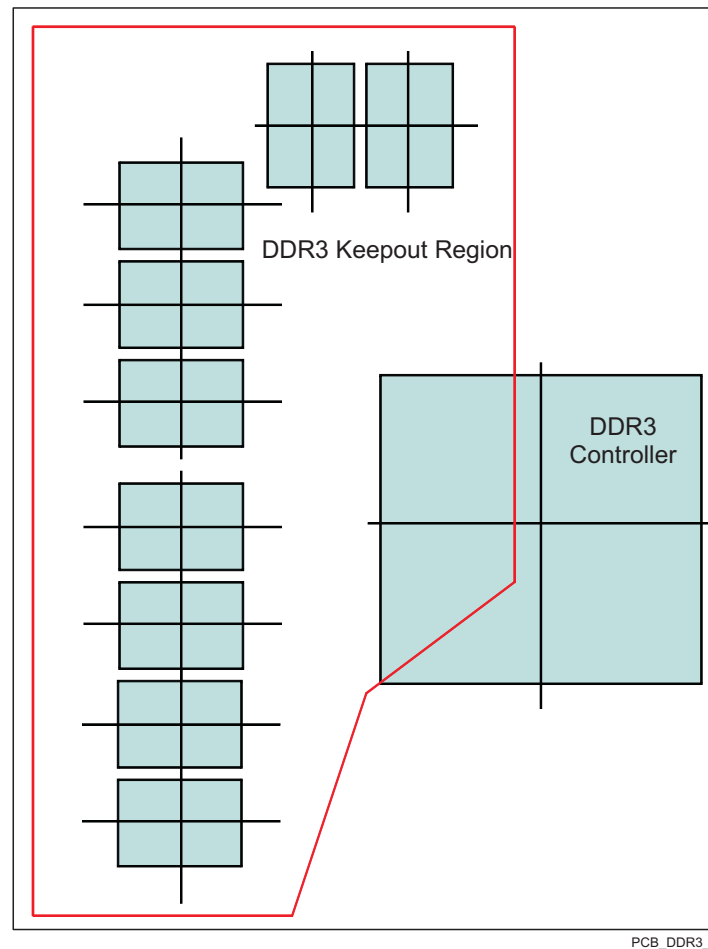


Figure 8-58. DDR3 Keepout Region

8.7.3.9 Bulk Bypass Capacitors

Bulk bypass capacitors are required for moderate speed bypassing of the DDR3 and other circuitry. [Table 8-45](#) contains the minimum numbers and capacitance required for the bulk bypass capacitors. Note that this table only covers the bypass needs of the DDR3 controllers and DDR3 devices. Additional bulk bypass capacitance may be needed for other circuitry.

Table 8-45. Bulk Bypass Capacitors

NO.	PARAMETER	MIN	MAX	UNIT
1	vdds_ddrx bulk bypass capacitor count ⁽¹⁾	1		Devices
2	vdds_ddrx bulk bypass total capacitance	22		μF

(1) These devices should be placed near the devices they are bypassing, but preference should be given to the placement of the high-speed (HS) bypass capacitors and DDR3 signal routing.

8.7.3.10 High-Speed Bypass Capacitors

High-speed (HS) bypass capacitors are critical for proper DDR3 interface operation. It is particularly important to minimize the parasitic series inductance of the HS bypass capacitors, processor/DDR power, and processor/DDR ground connections. [Table 8-46](#) contains the specification for the HS bypass capacitors as well as for the power connections on the PCB. Generally speaking, it is good to:

1. Fit as many HS bypass capacitors as possible.
2. Minimize the distance from the bypass cap to the pins/balls being bypassed.
3. Use the smallest physical sized capacitors possible with the highest capacitance readily available.
4. Connect the bypass capacitor pads to their vias using the widest traces possible and using the largest hole size via possible.
5. Minimize via sharing. Note the limites on via sharing shown in [Table 8-46](#).

Table 8-46. High-Speed Bypass Capacitors

NO.	PARAMETER	MIN	TYP	MAX	UNIT
1	HS bypass capacitor package size ⁽¹⁾		0201	0402	10 Mils
2	Distance, HS bypass capacitor to processor being bypassed ⁽²⁾⁽³⁾⁽⁴⁾			400	Mils
3	processor HS bypass capacitor count per vdds_ddrx rail ⁽¹²⁾		See Table 8-3 and ⁽¹¹⁾		Devices
4	processor HS bypass capacitor total capacitance per vdds_ddrx rail ⁽¹²⁾		See Table 8-3 and ⁽¹¹⁾		μF
5	Number of connection vias for each device power/ground ball ⁽⁵⁾				Vias
6	Trace length from device power/ground ball to connection via ⁽²⁾		35	70	Mils
7	Distance, HS bypass capacitor to DDR device being bypassed ⁽⁶⁾			150	Mils
8	DDR3 device HS bypass capacitor count ⁽⁷⁾	12			Devices
9	DDR3 device HS bypass capacitor total capacitance ⁽⁷⁾	0.85			μF
10	Number of connection vias for each HS capacitor ⁽⁸⁾⁽⁹⁾	2			Vias
11	Trace length from bypass capacitor connect to connection via ⁽²⁾⁽⁹⁾		35	100	Mils
12	Number of connection vias for each DDR3 device power/ground ball ⁽¹⁰⁾	1			Vias
13	Trace length from DDR3 device power/ground ball to connection via ⁽²⁾⁽⁸⁾		35	60	Mils

(1) LxW, 10-mil units, that is, a 0402 is a 40x20-mil surface-mount capacitor.

(2) Closer/shorter is better.

(3) Measured from the nearest processor power/ground ball to the center of the capacitor package.

(4) Three of these capacitors should be located underneath the processor, between the cluster of DDR_1V5 balls and ground balls, between the DDR interfaces on the package.

(5) See the Via Channel™ escape for the processor package.

(6) Measured from the DDR3 device power/ground ball to the center of the capacitor package.

(7) Per DDR3 device.

(8) An additional HS bypass capacitor can share the connection vias only if it is mounted on the opposite side of the board. No sharing of vias is permitted on the same side of the board.

(9) An HS bypass capacitor may share a via with a DDR device mounted on the same side of the PCB. A wide trace should be used for the connection and the length from the capacitor pad to the DDR device pad should be less than 150 mils.

(10) Up to a total of two pairs of DDR power/ground balls may share a via.

(11) The capacitor recommendations in this data manual reflect only the needs of this processor. Please see the memory vendor's guidelines for determining the appropriate decoupling capacitor arrangement for the memory device itself.

(12) For more information, see [Section 8.3, Core Power Domains](#)

8.7.3.10.1 Return Current Bypass Capacitors

Use additional bypass capacitors if the return current reference plane changes due to DDR3 signals hopping from one signal layer to another. The bypass capacitor here provides a path for the return current to hop planes along with the signal. As many of these return current bypass capacitors should be used as possible. Because these are returns for signal current, the signal via size may be used for these capacitors.

8.7.3.11 Net Classes

Table 8-47 lists the clock net classes for the DDR3 interface. Table 8-48 lists the signal net classes, and associated clock net classes, for signals in the DDR3 interface. These net classes are used for the termination and routing rules that follow.

Table 8-47. Clock Net Class Definitions

CLOCK NET CLASS	processor PIN NAMES
CK	ddrx_ck/ddrx_nck
DQS0	ddrx_dqs0 / ddrx_dqsn0
DQS1	ddrx_dqs1 / ddrx_dqsn1
DQS2 ⁽¹⁾	ddrx_dqs2 / ddrx_dqsn2
DQS3 ⁽¹⁾	ddrx_dqs3 / ddrx_dqsn3

(1) Only used on 32-bit wide DDR3 memory systems.

Table 8-48. Signal Net Class Definitions

SIGNAL NET CLASS	ASSOCIATED CLOCK NET CLASS	processor PIN NAMES
ADDR_CTRL	CK	ddrx_ba[2:0], ddrx_a[14:0], ddrx_csnj, ddrx_casn, ddrx_rasn, ddrx_wen, ddrx_cke, ddrx_odti
DQ0	DQS0	ddrx_d[7:0], ddrx_dqm0
DQ1	DQS1	ddrx_d[15:8], ddrx_dqm1
DQ2 ⁽¹⁾	DQS2	ddrx_d[23:16], ddrx_dqm2
DQ3 ⁽¹⁾	DQS3	ddrx_d[31:24], ddrx_dqm3

(1) Only used on 32-bit wide DDR3 memory systems.

8.7.3.12 DDR3 Signal Termination

Signal terminators are required for the CK and ADDR_CTRL net classes. The data lines are terminated by ODT and, thus, the PCB traces should be unterminated. Detailed termination specifications are covered in the routing rules in the following sections.

8.7.3.13 VREF_DDR Routing

ddrx_vref0 (VREF) is used as a reference by the input buffers of the DDR3 memories as well as the processor. VREF is intended to be half the DDR3 power supply voltage and is typically generated with the DDR3 VDD5 and VTT power supply. It should be routed as a nominal 20-mil wide trace with 0.1 μ F bypass capacitors near each device connection. Narrowing of VREF is allowed to accommodate routing congestion.

8.7.3.14 VTT

Like VREF, the nominal value of the VTT supply is half the DDR3 supply voltage. Unlike VREF, VTT is expected to source and sink current, specifically the termination current for the ADDR_CTRL net class Thevenin terminators. VTT is needed at the end of the address bus and it should be routed as a power sub-plane. VTT should be bypassed near the terminator resistors.

8.7.3.15 CK and ADDR_CTRL Topologies and Routing Definition

The CK and ADDR_CTRL net classes are routed similarly and are length matched to minimize skew between them. CK is a bit more complicated because it runs at a higher transition rate and is differential. The following subsections show the topology and routing for various DDR3 configurations for CK and ADDR_CTRL. The figures in the following subsections define the terms for the routing specification detailed in [Table 8-49](#).

8.7.3.15.1 Four DDR3 Devices

Four DDR3 devices are supported on the DDR EMIF consisting of four x8 DDR3 devices arranged as one bank (CS). These four devices may be mounted on a single side of the PCB, or may be mirrored in two pairs to save board space at a cost of increased routing complexity and parts on the backside of the PCB.

8.7.3.15.1.1 CK and ADDR_CTRL Topologies, Four DDR3 Devices

[Figure 8-59](#) shows the topology of the CK net classes and [Figure 8-60](#) shows the topology for the corresponding ADDR_CTRL net classes.

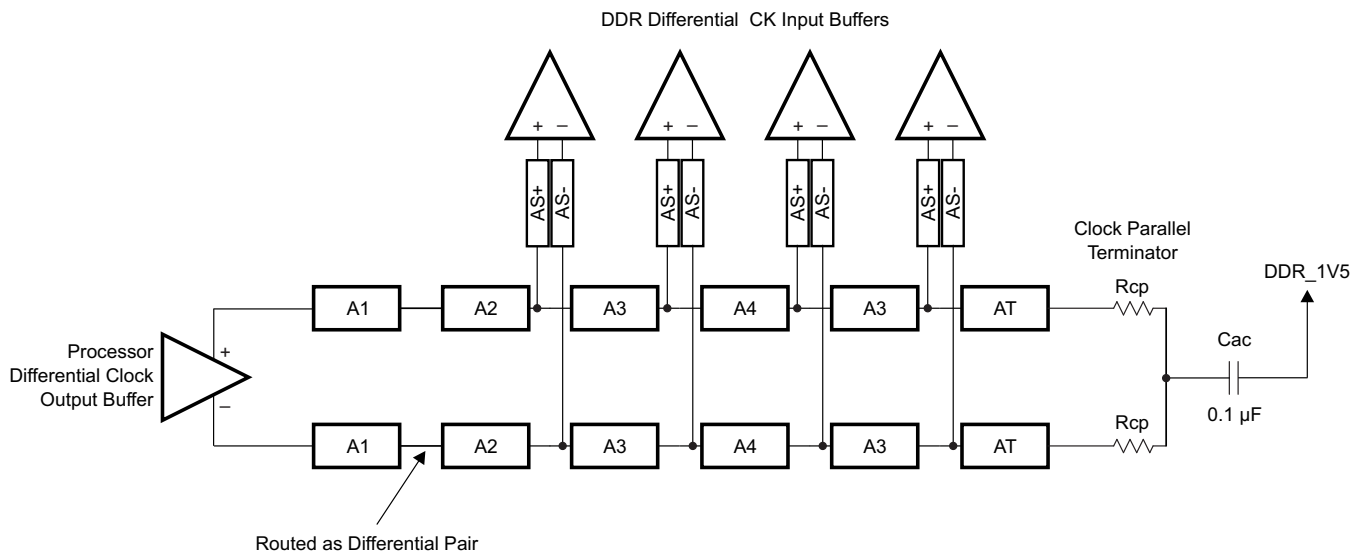


Figure 8-59. CK Topology for Four x8 DDR3 Devices

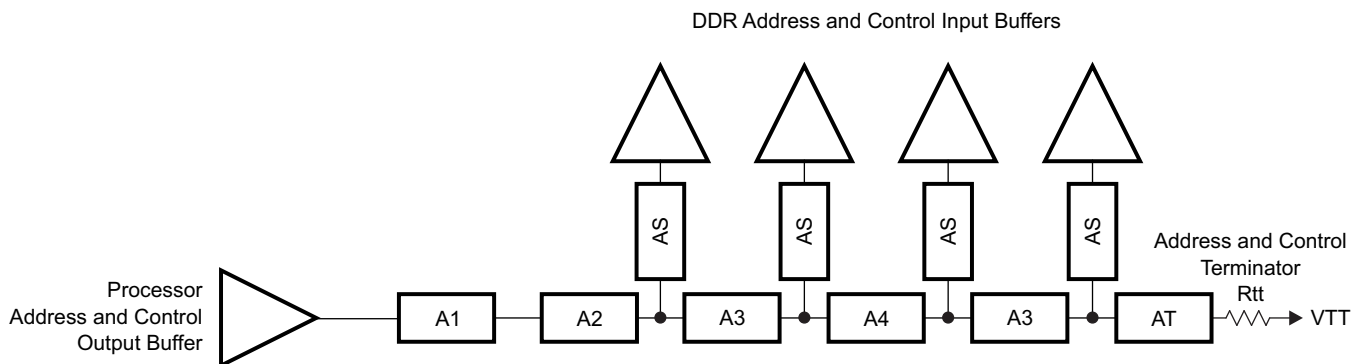


Figure 8-60. ADDR_CTRL Topology for Four x8 DDR3 Devices

8.7.3.15.1.2 CK and ADDR_CTRL Routing, Four DDR3 Devices

[Figure 8-61](#) shows the CK routing for four DDR3 devices placed on the same side of the PCB. [Figure 8-62](#) shows the corresponding ADDR_CTRL routing.

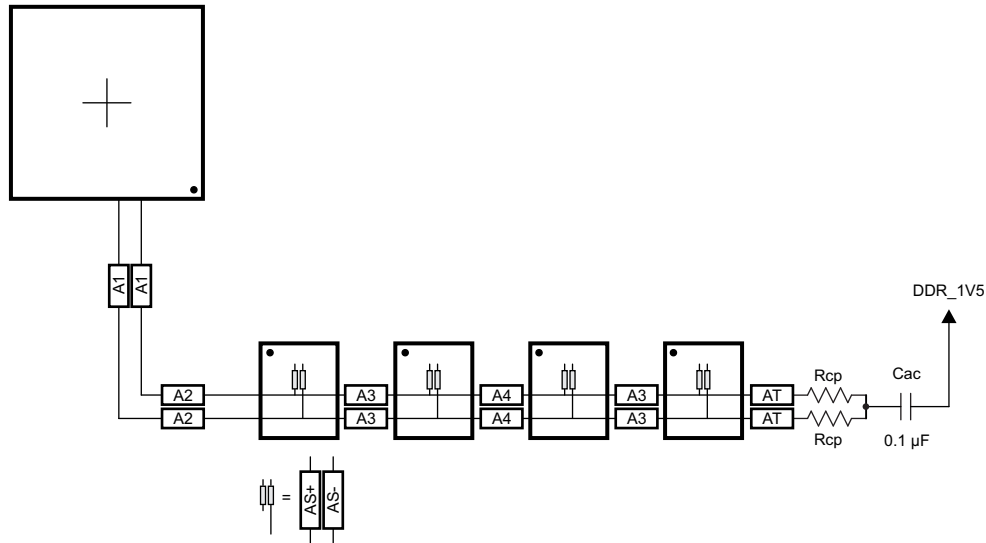


Figure 8-61. CK Routing for Four Single-Side DDR3 Devices

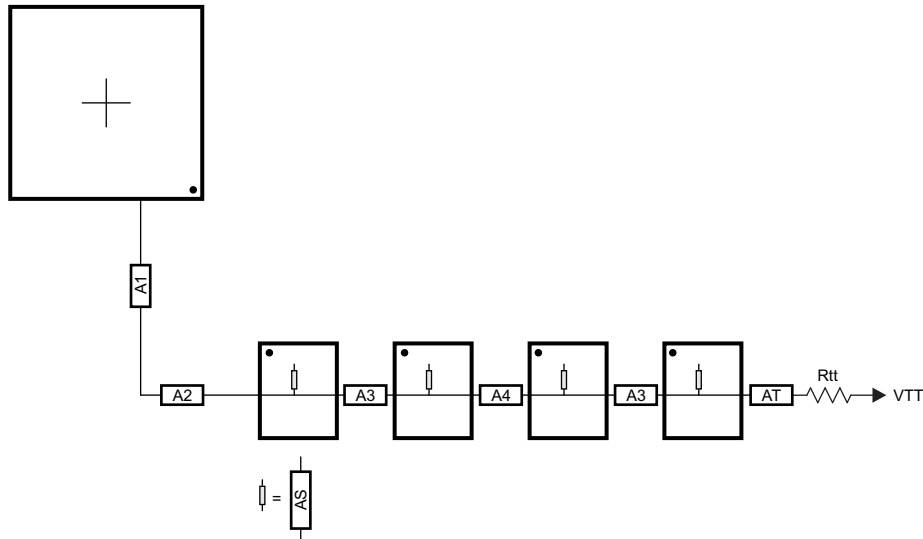


Figure 8-62. ADDR_CTRL Routing for Four Single-Side DDR3 Devices

To save PCB space, the four DDR3 memories may be mounted as two mirrored pairs at a cost of increased routing and assembly complexity. [Figure 8-63](#) and [Figure 8-64](#) show the routing for CK and ADDR_CTRL, respectively, for four DDR3 devices mirrored in a two-pair configuration.

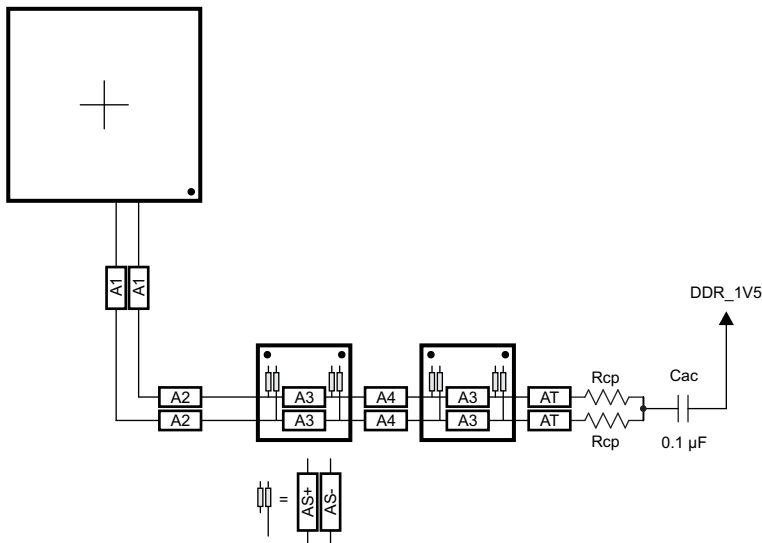


Figure 8-63. CK Routing for Four Mirrored DDR3 Devices

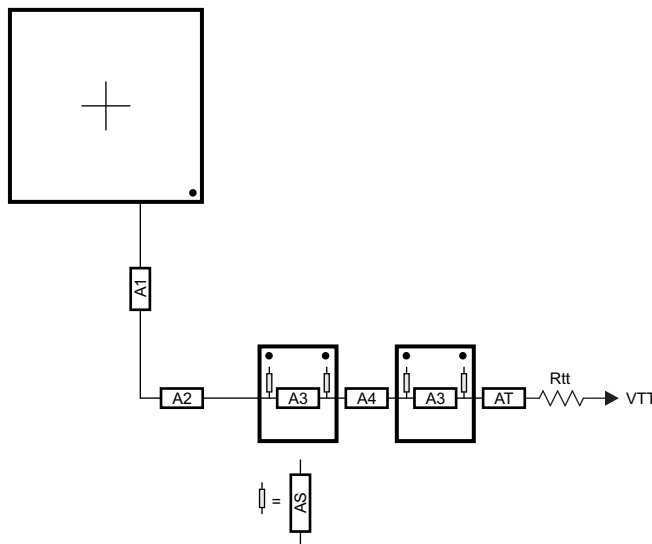


Figure 8-64. ADDR_CTRL Routing for Four Mirrored DDR3 Devices

8.7.3.15.2 Two DDR3 Devices

Two DDR3 devices are supported on the DDR EMIF consisting of two x8 DDR3 devices arranged as one bank (CS), 16 bits wide, or two x16 DDR3 devices arranged as one bank (CS), 32 bits wide. These two devices may be mounted on a single side of the PCB, or may be mirrored in a pair to save board space at a cost of increased routing complexity and parts on the backside of the PCB.

8.7.3.15.2.1 CK and ADDR_CTRL Topologies, Two DDR3 Devices

Figure 8-65 shows the topology of the CK net classes and Figure 8-66 shows the topology for the corresponding ADDR_CTRL net classes.

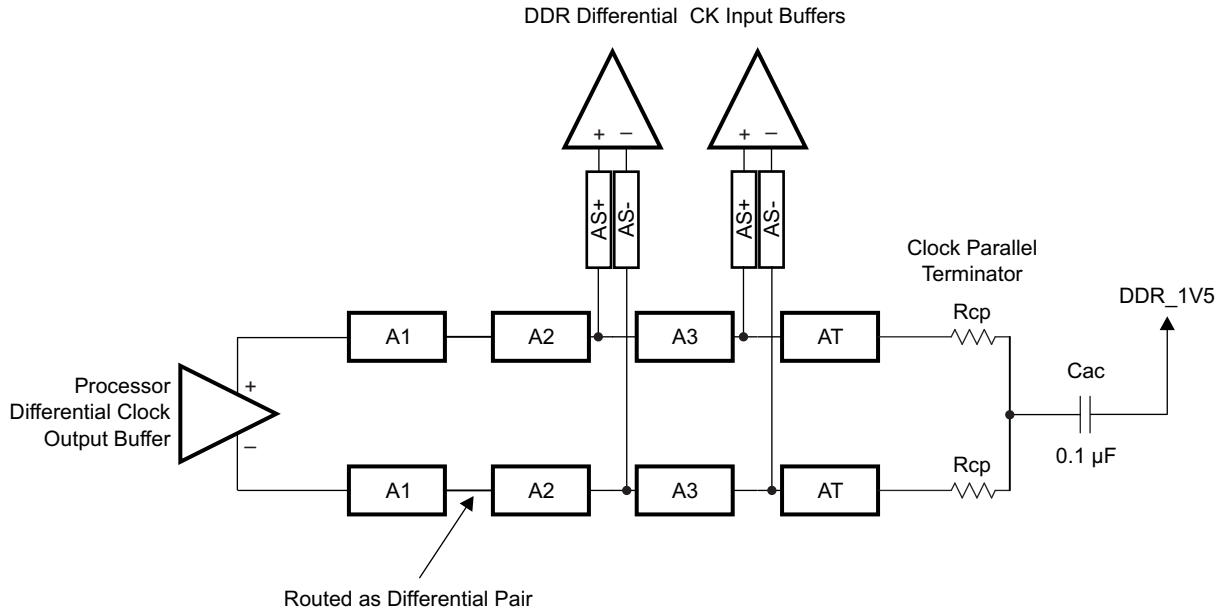


Figure 8-65. CK Topology for Two DDR3 Devices

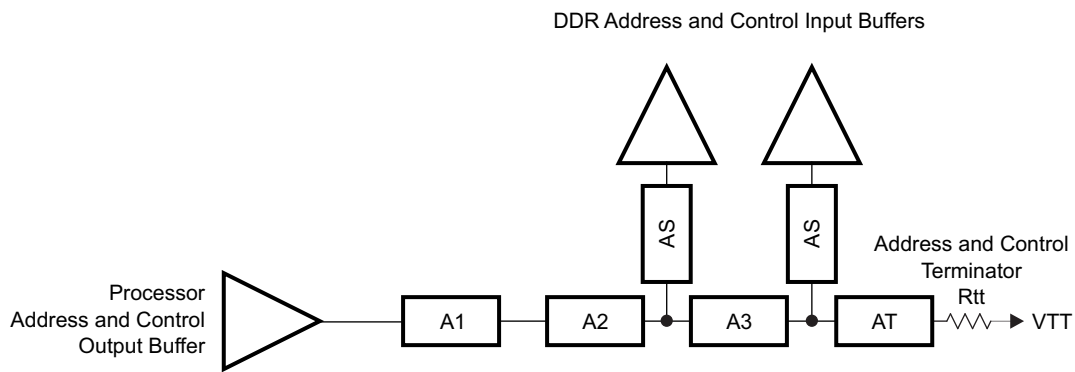


Figure 8-66. ADDR_CTRL Topology for Two DDR3 Devices

8.7.3.15.2.2 CK and ADDR_CTRL Routing, Two DDR3 Devices

Figure 8-67 shows the CK routing for two DDR3 devices placed on the same side of the PCB. Figure 8-68 shows the corresponding ADDR_CTRL routing.

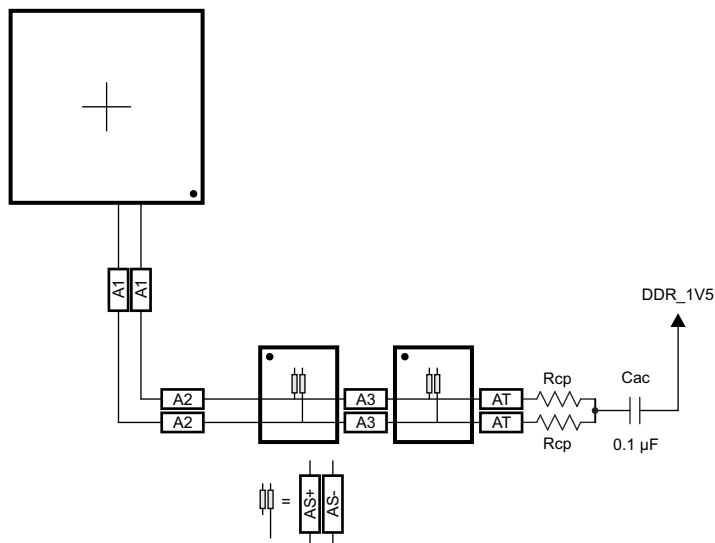


Figure 8-67. CK Routing for Two Single-Side DDR3 Devices

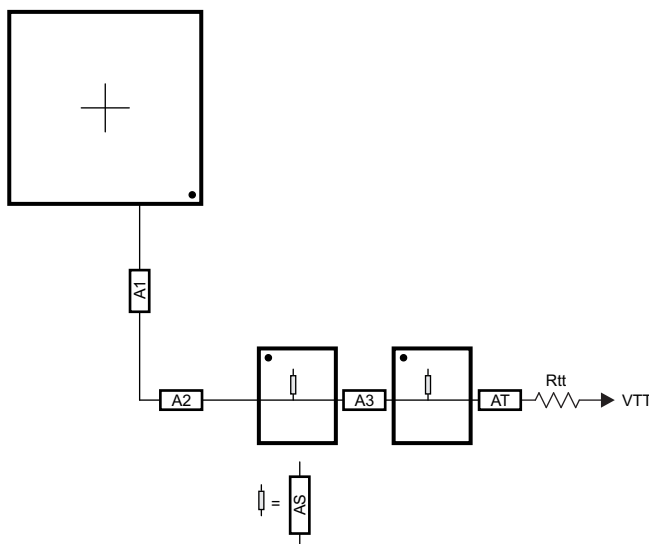


Figure 8-68. ADDR_CTRL Routing for Two Single-Side DDR3 Devices

To save PCB space, the two DDR3 memories may be mounted as a mirrored pair at a cost of increased routing and assembly complexity. [Figure 8-69](#) and [Figure 8-70](#) show the routing for CK and ADDR_CTRL, respectively, for two DDR3 devices mirrored in a single-pair configuration.

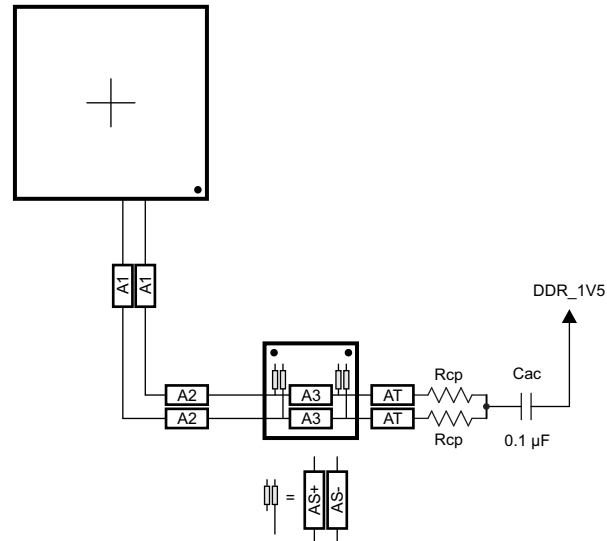


Figure 8-69. CK Routing for Two Mirrored DDR3 Devices

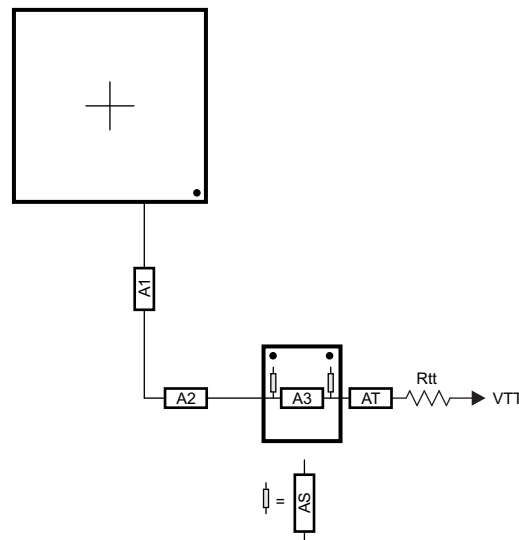


Figure 8-70. ADDR_CTRL Routing for Two Mirrored DDR3 Devices

8.7.3.15.3 One DDR3 Device

A single DDR3 device is supported on the DDR EMIF consisting of one x16 DDR3 device arranged as one bank (CS), 16 bits wide.

8.7.3.15.3.1 CK and ADDR_CTRL Topologies, One DDR3 Device

Figure 8-71 shows the topology of the CK net classes and Figure 8-72 shows the topology for the corresponding ADDR_CTRL net classes.

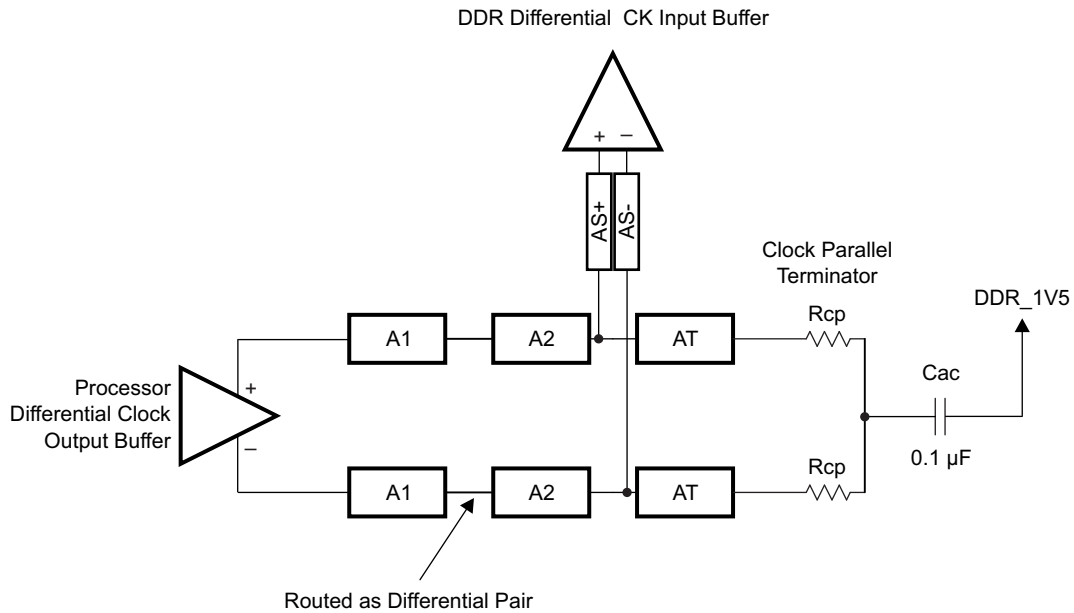


Figure 8-71. CK Topology for One DDR3 Device

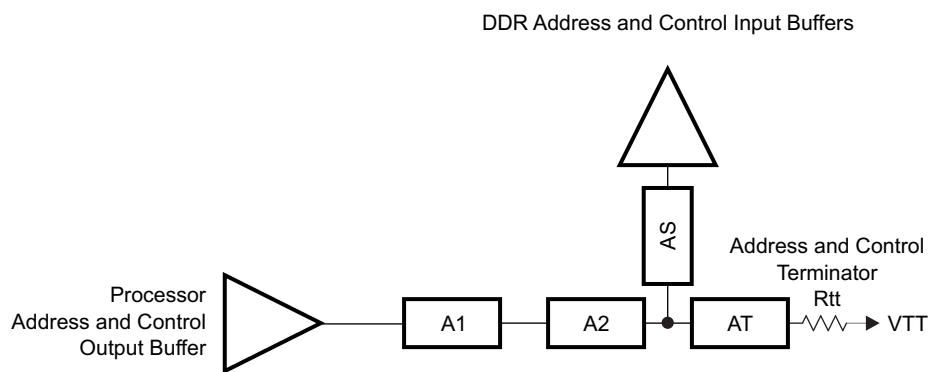


Figure 8-72. ADDR_CTRL Topology for One DDR3 Device

8.7.3.15.3.2 CK and ADDR_CTRL Routing, One DDR3 Device

Figure 8-73 shows the CK routing for one DDR3 device placed on the same side of the PCB. Figure 8-74 shows the corresponding ADDR_CTRL routing.

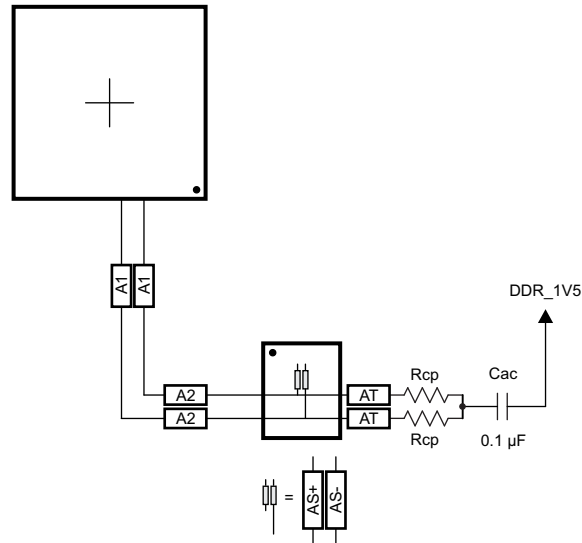


Figure 8-73. CK Routing for One DDR3 Device

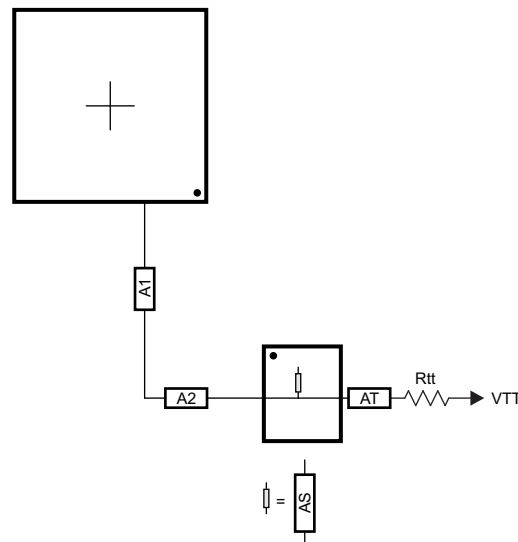


Figure 8-74. ADDR_CTRL Routing for One DDR3 Device

8.7.3.16 Data Topologies and Routing Definition

No matter the number of DDR3 devices used, the data line topology is always point to point, so its definition is simple.

Care should be taken to minimize layer transitions during routing. If a layer transition is necessary, it is better to transition to a layer using the same reference plane. If this cannot be accommodated, ensure there are nearby ground vias to allow the return currents to transition between reference planes if both reference planes are ground or vdds_dds. Ensure there are nearby bypass capacitors to allow the return currents to transition between reference planes if one of the reference planes is ground. The goal is to minimize the size of the return current loops.

8.7.3.16.1 DQS and DQ/DM Topologies, Any Number of Allowed DDR3 Devices

DQS lines are point-to-point differential, and DQ/DM lines are point-to-point singled ended. [Figure 8-75](#) and [Figure 8-76](#) show these topologies.

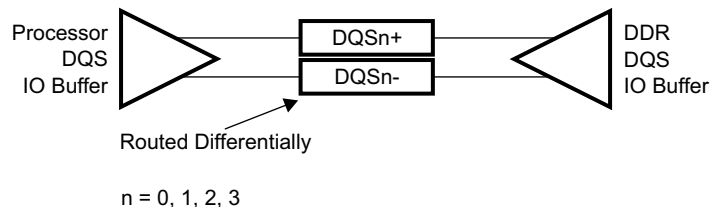


Figure 8-75. DQS Topology

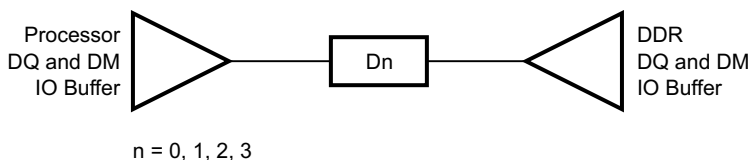


Figure 8-76. DQ/DM Topology

8.7.3.16.2 DQS and DQ/DM Routing, Any Number of Allowed DDR3 Devices

Figure 8-77 and Figure 8-78 show the DQS and DQ/DM routing.

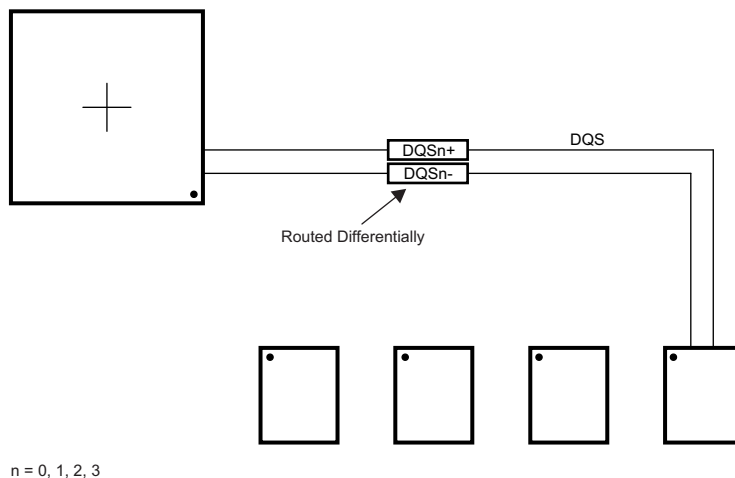


Figure 8-77. DQS Routing With Any Number of Allowed DDR3 Devices

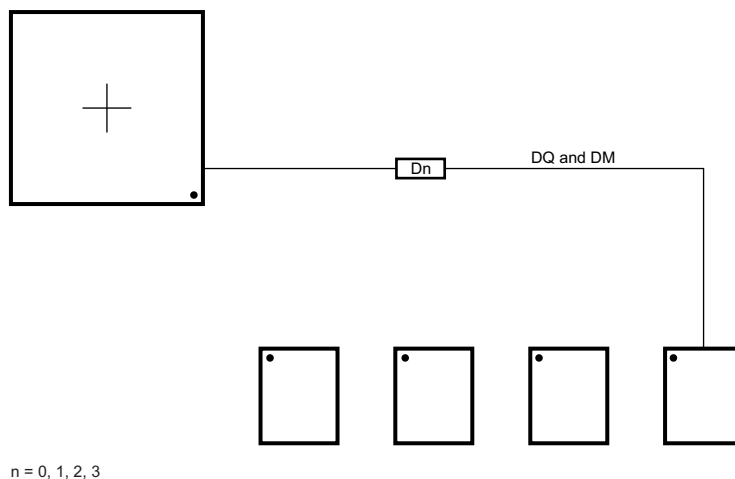


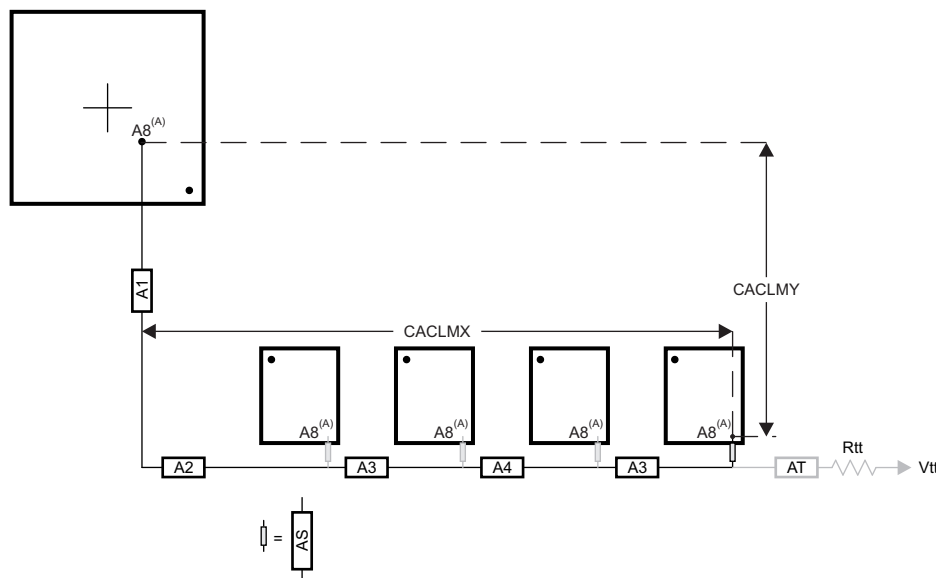
Figure 8-78. DQ/DM Routing With Any Number of Allowed DDR3 Devices

8.7.3.17 Routing Specification

8.7.3.17.1 CK and ADDR_CTRL Routing Specification

Skew within the CK and ADDR_CTRL net classes directly reduces setup and hold margin and, thus, this skew must be controlled. The only way to practically match lengths on a PCB is to lengthen the shorter traces up to the length of the longest net in the net class and its associated clock. A metric to establish this maximum length is Manhattan distance. The Manhattan distance between two points on a PCB is the length between the points when connecting them only with horizontal or vertical segments. A reasonable trace route length is to within a percentage of its Manhattan distance. CACLM is defined as Clock Address Control Longest Manhattan distance.

Given the clock and address pin locations on the processor and the DDR3 memories, the maximum possible Manhattan distance can be determined given the placement. Figure 8-79 and Figure 8-80 show this distance for four loads and two loads, respectively. It is from this distance that the specifications on the lengths of the transmission lines for the address bus are determined. CACLM is determined similarly for other address bus configurations; that is, it is based on the longest net of the CK/ADDR_CTRL net class. For CK and ADDR_CTRL routing, these specifications are contained in Table 8-49.



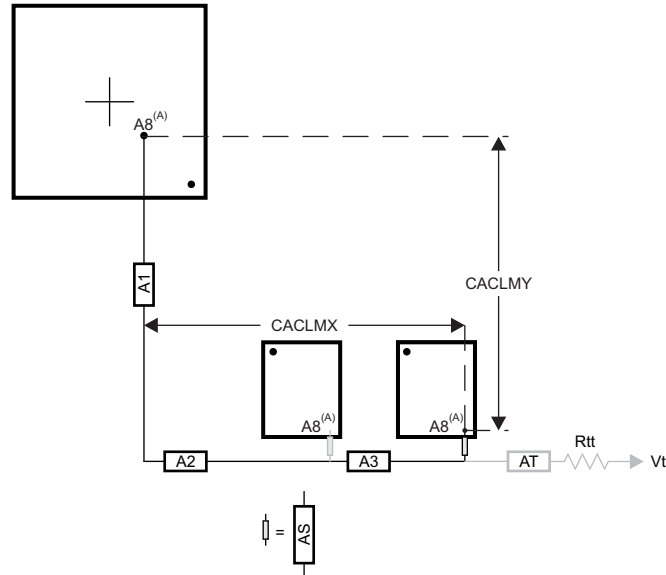
- A. It is very likely that the longest CK/ADDR_CTRL Manhattan distance will be for Address Input 8 (A8) on the DDR3 memories. CACLM is based on the longest Manhattan distance due to the device placement. Verify the net class that satisfies this criteria and use as the baseline for CK/ADDR_CTRL skew matching and length control.

The length of shorter CK/ADDR_CTRL stubs as well as the length of the terminator stub are not included in this length calculation. Non-included lengths are grayed out in the figure.

Assuming A8 is the longest, CALM = CACLMY + CACLMX + 300 mils.

The extra 300 mils allows for routing down lower than the DDR3 memories and returning up to reach A8.

Figure 8-79. CACLM for Four Address Loads on One Side of PCB



- A. It is very likely that the longest CK/ADDR_CTRL Manhattan distance will be for Address Input 8 (A8) on the DDR3 memories. CACLM is based on the longest Manhattan distance due to the device placement. Verify the net class that satisfies this criteria and use as the baseline for CK/ADDR_CTRL skew matching and length control.

The length of shorter CK/ADDR_CTRL stubs as well as the length of the terminator stub are not included in this length calculation. Non-included lengths are grayed out in the figure.

Assuming A8 is the longest, CALM = CACLMY + CACLMX + 300 mils.
The extra 300 mils allows for routing down lower than the DDR3 memories and returning up to reach A8.

Figure 8-80. CACLM for Two Address Loads on One Side of PCB

Table 8-49. CK and ADDR_CTRL Routing Specification⁽²⁾⁽³⁾

NO.	PARAMETER	MIN	TYP	MAX	UNIT
CARS31	A1+A2 length			500 ⁽¹⁾	ps
CARS32	A1+A2 skew			29	ps
CARS33	A3 length			125	ps
CARS34	A3 skew ⁽⁴⁾			6	ps
CARS35	A3 skew ⁽⁵⁾			6	ps
CARS36	A4 length			125	ps
CARS37	A4 skew			6	ps
CARS38	AS length		5 ⁽¹⁾	17	ps
CARS39	AS skew		1.3 ⁽¹⁾	14	ps
CARS310	AS+/AS- length		5	12	ps
CARS311	AS+/AS- skew			1	ps
CARS312	AT length ⁽⁶⁾		75		ps
CARS313	AT skew ⁽⁷⁾		14		ps
CARS314	AT skew ⁽⁸⁾			1	ps
CARS315	CK/ADDR_CTRL trace length			1020	ps
CARS316	Vias per trace			3 ⁽¹⁾	vias
CARS317	Via count difference			1 ⁽¹⁵⁾	vias
CARS318	Center-to-center CK to other DDR3 trace spacing ⁽⁹⁾	4w			
CARS319	Center-to-center ADDR_CTRL to other DDR3 trace spacing ⁽⁹⁾⁽¹⁰⁾	4w			
CARS320	Center-to-center ADDR_CTRL to other ADDR_CTRL trace spacing ⁽⁹⁾	3w			
CARS321	CK center-to-center spacing ⁽¹¹⁾⁽¹²⁾				

Table 8-49. CK and ADDR_CTRL Routing Specification⁽²⁾⁽³⁾ (continued)

NO.	PARAMETER	MIN	TYP	MAX	UNIT
CARS322	CK spacing to other net ⁽⁹⁾	4w			
CARS323	Rcp ⁽¹³⁾	Zo-1	Zo	Zo+1	Ω
CARS324	Rtt ⁽¹³⁾⁽¹⁴⁾	Zo-5	Zo	Zo+5	Ω

- (1) Max value is based upon conservative signal integrity approach. This value could be extended only if detailed signal integrity analysis of rise time and fall time confirms desired operation.
- (2) The use of vias should be minimized.
- (3) Additional bypass capacitors are required when using the DDR_1V5 plane as the reference plane to allow the return current to jump between the DDR_1V5 plane and the ground plane when the net class switches layers at a via.
- (4) Non-mirrored configuration (all DDR3 memories on same side of PCB).
- (5) Mirrored configuration (one DDR3 device on top of the board and one DDR3 device on the bottom).
- (6) While this length can be increased for convenience, its length should be minimized.
- (7) ADDR_CTRL net class only (not CK net class). Minimizing this skew is recommended, but not required.
- (8) CK net class only.
- (9) Center-to-center spacing is allowed to fall to minimum 2w for up to 1250 mils of routed length.
- (10) The ADDR_CTRL net class of the other DDR EMIF is considered *other DDR3 trace spacing*.
- (11) CK spacing set to ensure proper differential impedance.
- (12) The most important thing to do is control the impedance so inadvertent impedance mismatches are not created. Generally speaking, center-to-center spacing should be either 2w or slightly larger than 2w to achieve a differential impedance equal to twice the singleended impedance, Zo.
- (13) Source termination (series resistor at driver) is specifically not allowed.
- (14) Termination values should be uniform across the net class.
- (15) Via count difference may increase by 1 only if accurate 3-D modeling of the signal flight times – including accurately modeled signal propagation through vias – has been applied to ensure all segment skew maximums are not exceeded.

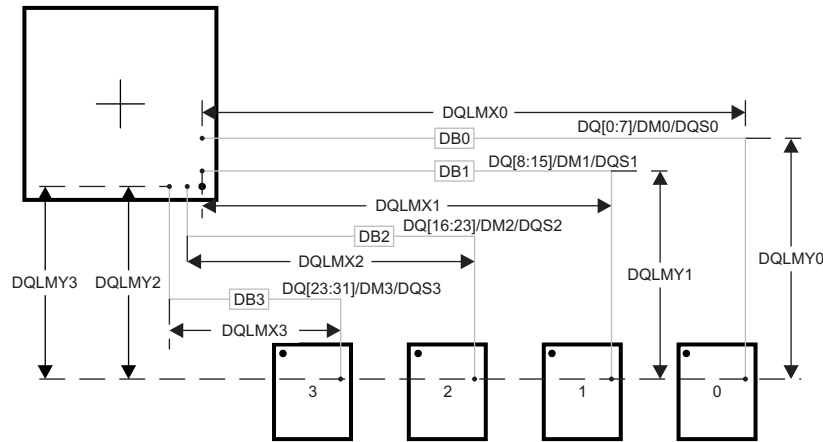
8.7.3.17.2 DQS and DQ Routing Specification

Skew within the DQS and DQ/DM net classes directly reduces setup and hold margin and thus this skew must be controlled. The only way to practically match lengths on a PCB is to lengthen the shorter traces up to the length of the longest net in the net class and its associated clock. As with CK and ADDR_CTRL, a reasonable trace route length is to within a percentage of its Manhattan distance. DQLMn is defined as DQ Longest Manhattan distance n, where n is the byte number. For a 32-bit interface, there are four DQLMs, DQLM0-DQLM3. Likewise, for a 16-bit interface, there are two DQLMs, DQLM0-DQLM1.

NOTE

It is not required, nor is it recommended, to match the lengths across all bytes. Length matching is only required within each byte.

Given the DQS and DQ/DM pin locations on the processor and the DDR3 memories, the maximum possible Manhattan distance can be determined given the placement. [Figure 8-81](#) shows this distance for four loads. It is from this distance that the specifications on the lengths of the transmission lines for the data bus are determined. For DQS and DQ/DM routing, these specifications are contained in [Table 8-50](#).



DB0 - DB3 represent data bytes 0 - 3.

There are four DQLMs, one for each byte (32-bit interface). Each DQLM is the longest Manhattan distance of the byte; therefore:

$$\begin{aligned} DQLM0 &= DQLMX0 + DQLMY0 \\ DQLM1 &= DQLMX1 + DQLMY1 \\ DQLM2 &= DQLMX2 + DQLMY2 \\ DQLM3 &= DQLMX3 + DQLMY3 \end{aligned}$$

Figure 8-81. DQLM for Any Number of Allowed DDR3 Devices

Table 8-50. Data Routing Specification⁽²⁾

NO.	PARAMETER	MIN	TYP	MAX	UNIT
DRS31	DB0 length			340	ps
DRS32	DB1 length			340	ps
DRS33	DB2 length			340	ps
DRS34	DB3 length			340	ps
DRS35	DBn skew ⁽³⁾			5	ps
DRS36	DQSn+ to DQSn- skew			1	ps
DRS37	DQSn to DBn skew ⁽³⁾⁽⁴⁾			5 ⁽¹⁰⁾	ps
DRS38	Vias per trace			2 ⁽¹⁾	vias
DRS39	Via count difference			0 ⁽¹⁰⁾	vias
DRS310	Center-to-center DBn to other DDR3 trace spacing ⁽⁶⁾	4			w ⁽⁵⁾
DRS311	Center-to-center DBn to other DBn trace spacing ⁽⁷⁾	3			w ⁽⁵⁾
DRS312	DQSn center-to-center spacing ^{(8) (9)}				
DRS313	DQSn center-to-center spacing to other net	4			w ⁽⁵⁾

- (1) Max value is based upon conservative signal integrity approach. This value could be extended only if detailed signal integrity analysis of rise time and fall time confirms desired operation.
- (2) External termination disallowed. Data termination should use built-in ODT functionality.
- (3) Length matching is only done within a byte. Length matching across bytes is neither required nor recommended.
- (4) Each DQS pair is length matched to its associated byte.
- (5) Center-to-center spacing is allowed to fall to minimum 2w for up to 1250 mils of routed length.
- (6) Other DDR3 trace spacing means other DDR3 net classes not within the byte.
- (7) This applies to spacing within the net classes of a byte.
- (8) DQS pair spacing is set to ensure proper differential impedance.
- (9) The most important thing to do is control the impedance so inadvertent impedance mismatches are not created. Generally speaking, center-to-center spacing should be either 2w or slightly larger than 2w to achieve a differential impedance equal to twice the singleended impedance, Zo.
- (10) Via count difference may increase by 1 only if accurate 3-D modeling of the signal flight times – including accurately modeled signal propagation through vias – has been applied to ensure DBn skew and DQSn to DBn skew maximums are not exceeded.

9 Device and Documentation Support

TI offers an extensive line of development tools, including methods to evaluate the performance of the processors, generate code, develop algorithm implementations, and fully integrate and debug software and hardware modules.

9.1 Device Nomenclature and Orderable Information

To designate the stages in the product development cycle, TI assigns prefixes to the part numbers of all microprocessors (MPUs) and support tools. Each device has one of three prefixes: X, P, or null (no prefix) (for example, TDA2x). Texas Instruments recommends two of three possible prefix designators for its support tools: TMDX and TMDS. These prefixes represent evolutionary stages of product development from engineering prototypes (TMDX) through fully qualified production devices and tools (TMDS).

Device development evolutionary flow:

- X** Experimental device that is not necessarily representative of the final device's electrical specifications and may not use production assembly flow.
- P** Prototype device that is not necessarily the final silicon die and may not necessarily meet final electrical specifications.
- null** Production version of the silicon die that is fully qualified.

Support tool development evolutionary flow:

- TMDX** Development-support product that has not yet completed Texas Instruments internal qualification testing.
- TMDS** Fully-qualified development-support product.

X and P devices and TMDX development-support tools are shipped against the following disclaimer:

"Developmental product is intended for internal evaluation purposes."

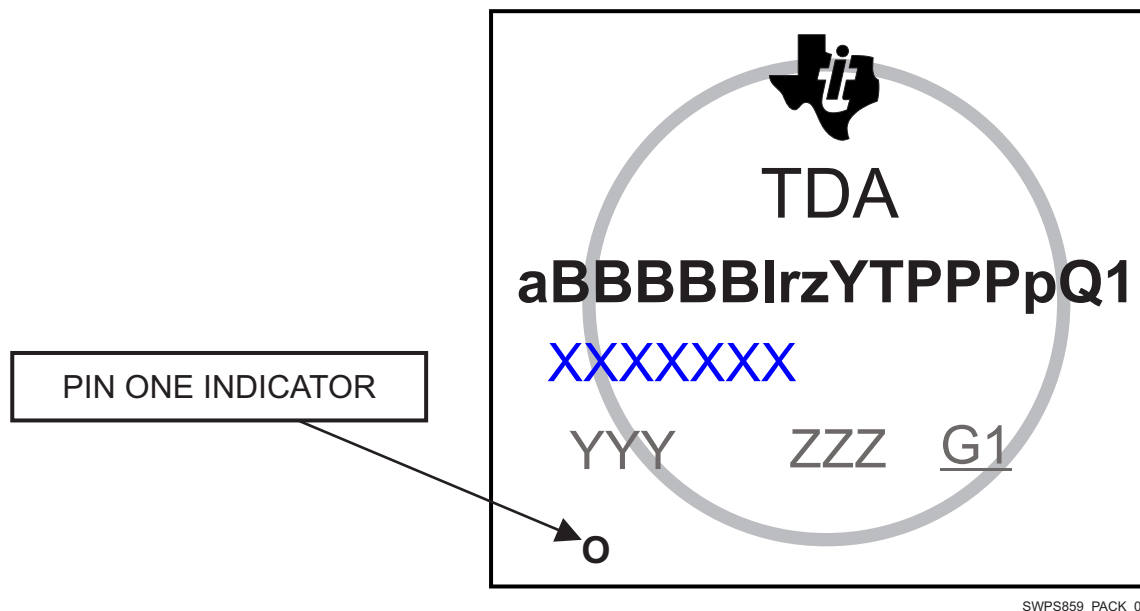
Production devices and TMDS development-support tools have been characterized fully, and the quality and reliability of the device have been demonstrated fully. TI's standard warranty applies.

Predictions show that prototype devices (X or P) have a greater failure rate than the standard production devices. Texas Instruments recommends that these devices not be used in any production system because their expected end-use failure rate still is undefined. Only qualified production devices are to be used.

For orderable part numbers of TDA2x devices in the AAS package type, see the Package Option Addendum of this document, the TI website (www.ti.com), or contact your TI sales representative.

For additional description of the device nomenclature markings on the die, see the Silicon Errata (literature number SPRZ397).

9.1.1 Standard Package Symbolization



SWPS859_PACK_01

Figure 9-1. Printed Device Reference

NOTE

Some devices have a cosmetic circular marking visible on the top of the device package which results from the production test process. These markings are cosmetic only with no reliability impact.

9.1.2 Device Naming Convention

Table 9-1. Nomenclature Description

FIELD PARAMETER	FIELD DESCRIPTION	VALUES		DESCRIPTION
		MARKING	ORDERABLE	
a	Device evolution stage ⁽¹⁾	X	Contact TI	Prototype
		P		Preproduction (production test flow, no reliability data)
		BLANK		Production
BBBBB	Base production part number	TDA2S		ADAS 2 nd Generation Super Tier
		TDA2H		ADAS 2 nd Generation High Tier
		TDA2M		ADAS 2 nd Generation Mid Tier
		TDA2L		ADAS 2 nd Generation Low Tier
I	Device Identity	A		Scene Analysis
		V		Scene Viewing
		E		Ethernet Decode
		R		Driver Recorder
		F		Fusion
		G		GFX enabled
		X		ADAS Superset
		D		DSP only

Table 9-1. Nomenclature Description (continued)

FIELD PARAMETER	FIELD DESCRIPTION	VALUES		DESCRIPTION
		MARKING	ORDERABLE	
r	Device revision	BLANK		SR 1.0
		A		SR 1.1
		B		SR 2.0
z	Device Speed	A		Indicates the speed grade for each of the cores in the device. For more information see Section 3.1, Device Comparison Table .
		B		
		D		
		F		
		N		
		R		
		T		
Y	Device type	BLANK		General purpose (Prototype and Production)
		E		Emulation (E) devices
		D		High security devices
T	Temperature ⁽²⁾	I		Industrial: -40°C to 85°C (initial prototypes)
		Q		Full temp range: -40°C to 125°C
PPP	Package designator	AAS		AAS S-PBGA-N625 (17mm x 17mm) Package
p	Package Revision	BLANK		Initial Package
		OTHER		Package revision identifier
c	Carrier designator	N/A	BLANK	Tray
		N/A	R	Tape & Reel
Q1	Automotive Designator	BLANK		Does not meets automotive qualification
		Q1		Meets Q100 equal requirements, with exceptions as specified in DM.
XXXXXX		<i>As marked</i>	N/A	Lot Trace Code
YYY		<i>As marked</i>	N/A	Production Code, For TI use only
ZZZ		<i>As marked</i>	N/A	Production Code, For TI use only
O		<i>As marked</i>	N/A	Pin one designator
G1		<i>As marked</i>	N/A	ECAT—Green package designator

(1) To designate the stages in the product development cycle, TI assigns prefixes to the part numbers. These prefixes represent evolutionary stages of product development from engineering prototypes through fully qualified production devices. Prototype devices are shipped against the following disclaimer:

"This product is still in development and is intended for internal evaluation purposes."

Notwithstanding any provision to the contrary, TI makes no warranty expressed, implied, or statutory, including any implied warranty of merchantability of fitness for a specific purpose, of this device.

(2) Applies to device max junction temperature.

NOTE

BLANK in the symbol or part number is collapsed so there are no gaps between characters.

9.2 Tools and Software

The following products support development for TDA2x platforms:

TDA2x Pad Configuration Tool is an interactive pad-configuration tool that allows the user to visualize the device pad configuration state on power-on reset and then customize the configuration of the pads for the specific use-case and identify the device register settings associated to that configuration.

TDA2x Register Descriptor is an interactive device register configuration tool that allows users to visualize the register state on power-on reset, and then customize the configuration of the device for the specific use-case.

TDA2x Clock Tree Tool is interactive clock tree configuration software that allows the user to visualize the device clock tree, interact with clock tree elements and view the effect on PRCM registers, interact with the PRCM registers and view the effect on the device clock tree, and view a trace of all the device registers affected by the user interaction with the clock tree.

For a complete listing of development-support tools for the processor platform, visit the Texas Instruments website at www.ti.com. For information on pricing and availability, contact the nearest TI field sales office or authorized distributor.

9.3 Documentation Support

The following documents describe the TDA2x devices.

TRM [TDA2x ADAS Applications Processor Technical Reference Manual](#) Details the integration, the environment, the functional description, and the programming models for each peripheral and subsystem in the TDA2x family of devices.

Errata [TDA2x Silicon Errata](#) Describes known advisories on silicon and provides workarounds.

9.3.1 FCC Warning

This equipment is intended for use in a laboratory test environment only. It generates, uses, and can radiate radio frequency energy and has not been tested for compliance with the limits of computing devices pursuant to subpart J of part 15 of FCC rules, which are designed to provide reasonable protection against radio frequency interference. Operation of this equipment in other environments may cause interference with radio communications, in which case the user at his own expense will be required to take whatever measures may be required to correct this interference.

9.3.2 Information About Cautions and Warnings

This book may contain cautions and warnings.

CAUTION

This is an example of a caution statement.

A caution statement describes a situation that could potentially damage your software or equipment.

WARNING

This is an example of a warning statement.

A warning statement describes a situation that could potentially cause harm to you.

The information in a caution or a warning is provided for your protection. Please read each caution and warning carefully.

9.4 Receiving Notification of Documentation Updates

To receive notification of documentation updates — including silicon errata — go to the product folder for your device on www.ti.com. In the upper right-hand corner, click the "Alert me" button. This registers you to receive a weekly digest of product information that has changed (if any). For change details, check the revision history of any revised document.

9.5 Related Links

The table below lists quick access links. Categories include technical documents, support and community resources, tools and software, and quick access to sample or buy.

Table 9-2. Related Links

PARTS	PRODUCT FOLDER	SAMPLE & BUY	TECHNICAL DOCUMENTS	TOOLS & SOFTWARE	SUPPORT & COMMUNITY
TDA2HA	Click here	Click here	Click here	Click here	Click here
TDA2HG	Click here	Click here	Click here	Click here	Click here

9.6 Community Resources

The following links connect to TI community resources. Linked contents are provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's [Terms of Use](#).

TI Embedded Processors Wiki Texas Instruments Embedded Processors Wiki.

Established to help developers get started with Embedded Processors from Texas Instruments and to foster innovation and growth of general knowledge about the hardware and software surrounding these devices.

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9.8 Electrostatic Discharge Caution



This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

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9.10 Glossary

TI Glossary This glossary lists and explains terms, acronyms, and definitions.

10 Mechanical Packaging and Orderable Information

The following pages include mechanical packaging information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

10.1 Mechanical Data

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
TDA2HABDQAASRQ1	ACTIVE	FCBGA	AAS	625	500	Green (RoHS & no Sb/Br)	Call TI SNAGCU	Level-4-250C-72 HR	-40 to 125	TDA2HABDQAASQ1 TDA	Samples

(1) The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".

RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.

Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

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