Overvoltage Protection for 2-Series to 4-Series Cell Li-Ion Batteries with External Delay Capacitor

Check for Samples: bq771600, bq771601, bq771602, bq771604

FEATURES

- **2-, 3-, and 4-Series Cell Overvoltage Protection**
- **External Capacitor-Programmed Delay Timer**
- **Fixed OVP Threshold**
- **High-Accuracy Overvoltage Protection: ±10 mV**
- **Low Power Consumption I_{CC} ≈ 1 µA ($V_{CELL(ALL)}$ < $V_{PROTECT}$)**
- **Low Leakage Current Per Cell Input < 100 nA**
- **Small Package Footprint**
  - **8-pin QFN (3 mm x 4 mm)**

APPLICATIONS

- **Power Tools**
- **UPS Battery Backup**
- **Light Electric Vehicles**
  - **eBike**
  - **eScooter**
  - **Pedal Assist Bicycles**

DESCRIPTION

The bq7716xy family of products is an overvoltage monitor and protector for Li-Ion battery pack systems. Each cell is monitored independently for an overvoltage condition.

In the bq7716xy device, an external delay timer is initiated upon detection of an overvoltage condition on any cell. Upon expiration of the delay timer, the output is triggered into its active state (either high or low, depending on the configuration). The external delay timer feature also includes the ability to detect an open or shorted delay capacitor on the CD pin, which will similarly trigger the output driver in an overvoltage condition.

For quicker production-line testing, the bq7716xy device provides a Customer Test Mode with greatly reduced delay time.

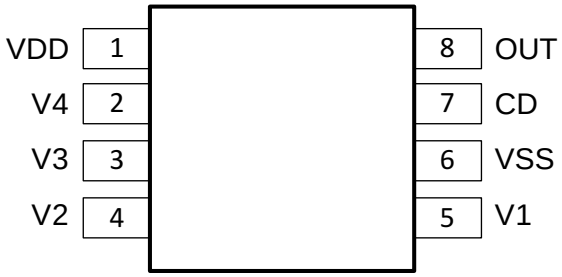


Figure 1. bq7716xy Pinout

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These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

ORDERING INFORMATION

T_A	Part Number	Package	Package Designator	OVP (V)	OV Hysteresis (V)	Output Drive	Tape and Reel (Large)	Tape and Reel (Small)
–40°C to 110°C	bq771600	8-pin QFN	DPJ	4.300	0.300	CMOS Active High	bq771600DPJR	bq771600DPJT
	bq771601			4.225	0.050	CMOS Active High	bq771601DPJR	bq771601DPJT
	bq771602			4.225	0.050	NCH Active Low, Open Drain	bq771602DPJR	bq771602DPJT
	bq771603(1)			4.325	0.050	NCH Active Low, Open Drain	bq771603DPJR	bq771603DPJT
	bq771604			4.200	0.050	CMOS Active High	bq771604DPJR	bq771604DPJT
	bq771605(1)			3.850	0.250	NCH Active Low	bq771605DPJR	bq771605DPJT
	bq771607(1)			4.200	0.250	CMOS Active High	bq771607DPJR	bq771607DPJT
	bq771608(1)			4.225	0.250	CMOS Active High	bq771608DPJR	bq771608DPJT
	bq771609(1)			4.250	0.050	CMOS Active High	bq771609DPJR	bq771609DPJT
	bq771610(1)			4.250	0.250	CMOS Active High	bq771610DPJR	bq771610DPJT
	bq771611(1)			4.350	0.300	CMOS Active High	bq771611DPJR	bq771611DPJT
	bq771612(1)			3.900	0.300	CMOS Active High	bq771612DPJR	bq771612DPJT
	bq771613(1)			4.200	0.050	NCH Active Low	bq771613DPJR	bq771613DPJT
	bq771614(1)			4.225	0.250	NCH Active Low	bq771614DPJR	bq771614DPJT
	bq771615(1)			4.250	0.050	NCH Active Low	bq771615DPJR	bq771615DPJT
	bq7716xy(2)			3.850–4.650	0–0.300	CMOS Active High or NCH Active Low, Open Drain	bq7716xyTBD	bq7716xyTBD

(1) Product Preview only.
(2) Future Option, contact TI.

THERMAL INFORMATION

THERMAL METRIC(1)		bq7716xy	UNITS
		8 PINS	
θ_{JA}	Junction-to-ambient thermal resistance	56.6	°C/W
$\theta_{JC(top)}$	Junction-to-case(top) thermal resistance	56.4	
θ_{JB}	Junction-to-board thermal resistance	30.6	
ψ_{JT}	Junction-to-top characterization parameter	1.0	
ψ_{JB}	Junction-to-board characterization parameter	37.8	
$\theta_{JC(bottom)}$	Junction-to-case(bottom) thermal resistance	11.3	

(1) For more information about traditional and new thermal metrics, see the *IC Package Thermal Metrics* application report, SPRA953.

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PIN FUNCTIONS

bq7716xy	Pin Name	Type I/O	Description
1	VDD	P	Power supply
2	V4	I	Sense input for positive voltage of the fourth cell from the bottom of the stack
3	V3	I	Sense input for positive voltage of the third cell from the bottom of the stack
4	V2	I	Sense input for positive voltage of the second cell from the bottom of the stack
5	V1	I	Sense input for positive voltage of the lowest cell in the stack
6	VSS	P	Electrically connected to IC ground and negative terminal of the lowest cell in the stack
7	CD	I/O	External capacitor connection for delay timer
8	OUT	OA	Output drive for overvoltage fault signal

PIN DETAILS

In the bq7716xy device, each cell is monitored independently. Overvoltage is detected by comparing the actual cell voltage to a protection voltage reference, V_{OV}. If any cell voltage exceeds the programmed OV value, a timer circuit is activated. This timer circuit charges the CD pin to a nominal value, then slowly discharges it with a fixed current back down to VSS. When the CD pin falls below a nominal threshold near VSS, the OUT terminal goes from inactive to active state. Additionally, a timeout detection circuit checks to ensure that the CD pin successfully begins charging to above VSS and subsequently drops back down to VSS, and if a timeout error is detected in either direction, it will similarly trigger the OUT pin to become active. See Figure 2 for reference.

For an NCH Open Drain Active Low configuration, the OUT pin pulls down to VSS when active (OV present) and is high impedance when inactive (no OV).

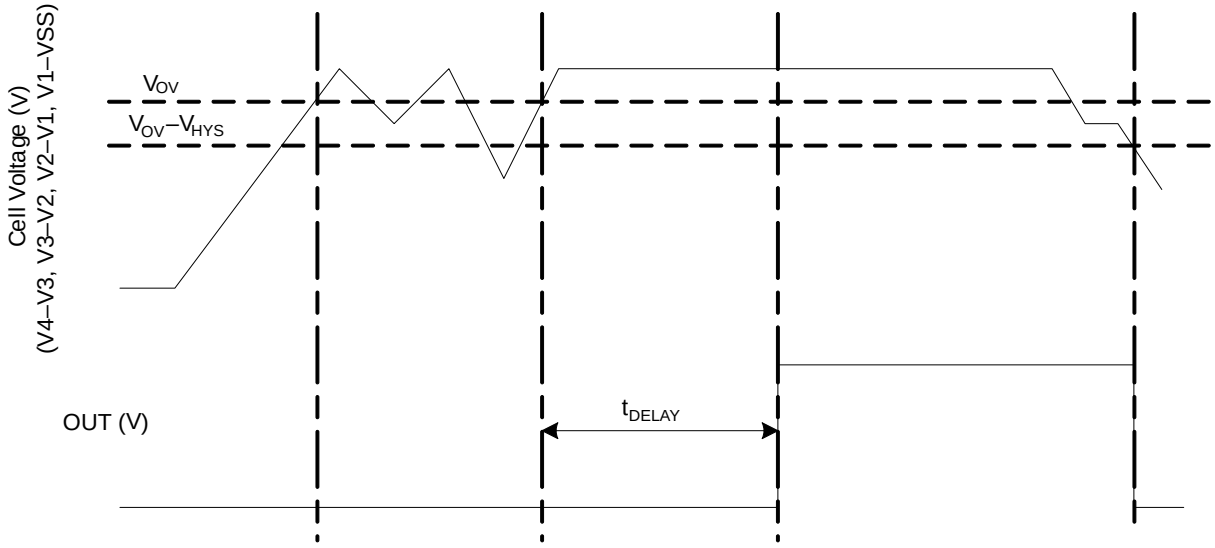


Figure 2. Timing for Overvoltage Sensing

Figure 3 shows the behavior of the CD pin during an OV sequence.

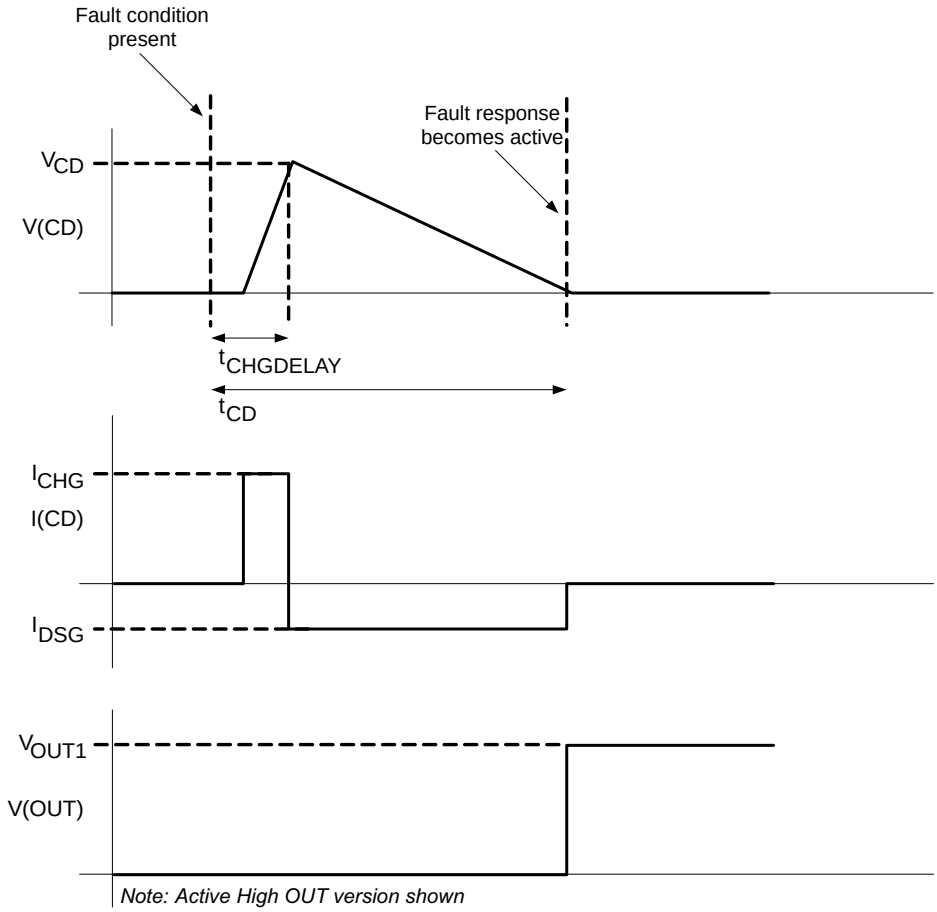


Figure 3. CD Pin Mechanism

Sense Positive Input for Vx

This is an input to sense each single battery cell voltage. A series resistor and a capacitor across the cell for each input is required for noise filtering and stable voltage monitoring.

Output Drive, OUT

This terminal serves as the fault signal output, and may be ordered in either active HIGH or LOW options.

Supply Input, VDD

This terminal is the unregulated input power source for the IC. A series resistor is connected to limit the current, and a capacitor is connected to ground for noise filtering.

External Delay Capacitor, CD

This terminal is connected to an external capacitor that is used for setting the delay timer during an overvoltage fault event.

The CD pin includes a timeout detection circuit to ensure that the output drives active even with a shorted or open capacitor during an overvoltage event.

The capacitor connected on the CD pin rapidly charges to a voltage if any one of the cell inputs exceeds the OV threshold. Then the delay circuit gradually discharges the capacitor on the CD pin. Once this capacitor discharges below a set voltage, the OUT transitions from an inactive to active state.

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To calculate the delay, use the following equation:

t_{CD} (sec) = K × C_{CD} (µF), where K = 10 to 20 range. (1)

Example: If C_{CD}= 0.1 µF (typical), then the delay timer range is

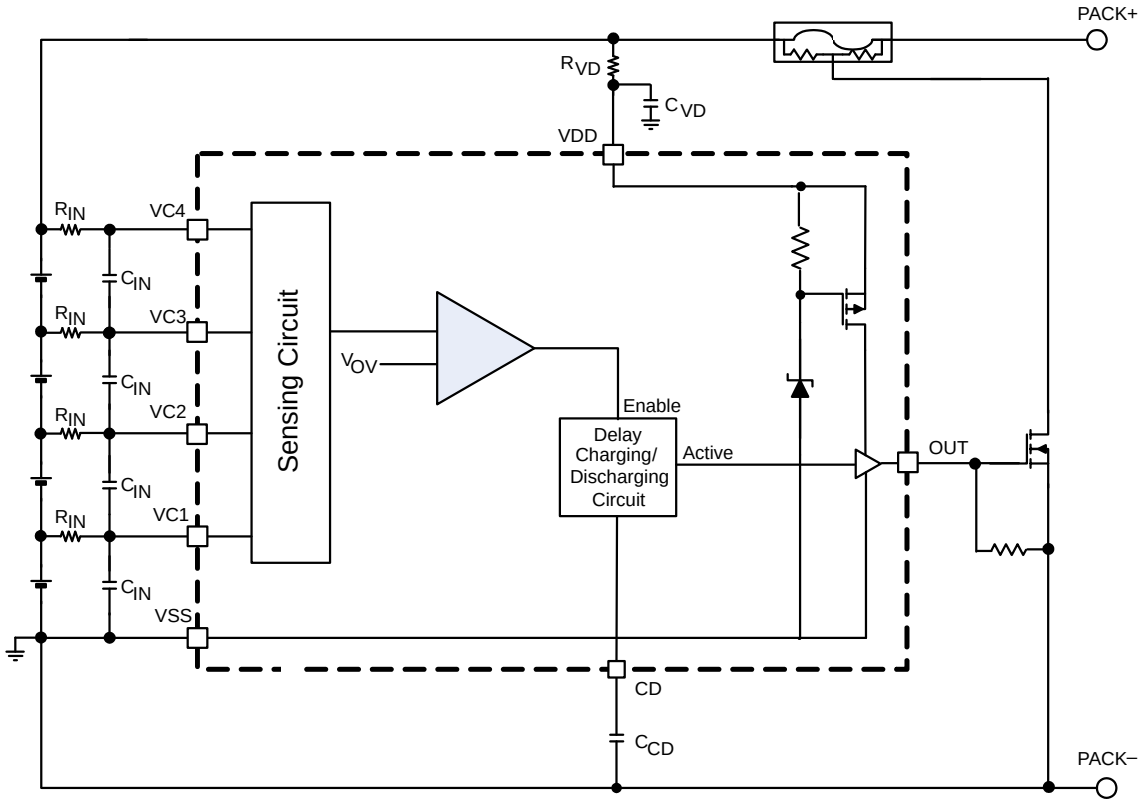
t_{CD} (sec) = 10 × 0.1 = 1 s (Minimum)

t_{CD} (sec) = 20 × 0.1 = 2 s (Maximum)

NOTE

The tolerance on the capacitor used for C_{CD} increases the range of the t_{CD} timer.

FUNCTIONAL BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS

Over operating free-air temperature range (unless otherwise noted)(1)

PARAMETER	CONDITION	VALUE/UNIT
Supply voltage range	VDD–VSS	–0.3 to 30 V
Input voltage range	V4–V3, V3–V2, V2–V1, V1–VSS, or CD–VSS	–0.3 to 30 V
Output voltage range	OUT–VSS	–0.3 to 30 V
Continuous total power dissipation, P_{TOT}		See package dissipation rating.
Functional temperature		–40 to 110°C
Storage temperature range, T_{STG}		–65 to 150°C
Lead temperature (soldering, 10 s), T_{SOLDER}		300°C

(1) Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum–rated conditions for extended periods may affect device reliability.

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RECOMMENDED OPERATING CONDITIONS

Over operating free-air temperature range (unless otherwise noted)

PARAMETER		MIN	NOM	MAX	UNIT
Supply voltage, V_{DD} (1)		3		20	V
Input voltage range	V4–V3, V3–V2, V2–V1, V1–VSS, or CD–VSS	0		5	V
Operating ambient temperature range, T_A		–40		110	°C

(1) See APPLICATION SCHEMATIC.

DC CHARACTERISTICS

Typical values stated where T_A = 25°C and VDD = 14.4 V, MIN/MAX values stated where T_A = –40°C to 110°C and V_{DD} = 3 V to 20 V (unless otherwise noted).

SYMBOL	PARAMETER	CONDITION	MIN	TYP	MAX	UNIT
Voltage Protection Threshold VCx						
V_{OV}	$V_{(PROTECT)}$ Overvoltage Detection	bq771600		4.300		V
		bq771601		4.225		V
		bq771602		4.225		V
		bq771603 (1)		4.325		V
		bq771604		4.200		V
		bq771605 (1)		3.850		V
		bq771607 (1)		4.200		V
		bq771608 (1)		4.225		V
		bq771609 (1)		4.250		V
		bq771610 (1)		4.250		V
		bq771611 (1)		4.350		V
		bq771612 (1)		3.900		V
		bq771613 (1)		4.200		V
		bq771614 (1)		4.225		V
		bq771615 (1)		4.250		V
V_{HYS}	OV Detection Hysteresis	bq771600	250	300	400	mV
		bq771601	25	50	75	mV
		bq771602	25	50	75	mV
		bq771603 (1)	25	50	75	mV
		bq771604	25	50	75	mV
		bq771605 (1)	200	250	300	mV
		bq771607 (1)	200	250	300	mV
		bq771608 (1)	200	250	300	mV
		bq771609 (1)	25	50	75	mV
		bq771610 (1)	200	250	300	mV
		bq771611 (1)	250	300	400	mV
		bq771612 (1)	250	300	400	mV
		bq771613 (1)	25	50	75	mV
		bq771614 (1)	200	250	300	mV
		bq771615 (1)	25	50	75	mV
V_{OA}	OV Detection Accuracy	T_A = 25°C	–10		10	mV

(1) Future option. Contact TI.

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DC CHARACTERISTICS (continued)

Typical values stated where T_A = 25°C and VDD = 14.4 V, MIN/MAX values stated where T_A = –40°C to 110°C and V_{DD} = 3 V to 20 V (unless otherwise noted).

SYMBOL	PARAMETER	CONDITION	MIN	TYP	MAX	UNIT
$V_{OADRIFT}$	OV Detection Accuracy Across Temperature	T_A = –40°C	–40		44	mV
		T_A = 0°C	–20		20	mV
		T_A = 60°C	–24		24	mV
		T_A = 110°C	–54		54	mV
Supply and Leakage Current						
I_{CC}	Supply Current	(V4–V3) = (V3–V2) = (V2–V1) = (V1–VSS) = 4.0 V (See Figure 13.)		1	2	µA
I_{IN}	Input Current at Vx Pins	(V4–V3) = (V3–V2) = (V2–V1) = (V1–VSS) = 4.0 V (See Figure 13.)	–0.1		0.1	µA
Output Drive OUT, CMOS Active High Versions Only						
V_{OUT1}	Output Drive Voltage, Active High	(V4–V3), (V3–V2), (V2–V1), or (V1–VSS) > V_{OV}, VDD = 14.4 V, I_{OH} = 100 µA	6			V
		If three of four cells are short circuited, only one cell remains powered and > V_{OV}, VDD = Vx (cell voltage), I_{OH} = 100 µA	VDD – 0.3			V
		(V4–V3), (V3–V2), (V2–V1), and (V1–VSS) < V_{OV}, VDD = 14.4 V, I_{OL} = 100 µA measured into OUT pin		250	400	mV
I_{OUTH1}	OUT Source Current (During OV)	(V4–V3), (V3–V2), (V2–V1), or (V1–VSS) > V_{OV}, VDD = 14.4 V, OUT = 0 V. Measured out of OUT pin			4.5	mA
I_{OUTL1}	OUT Sink Current (No OV)	(V4–V3), (V3–V2), (V2–V1), and (V1–VSS) < V_{OV}, VDD = 14.4 V, OUT = VDD. Measured into OUT pin	0.5		14	mA
Output Drive OUT, NCH Open Drain Active Low Versions Only						
V_{OUT2}	Output Drive Voltage, Active Low	(V4–V3), (V3–V2), (V2–V1), or (V1–VSS) > V_{OV}, VDD = 14.4 V, I_{OL} = 100 µA measured into OUT pin		250	400	mV
I_{OUTH2}	OUT Sink Current (During OV)	(V4–V3), (V3–V2), (V2–V1), or (V1–VSS) > V_{OV}, VDD = 14.4 V. OUT = VDD. Measured into OUT pin	0.5		14	mA
I_{OUTLK}	OUT Pin Leakage	(V4–V3), (V3–V2), (V2–V1), and (V1–VSS) < V_{OV}, VDD = 14.4 V, OUT = VDD. Measured out of OUT pin			100	nA
Delay Timer						
t_{CD}	OV Delay Time	C_{CD} = 0.1 µF (For capacitor sizing, see PIN DETAILS.)	1	1.5	2	s
V_{CD}	CD Fault Detection External Comparator Threshold, Initial Charge Value	The CD pin will first be quickly charged to this value before being discharged back to VSS.		1.5		V
$t_{CHGDELAY}$	CD Charging Delay	OVP to OUT delay with CD shorted to ground	20		170	ms
I_{CHG}	OV Detection Charging Current	CD pin fast charging current from VSS to V_{CD} to begin delay countdown		300		µA
I_{DSG}	OV Detection Discharging Current	CD pin discharging current from V_{DELAY} to VSS		100		nA

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TYPICAL CHARACTERISTICS

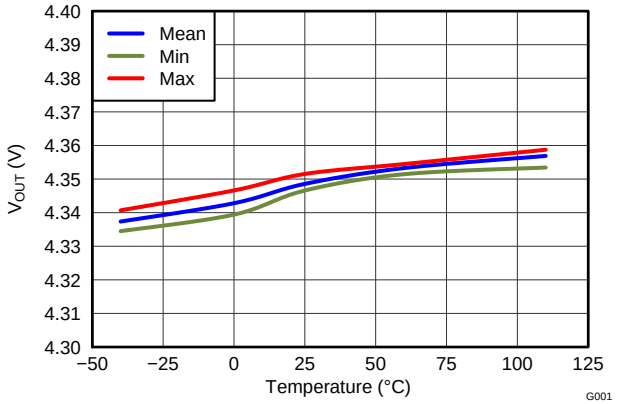


Figure 4. Overvoltage Threshold (OVT) vs. Temperature

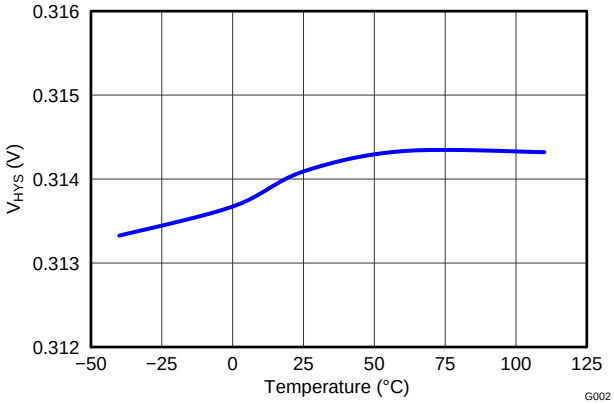


Figure 5. Hysteresis V_{HYS} vs. Temperature

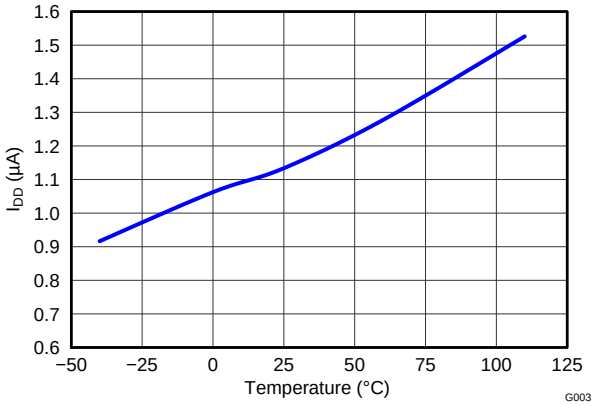


Figure 6. I_{DD} Current Consumption vs. Temperature at VDD = 16 V

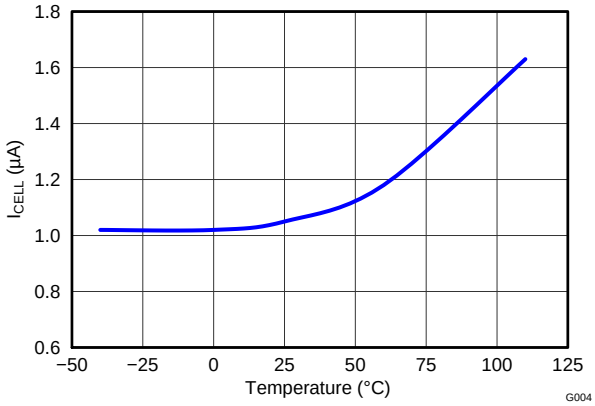


Figure 7. I_{CELL} vs. Temperature at V_{CELL}= 9.2 V

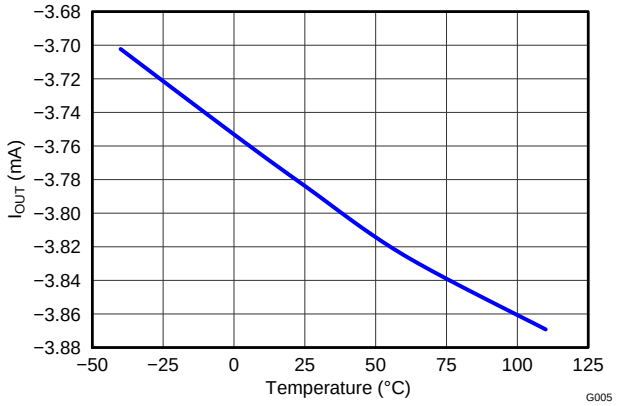


Figure 8. Output Current I_{OUT} vs. Temperature

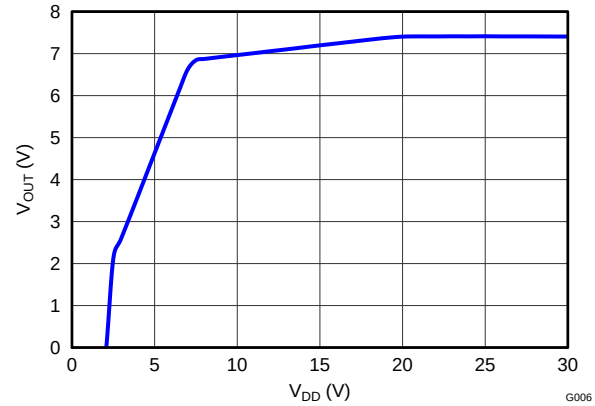


Figure 9. V_{OUT} vs. V_{DD}

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APPLICATION INFORMATION

Figure 10 shows each external component.

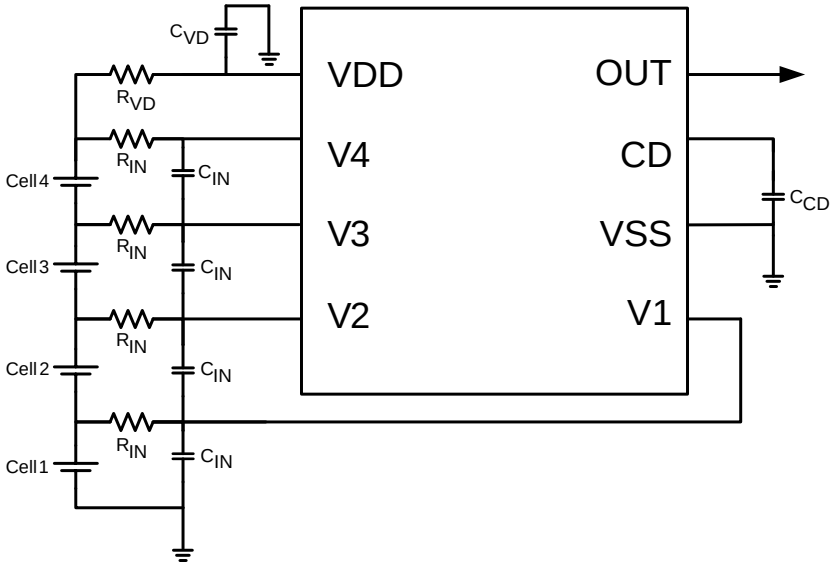


Figure 10. Application Configuration

NOTE

In the case of an Open Drain Active Low configuration, an external pull-up resistor is required on the OUT terminal.

Changes to the ranges stated in Table 1 will impact the accuracy of the cell measurements.

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Table 1. Parameters

PARAMETER	EXTERNAL COMPONENT	MIN	NOM	MAX	UNIT
Voltage monitor filter resistance	RIN	900	1000	1100	Ω
Voltage monitor filter capacitance	CIN	0.01		0.1	µF
Supply voltage filter resistance	RVD	100		1K	Ω
Supply voltage filter capacitance	CVD		0.1		µF
CD external delay capacitance	CCD		0.1	1	µF
OUT Open drain version pull-up resistance to PACK+	ROUT		100k		Ω

NOTE

The device is calibrated using an R_{IN} value = 1 kΩ. Using a value other than this recommended value changes the accuracy of the cell voltage measurements and V_{OV} trigger level.

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APPLICATION SCHEMATIC

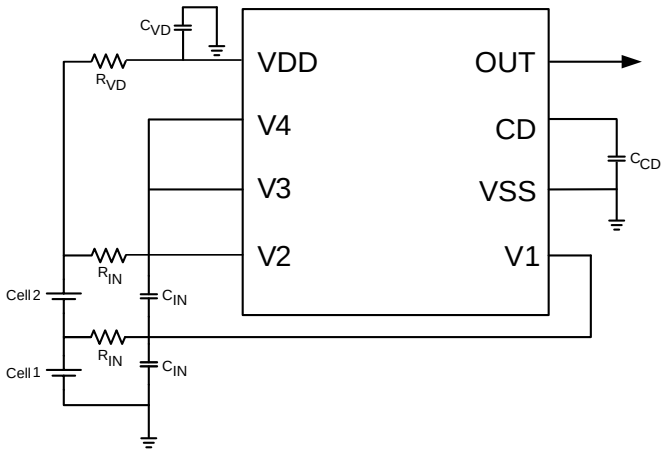


Figure 11. 2-Series Cell Configuration with Capacitor-Programmed Delay

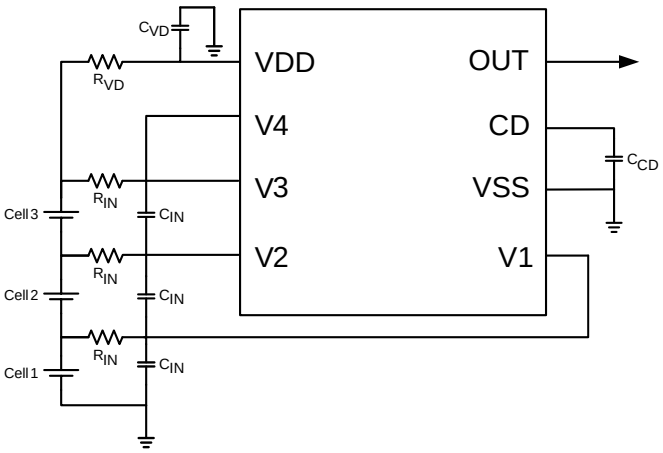


Figure 12. 3-Series Cell Configuration with Capacitor-Programmed Delay

NOTE

In these application examples of 2 s and 3 s, an external pull-up resistor is required on the OUT terminal to configure for an Open Drain Active Low operation.

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CUSTOMER TEST MODE

It is possible to reduce test time for checking the overvoltage function by simply shorting the external CD capacitor to VSS. In this case, the OV delay would be reduced to the $t_{(CHGDELAY)}$ value, which has a maximum of 170 ms.

CAUTION

Avoid exceeding any Absolute Maximum Voltages on any pins when placing the part into Customer Test Mode. Also avoid exceeding Absolute Maximum Voltages for the individual cell voltages (V4–V3), (V3–V2), (V2–V1), and (V1–VSS). Stressing the pins beyond the rated limits may cause permanent damage to the device.

Figure 13 shows the timing for the Customer Test Mode.

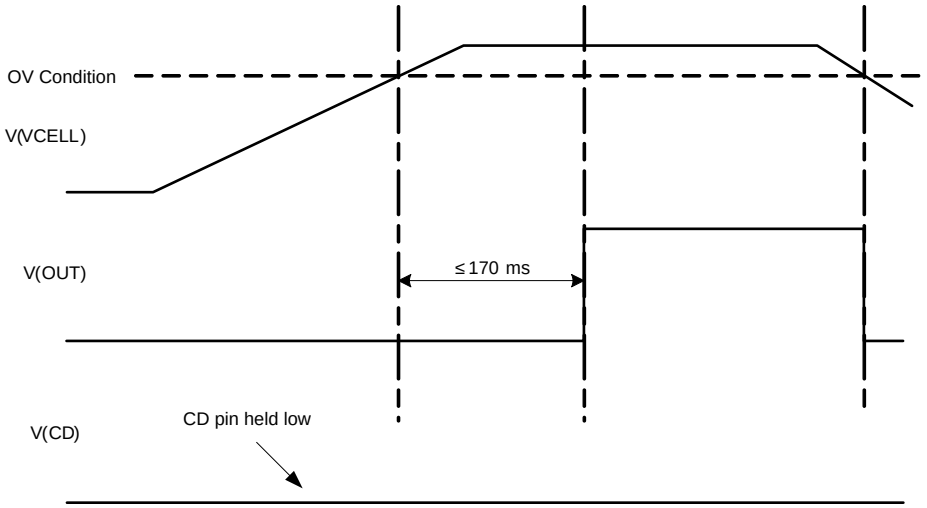


Figure 13. Timing for Customer Test Mode

Figure 14 shows the measurement for current consumption for the product for both VDD and Vx.

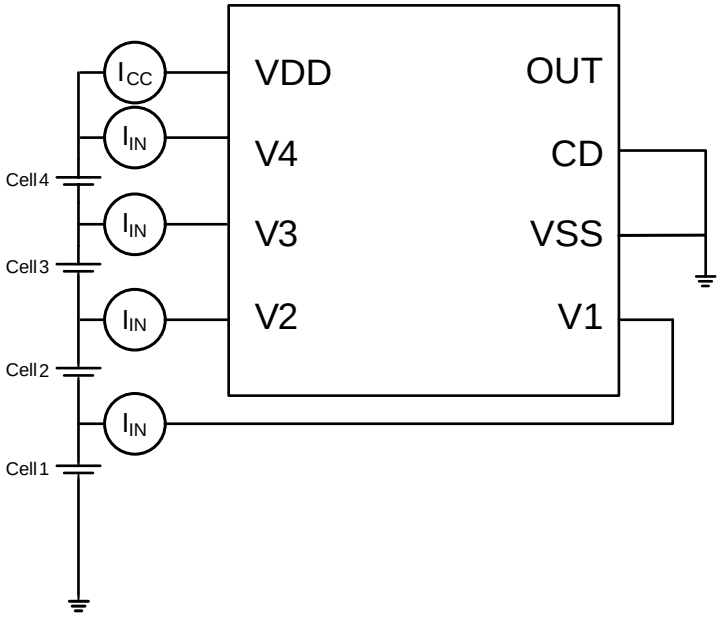


Figure 14. Configuration for IC Current Consumption Test

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REVISION HISTORY

Changes from Original (December 2012) to Revision A	Page
• Added the bq771604 device to Production Data	2

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
BQ771600DPJR	ACTIVE	WSON	DPJ	8	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR		771600	Samples
BQ771600DPJT	ACTIVE	WSON	DPJ	8	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR		771600	Samples
BQ771601DPJR	ACTIVE	WSON	DPJ	8	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR		771601	Samples
BQ771601DPJT	ACTIVE	WSON	DPJ	8	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR		771601	Samples
BQ771602DPJR	ACTIVE	WSON	DPJ	8	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR		771602	Samples
BQ771602DPJT	ACTIVE	WSON	DPJ	8	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR		771602	Samples
BQ771604DPJR	ACTIVE	WSON	DPJ	8	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 85	771604	Samples
BQ771604DPJT	ACTIVE	WSON	DPJ	8	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 85	771604	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

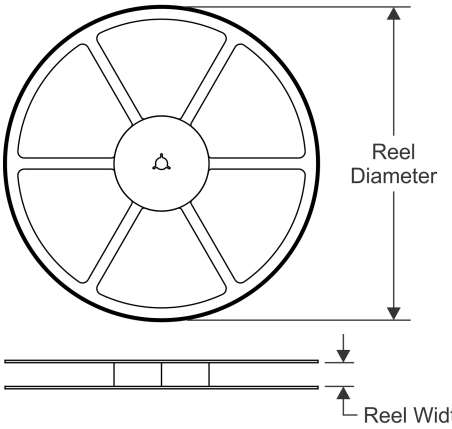
(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

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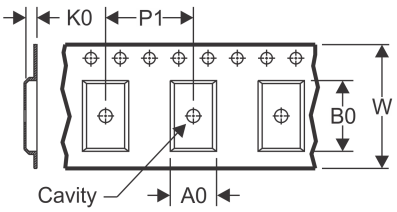
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TAPE AND REEL INFORMATION

REEL DIMENSIONS

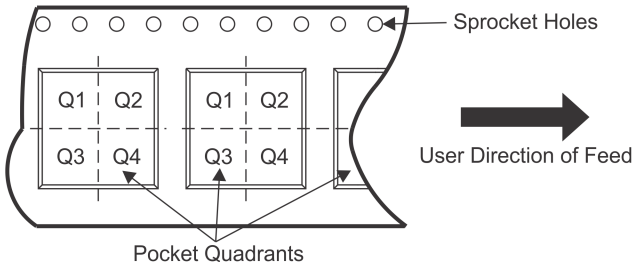


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

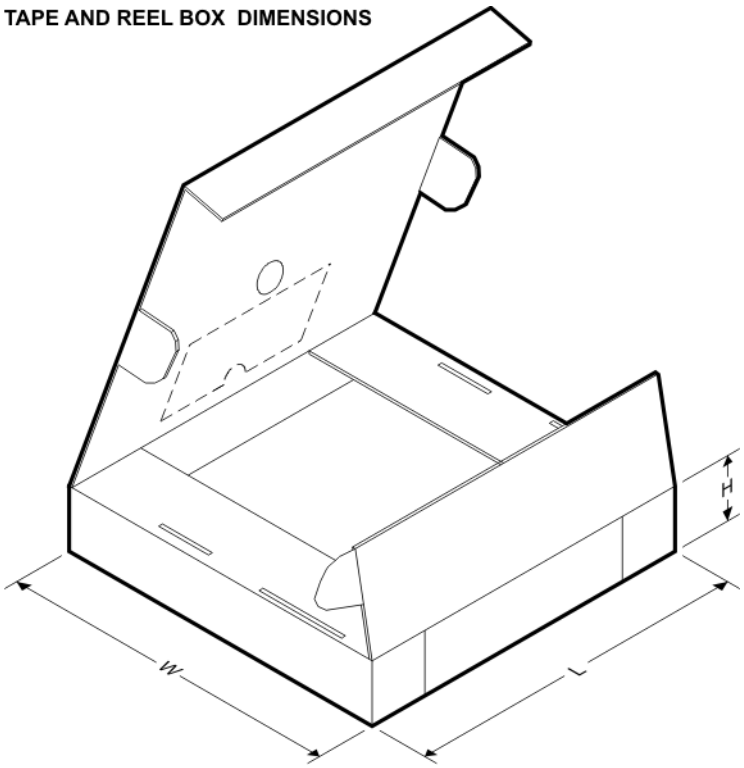
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
BQ771600DPJR	WSON	DPJ	8	3000	330.0	12.4	3.3	4.3	1.1	8.0	12.0	Q2
BQ771600DPJT	WSON	DPJ	8	250	180.0	12.4	3.3	4.3	1.1	8.0	12.0	Q2
BQ771601DPJR	WSON	DPJ	8	3000	330.0	12.4	3.3	4.3	1.1	8.0	12.0	Q2
BQ771601DPJT	WSON	DPJ	8	250	180.0	12.4	3.3	4.3	1.1	8.0	12.0	Q2
BQ771602DPJR	WSON	DPJ	8	3000	330.0	12.4	3.3	4.3	1.1	8.0	12.0	Q2
BQ771602DPJT	WSON	DPJ	8	250	180.0	12.4	3.3	4.3	1.1	8.0	12.0	Q2
BQ771604DPJR	WSON	DPJ	8	3000	330.0	12.4	3.3	4.3	1.1	8.0	12.0	Q2
BQ771604DPJT	WSON	DPJ	8	250	180.0	12.4	3.3	4.3	1.1	8.0	12.0	Q2

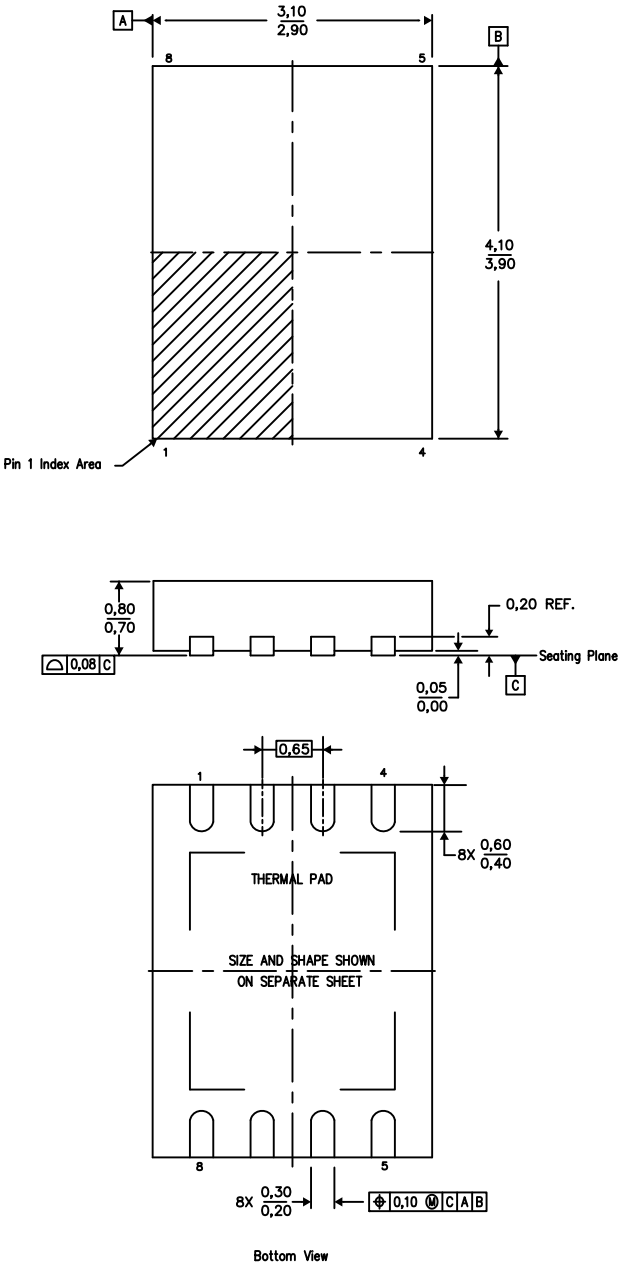
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
BQ771600DPJR	WSON	DPJ	8	3000	367.0	367.0	35.0
BQ771600DPJT	WSON	DPJ	8	250	210.0	185.0	35.0
BQ771601DPJR	WSON	DPJ	8	3000	367.0	367.0	35.0
BQ771601DPJT	WSON	DPJ	8	250	210.0	185.0	35.0
BQ771602DPJR	WSON	DPJ	8	3000	367.0	367.0	35.0
BQ771602DPJT	WSON	DPJ	8	250	210.0	185.0	35.0
BQ771604DPJR	WSON	DPJ	8	3000	367.0	367.0	35.0
BQ771604DPJT	WSON	DPJ	8	250	210.0	185.0	35.0

DPJ (R–PWSON–N8) PLASTIC SMALL OUTLINE NO–LEAD



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NOTES:
A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M–1994.
B. This drawing is subject to change without notice.
C. Small Outline No–Lead (SON) package configuration.
D. The package thermal pad must be soldered to the board for thermal and mechanical performance.
E. See the additional figure in the Product Data Sheet for details regarding the exposed thermal pad features and dimensions.

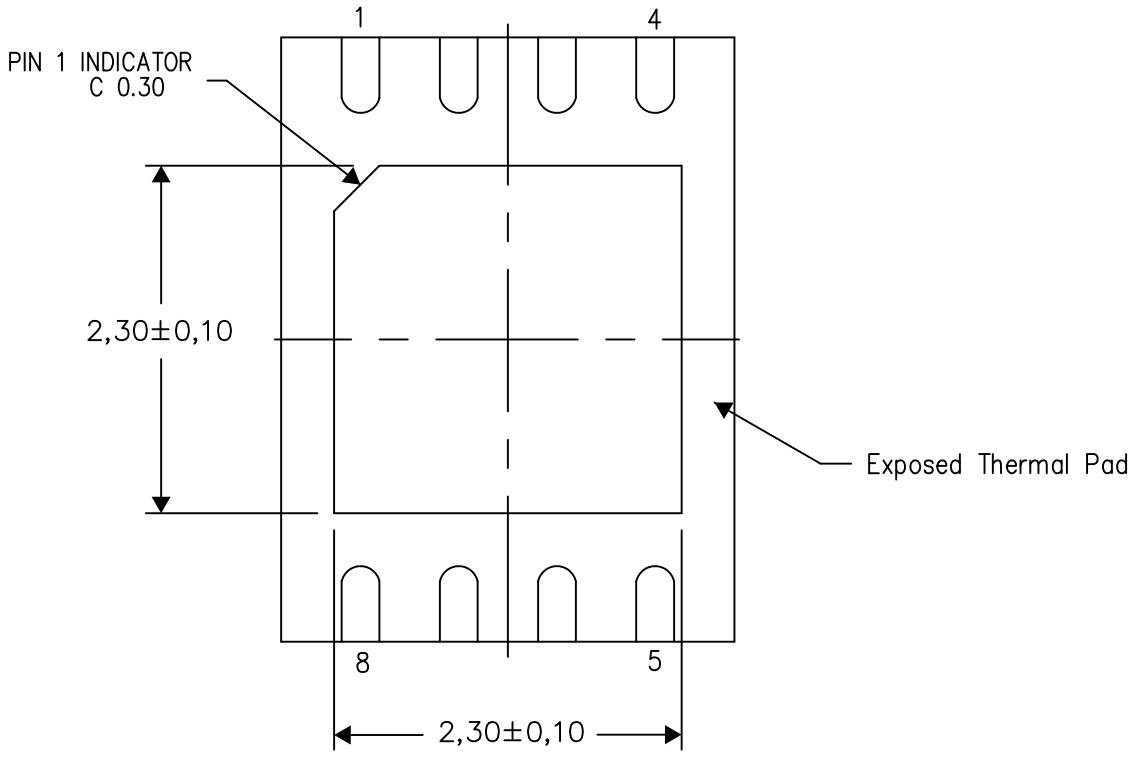
DPJ (R–PWSON–N8) PLASTIC SMALL OUTLINE NO–LEAD

THERMAL INFORMATION

This package incorporates an exposed thermal pad that is designed to be attached directly to an external heatsink. The thermal pad must be soldered directly to the printed circuit board (PCB). After soldering, the PCB can be used as a heatsink. In addition, through the use of thermal vias, the thermal pad can be attached directly to the appropriate copper plane shown in the electrical schematic for the device, or alternatively, can be attached to a special heatsink structure designed into the PCB. This design optimizes the heat transfer from the integrated circuit (IC).

For information on the Quad Flatpack No–Lead (QFN) package and its advantages, refer to Application Report, QFN/SON PCB Attachment, Texas Instruments Literature No. SLUA271. This document is available at www.ti.com.

The exposed thermal pad dimensions for this package are shown in the following illustration.



Bottom View

Exposed Thermal Pad Dimensions

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NOTE: All linear dimensions are in millimeters

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