rev 1.4

LCD Panel EMI Reduction IC

Features

- FCC approved method of EMI attenuation.
- Provides up to 15dB of EMI suppression
- Generates a low EMI spread spectrum clock of the input frequency
- 50MHz to 170MHz input frequency range
- Optimized for 54MHz, 65MHz, 81MHz, 140MHz, and 162MHz pixel clock frequencies
- Internal loop filter minimizes external components and board space
- 8 selectable spread ranges, up to ± 2.2%
- SSON# control pin for spread spectrum enable and disable options
- 2 selectable modulation rates
- Low Cycle-to-cycle jitter
- 3.3V Operating Voltage
- Ultra low power CMOS design
- Supports most mobile graphic accelerator and LCD timing controller specifications
- Available in 8 pin SOIC and TSSOP Packages

Product Description

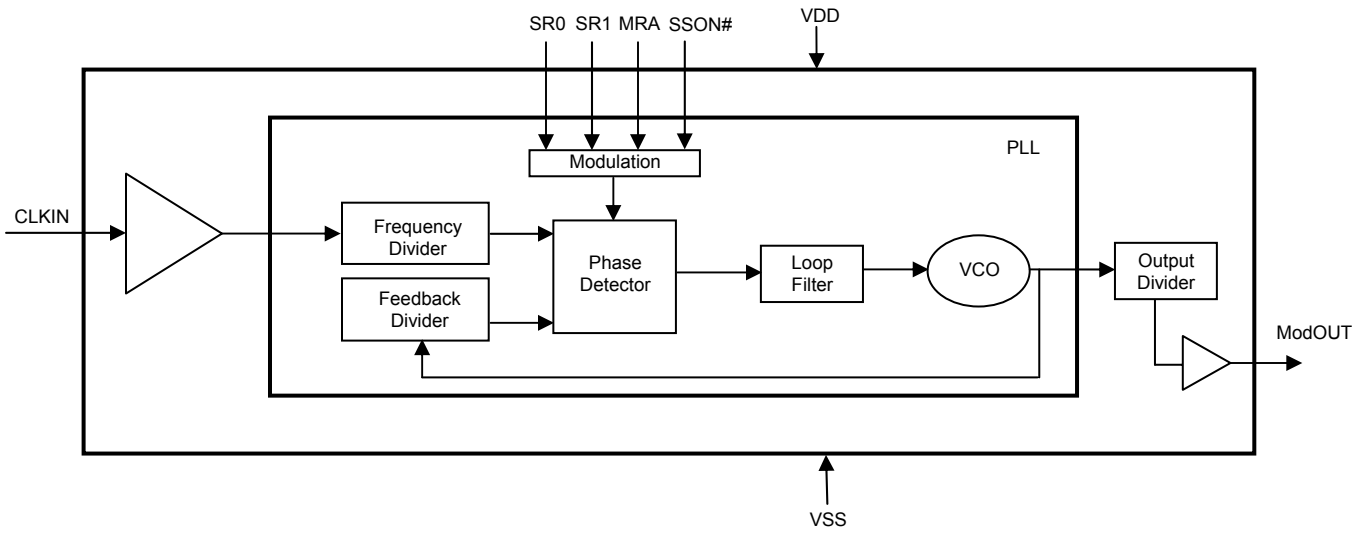
The P2040C is a selectable spread spectrum frequency modulator designed specifically for digital flat panel applications. The P2040C reduces electromagnetic interference (EMI) at the clock source which provides system wide reduction of EMI of all clock dependent signals. The P2040C allows significant system cost savings by reducing the number of circuit board layers and shielding that are traditionally required to pass EMI regulations.

The P2040C uses the most efficient and optimized modulation profile approved by the FCC and is implemented in a proprietary all-digital method. The P2040C modulates the output of a single PLL in order to "spread" the bandwidth of a synthesized clock and, more importantly, decreases the peak amplitudes of its harmonics. This result in a significantly lower system EMI compared to the typical narrow band signal produced by oscillators and most frequency generators. Lowering EMI by increasing a signal's bandwidth is called 'spread spectrum clock generation'.

Applications

The P2040C is targeted towards digital flat panel applications for Notebook PCs, Palm-size PCs, Office Automation Equipments and LCD Monitors.

Block Diagram

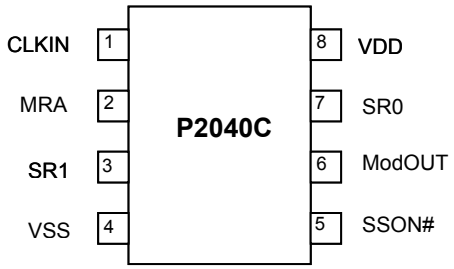


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Pin Configuration



Pin Description

Pin#	Pin Name	Type	Description
1	CLKIN	I	External reference frequency input. Connect to externally generated reference signal.
2	MRA	I	Digital logic input used to select modulation rate. This pin has an internal pull-up resistor.
3	SR1	I	Digital logic input used to select Spreading Range. This pin has an internal pull-up resistor.
4	VSS	P	Ground to entire chip. Connect to system ground.
5	SSON#	I	Digital logic input used to enable Spread Spectrum function (Active LOW). Spread Spectrum function enabled when LOW, disabled when HIGH. This pin has an internal pull-low resistor.
6	ModOUT	O	Spread spectrum Clock Output.
7	SR0	I	Digital logic input used to select Spreading Range. This pin has an internal pull-up resistor.
8	VDD	P	Power supply for the entire chip.

Modulation Selection (Commercial) – Table 1

MRA	SR1	SR0	Spreading Range					Modulation Rate
			54MHz	65MHz	81MHz	140MHz	162MHz	
0	0	0	±1.4%	±1.2%	±1.0%	±0.6%	±0.4%	(Fin/80) * 62.49KHz
0	0	1	±2.0%	±1.9%	±1.6%	±1.0%	±0.8%	(Fin/80) * 62.49KHz
0	1	0	±1.1%	±0.9%	±0.5%	±0.3%	±0.3%	(Fin/80) * 62.49KHz
0	1	1	±1.8%	±1.5%	±1.0%	±0.54%	±0.4%	(Fin/80) * 62.49KHz
1	0	0	±1.3%	±1.3%	±1.3%	±1.25%	±1.1%	(Fin/80) * 20.83KHz
1	0	1	±2.2%	±2.1%	±2.1%	±2.0%	±1.8%	(Fin/80) * 20.83KHz
1	1	0	±1.4%	±1.3%	±1.4%	±1.2%	±0.9%	(Fin/80) * 20.83KHz
1	1	1	±2.1%	±2.1%	±2.1%	±1.9%	±1.4%	(Fin/80) * 20.83KHz

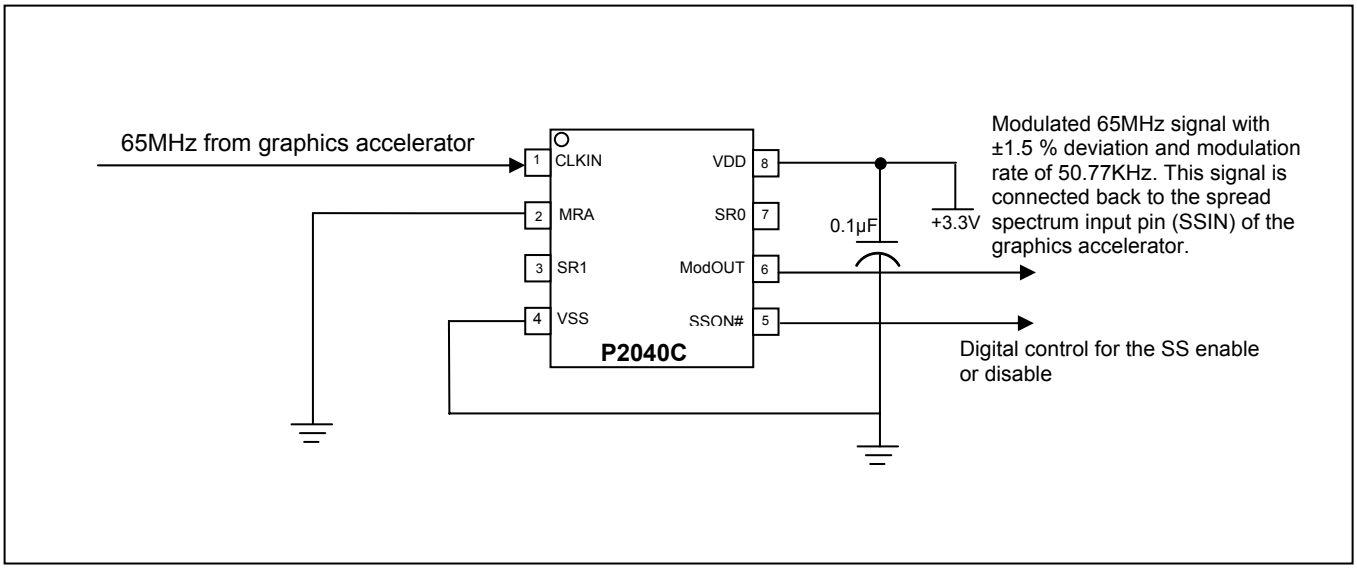
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Spread Spectrum Selection

Table 1 illustrates the possible spread spectrum options. The optimal setting should minimize system EMI to the fullest without affecting system performance. The spreading is described as a percentage deviation of the center frequency
(Note: The center frequency is the frequency of the external reference input on CLKIN, Pin 1).

Example: P2040C is designed for high resolution flat panel applications and is able to support panel frequencies from 50MHz to 170MHz. For a 65MHz pixel clock frequency, a spreading selection of MRA=0, SR1=1 and SR0 =1 provides a percentage deviation of ±1.50% (see Table 1). This result in frequency on ModOUT being swept from 64.03MHz to 65.98MHz at a modulation rate of 50.77KHz (see Table 1). This particular example (see Figure below) given here is a common EMI reduction method for notebook LCD panel and has already been implemented by most of the leading OEM and mobile graphic accelerator manufacturers.

Application Schematic for Mobile LCD Graphics Controllers



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Absolute Maximum Ratings

Symbol	Parameter		Rating	Unit
VDD, V_{IN}	Voltage on any pin with respect to Ground		-0.5 to +7.0	V
T_{STG}	Storage temperature		-65 to +125	°C
T_A	Operating temperature		-20 to +85	°C
T_s	Max. Soldering Temperature (10 sec)		260	°C
θ_{JA}	Thermal Resistance from Junction to Ambient (No Air Flow)	For SOIC Package	156.5	°C/W
		For TSSOP Package	124	
T_J	Junction Temperature		150	°C
T_{DV}	Static Discharge Voltage (As per JEDEC STD22- A114-B)		2	KV

Note: These are stress ratings only and are not implied for functional use. Exposure to absolute maximum ratings for prolonged periods of time may affect device reliability.

DC Electrical Characteristics

(Test condition: All parameters are measured at room temperature (+25°C) unless otherwise stated)

Symbol	Parameter	Min	Typ	Max	Unit
V_{IL}	Input low voltage	VSS - 0.3	-	0.8	V
V_{IH}	Input high voltage	2.0	-	VDD + 0.3	V
I_{IL}	Input low current (pull-up resistor on inputs SR0, SR1 and MRA)	-	-	-40	µA
I_{IH}	Input high current (pull-down resistor on input SSON#)	-	-	40	µA
V_{OL}	Output low voltage (VDD = 3.3V, I_{OL} = 20mA)	-	-	0.4	V
V_{OH}	Output high voltage (VDD = 3.3V, I_{OL} = 20mA)	2.5	-	-	V
I_{DD}	Static supply current standby mode	-	0.7	-	mA
I_{CC}	Dynamic supply current (3.3V and 10pF loading)	9	16	22	mA
VDD	Operating Voltage	3.0	3.3	3.6	V
t_{ON}	Power-up time (first locked cycle after power up)	-	0.18	-	mS
Z_{OUT}	Clock output impedance	-	50	-	Ω

AC Electrical Characteristics

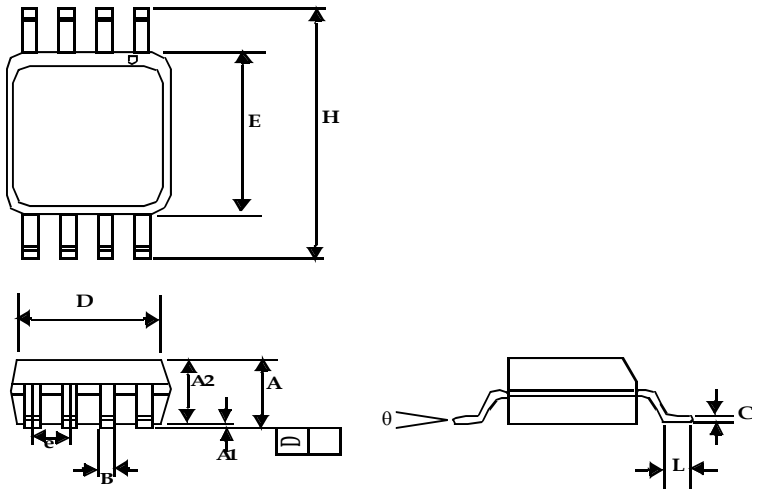
Symbol	Parameter	Min	Typ	Max	Unit
f_{IN}	Input frequency	50		170	MHz
t_{LH}*	Output rise time (measured at 0.8V to 2.0V)	0.3	0.7	1.0	nS
t_{HL}*	Output fall time (measured at 2.0V to 0.8V)	0.3	0.7	1.0	nS
t_{JC}	Jitter (cycle to cycle)	-	-	360	pS
t_D	Output duty cycle	45	50	55	%

*t_{LH} and t_{HL} are measured into a capacitive load of 15pF

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Package Information

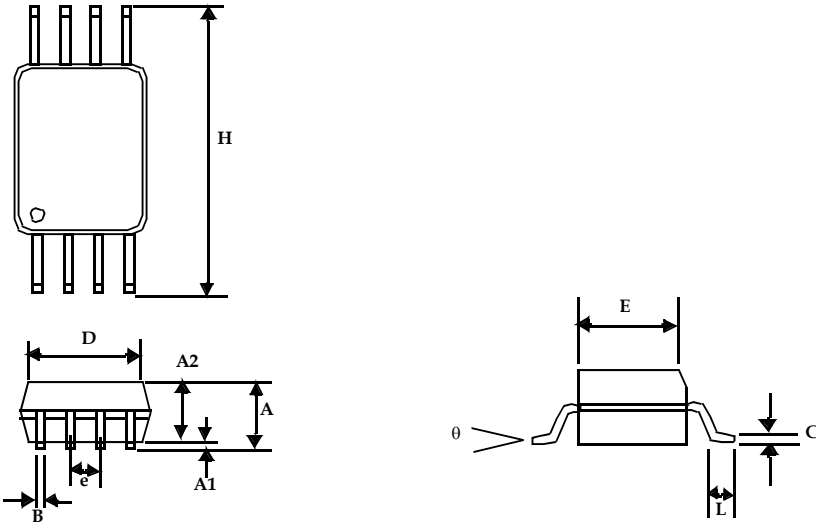
8-lead (150-mil) SOIC Package



Symbol	Dimensions			
	Inches		Millimeters	
	Min	Max	Min	Max
A1	0.004	0.010	0.10	0.25
A	0.053	0.069	1.35	1.75
A2	0.049	0.059	1.25	1.50
B	0.012	0.020	0.31	0.51
C	0.007	0.010	0.18	0.25
D	0.193 BSC		4.90 BSC	
E	0.154 BSC		3.91 BSC	
e	0.050 BSC		1.27 BSC	
H	0.236 BSC		6.00 BSC	
L	0.016	0.050	0.41	1.27
θ	0°	8°	0°	8°

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8-lead Thin Shrunk Small Outline Package (4.40-MM Body)



Symbol	Dimensions			
	Inches		Millimeters	
	Min	Max	Min	Max
A		0.043		1.10
A1	0.002	0.006	0.05	0.15
A2	0.033	0.037	0.85	0.95
B	0.008	0.012	0.19	0.30
c	0.004	0.008	0.09	0.20
D	0.114	0.122	2.90	3.10
E	0.169	0.177	4.30	4.50
e	0.026 BSC		0.65 BSC	
H	0.252 BSC		6.40 BSC	
L	0.020	0.028	0.50	0.70
θ	0°	8°	0°	8°

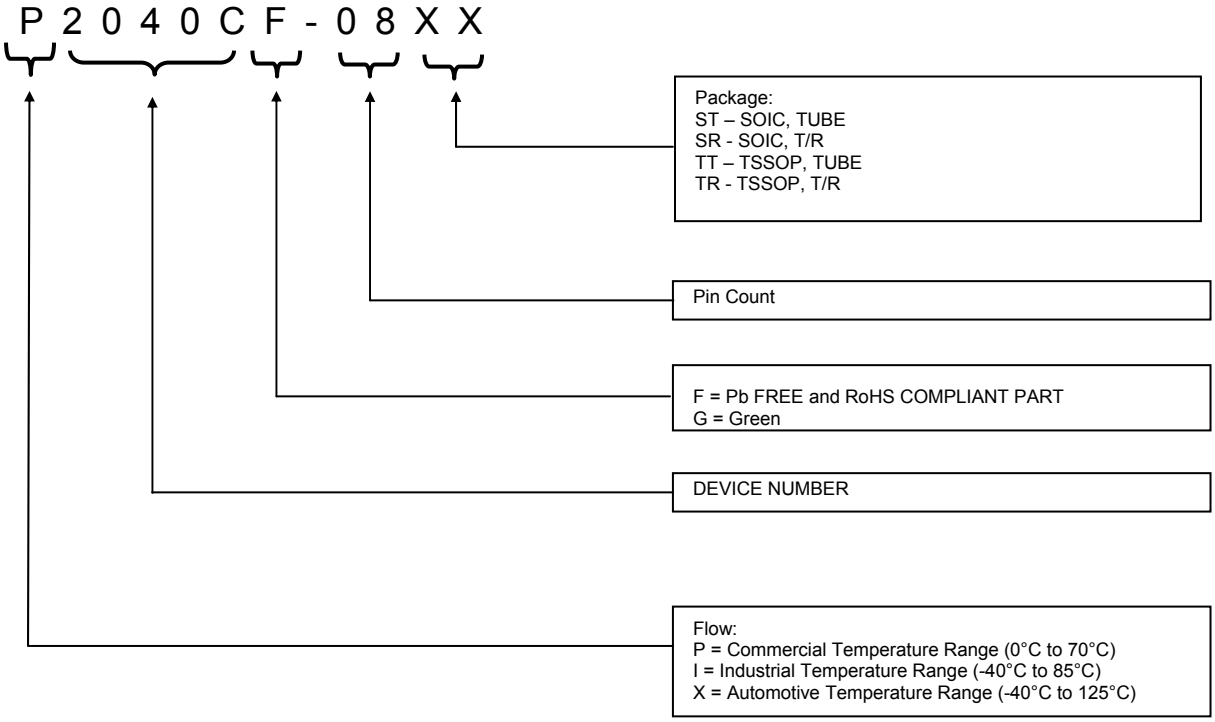
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Ordering Information

Part Number	Marking	Package Type	Qty/reel	Temperature
P2040C-08ST	P2040C	8-Pin SOIC, TUBE		See Flow
P2040C-08SR	P2040C	8-Pin SOIC, TAPE & REEL	2500	See Flow
P2040C-08TT	P2040C	8-Pin TSSOP, TUBE		See Flow
P2040C-08TR	P2040C	8-Pin TSSOP, TAPE & REEL	2500	See Flow
I2040C-08ST	I2040C	8-Pin SOIC, TUBE		See Flow
I2040C-08SR	I2040C	8-Pin SOIC, TAPE & REEL	2500	See Flow
I2040C-08TT	I2040C	8-Pin TSSOP, TUBE		See Flow
I2040C-08TR	I2040C	8-Pin TSSOP, TAPE & REEL	2500	See Flow
X2040C-08ST	X2040C	8-Pin SOIC, TUBE		See Flow
X2040C-08SR	X2040C	8-Pin SOIC, TAPE & REEL	2500	See Flow
X2040C-08TT	X2040C	8-Pin TSSOP, TUBE		See Flow
X2040C-08TR	X2040C	8-Pin TSSOP, TAPE & REEL	2500	See Flow
P2040CF-08ST	P2040CF	8-Pin SOIC, TUBE, Pb Free		See Flow
P2040CF-08SR	P2040CF	8-Pin SOIC, TAPE & REEL, Pb Free	2500	See Flow
P2040CF-08TT	P2040CF	8-Pin TSSOP, TUBE, Pb Free		See Flow
P2040CF-08TR	P2040CF	8-Pin TSSOP, TAPE & REEL, Pb Free	2500	See Flow
I2040CF-08ST	I2040CF	8-Pin SOIC, TUBE, Pb Free		See Flow
I2040CF-08SR	I2040CF	8-Pin SOIC, TAPE & REEL, Pb Free	2500	See Flow
I2040CF-08TT	I2040CF	8-Pin TSSOP, TUBE, Pb Free		See Flow
I2040CF-08TR	I2040CF	8-Pin TSSOP, TAPE & REEL, Pb Free	2500	See Flow
X2040CF-08ST	X2040CF	8-Pin SOIC, TUBE, Pb Free		See Flow
X2040CF-08SR	X2040CF	8-Pin SOIC, TAPE & REEL, Pb Free	2500	See Flow
X2040CF-08TT	X2040CF	8-Pin TSSOP, TUBE, Pb Free		See Flow
X2040CF-08TR	X2040CF	8-Pin TSSOP, TAPE & REEL, Pb Free	2500	See Flow
P2040CG-08ST	P2040CG	8-Pin SOIC, TUBE, Green		See Flow
P2040CG-08SR	P2040CG	8-Pin SOIC, TAPE & REEL, Green	2500	See Flow
P2040CG-08TT	P2040CG	8-Pin TSSOP, TUBE, Green		See Flow
P2040CG-08TR	P2040CG	8-Pin TSSOP, TAPE & REEL, Green	2500	See Flow
I2040CG-08ST	I2040CG	8-Pin SOIC, TUBE, Green		See Flow
I2040CG-08SR	I2040CG	8-Pin SOIC, TAPE & REEL, Green	2500	See Flow
I2040CG-08TT	I2040CG	8-Pin TSSOP, TUBE, Green		See Flow
I2040CG-08TR	I2040CG	8-Pin TSSOP, TAPE & REEL, Green	2500	See Flow
X2040CG-08ST	X2040CG	8-Pin SOIC, TUBE, Green		See Flow
X2040CG-08SR	X2040CG	8-Pin SOIC, TAPE & REEL, Green	2500	See Flow
X2040CG-08TT	X2040CG	8-Pin TSSOP, TUBE, Green		See Flow
X2040CG-08TR	X2040CG	8-Pin TSSOP, TAPE & REEL, Green	2500	See Flow

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Device Ordering Information



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Preliminary Information
Part Number: P2040C
Document Version: v1.4

Note: This product utilizes US Patent # 6,646,463 Impedance Emulator Patent issued to Alliance Semiconductor, dated 11-11-2003

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