



Actual Size
4 mm x 4 mm



SLVS493B – MARCH 2004 – REVISED SEPTEMBER 2004

# POSITIVE AND NEGATIVE OUTPUT DC-DC CONVERTER

## FEATURES

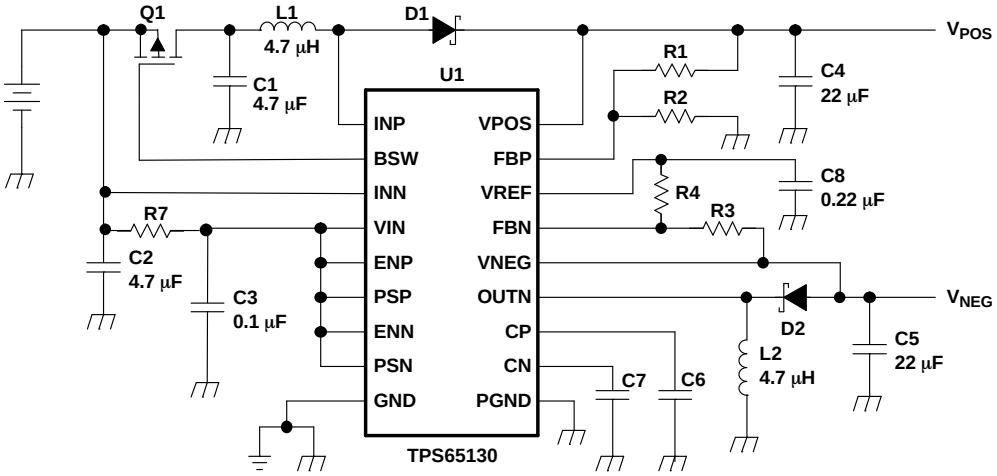
- **Dual Adjustable Output Voltages Up to +15 V and Down to –15 V**
- **800-mA Typical Switch Current Limit at Boost and Inverter Main Switches at TPS65130**
- **2-A Typical Switch Current Limit at Boost and Inverter Main Switches at TPS65131**
- **Up to 89% Efficiency at Positive Output Voltage Rail**
- **Up to 81% Efficiency at Negative Output Voltage Rail**
- **Power-Save Mode for High Efficiency at Low Load Currents**
- **Independent Enable Inputs for Power Up and Power Down Sequencing**
- **Control Output for External PFET to Support Completely Disconnecting the Battery**
- **2.7-V to 5.5-V Input Voltage Range**
- **Minimum 1.25-MHz Fixed Frequency PWM Operation**
- **Thermal Shutdown**
- **Overvoltage Protection on Both Outputs**
- **1-µA Shutdown Current**
- **Small 4 mm x 4 mm QFN-24 Package (RGE)**

## APPLICATIONS

- **Small to Medium Size OLED Displays**
- **(TFT) LCD and CCD Bias Supply**
- **PDAs, Pocket PCs, Smartphones**
- **Digital Cameras**
- **Camcorders**

## DESCRIPTION

The TPS65130/1 is dual-output dc-dc converter generating a positive output voltage up to 15 V and a negative output voltage down to -15 V with output currents in a 200-mA range in typical applications, depending on input voltage to output voltage ratio. With a total efficiency up to 85%, the device is ideal for portable battery-powered equipment. The input voltage range of 2.7 V to 5.5 V allows the TPS65130/1 to be directly powered from a Li-ion battery, from 3 cells NiMH/NiCd or alkaline batteries. The TPS65130/1 comes in a small 4 mm x 4 mm QFN-24 package. Together with a minimum switching frequency of 1.25 MHz it enables designing small power supply applications because it requires only a few small external components.




Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.

PowerPAD is a trademark of Texas Instruments.

PRODUCTION DATA information is current as of publication date. Products conform to specifications per the terms of the Texas Instruments standard warranty. Production processing does not necessarily include testing of all parameters.

Copyright © 2004, Texas Instruments Incorporated



This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

## DESCRIPTION (CONTINUED)

The converter operates with a fixed frequency PWM control topology and, if power-save mode is enabled, it uses a pulse-skipping mode at light load currents. It operates with only 500-µA device quiescent current. Independent enable pins allow power up and power down sequencing for both outputs. The device has an internal current limit overvoltage protection and a thermal shutdown for highest reliability under fault conditions.

### ORDERING INFORMATION

| $T_A$ | SWITCH CURRENT LIMIT | | PART NUMBER(1) |
|---|---|---|---|
| | BOOST CONVERTER | INVERTING CONVERTER | |
| –40°C to 85°C | 800 mA | 800 mA | TPS65130RGE |
| –40°C to 85°C | 1950 mA | 1950 mA | TPS65131RGE |

(1) The RGE package is availabletaped and reeled. Add an R suffix to the device type (i.e., TPS65130RGER) toorder quantities of 3000 devices per reel. It is also available in minireels. Add a T suffix to the device type (i.e., TPS65130RGET) toorder quantities of 250 devices per reel.

## ABSOLUTE MAXIMUM RATINGS

over operating free-air temperature range unless otherwise noted(1)

| | | TPS65130/1 |
|---|---|---|
| VIN, INN | Input voltage range at pins (2) | –0.3 V to +6.0 V |
| VPOS | Maximum voltage at pin (2) | 17 V |
| VNEG | Minimum voltage at pin (2) | –17 V |
| | Voltage at pins ENN, ENP, FBP, FBN, CN, CP, PSP, PSN, BSW (2) | –0.3 V to $V_{IN}$ + 0.3 V |
| INP | Input voltage at pin (2) | 17 V |
| | Differential voltage between pins OUTN to $V_{INN}$(2) | 24 V |
| $T_J$ | Operating virtual junction temperature | –40°C to 150°C |
| $T_{STG}$ | Storage temperature range | –65°C to 150°C |

(1) Stresses beyond those listedunder "absolute maximum ratings" may cause permanent damage to thedevice. These are stress ratings only, and functional operation of the deviceat these or any other conditions beyond those indicated under "recommendedoperating conditions" is not implied. Exposure to absolute-maximum-ratedconditions for extended periods may affect device reliability.
(2) All voltage values are withrespect to network ground terminal, unless otherwisenoted.

## DISSIPATION RATINGS TABLE(1)

| PACKAGE | $\Theta_{JA}$ | $\Theta_{JB}$ | $\Theta_{JC}$ | $T_A \leq 25°C$ POWER RATING | DERATING FACTOR ABOVE $T_A = 25°C$ | $T_A = 70°C$ POWER RATING | $T_A = 85°C$ POWER RATING |
|---|---|---|---|---|---|---|---|
| RGE | 37.8 °C/W | 27.8 °C/W | 57.9 °C/W | 2646 mW | 26 mW/°C | 1455 mW | 1058 mW |

(1) This thermal data is based on assembly of the device on a JEDEC high K board. The PowerPAD must be soldered on a pad on the board. There must be vias within the pad that contact the ground plane in the PCB. Exceeding the maximum junctiontemperature will force the device into thermalshutdown.

## RECOMMENDED OPERATING CONDITIONS

| | | MIN | NOM | MAX | UNIT |
|---|---|---|---|---|---|
| $V_I$ | Input voltage range | 2.7 | | 5.5 | V |
| $T_A$ | Operating free-air temperature range | -40 | | 85 | °C |
| $T_J$ | Operating virtual junction temperature range | -40 | | 125 | °C |

## ELECTRICAL CHARACTERISTICS

Over recommended free-air temperature range and over recommended input voltage range, typical at an ambient temperature of 25°C (unless otherwise noted)

| PARAMETER | | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|---|
| **DC-DC STAGE ($V_{POS}$, $V_{NEG}$)** | | | | | | |
| $V_{POS}$ | Adjustable output voltage range | | $V_{IN}$+ 0.5 V | | 15 | V |
| $V_{NEG}$ | Adjustable output voltage range | | -15 | | -2 | V |
| $V_{REF}$ | Reference voltage | $I_{REF}$ = 10 µA | 1.2 | 1.213 | 1.225 | V |
| $I_{FBP}$ | Positive feedback input bias current | $V_{FBP} = V_{REF}$ | | 50 | | nA |
| $I_{FBN}$ | Negative feedback input bias current | $V_{FBN}$ = 0.1 $V_{REF}$ | | 50 | | nA |
| $V_{FBP}$ | Positive feedback regulation voltage | $V_{IN}$ = 2.7 V to 5.5 V | 1.189 | 1.213 | 1.237 | V |
| $V_{FBN}$ | Negative feedback regulation voltage | $V_{IN}$ = 2.7 V to 5.5 V | -0.024 | 0 | 0.024 | V |
| | Total Output DC accuracy | | | +3% | | |
| $R_{DS(ONN)}$ | Inverter switch on-resistance | $V_{IN}$ = 3.6 V | | 440 | 620 | mΩ |
| | | $V_{IN}$ = 5.0 V | | 330 | 530 | |
| $I_{LIMN}$ | TPS65130 Inverter switch current limit | 2.7 V < $V_{IN}$ < 5.5 V | 700 | 800 | 900 | mA |
| $I_{LIM}$ | TPS65131 Inverter switch current limit | $V_{IN}$ = 3.6 V | 1800 | 1950 | 2200 | mA |
| $R_{DS(ONP)}$ | Boost switch on-resistance | $V_{POS}$ = 5 V | | 230 | 300 | mΩ |
| | | $V_{POS}$ = 10 V | | 170 | 200 | |
| $I_{LIMP}$ | TPS65130 Boost switch current limit | 2.7 V < $V_{IN}$ < 5.5 V | 700 | 800 | 900 | mA |
| $I_{LIMP}$ | TPS65131 Boost switch current limit | $V_{IN}$ = 3.6 V, $V_{POS}$ = 8.0 V | 1800 | 1950 | 2200 | mA |
| $D_{MAXP}$ | Maximum duty cycle boost converter | | | 87.5% | | |
| $D_{MAXN}$ | Maximum duty cycle inverting converter | | | 87.5% | | |
| $D_{MINP}$ | Minimum duty cycle boost converter | | | 12.5% | | |
| $D_{MINN}$ | Minimum duty cycle inverting converter | | | 12.5% | | |
| **CONTROL STAGE** | | | | | | |
| $f_S$ | Oscillator frequency | | 1250 | 1380 | 1500 | kHz |
| $V_{ENP,ENN,PSP,PSN}$ | High level input voltage | | 1.4 | | | V |
| $V_{ENP,ENN,PSP,PSN}$ | Low level input voltage | | | | 0.4 | V |
| $I_{ENP,ENN,PSP,PSN}$ | Input current | ENP, ENN, PSP, PSN = GND or VIN | | 0.01 | 0.1 | µA |
| $R_{BSW}$ | Output resistance | | | 27 | | kΩ |
| $V_{IN}$ | Input voltage range | | 2.7 | | 5.5 | V |

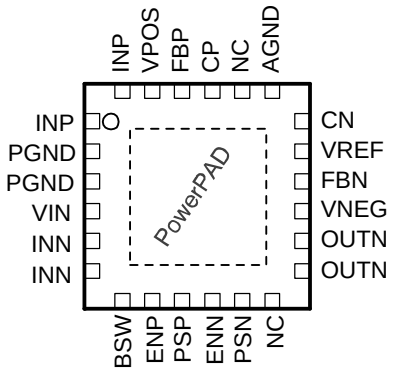
## ELECTRICAL CHARACTERISTICS (continued)

Over recommended free-air temperature range and over recommended input voltage range, typical at an ambient temperature of 25°C (unless otherwise noted)

| PARAMETER | | | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|---|---|
| $I_{(Q)}$ | Quiescent current | VIN | $V_{IN}$ = 3.6 V, $I_{OUTP}$ = $I_{OUTN}$ = 0, ENP = ENN = PSP = PSN = $V_{IN}$, $V_{POS}$ = 8 V, $V_{NEG}$ = -5 V | | 300 | 500 | µA |
| | | VPOS | | | 100 | 120 | µA |
| | | VNEG | | | 100 | 120 | µA |
| $I_{SD}$ | Shutdown supply current | | ENN = ENP = GND | | 0.2 | 1.5 | µA |
| $V_{UVLO}$ | Undervoltage lockout threshold | | | 2.1 | 2.35 | 2.7 | V |
| | Thermal shutdown | | | | 150 | | °C |
| | Thermal shutdown hysteresis | | Junction temperature decreasing | | 5 | | °C |

## PIN ASSIGNMENTS

**HTTSOP PowerPAD™**
**(TOP VIEW)**




NC − No internal connection

### Terminal Functions

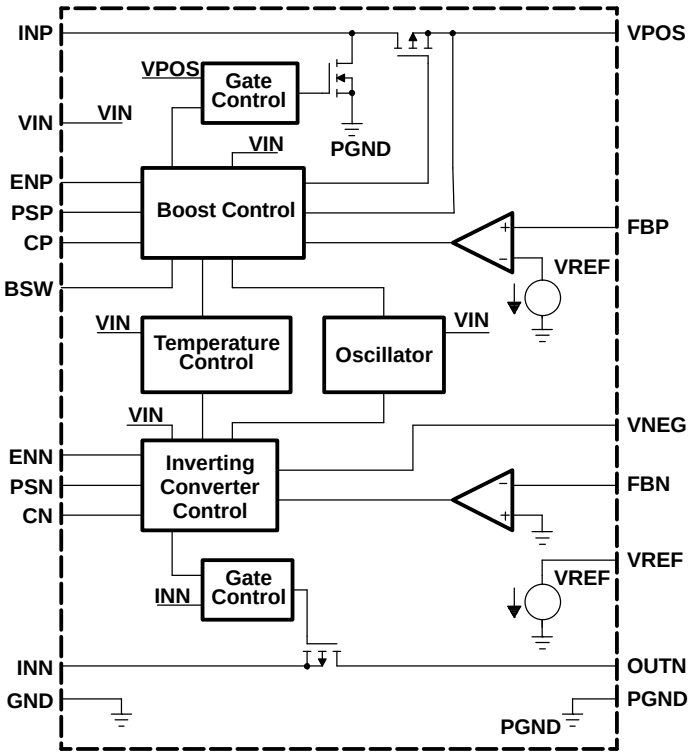
| TERMINAL NAME | TERMINAL NO. | I/O | DESCRIPTION |
|---|---|---|---|
| INP | 1, 24 | I | Boost converter switch input. |
| INN | 5, 6 | I | Inverting converter switch input |
| PGND | 2, 3 | | Power ground pin |
| AGND | 19 | | Analog ground pin |
| ENN | 10 | I | Enable pin for the negative output voltage (0 V: disabled, VIN: enabled) |
| ENP | 8 | I | Enable pin for the positive output voltage (0 V: disabled, VIN: enabled) |
| FBN | 16 | I | Feedback pin for the negative output voltage divider |
| FBP | 22 | I | Feedback pin for the positive output voltage divider |
| OUTN | 13, 14 | O | Inverting converter switch output. |
| VREF | 17 | O | Reference output voltage. Bypass this pin with a 220-nF capacitor to ground. Connect the lower resistor of the negative output voltage divider to this pin |
| CP | 21 | | Compensation pin for boost converter control |
| CN | 18 | | Compensation pin for inverting converter control |
| VIN | 4 | I | Control supply input |
| VPOS | 23 | I | Positive output voltage sense input |
| VNEG | 15 | I | Negative output voltage sense input |

## PIN ASSIGNMENTS (continued)

### Terminal Functions (continued)

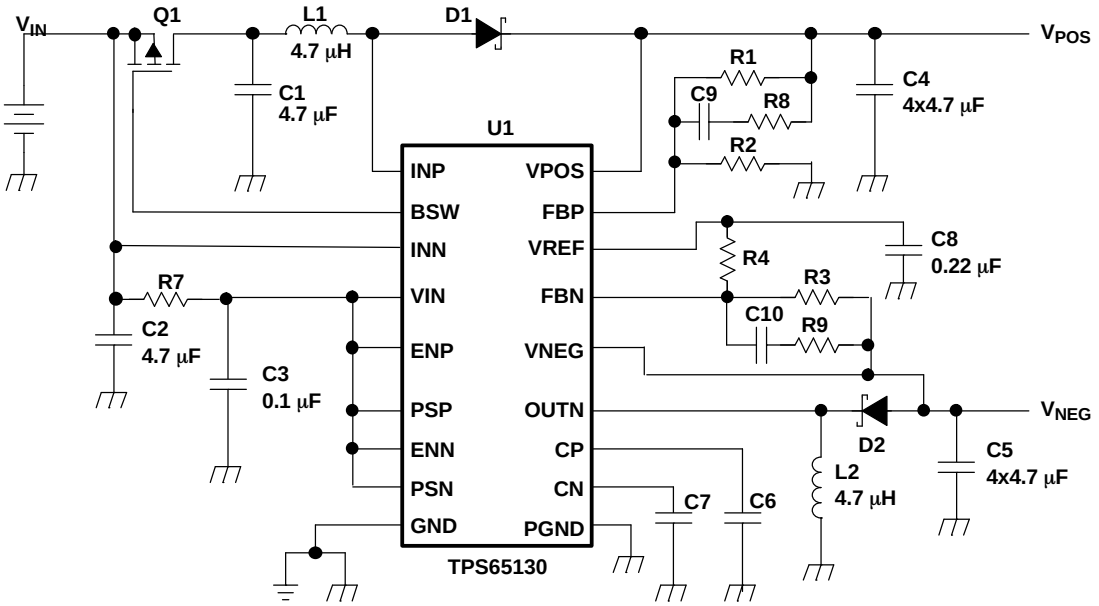
| TERMINAL NAME | TERMINAL NO. | I/O | DESCRIPTION |
|---|---|---|---|
| PSP | 9 | I | Power-save mode enable for boost converter stage (0 V: disabled, VIN: enabled) |
| PSN | 11 | I | Power-save mode enable for inverter stage (0 V: disabled, VIN: enabled) |
| BSW | 7 | O | Gate control pin for external battery switch. This pin goes low when ENP is set high. |
| NC | 12, 20 | | Not connected |

### FUNCTIONAL BLOCK DIAGRAM



## TYPICAL CHARACTERISTICS

## PARAMETER MEASUREMENT INFORMATION




### List of Components

| REFERENCE | DESCRIPTION |
|---|---|
| C1, C2 | X7R/X5R ceramic |
| C4, C5 | 4x4.7 µF X7R/X5R ceramic |
| D1, D2 | MBRM120 |
| L1, L2 | Wurth Elektronik 7447789004 (TPS65130), EPCOS B82462-G4472 (TPS65131) |

## PERFORMANCE GRAPHS

### Table of Graphs

| GRAPH | DESCRIPTION |
|---|---|
| Figure 1 | TPS65130 maximum output current versus input voltage, $V_{POS}$ = 12 V, 8 V, 5 V |
| Figure 2 | TPS65131 maximum output current versus input voltage, $V_{POS}$ = 15 V, 10 V, 5 V |
| Figure 3 | TPS65130 maximum output current versus input voltage, $V_{NEG}$ = –4 V, –8 V, –10 V |
| Figure 4 | TPS65131 maximum output current versus input voltage, $V_{NEG}$ = –4 V, –10 V, –15 V |
| Figure 5 | TPS65130 efficiency versus output current, $V_{POS}$= 5 V |
| Figure 6 | TPS65131 efficiency versus output current, $V_{POS}$= 5 V |
| Figure 7 | TPS65130 efficiency versus output current, $V_{POS}$= 8 V |
| Figure 8 | TPS65131 efficiency versus output current, $V_{POS}$= 10 V |
| Figure 9 | TPS65130 efficiency versus output current, $V_{POS}$= 12 V |
| Figure 10 | TPS65131 efficiency versus output current, $V_{POS}$= 15 V |
| Figure 11 | TPS65130 efficiency versus output current, $V_{NEG}$= –4 V, ($V_{IN}$ = 4 V, 3 V) |
| Figure 12 | TPS65131 efficiency versus output current, $V_{NEG}$= –4 V, ($V_{IN}$ = 5 V, 3 V) |
| Figure 13 | TPS65130 efficiency versus output current, $V_{NEG}$= –8 V, ($V_{IN}$ = 4.2 V, 3 V) |
| Figure 14 | TPS65131 efficiency versus output current, $V_{NEG}$= –10 V, ($V_{IN}$ = 5 V, 3 V) |
| Figure 15 | TPS65130 efficiency versus output current, $V_{NEG}$= –10 V, ($V_{IN}$ = 4.2 V, 3 V) |

## Table of Graphs (continued)

| GRAPH | DESCRIPTION |
|---|---|
| Figure 16 | TPS65131 efficiency versus output current, $V_{NEG}$= –15 V, ($V_{IN}$ = 5 V, 3 V) |
| Figure 17 | TPS65130 efficiency versus input voltage, $V_{POS}$= 5 V in power-save mode |
| Figure 18 | TPS65130 efficiency versus input voltage, $V_{POS}$= 8 V in power-save mode |
| Figure 19 | TPS65130 efficiency versus input voltage, $V_{POS}$= 12 V in power-save mode |
| Figure 20 | TPS65130 efficiency versus input voltage, $V_{NEG}$= –4 V in power-save mode |
| Figure 21 | TPS65130 efficiency versus input voltage, $V_{NEG}$= –8 V in power-save mode |
| Figure 22 | TPS65130 efficiency versus input voltage, $V_{NEG}$= –10 V in power-save mode |
| Figure 23 | TPS65130 efficiency versus output current, $V_O$= 13.5 V (+9 V, –4.5 V), ($V_{IN}$ = 4.2 V, 3 V) |
| Figure 24 | TPS65131 efficiency versus output current, $V_O$= 30 V (±15 V, ($V_{IN}$ 5 V, 3 V) |
| Figure 25 | TPS65130 efficiency versus input voltage, $V_O$= 13.5 V (9 V, –4.5 V) in power save mode |
| Figure 26 | TPS65130 output voltage versus output current, $V_{POS}$= 5 V, $V_{IN}$ = 3 V |
| Figure 27 | TPS65131 output voltage versus output current, $V_{POS}$= 5 V, $V_{IN}$ = 4.2 V |
| Figure 28 | TPS65130 output voltage versus output current, $V_{POS}$= 8 V, $V_{IN}$ = 3 V |
| Figure 29 | TPS65131 output voltage versus output current, $V_{POS}$= 10 V, $V_{IN}$ = 5 V |
| Figure 30 | TPS65130 output voltage versus output current, $V_{POS}$= 12 V ($V_{IN}$ = 3 V) |
| Figure 31 | TPS65131 output voltage versus output current, $V_{POS}$= 15 V ($V_{IN}$ = 5 V) |
| Figure 32 | TPS65130 output voltage versus output current, $V_{NEG}$= –4 V, $V_{IN}$ = 3 V |
| Figure 33 | TPS65131 output voltage versus output current, $V_{NEG}$= –4 V, $V_{IN}$ = 5 V |
| Figure 34 | TPS65130 output voltage versus output current, $V_{NEG}$= –8 V, $V_{IN}$ = 3 V |
| Figure 35 | TPS65131 output voltage versus output current, $V_{NEG}$= –10 V, $V_{IN}$ = 5 V |
| Figure 36 | TPS65130 output voltage versus output current, $V_{NEG}$= –10 V, $V_{IN}$ = 3 V |
| Figure 37 | TPS65131 output voltage versus output current, $V_{NEG}$= –15 V, $V_{IN}$ = 5 V |
| Figure 38 | No load supply current into $V_{IN}$ versus input voltage |
| Figure 39 | No load supply current into $V_{POS}$ versus input voltage |
| Figure 40 | No load supply current into $V_{NEG}$ versus input voltage |
| Figure 41 | Positive output voltage in continuous current mode |
| Figure 42 | Negative output voltage in continuous current mode |
| Figure 43 | Positive output voltage at power-save mode disabled |
| Figure 44 | Negative output voltage at power-save mode disabled |
| Figure 45 | Positive output voltage in power-save mode, $V_I$ = 3.6 V, $V_{POS}$ = 5.5 V |
| Figure 46 | Negative output voltage in power-save mode, $V_I$ = 3.6 V, $V_{NEG}$ = –8 V |
| Figure 47 | Load transient response, $V_I$ = 3.6 V, $V_{POS}$ = 8 V |
| Figure 48 | Load transient response, $V_I$ = 3.6 V, $V_{NEG}$ = –8 V |
| Figure 49 | Line transient response, $V_I$ = 3.6 V to 4.2 V, $V_{POS}$ = 8 V |
| Figure 50 | Line transient response, $V_I$ = 3.6 V to 4.2 V, $V_{NEG}$ = –8 V |
| Figure 51 | Start-up after enable, $V_{POS}$ = 8 V, $V_I$ = 3.6 V |
| Figure 52 | Start-up after enable, $V_{NEG}$ = –8 V, $V_I$ = 3.6 V |

## TYPICAL CHARACTERISTICS

TPS65130
MAXIMUM OUTPUT CURRENT
vs
INPUT VOLTAGE

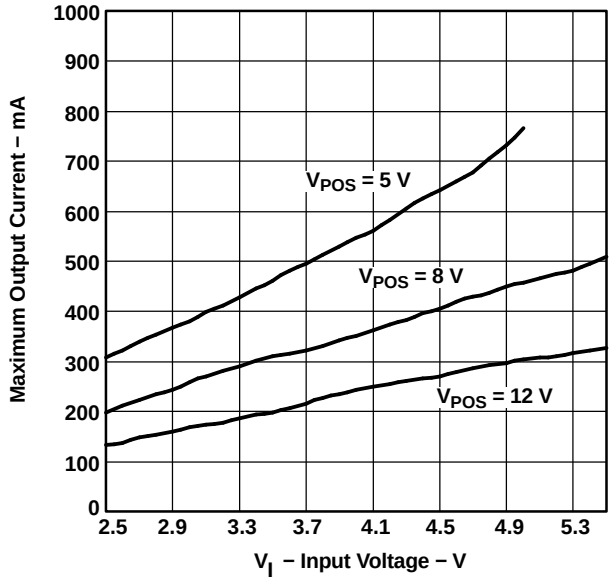



Figure 1.

TPS65131
MAXIMUM OUTPUT CURRENT
vs
INPUT VOLTAGE

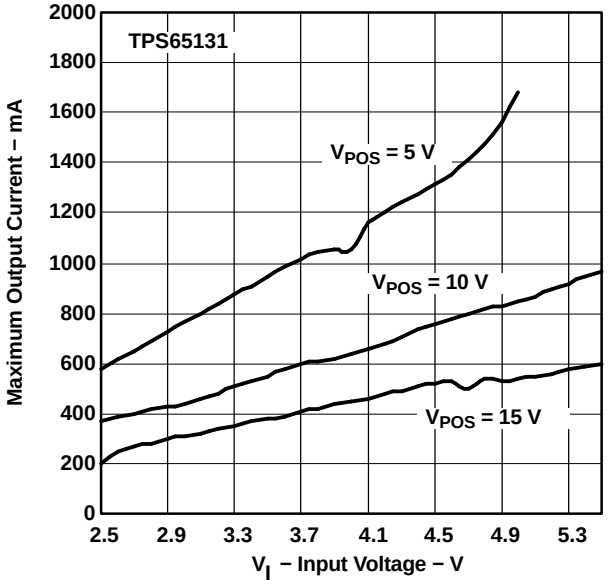



Figure 2.

TPS65130
MAXIMUM OUTPUT CURRENT
vs
INPUT VOLTAGE

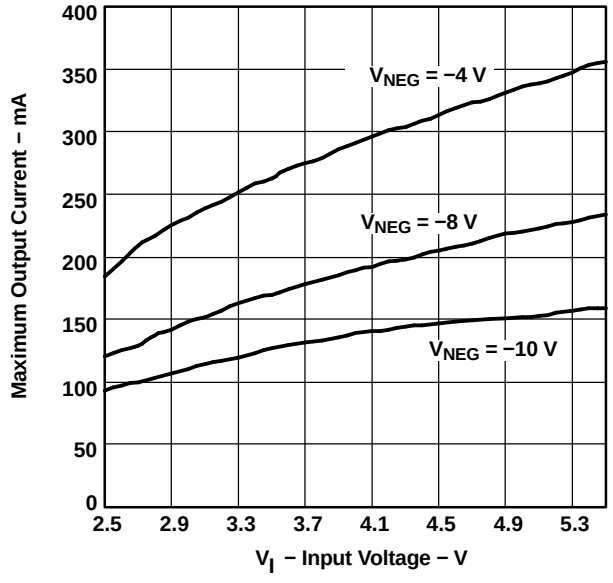



Figure 3.

TPS65131
MAXIMUM OUTPUT CURRENT
vs
INPUT VOLTAGE

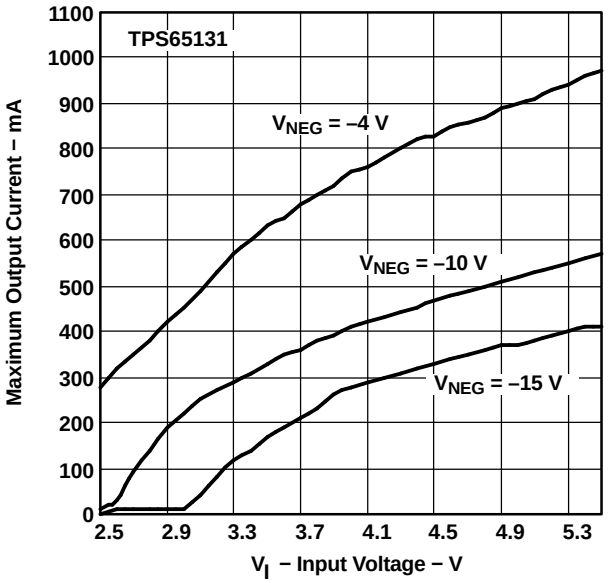



Figure 4.

## TYPICAL CHARACTERISTICS (continued)

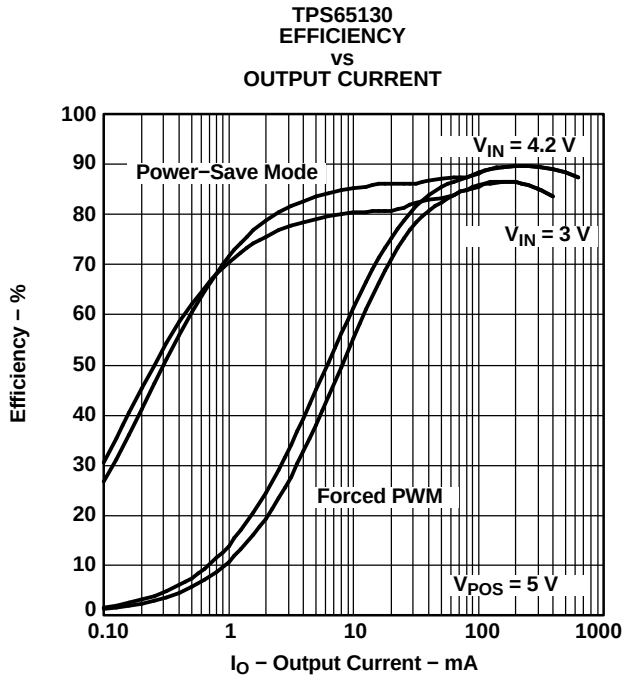



Figure 5.

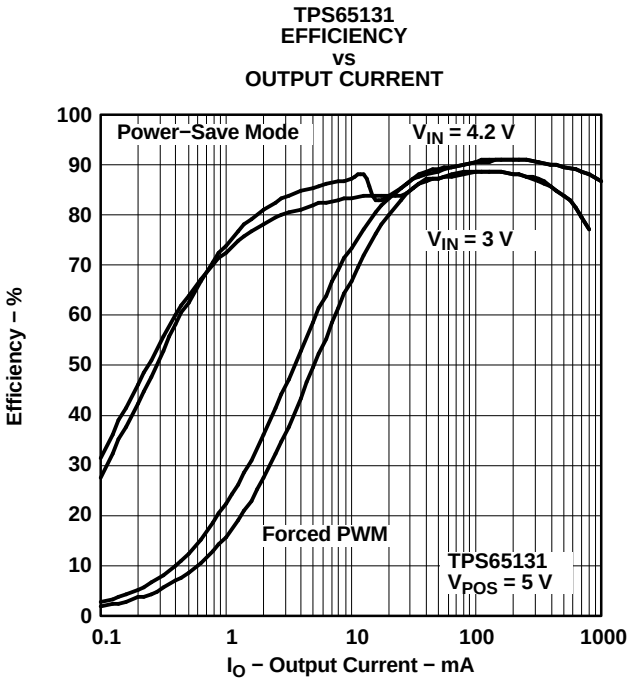



Figure 6.

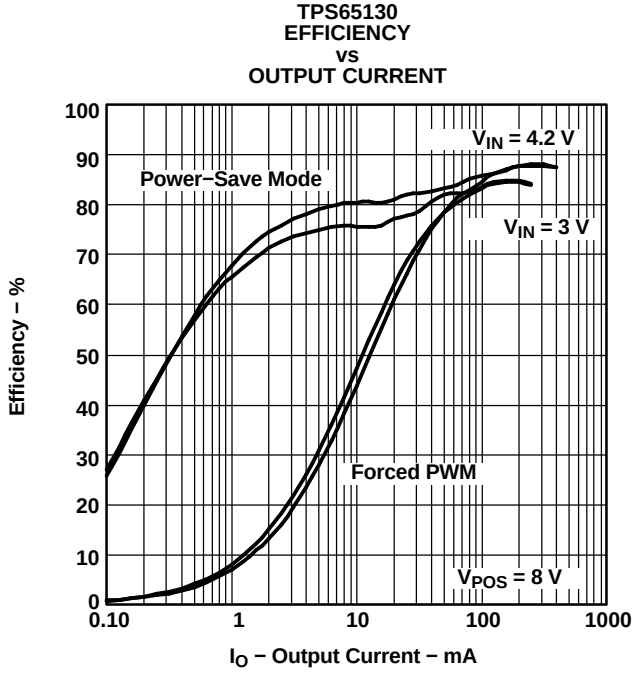



Figure 7.

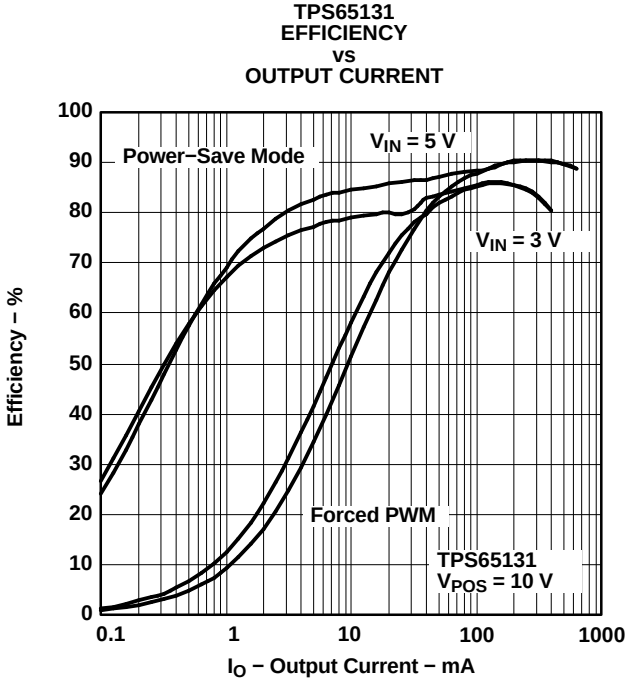



Figure 8.

## TYPICAL CHARACTERISTICS (continued)

TPS65130
EFFICIENCY
vs
OUTPUT CURRENT

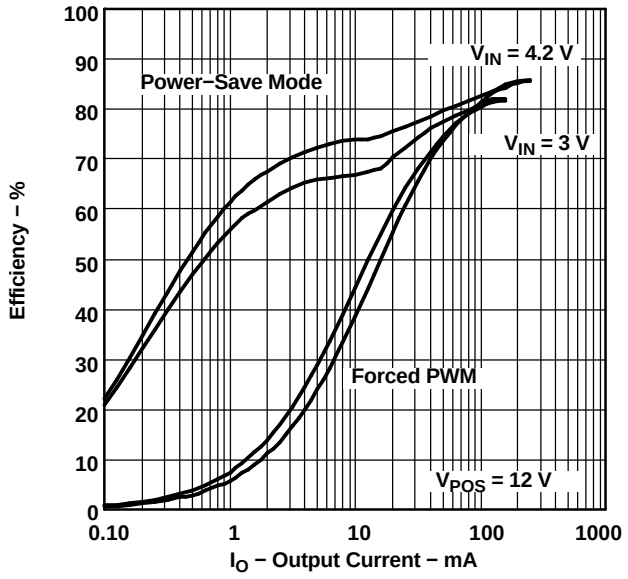



Figure 9.

TPS65131
EFFICIENCY
vs
OUTPUT CURRENT

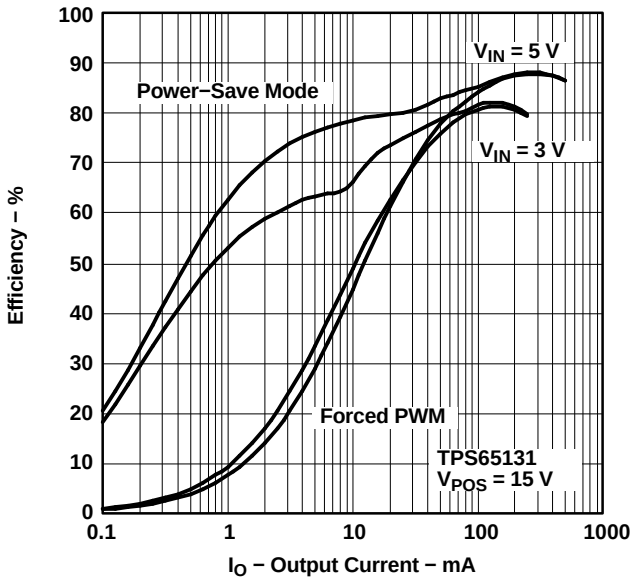



Figure 10.

TPS65130
EFFICIENCY
vs
OUTPUT CURRENT

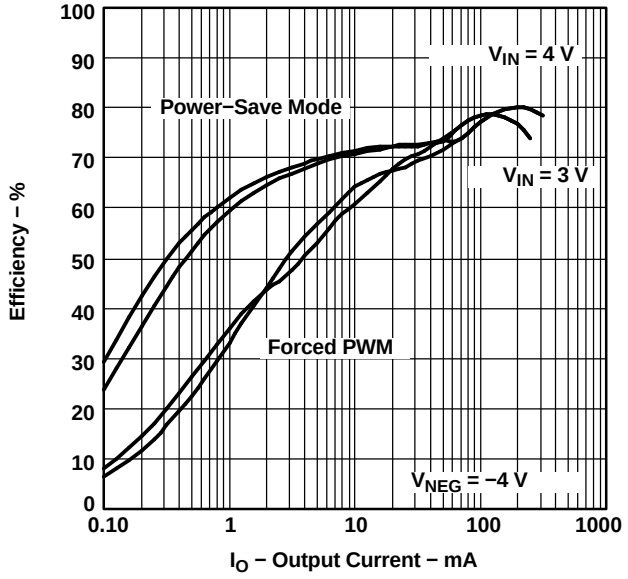



Figure 11.

TPS65131
EFFICIENCY
vs
OUTPUT CURRENT

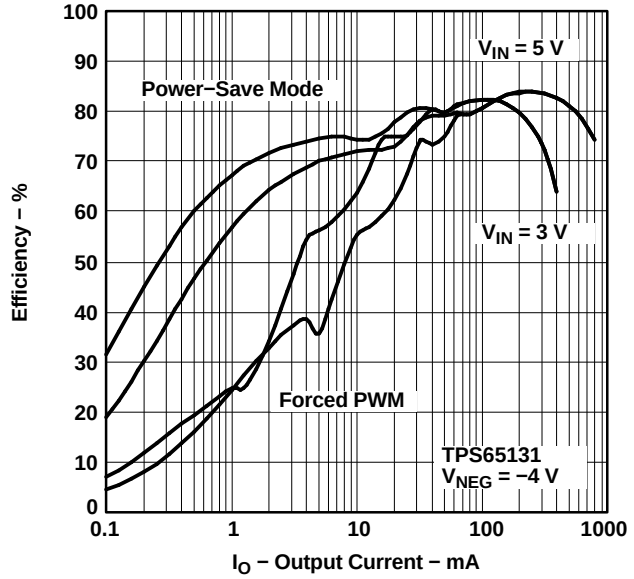



Figure 12.

## TYPICAL CHARACTERISTICS (continued)

TPS65130
EFFICIENCY
vs
OUTPUT CURRENT

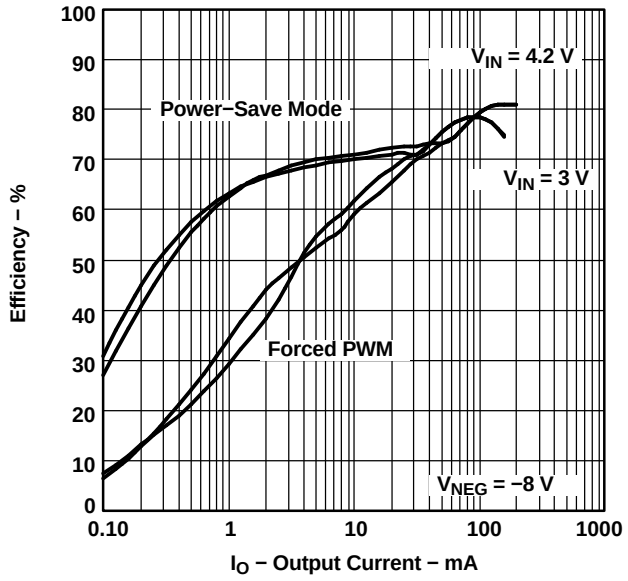



Figure 13.

TPS65131
EFFICIENCY
vs
OUTPUT CURRENT

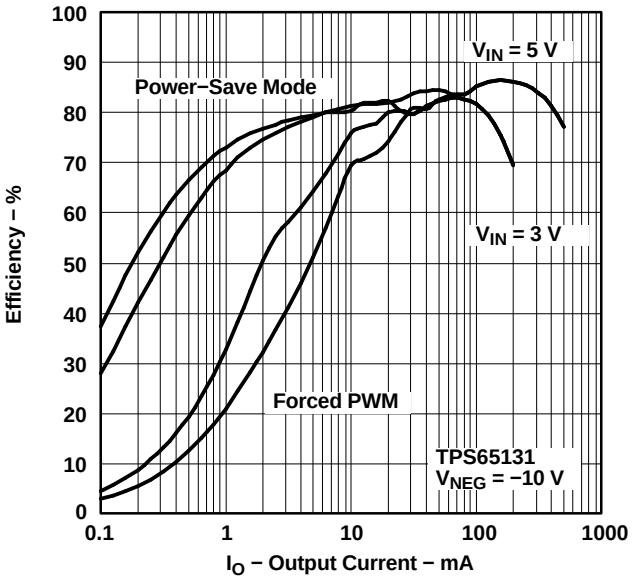



Figure 14.

TPS65130
EFFICIENCY
vs
OUTPUT CURRENT

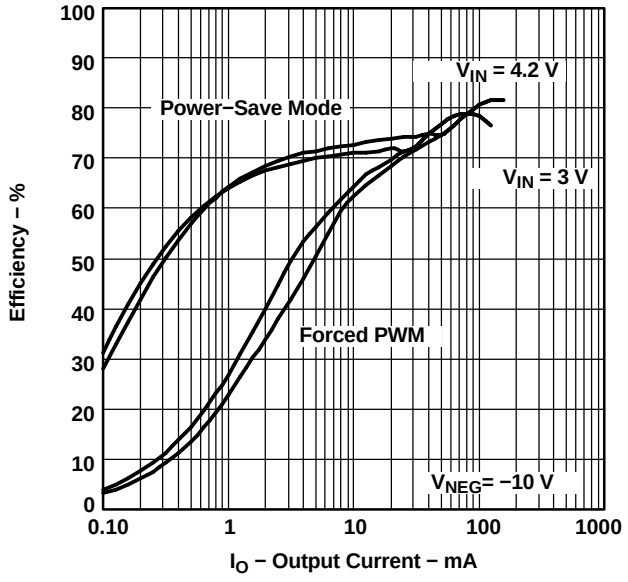



Figure 15.

TPS65131
EFFICIENCY
vs
OUTPUT CURRENT

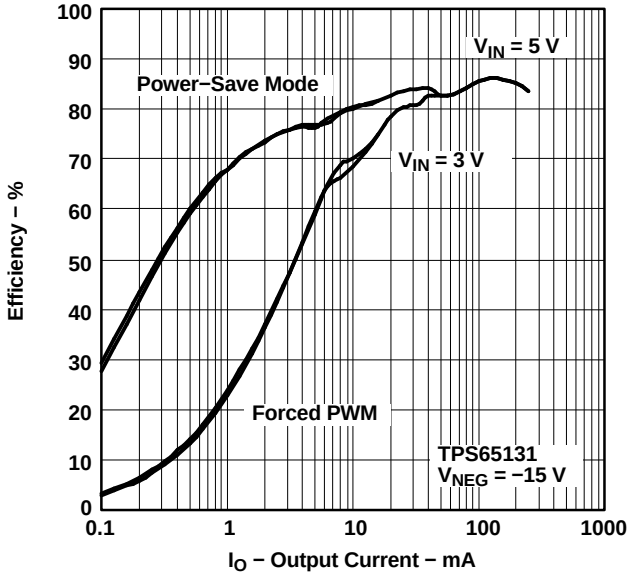



Figure 16.

## TYPICAL CHARACTERISTICS (continued)

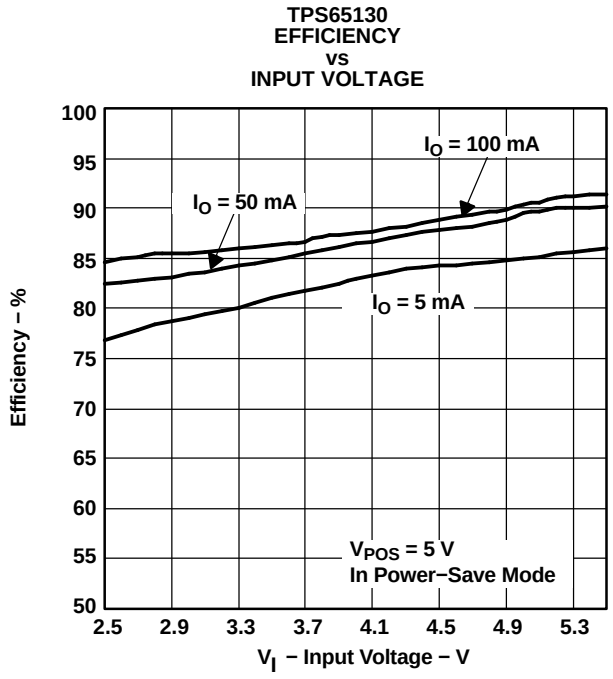



Figure 17.

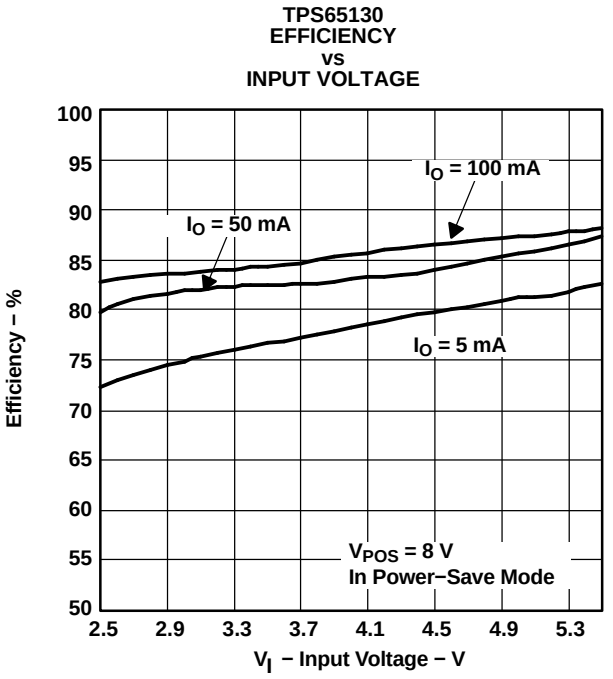



Figure 18.

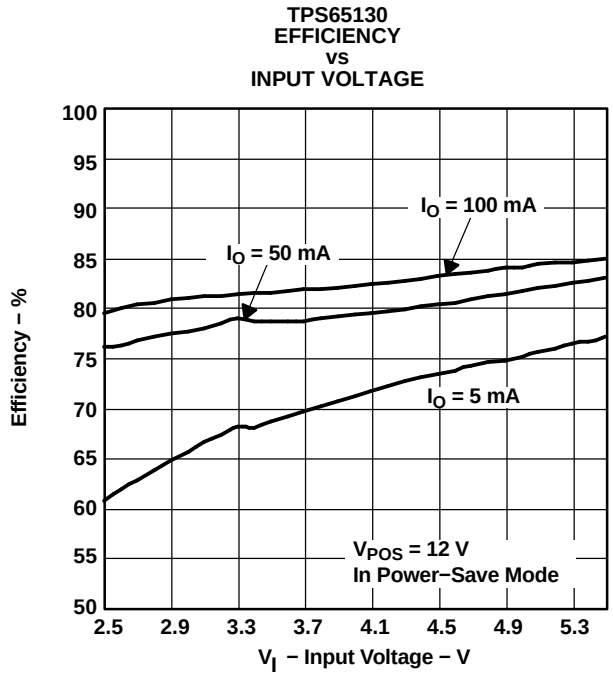



Figure 19.

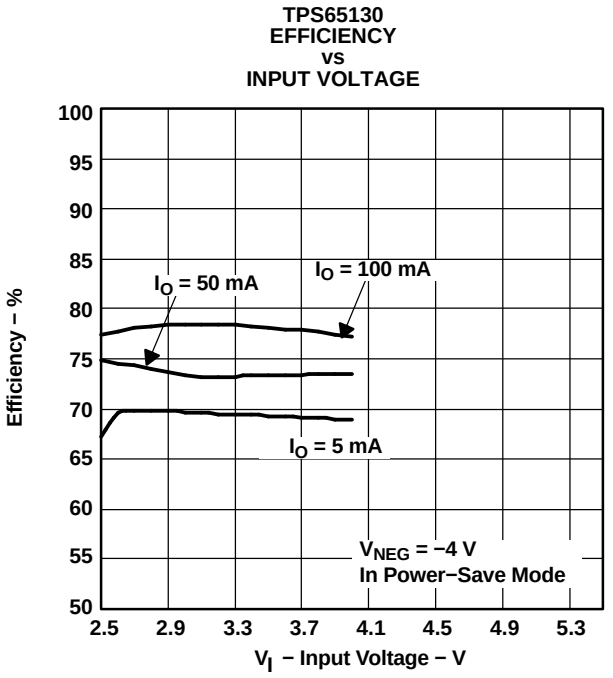



Figure 20.

## TYPICAL CHARACTERISTICS (continued)

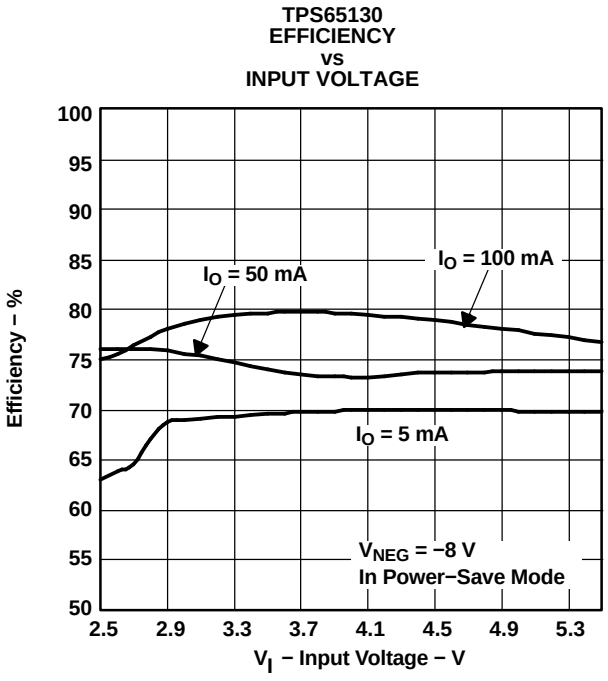



Figure 21.

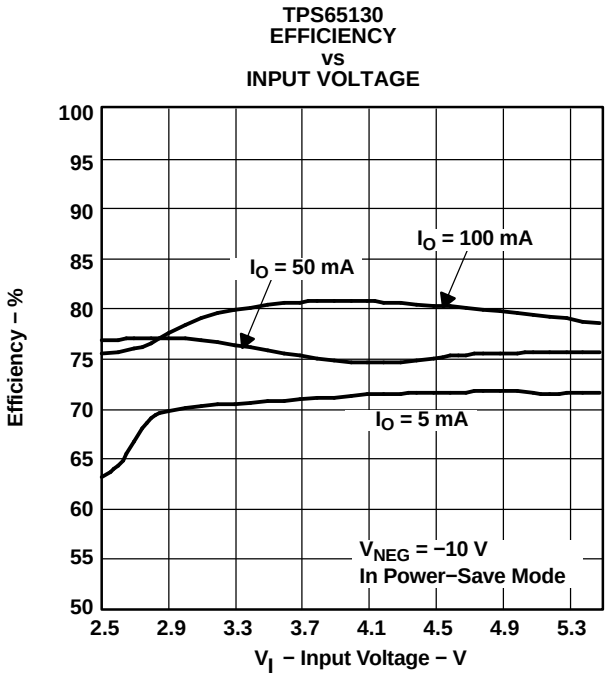



Figure 22.

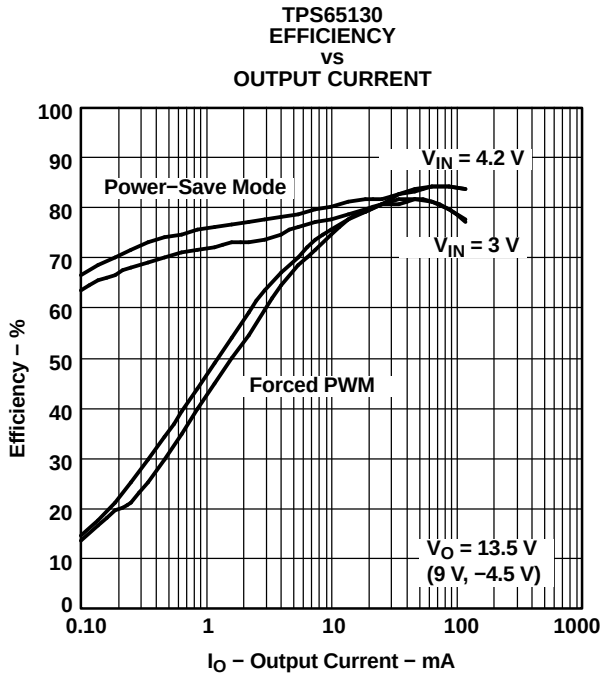



Figure 23.

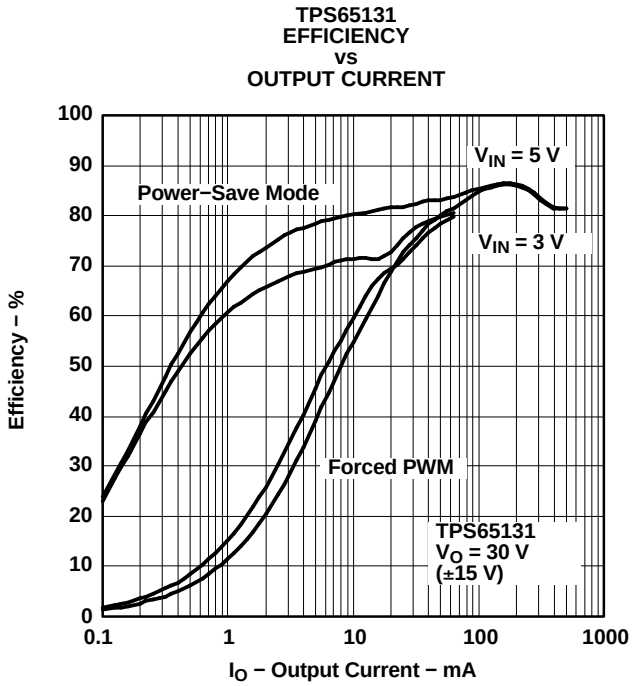



Figure 24.

## TYPICAL CHARACTERISTICS (continued)

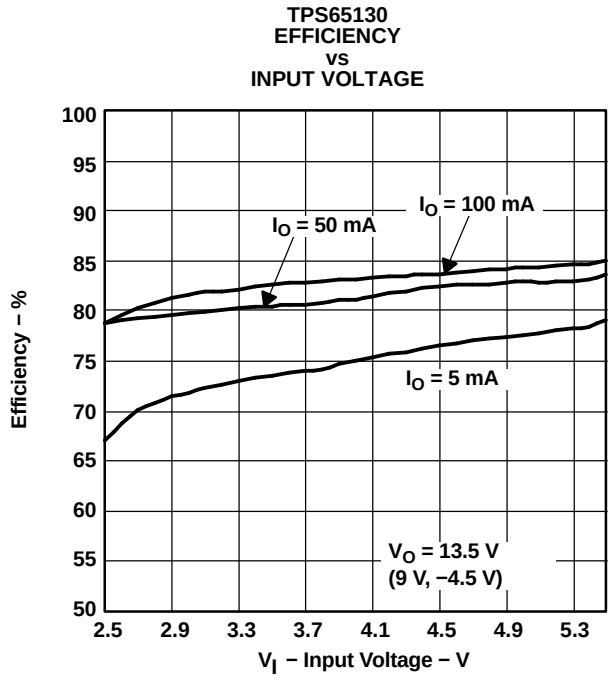



Figure 25.

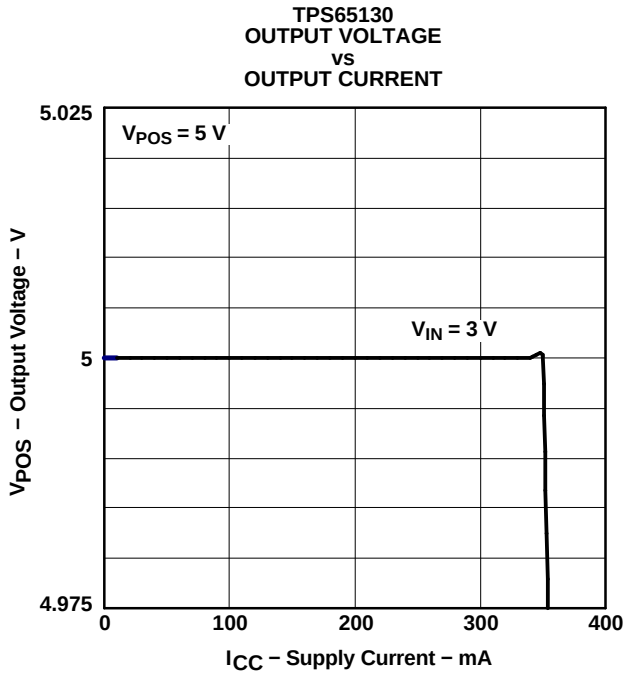



Figure 26.

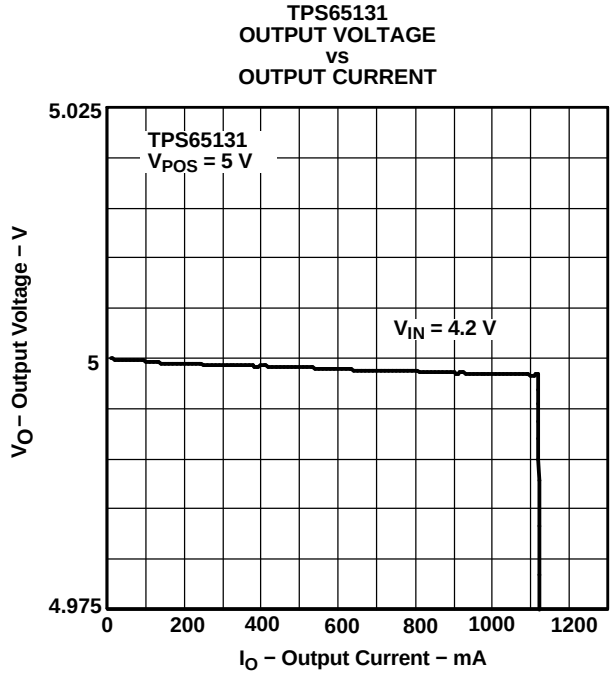



Figure 27.

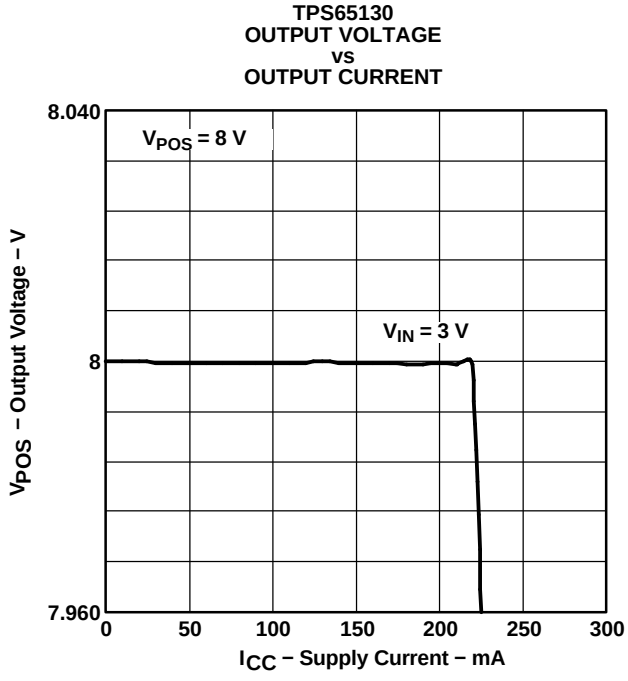



Figure 28.

## TYPICAL CHARACTERISTICS (continued)

TPS65131
OUTPUT VOLTAGE
vs
OUTPUT CURRENT

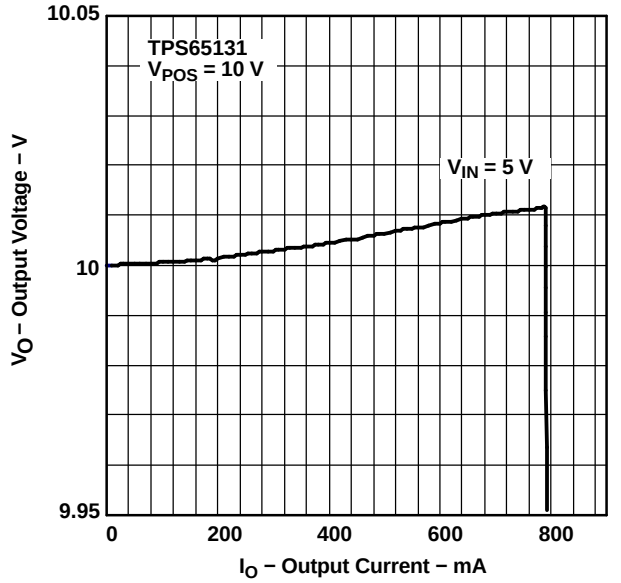



Figure 29.

TPS65130
OUTPUT VOLTAGE
vs
OUTPUT CURRENT

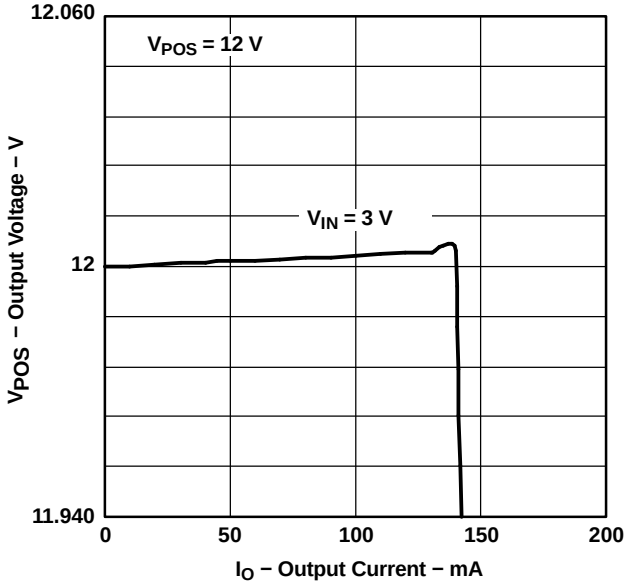



Figure 30.

TPS65131
OUTPUT VOLTAGE
vs
OUTPUT CURRENT

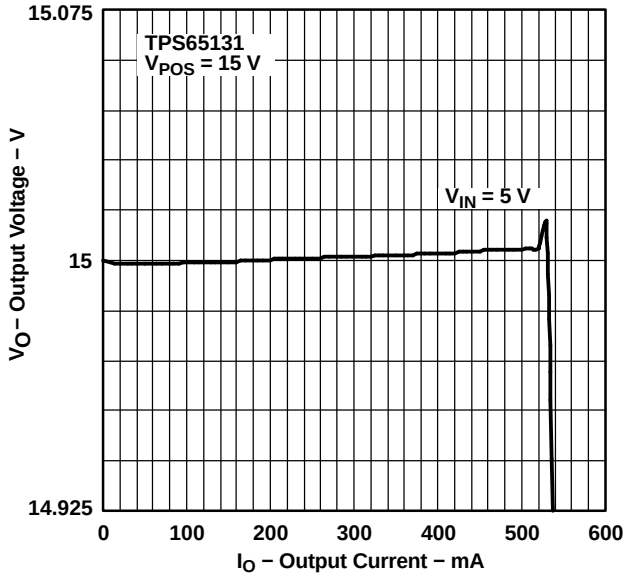



Figure 31.

TPS65130
OUTPUT VOLTAGE
vs
OUTPUT CURRENT

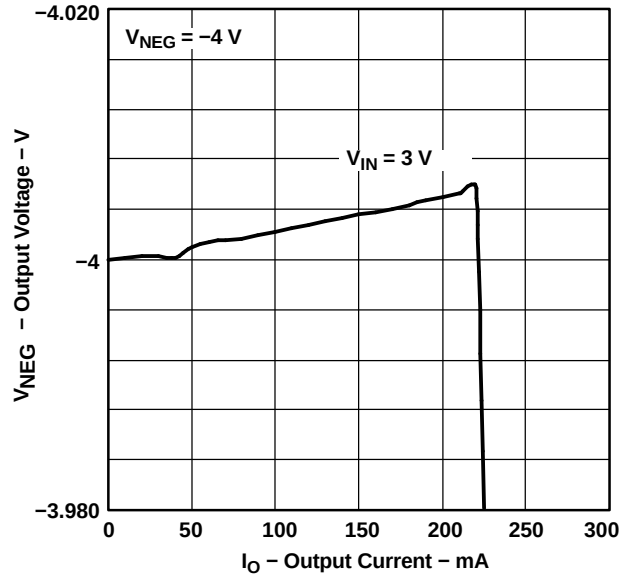



Figure 32.

## TYPICAL CHARACTERISTICS (continued)

TPS65131
OUTPUT VOLTAGE
vs
OUTPUT CURRENT

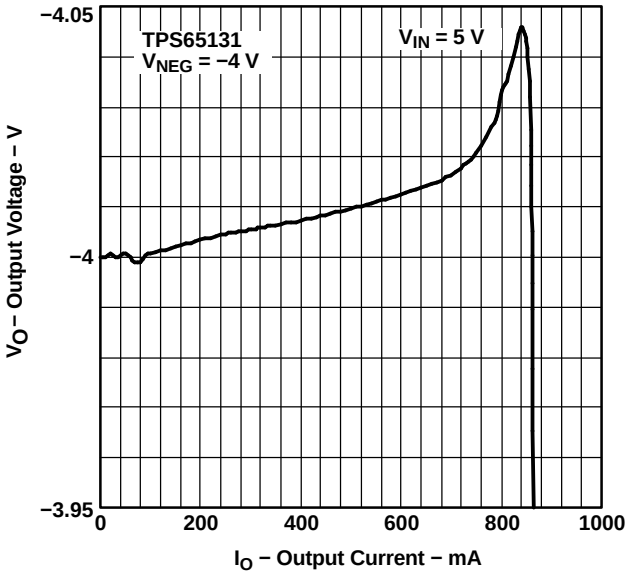



Figure 33.

TPS65130
OUTPUT VOLTAGE
vs
OUTPUT CURRENT

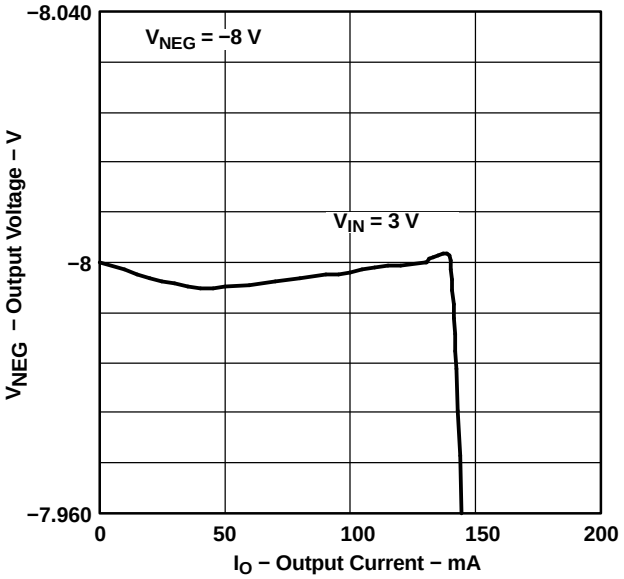



Figure 34.

TPS65131
OUTPUT VOLTAGE
vs
OUTPUT CURRENT

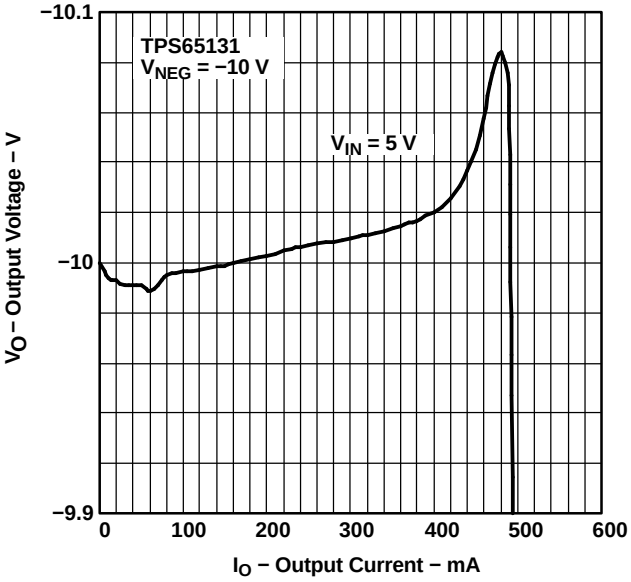



Figure 35.

TPS65130
OUTPUT VOLTAGE
vs
OUTPUT CURRENT

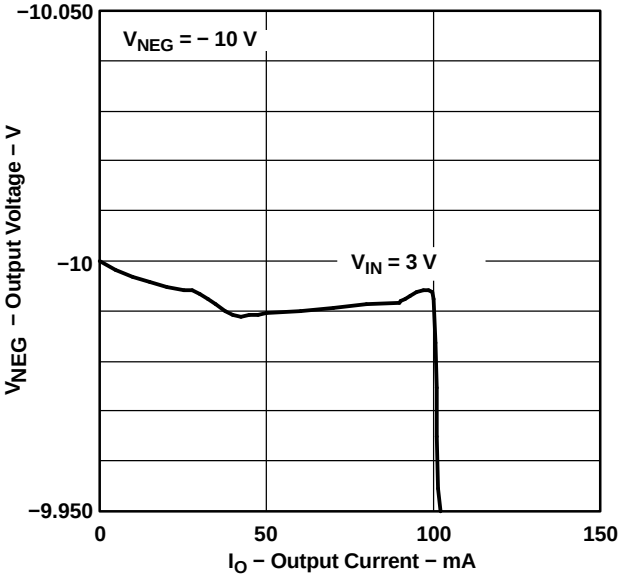



Figure 36.

## TYPICAL CHARACTERISTICS (continued)

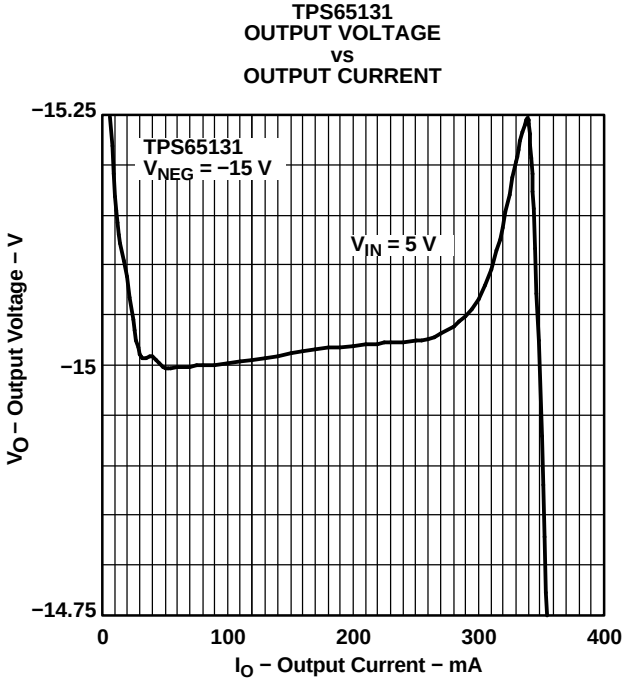



Figure 37.

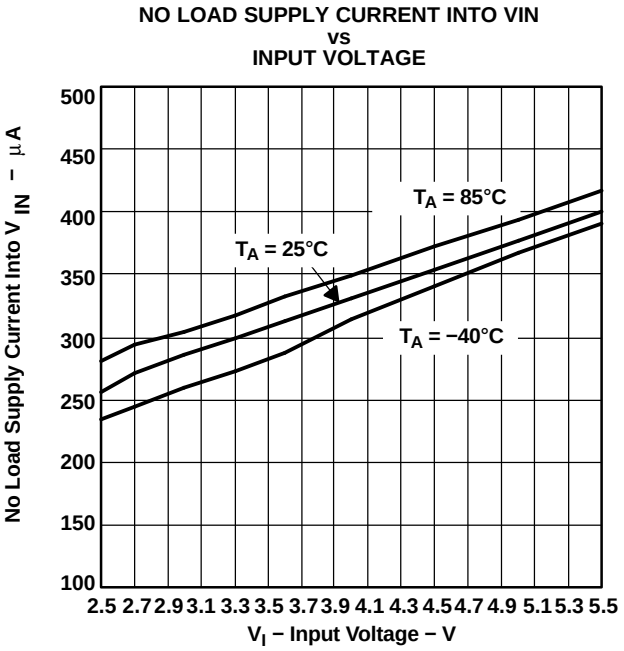



Figure 38.

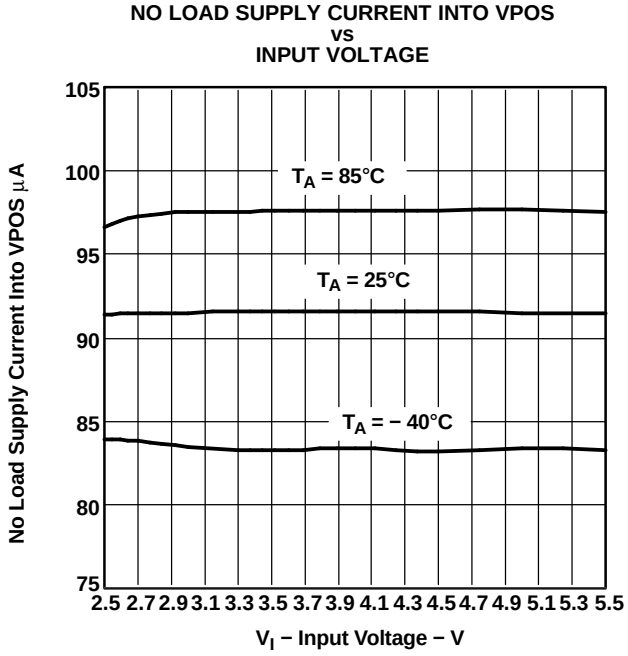



Figure 39.

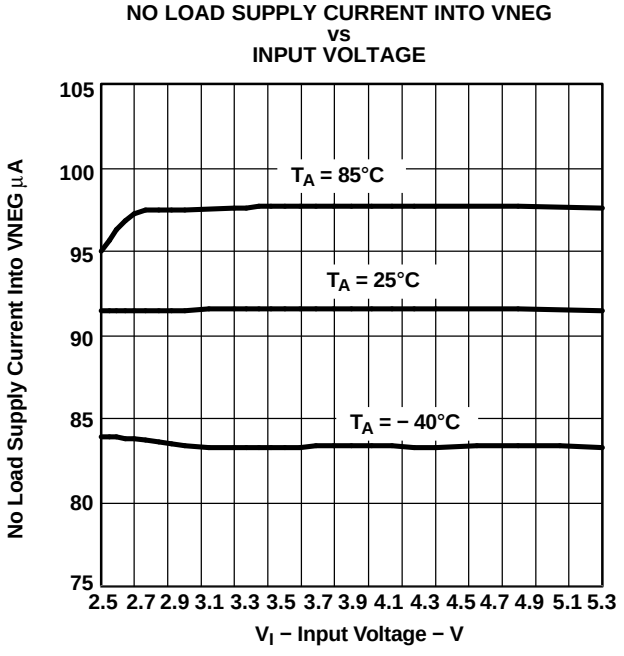



Figure 40.

## TYPICAL CHARACTERISTICS (continued)

**POSITIVE OUTPUT VOLTAGE IN CONTINUOUS CURRENT MODE**

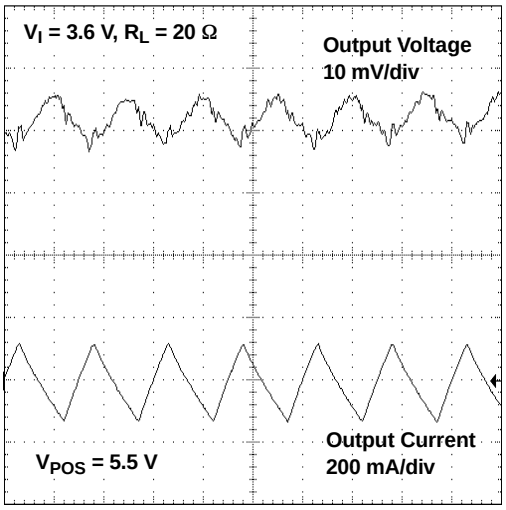



Figure 41.

**NEGATIVE OUTPUT VOLTAGE IN CONTINUOUS CURRENT MODE**

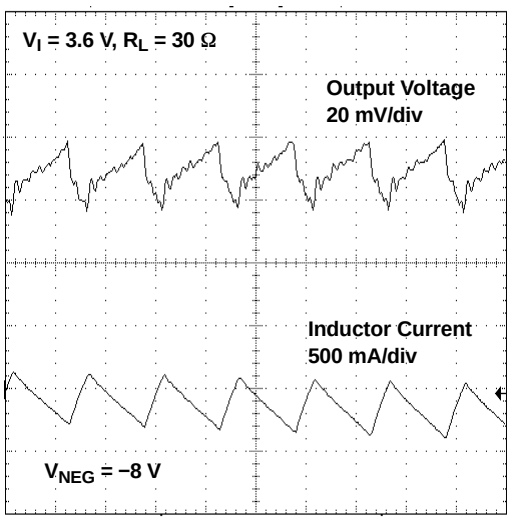



Figure 42.

**POSITIVE OUTPUT VOLTAGE AT POWER-SAVE MODE DISABLED**

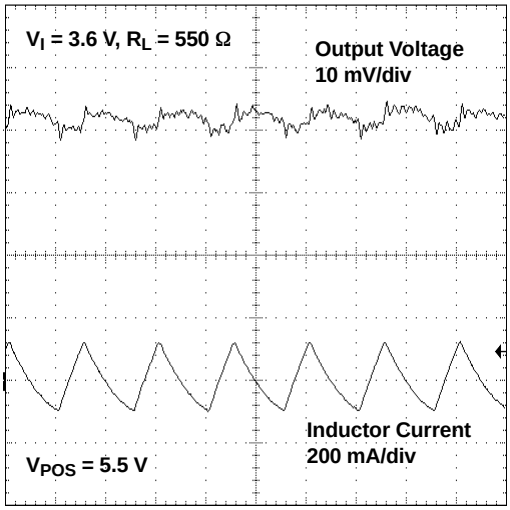



Figure 43.

**NEGATIVE OUTPUT VOLTAGE AT POWER-SAVE MODE DISABLED**

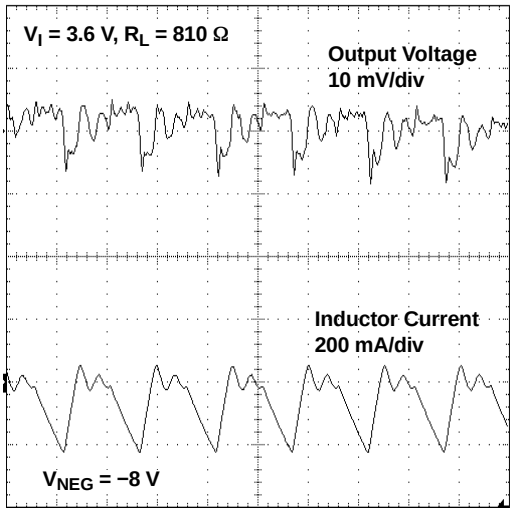
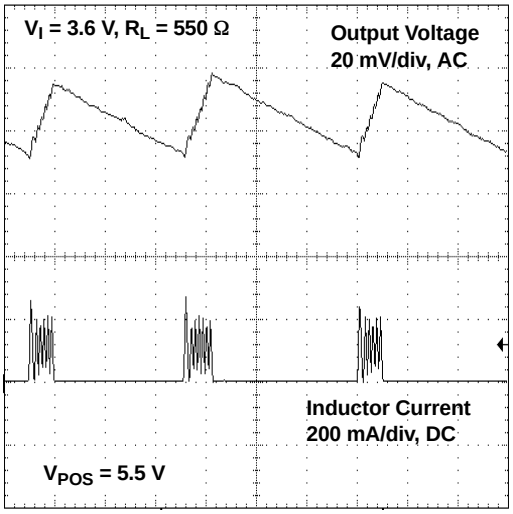



Figure 44.

## TYPICAL CHARACTERISTICS (continued)

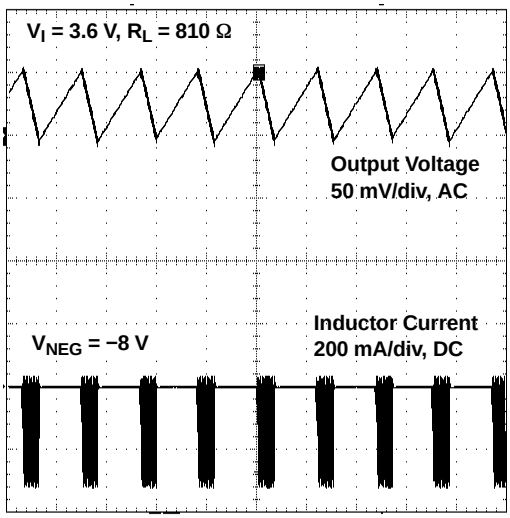
**POSITIVE OUTPUT VOLTAGE IN POWER-SAVE MODE**




t − Time − 10 μs/div

Figure 45.

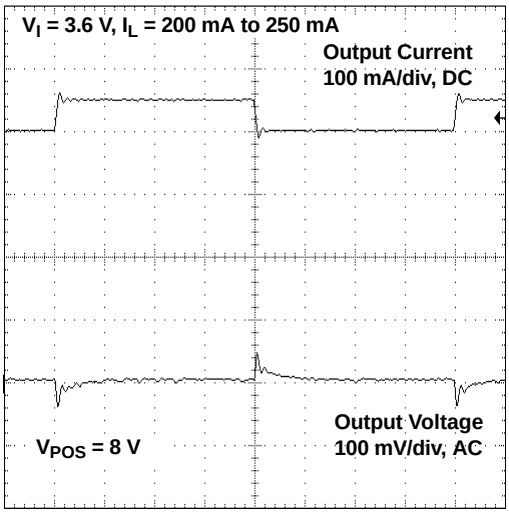
**NEGATIVE OUTPUT VOLTAGE IN POWER-SAVE MODE**




t − Time − 50 μs/div

Figure 46.

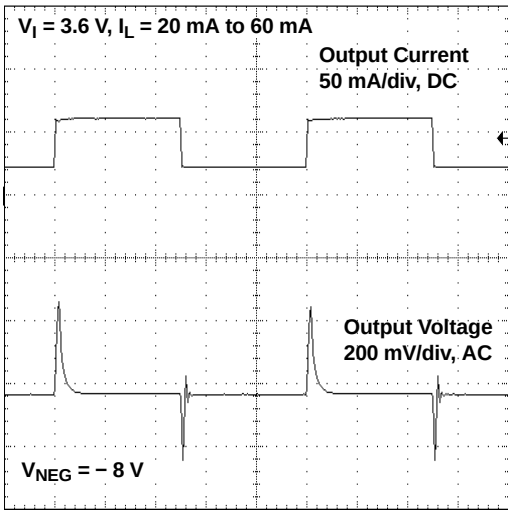
**LOAD TRANSIENT RESPONSE**




t − Time − 500 μs/div

Figure 47.

**LOAD TRANSIENT RESPONSE**

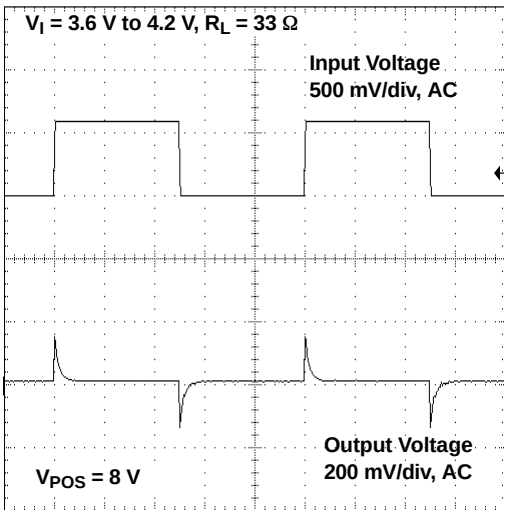



t − Time − 2 ms/div

Figure 48.

## TYPICAL CHARACTERISTICS (continued)

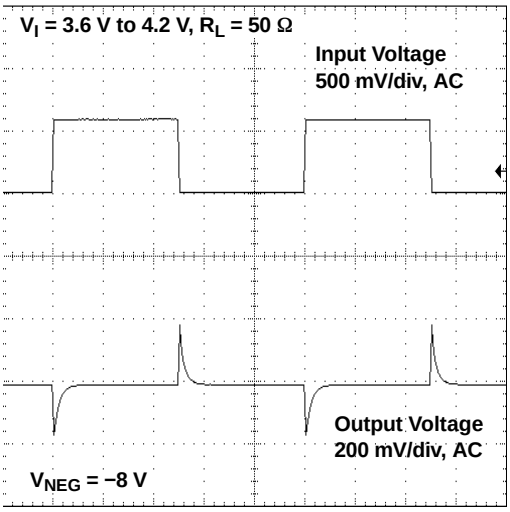
**LINE TRANSIENT RESPONSE**




t − Time − 2 ms/div

Figure 49.

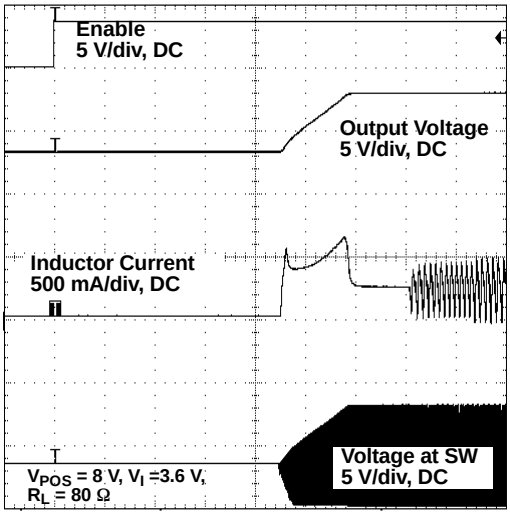
**LINE TRANSIENT RESPONSE**




t − Time − 2 ms/div

Figure 50.

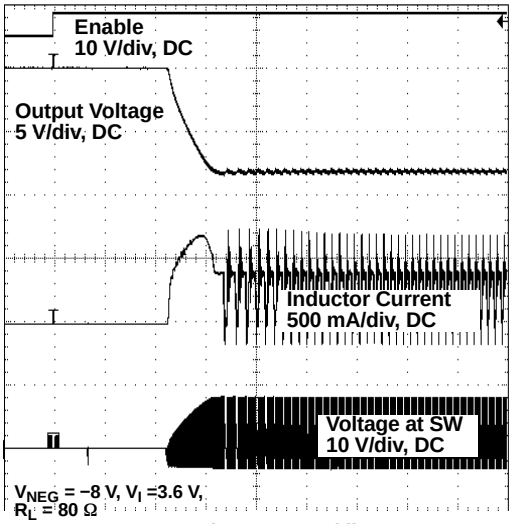
**START-UP AFTER ENABLE**




t − Time − 200 μs/div

Figure 51.

**START-UP AFTER ENABLE**




t − Time − 500 μs/div

Figure 52.

## DETAILED DESCRIPTION

The TPS65130/1 operates with an input voltage range of 2.7 V to 5.5 V and can generate both a positive and negative output. Both converters work independently of each other. They only share a common clock and a common voltage reference. Both outputs are seperately controlled by a fixed-frequency, pulse-width-modulated (PWM) regulator. In general, each converter operates at continuous conduction mode (CCM). At light loads, the negative converter can enter discontinuous conduction mode (DCM). As the load current decreases, the converters can enter a power-save mode if enabled. This works independently at both converters. Output voltages can go up to 15 V at the boost output and down to –15 V at the inverter output.

## DETAILED DESCRIPTION (continued)

### Power Conversion

Both converters operate in a fixed-frequency, PWM control scheme. So, the on-time of the switches varies depending on input-to-output voltage ratio and the load. During this on-time, the inductors connected to the converters are charged with current. In the remaining time, the time period set by the fixed operating frequency, the inductors discharge into the output capacitors via the rectifier diodes. Usually at higher loads, the inductor currents are continuous. At lighter loads, the boost converter uses an additional internal switch to allow current flowing back to the input. This avoids inductor current becoming discontinuous in the boost converter. So, the boost converter is always controlled in a continuous current mode. At the inverting converter, during light loads, the inductor current can become discontinuous. In this case, the control circuit of the inverting controller output automatically takes care of these changing conditions to always operate with an optimum control setup.

### Control

The controller circuits of both converters are based on a fixed-frequency, multiple-feedforward controller topology. Input voltage, output voltage, and voltage drop across the switches are monitored and forwarded to the regulator. Changes in the operating conditions of the converters directly affect the duty cycle and must not take the indirect and slow way through the output voltage control loops. Measurement errors in this feedforward system are corrected by a self-learning control system. To avoid output voltage steps due to output changes of this self-learning control system, its output is dampened by an external capacitor.

The voltage loops, determined by the error amplifiers, only have to handle small signal errors. The error amplifiers are internally compensated. Their inputs are the feedback voltages on the FBP and FBN pins. These voltages are compared with the internal reference voltage to generate an accurate and stable output voltage.

### Power-Save Mode

The PSN and PSP can be used to select different operating modes. To enable power-save mode for the corresponding converter, the dedicated PS pin must be set high. Power-save mode can be used to improve efficiency at light load. In power-save mode, the converter only operates when the output voltage falls below a set threshold voltage. It ramps up the output voltage with one or several operating pulses and goes again into power-save mode once the inductor current goes discontinuous. The power-save mode can be disabled seperately for each converter by setting the corresponding PS pin low.

### Enable

Applying a low signal at the enable ENP or ENN pins shuts down the corresponding converter. When both enable pins are tied low, the device enters shutdown mode, where all internal circuitry is turned off. The device now just consumes low shutdown current flowing into the VIN pin. The output loads of the converters are disconnected from the battery as described in the following paragraph. Pulling the enable pins high enables the corresponding converter. Internal circuitry, necessary to operate the specific converter, is then turned on.

### Load Disconnect

The device supports completely disconnecting the load, when the converters are disabled. At the inverting converter, this is done by just turning off the internal PMOS switch. If the inverting converter is turned off, no DC current path remains which could discharge the battery. This is different at the boost converter. The external rectifying diode, together with the boost inductor, form a DC current path which could discharge the battery if any load is connected at the output. The device has no internal switch to prevent current from flowing. For this reason, a PMOS gate control output (BSW) is implemented. A PMOS switch can be placed into this DC current path, ideally, directly between the boost inductor and battery. To be able to really disconnect the battery, the forward direction of the parasitic backgate diode of this switch must point to the battery. The external PMOS switch, connected to BSW, turns on when the boost converter is enabled and is turned off when the boost converter is disabled.

## DETAILED DESCRIPTION (continued)

### Soft Start

Both converters have implemented soft-start functions. When each converter is enabled, the implemented switch current limit ramps up slowly to its nominal programmed value in about 1 ms. Soft start is implemented to limit the input current during start-up to avoid high peak currents at the battery which could interfere with other systems connected to the same battery. Without soft start, uncontrolled input peak currents flow to charge up the output capacitors and to supply the load during start-up. Their values could increase the implemented switch current limit, which has serious impact to the converter itself and other parts of the system, by causing significant voltage drops across the series resistance of the battery and its connections.

### Overvoltage Protection

Both built-in converters have implemented overvoltage protection. If the feedback voltage under normal operation exceeds the nominal value by typically 5%, the corresponding converter shuts down immediately to protect any connected circuitry from possible damage.

### Undervoltage Lockout

An undervoltage lockout prevents the device from starting up and operating if the supply voltage at VIN is lower than the programmed threshold shown in the electrical characteristic table. The device automatically shuts down both converters when the supply voltage at VIN falls below this threshold. Nevertheless, parts of the control circuits remain active, which is different than device shutdown using EN inputs. The undervoltage lockout function is implemented to prevent device malfunction.

### Overtemperature Shutdown

The device automatically shuts down both converters if the implemented internal temperature detector detects a chip temperature above the programmed theshold shown in the electrical characteristics table. It automatically starts operating again when the chip temperature falls below this threshold. A built-in hysteresis avoids undefined operation caused by ringing from shutdown and prevents operating at a temperature close to the overtemperature shutdown threshold.

## APPLICATION INFORMATION

### Design Procedure

The TPS65130/1 dc-dc converter is intended for systems typically powered by a single-cell Li-ion or Li-polymer battery with a terminal voltage between 2.7 V up to 4.2 V. Because the recommended input voltage goes up to 5.5 V, the device is also suitable for 3-cell alkaline, NiCd, or NiMH batteries, as well as any regulated supply voltages between 2.7 V and 5.5 V. It provides two independent output voltage rails which are programmed as follows.

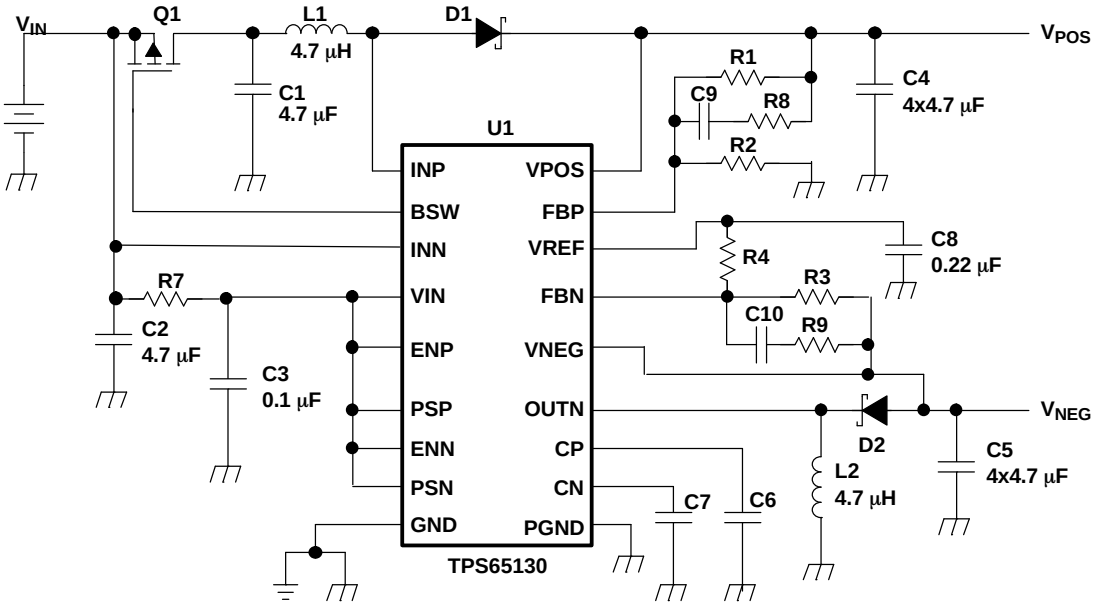
#### Programming the Output Voltage

##### *Boost Converter*

The output voltage of the TPS65130/1 boost converter stage can be adjusted with an external resistor divider connected to the FBP pin. The typical value of the voltage at the FBP pin is the reference voltage, which is 1.213 V. The maximum recommended output voltage at the boost converter is 15 V. To achieve appropriate accuracy, the current through the feedback divider should be about 100 times higher than the current into the FBP pin. Typical current into the FBP pin is 0.05 µA, and the voltage across $R_2$ is 1.213 V. Based on those values, the recommended value for $R_2$ should be lower than 200 kΩ in order to set the divider current at 5 µA or higher. Depending on the needed output voltage ($V_{POS}$), the value of the resistor $R_1$ can then be calculated using Equation 1:

$$R1 = R2 \times \left( \frac{V_{POS}}{V_{REF}} - 1 \right) \quad (1)$$

As an example, if an 8-V output is needed, and a resistor of 180 kΩ has been chosen for $R_2$, a 1-MΩ resistor is needed to program the desired output voltage.




##### *Inverting Converter*

The output voltage of the TPS65130/1 inverting converter stage can also be adjusted with an external resistor divider. It must be connected to the FBN pin. In difference to the feedback divider at the boost converter, the reference point of the feedback divider is not GND; it is $V_{REF}$. So the typical value of the voltage at the FBN pin is 0 V. The minimum recommended output voltage at the inverting converter is –15 V. Feedback divider current

## APPLICATION INFORMATION (continued)

considerations are similar to the considerations at the boost converter. For the same reasons, the feedback divider current should be in the range of 5 µA or higher. The voltage across $R_4$ is 1.213 V. Based on those values, the recommended value for $R_4$ should be lower than 200 kΩ in order to set the divider current at the required value. The value of the resistor $R_3$, depending on the needed output voltage ($V_{NEG}$), can be calculated using Equation 2:

$$R3 = R4 \times \left( \frac{V_{REF} - V_{NEG}}{V_{REF}} - 1 \right) \quad (2)$$

If as an example an output voltage of –5 V is needed and a resistor of 180 kΩ has been chosen for $R_4$, a 750-kΩ resistor is needed to program the desired output voltage.

### Inductor Selection

An inductive converter normally requires two main passive components for storing energy during the conversion. An inductor and a storage capacitor at the output are required. In selecting the right inductor, it is recommended to keep the possible peak inductor current below the current-limit threshold of the power switch in the chosen configuration. For example, the current-limit threshold of the switch for the boost converter and for the inverting converter, is nominally 800 mA at TPS65130 and 1950 mA at TPS65131. The highest peak current through the switches and the inductor depend on the output load, the input voltage ($V_{IN}$), and the output voltages ($V_{POS}$, $V_{NEG}$). Estimation of the peak inductor current in the boost converter can be done using Equation 3. Equation 4 shows the corresponding formula for the inverting converter.

$$I_{LP} = \frac{V_{POS}}{V_{IN} \times 0.64} \times I_{OUTP} \quad (3)$$

$$I_{LN} = \frac{V_{IN} - V_{NEG}}{V_{IN} \times 0.64} \times I_{OUTN} \quad (4)$$

The second parameter for choosing the inductor is the desired current ripple in the inductor. Normally, it is advisable to work with a ripple of less than 20% of the average inductor current. A smaller ripple reduces the losses in the inductor, as well as output voltage ripple and EMI. But in the same way, output voltage regulation gets slower, causing higher voltage changes at fast load changes. In addition, a larger inductor usually increases the total system cost. Keeping those parameters in mind, the possible inductor value can be calculated using Equation 5 for the boost converter and Equation 6 for the inverting converter.

$$L_P = \frac{V_{IN} \times \left( V_{POS} - V_{IN} \right)}{\Delta I_{LP} \times f_S \times V_{POS}} \quad (5)$$

$$L_N = \frac{V_{IN} \times V_{NEG}}{\Delta I_{LN} \times f_S \times \left( V_{NEG} - V_{IN} \right)} \quad (6)$$

Parameter *f* is the switching frequency and $\Delta I_L$ is the ripple current in the inductor, i.e., 20% x $I_L$. $V_{IN}$ is the input voltage, which is assumed to be at 3.3 V in this example. So, the calculated inductance value for the boost inductor is 5.1 µH and for the inverting converter inductor is 5.1 µH. With these calculated values and the calculated currents, it is possible to choose a suitable inductor. In typical applications, a 4.7-µH inductor is recommended. The device has been optimized to work with inductance values between 3.3 µH and 6.8 µH. Nevertheless, operation with higher inductance values may be possible in some applications. Detailed stability analysis is then recommended. Care has to be taken for the possibility that load transients and losses in the circuit can lead to higher currents as estimated in Equation 3 and Equation 4. Also, the losses caused by magnetic hysteresis losses and copper losses are a major parameter for total circuit efficiency.

## APPLICATION INFORMATION (continued)

The following inductor series from different suppliers have been used with the TPS65130/1 converter:

**List of Inductors**

| VENDOR | INDUCTOR SERIES |
|---|---|
| EPCOS | B8246284-G4 |
| Wurth Elektronik | 7447789XXX |
| | 744031XXX |
| TDK | VLF3010 |
| | VLF4012 |
| Cooper Electronics Technologies | SD12 |

### Capacitor Selection

#### *Input Capacitor*

At least a 4.7-µF input capacitor is recommended for the input of the boost converter (INP) and for the input of the inverting converter (INN) to improve transient behavior of the regulators and EMI behavior of the total power supply circuit. A ceramic capacitor or a tantalum capacitor with a smaller ceramic capacitor (100 nF) in parallel, placed close to the input pins, is recommended.

#### *Output Capacitors*

One of the major parameters necessary to define the capacitance value of the output capacitor is the maximum allowed output voltage ripple of the converter. This ripple is determined by two parameters of the capacitor, the capacitance and the ESR. It is possible to calculate the minimum capacitance needed for the defined ripple, supposing that the ESR is zero, by using Equation 7 for the boost converter output capacitor and Equation 8 for the inverting converter output capacitor.

$$C_{minP} = \frac{I_{OUTP} \times \left(V_{POS} - V_{IN}\right)}{f_S \times \Delta V_P \times V_{POS}} \quad (7)$$

$$C_{minN} = \frac{I_{OUTN} \times V_{NEG}}{f_S \times \Delta V_N \times \left(V_{NEG} - V_{IN}\right)} \quad (8)$$

Parameter *f* is the switching frequency and $\Delta V$ is the maximum allowed ripple.

With a chosen ripple voltage in the range of 10 mV, a minimum capacitance of 12 µF is needed. The total ripple is larger due to the ESR of the output capacitor. This additional component of the ripple can be calculated using Equation 9 for the boost converter and Equation 10 for the inverting converter.

$$\Delta V_{ESRP} = I_{OUTP} \times R_{ESRP} \quad (9)$$

$$\Delta V_{ESRN} = I_{OUTN} \times R_{ESRN} \quad (10)$$

An additional ripple of 2 mV is the result of using a typical ceramic capacitor with an ESR in a 10-mΩ range. The total ripple is the sum of the ripple caused by the capacitance and the ripple caused by the ESR of the capacitor. In this example, the total ripple is 10 mV. Additional ripple is caused by load transients. When the load current increases rapidly, the output capacitor must provide the additional current until the inductor current has been increased by the control loop by setting a higher on-time at the main switch (duty cycle). The higher duty cycle results in longer inductor charging periods. But the rate of increase of the inductor current is also limited by the inductance itself. When the load current decreases rapidly, the output capacitor needs to store the exessive energy (stored in the inductor) until the regulator has decreased the inductor current by reducing the duty cycle. The recommendation is to use higher capacitance values, as the aforegoing calculations show.

### Stabilizing the Control Loop

#### *Feedback Divider*

To speed up the control loop, feedforward capacitors are recommended in the feedback divider, parallel to R1 (boost converter) and R3 (inverting converter). Equation 11 shows how to calculate the appropriate value for the boost converter, and Equation 12 for the inverting converter.

$$C9 = \frac{6.8\ \mu s}{R1} \tag{11}$$

$$C10 = \frac{7.5\ \mu s}{R3} \tag{12}$$

To avoid coupling noise into the control loop from the feedforward capacitors, the feedforward effect can be bandwith-limited by adding a series resistor. Any value between 10 kΩ and 100 kΩ is suitable. The higher the resistance, the lower the noise coupled into the control loop system.

#### *Compensation Capacitors*

The control loops of both converters are completely compensated internally. The complex internal input voltage output voltage, and input-current feedforward system has built-in error correction which requires external capacitors. A 10-nF capacitor at CP of the boost converter and a 4.7-nF capacitor at CN of the inverting converter is recommended.

### Layout Considerations

As for all switching power supplies, the layout is an important step in the design, especially at high peak currents and high switching frequencies. If the layout is not carefully done, the regulator could show stability problems as well as EMI problems. Therefore, use wide and short traces for the main current paths and for the power ground tracks. The input capacitors, output capacitors, the inductors, and the rectifying diodes should be placed as close as possible to the IC to keep parasitic inductances low. Use a common ground node for power ground and a different node for control grounds to minimize the effects of ground noise. Connect these ground nodes at any place close to one of the ground pins of the IC.

The feedback dividers should be placed as close as possible to the control ground pin (boost converter) or the VREF pin (inverting converter) of the IC. To lay out the control ground, it is recommended to use short traces as well, seperated from the power ground traces. This avoids ground shift problems, which can occur due to superimposition of power ground current and control ground current.

## THERMAL INFORMATION

Implementation of integrated circuits in low-profile and fine-pitch surface-mount packages typically requires special attention to power dissipation. Many system-dependent issues, such as thermal coupling, airflow, added heatsinks and convection surfaces, and the presence of heat-generating components affect the power-dissipation limits of a given component.

Three basic approaches for enhancing thermal performance follow.

- Improving the power dissipation capability of the PCB design
- Improving the thermal coupling of the component to the PCB
- Introducing airflow to the system

The maximum recommended junction temperature ($T_J$) of the TPS65130/1 devices is 125°C. The thermal resistance of the 24-pin QFN, 4x4-mm package (RGE) is $R_{\theta JA}$ = 37.8°C/W. Specified regulator operation is ensured to a maximum ambient temperature $T_A$ of 85°C. Therefore, the maximum power dissipation is about 1058 mW. More power can be dissipated if the maximum ambient temperature of the application is lower.

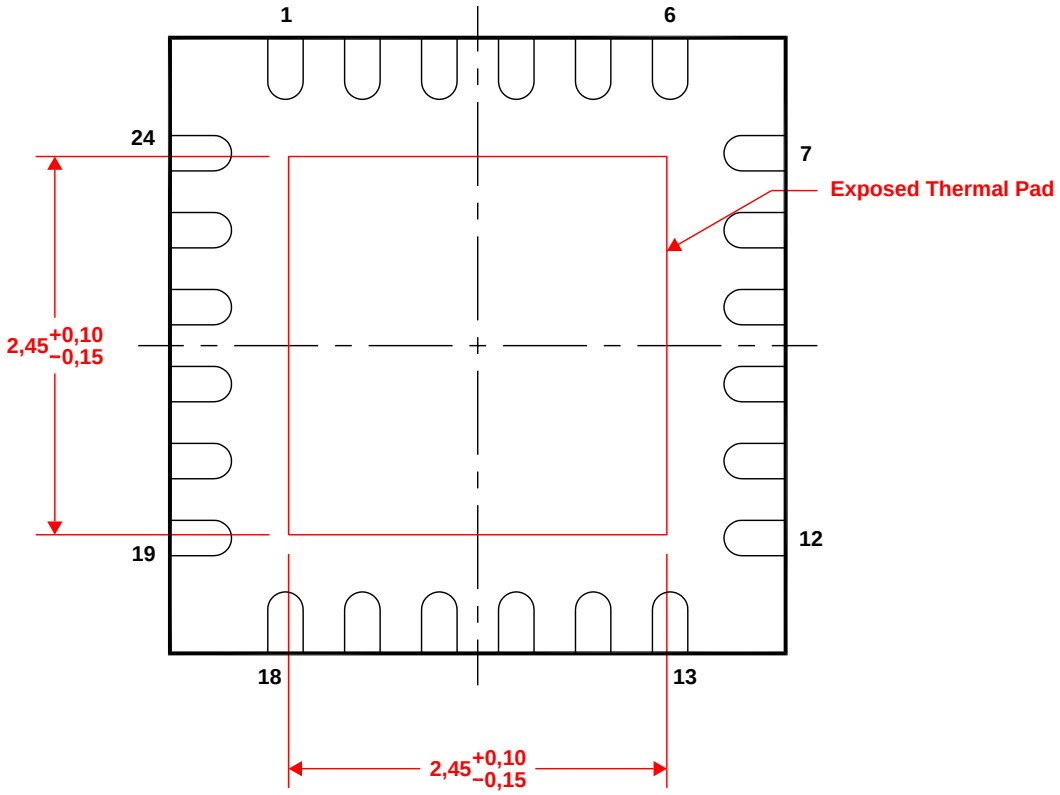
$$P_{DMAX} = \frac{T_{JMAX} - T_A}{R_{\theta JA}} \tag{13}$$

## THERMAL INFORMATION

This package incorporates an exposed thermal pad that is designed to be attached directly to an external heatsink. The thermal pad must be soldered directly to the printed circuit board (PCB). After soldering, the PCB can be used as a heatsink. In addition, through the use of thermal vias, the thermal pad can be attached directly to a ground plane or special heatsink structure designed into the PCB. This design optimizes the heat transfer from the integrated circuit (IC).

For additional information on the Quad Flatpack No-Lead (QFN) package and how to take advantage of its heat dissipating abilities, refer to Application Report, *Quad Flatpack No-Lead Logic Packages*, Texas Instruments Literature No. SCBA017 and Application Report, *56-Pin Quad Flatpack No-Lead Logic Package*, Texas Instruments Literature No. SCEA032. Both documents are available at www.ti.com.

The exposed thermal pad dimensions for this package are shown in the following illustration.



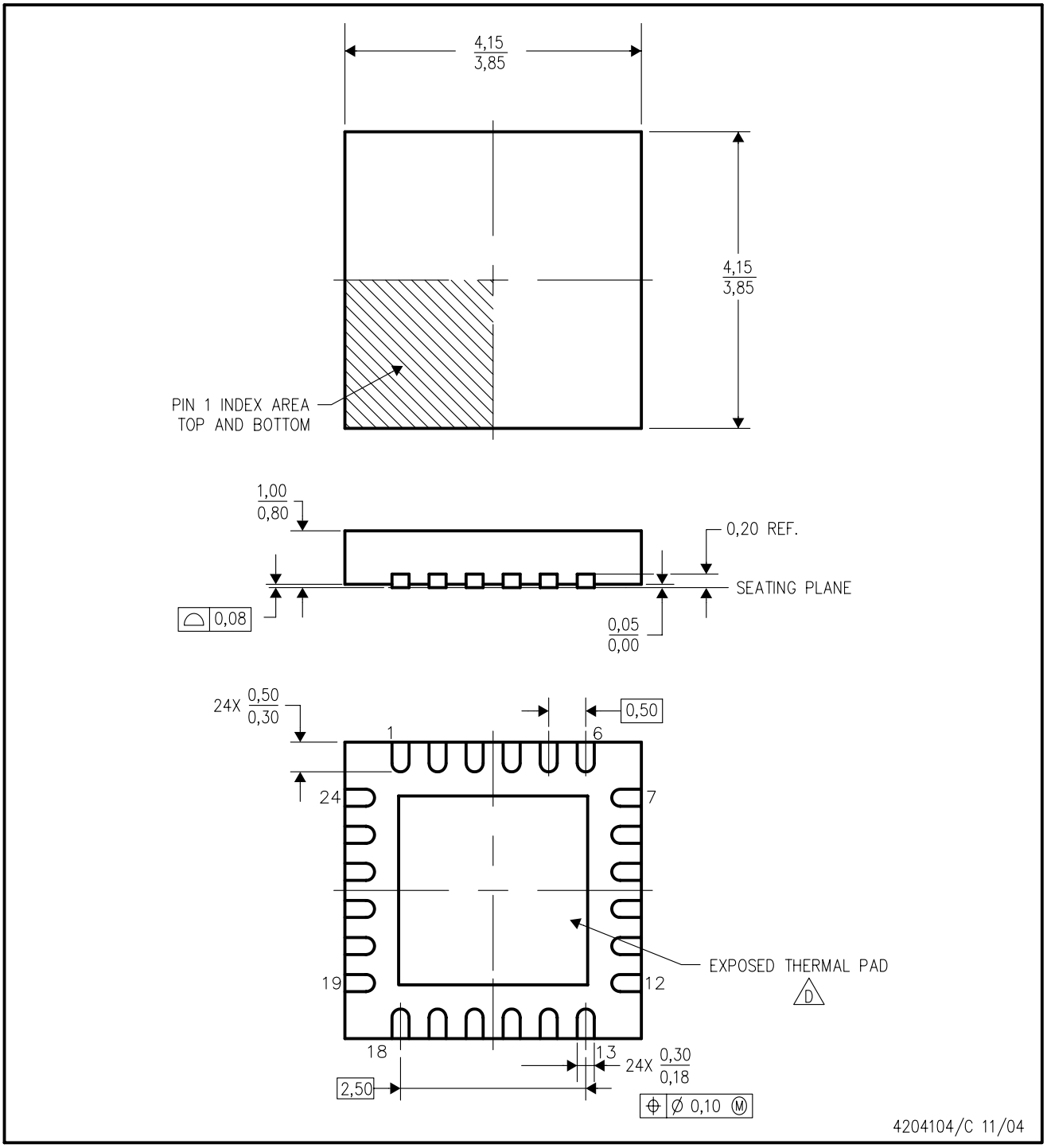

**Bottom View**

NOTE: All linear dimensions are in millimeters

QFND025

**Exposed Thermal Pad Dimensions**

RGE (S–PQFP–N24) PLASTIC QUAD FLATPACK




NOTES:
A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M–1994.
B. This drawing is subject to change without notice.
C. Quad Flatpack, No–Leads (QFN) package configuration.
D. The package thermal pad must be soldered to the board for thermal and mechanical performance. See the Product Data Sheet for details regarding the exposed thermal pad dimensions.
E. Falls within JEDEC MO–220.

## IMPORTANT NOTICE

Texas Instruments Incorporated and its subsidiaries (TI) reserve the right to make corrections, modifications, enhancements, improvements, and other changes to its products and services at any time and to discontinue any product or service without notice. Customers should obtain the latest relevant information before placing orders and should verify that such information is current and complete. All products are sold subject to TI's terms and conditions of sale supplied at the time of order acknowledgment.

TI warrants performance of its hardware products to the specifications applicable at the time of sale in accordance with TI's standard warranty. Testing and other quality control techniques are used to the extent TI deems necessary to support this warranty. Except where mandated by government requirements, testing of all parameters of each product is not necessarily performed.

TI assumes no liability for applications assistance or customer product design. Customers are responsible for their products and applications using TI components. To minimize the risks associated with customer products and applications, customers should provide adequate design and operating safeguards.

TI does not warrant or represent that any license, either express or implied, is granted under any TI patent right, copyright, mask work right, or other TI intellectual property right relating to any combination, machine, or process in which TI products or services are used. Information published by TI regarding third-party products or services does not constitute a license from TI to use such products or services or a warranty or endorsement thereof. Use of such information may require a license from a third party under the patents or other intellectual property of the third party, or a license from TI under the patents or other intellectual property of TI.

Reproduction of information in TI data books or data sheets is permissible only if reproduction is without alteration and is accompanied by all associated warranties, conditions, limitations, and notices. Reproduction of this information with alteration is an unfair and deceptive business practice. TI is not responsible or liable for such altered documentation.

Resale of TI products or services with statements different from or beyond the parameters stated by TI for that product or service voids all express and any implied warranties for the associated TI product or service and is an unfair and deceptive business practice. TI is not responsible or liable for any such statements.

Following are URLs where you can obtain information on other Texas Instruments products and application solutions:

| **Products** | | **Applications** | |
|---|---|---|---|
| Amplifiers | amplifier.ti.com | Audio | www.ti.com/audio |
| Data Converters | dataconverter.ti.com | Automotive | www.ti.com/automotive |
| DSP | dsp.ti.com | Broadband | www.ti.com/broadband |
| Interface | interface.ti.com | Digital Control | www.ti.com/digitalcontrol |
| Logic | logic.ti.com | Military | www.ti.com/military |
| Power Mgmt | power.ti.com | Optical Networking | www.ti.com/opticalnetwork |
| Microcontrollers | microcontroller.ti.com | Security | www.ti.com/security |
| | | Telephony | www.ti.com/telephony |
| | | Video & Imaging | www.ti.com/video |
| | | Wireless | www.ti.com/wireless |

Mailing Address: Texas Instruments
Post Office Box 655303 Dallas, Texas 75265

Copyright © 2004, Texas Instruments Incorporated