OKI Semiconductor

This version: Jan. 1998
Previous version: Nov. 1996

MSM65354/65353A

8-Bit Microcontroller with A/D Converter (with LCD Driver)

GENERAL DESCRIPTION

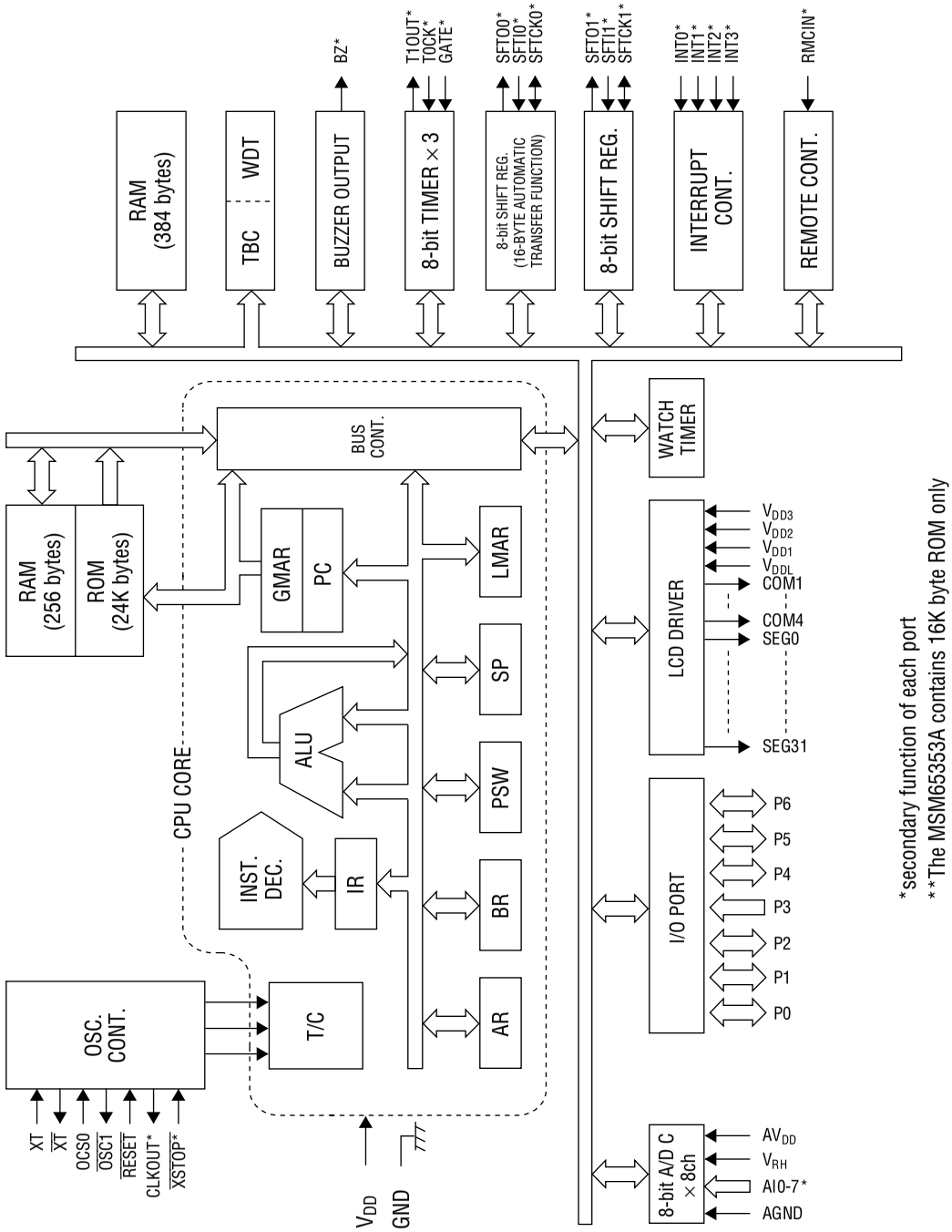
The MSM65354/MSM65353A is a high performance 8-bit microcontroller that employs OKI original CPU core nX-8/50. The MSM65354 contains 24K-byte program memory, 640-byte data memory, LCD driver, A/D converter and shift register. The MSM65353A contains 16K-byte program memory, 384-byte data memory, LCD driver, A/D converter and shift register. Also available is the MSM65P354, which replace the on-chip program memory with one-time PROM.

FEATURES

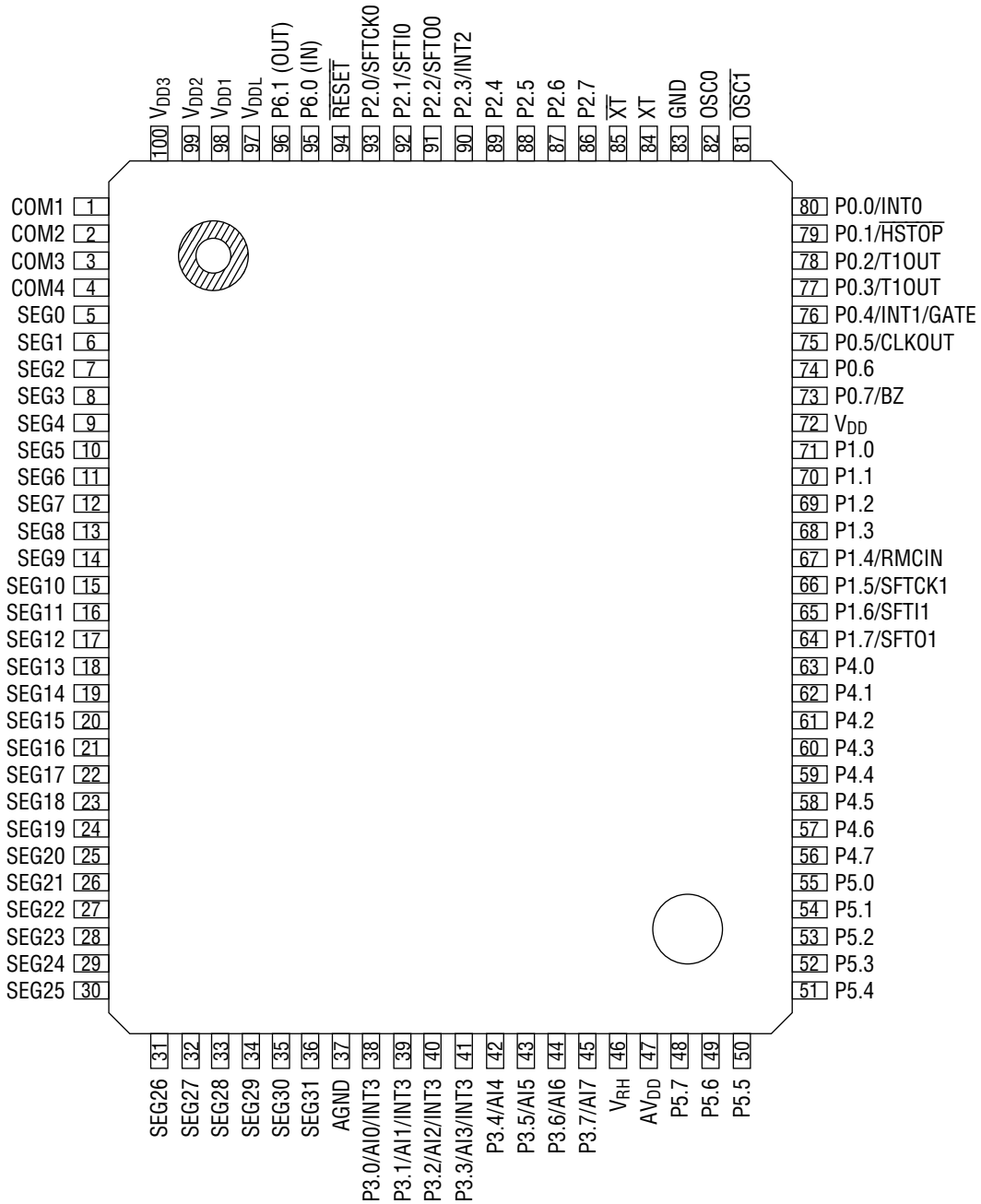
- Operating range
  - Operating voltage : 2.7V to 5.5V
  - Operating temperature : –20°C to +70°C
  - Operating frequency (dual clock)
    - High speed side : 0 to 10MHz (@V_{DD}=5V±10%)
      0 to 5MHz (@V_{DD}=2.7V to 5.5V)
    - Low speed side : 32.768kHz (@V_{DD}=2.7V to 5.5V)
  - Current consumption (Typ.)
    - High speed side : 5mA (@5MHz, V_{DD}=3V)
      20mA (@10MHz, V_{DD}=5V)
      1.5mA (@5MHz, V_{DD}=3V, Halt mode)
      4µA (V_{DD}=3V), Stop mode)
    - Low speed side : 45µA (@32.768kHz, V_{DD}=3V)
- Minimum instruction execution time : 400ns (@10MHz), 800ns (@5MHz)
- CPU core : 8-bit CPU core nX-8/50
- General memory space : 24K-byte program memory + 256-byte data memory (MSM65354)
  16K-byte program memory (MSM65353A)
- Local memory space : 384-byte data memory + SFR
- LCD driver : 32 × 4 (selectable duty cycle from 1/4, 1/3 or 1/2 with software)
- I/O port
  - Input-output port : 5 ports × 8 bits
  - Input port : 1 port × 1 bit, 1 port × 8 bits
  - Output port : 1 port × 1 bit
- Timer : 8-bit auto-reload timer × 3 (one of them can be used for the shift clock of shift register)
  : Watch timer counter × 1
- Counter : Time base counter × 1 (14 bits)
- Buzzer output circuit : 1 line, selectable from 1000Hz to 16000Hz (@10MHz)
- Shift register : 2ch, with 16-byte automatic transfer function × 1, clock sync mode × 1
- A/D converter : 8ch, 8 bits (4ch of them can start the CPU according to level detection interrupt)

- External interrupt : Three lines, selectable from rising edge/ falling edge/both edges
- Remote control circuit : Receives signal in 32.768kHz/5MHz/ 10MHz operations
- Interrupt source : 13
- Package:
  100-pin plastic QFP (QFP100-P-1420-0.65-BK4) (Product name:MSM65354-×××GS-BK4, MSM65353A-×××GS-BK4)
  ××× indicates the code number.
- Others : CPU clock can be an OSC, half-OSC, XT or 4 times XT clock
  : Time base counter clock can be selected with 1/4n of a CPU clock (n=1 to 8)
  : Stop status can be set at each port (high impedance or prior status is retained)
  : Pull-up or open can be set for each input-output port

BLOCK DIAGRAM



PIN CONFIGURATION (TOP VIEW)



100-Pin Plastic QFP

PIN DESCRIPTIONS

Basic Function

Function	Pin	Symbol	Type	Description
Power Supply	72	V_{DD}	—	Digital supply voltage (5V)
	83	GND	—	Digital ground
	47	AV_{DD}	—	Analog supply voltage (5V)
	37	AGND	—	Analog ground
	98	V_{DD1}	—	Bias supply pin for LCD driver
	99	V_{DD2}	—	Bias supply pin for LCD driver
	100	V_{DD3}	—	Bias supply pin for LCD driver
	97	V_{DDL}	—	Bias control pin for LCD driver
Oscillation	82	OSC0	I	Oscillation input pin on the OSC side: Connect to a quartz oscillator (ceramic resonator), or input external clock.
	81	$\overline{OSC1}$	O	Oscillation output pin on the OSC side: Connect to a quartz oscillator (ceramic resonator). When external clock is input to the OSC0 pin, the $\overline{OSC1}$ pin should be open.
	84	XT	I	Oscillation input pin on the XT side: Connect to a quartz oscillator of 32.768kHz.
	85	$\overline{XT}$	O	Oscillation output pin on the XT side: Connect to a quartz oscillator of 32.768kHz.

Basic Function (Continued)

Function	Pin	Symbol	Type	Description
Control	94	$\overline{\text{RESET}}$	I	System reset input: When this pin is set to the "L" level, the internal status is initialized to start execution of instructions from address 0040H. The input is pulled up to V_{DD} with an internal pull-up resistor.
Ports	80 to 73	P0.0 to P0.7	I/O	8-bit input-output port (port 0): Each of bits 0 to 7 is configured to be input or output by use of the direction register of port 0 (P0DIR). In addition to the basic function as the input-output port, a secondary function is allocated to each of P0.0 through P0.7. See Secondary function.
	71 to 64	P1.0 to P1.7	I/O	8-bit input-output port (port 1): Each of bits 0 to 7 is configured to be input or output by use of the direction register of port 1 (P1DIR). In addition to the basic function as the input-output port, a secondary function is allocated to each of P1.0 through P1.7. See Secondary function.
	93 to 86	P2.0 to P2.7	I/O	8-bit input-output port (port 2): Each of bits 0 to 7 is configured to be input or output by use of the direction register of port 2 (P2DIR). In addition to the basic function as the input-output port, a secondary function is allocated to each of P2.0 through P2.3. See Secondary function.

Basic Function (Continued)

Function	Pin	Symbol	Type	Description
Ports	38 to 45	P3.0 to P3.7	I	8-bit input port (port 3): Each of P3.0 to P3.7 funcitons as analog input channel of A/D converter.
	63 to 56	P4.0 to P4.7	I/O	8-bit input-output port (port 4): 8-bit input-output port.
	55 to 48	P5.0 to P5.7	I/O	8-bit input-output port (port 5): Each of bits 0 to 7 is configured to be input or output by the direction register of port 5 (P5DIR).
	95	P6.0 (IN)	I	1-bit input port (port 6.0): 1-bit input port.
	96	P6.1 (OUT)	O	1-bit output port (port 6.1): Pulled high at the time of reset. If this pin is set to the "0" level during reset, this IC goes into a test mode, disabling execution of the user program.
LCD Driver	1 to 4	COM1 to COM4	O	LCD common signal output pins.
	5 to 36	SEG0 to SEG31	O	LCD segment signal output pins.

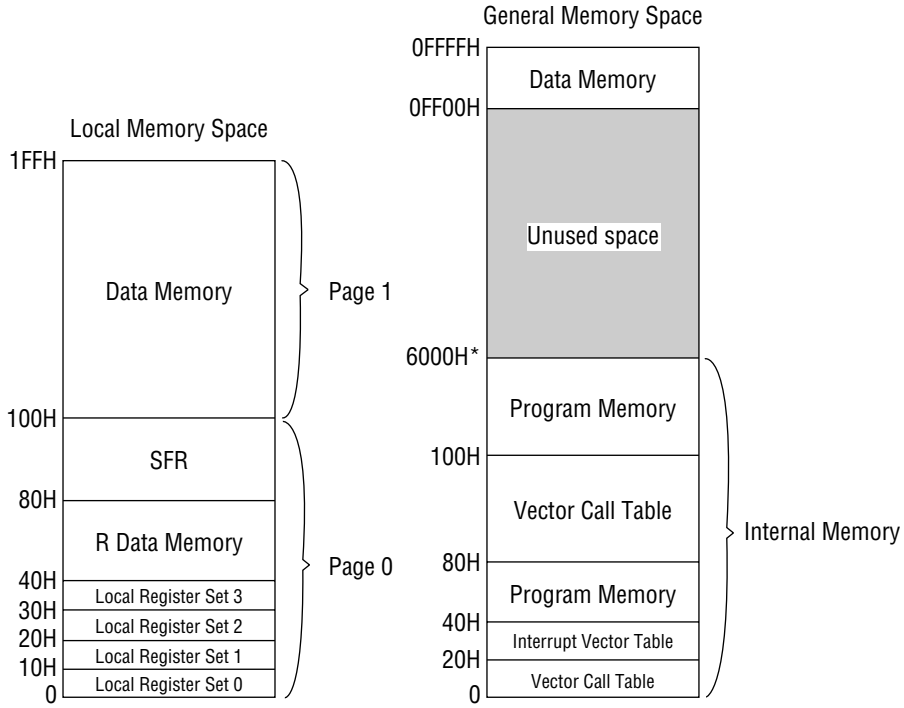
Secondary Function

Function	Pin	Symbol	Type	Description
External Interrupt	80	INT0	I	Secondary function of P0.0: Input pin for external interrupt 0. This pin can receive input at the rising edge, falling edge, or both the rising/falling edges.
	76	INT1	I	Secondary function of P0.4: Input pin for external interrupt 1. This pin can receive input at the rising edge, falling edge, or both the rising/falling edges. Also used as a gate signal input pin to enable or disable the count of timer 0.
	90	INT2	I	Secondary function of P2.3: Input pin for external interrupt 2. This pin can receive input at the rising edge, falling edge, or the both rising/falling edges.
	38 to 41	INT3	I	Secondary function of P3.0 to 3.3: Input pin for external interrupt 3. This pin can receive input at the rising edge, falling edge, or both the rising/falling edges.
Control	79	$\overline{\text{HSTOP}}$	I	Secondary function of P0.1: Hardware stop mode input pin. When this pin is set to the "L" level while the HSTP bit in SBYCON is set to "1", the hardware stop mode is entered. In the hardware stop mode, oscillation on the OSC side is stopped for low power consumption.
Timer 0	77	T0CK	I	Secondary function of P0.3: External clock input pin for timer 0.
Timer 1	78	T1OUT	O	Secondary function of P0.2: Output pin that provides waveform with a cycle twice the overflow of timer 1.
A/D Converter	38 to 45	AI0 to AI7	I	Secondary function of P3.0 to 3.7: These are used for analog input channels in A/D conversion.

Secondary Function (Continued)

Function	Pin	Symbol	Type	Description
Clock Output	75	CLKOUT	O	Secondary function of P0.5: Output pin for OSCCLK divided by 2 or 4 or for XTCLK divided by 2 or 4.
Buzzer Output	73	BZ	O	Secondary function of P0.7: Output pin for buzzer.
Remote Control Input	67	RMCIN	I	Secondary function of P1.4: Input pin for remote control.
Shift Register	91	SFTO0	O	Secondary function of P2.2: Data output pin for shift register 0.
	92	SFTI0	I	Secondary function of P2.1: Data Input pin for shift register 0.
	93	SFTCK0	I/O	Secondary function of P2.2: Sync. clock input-output pin for shift register 0. This provides a clock output when used as the master, or it functions as clock input when used as a slave.
	64	SFTO1	O	Secondary function of P1.7: Data output pin for shift register 1.
	65	SFTI1	I	Secondary function of P1.6: Data Input pin for shift register 1.
	66	SFTCK1	I/O	Secondary function of P1.5: Sync. clock input-output pin for shift register 1. This provides a clock output when used as the master, or it functions as clock input when used as a slave.

MEMORY MAPS



* 4000H, in the case of MSM65353A

ABSOLUTE MAXIMUM RATINGS

Parameter	Symbol	Condition	Rating	Unit
Supply Voltage	V_{DD}	Ta = 25°C	–0.3 to 7.0	V
Input Voltage	V_I		–0.3 to V_{DD}+0.3	
Output Voltage	V_O		–0.3 to V_{DD}+0.3	
Maximum Allowable Dissipation	P_D	Ta = 25°C, per package	400	mW
		Ta = 25°C, per output	50	
Storage Temperature	T_{STG}	—	–55 to +150	°C

RECOMMENDED OPERATING CONDITIONS

Parameter	Symbol	Condition	Range	Unit
Supply Voltage	V_{DD}	—	2.7 to 5.5	V
Memory Hold Voltage	V_{DDMH}	f_{OSC} = 0Hz	2.0 to 5.5	
Oscillation Frequency*1	f_{OSC}	—	1 to 10	MHz
	f_{XT}	V_{DD} = 2.7 to 5.5	32.768/75	kHz
External Clock Operating Frequency*2	f_{EXTCLK}	—	1 to 10	MHz
Operating Temperature	T_{op}	—	–20 to +70	°C

*1 Determined by the crystal oscillator or ceramic resonator to be used.
*2 External clock cannot be used in the XT pin.

ELECTRICAL CHARACTERISTICS

DC Characteristics 1 (V_{DD}=4.5 to 5.5V)

(GND = 0V, Ta = –20 to +70°C)

Parameter	Symbol	Condition	Min.	Typ.	Max.	Unit
"H" Input Voltage 1 *1	V_{IH1}	CPUCLK=1MHz	2.4	—	—	V
"H" Input Voltage 2 *2	V_{IH2}	CPUCLK=1MHz	$0.75V_{DD}$	—	—	
"L" Input Voltage	V_{IL}	CPUCLK=1MHz	—	—	0.8	
"H" Output Voltage 1 *3	V_{OH1}	I_{OH} = –200µA	$0.75V_{DD}$	—	—	
"H" Output Voltage 2 *4	V_{OH2}	I_{OH} = –400µA	$0.75V_{DD}$	—	—	
"L" Output Voltage 1 *3	V_{OL1}	I_{OL} = 1.6mA	—	—	0.4	
"L" Output Voltage 2 *4	V_{OL2}	I_{OL} = 3.2mA	—	—	0.4	
Segment and Common Driver Output Voltage	V_0	I = +10µA	—	—	0.4	
	V_1	V_{DD1} = 1.4V, I = ±10µA	V_{DD1}–0.4	—	V_{DD1}+0.4	
	V_2	V_{DD2} = 2.8V, I = ±10µA	V_{DD2}–0.4	—	V_{DD2}+0.4	
	V_3	V_{DD3} = 4.2V, I = –10µA	V_{DD3}–0.4	—	—	
Input Leakage Current *5	I_{LI2}	V_I = V_{DD}/0V	—	—	±10	µA
"L" Input Current *6	I_{IL}	V_I = 0V, V_{DD} = 5V	–40	–200	–400	
Input Capacitance	C_I	f = 1MHz, Ta = 25°C	—	5	—	pF
Operating Current Consumption V_{DD} = 5V XT = 32kHz OSC = 10MHz	I_{DD1}	Stop mode, during LCD stop, no load *7	—	7	14	µA
	I_{DD2}	Stop mode, during LCD operation, no load *7	—	15	30	µA
	I_{DD3}	CPUCLK = 32kHz, HALT mode *8	—	30	60	µA
	I_{DD4}	CPUCLK = 32kHz, no load *9	—	80	160	µA
	I_{DD5}	CPUCLK = 10MHz, HALT mode	—	8	16	mA
	I_{DD6}	CPUCLK = 10MHz, no load	—	20	50	mA

*1 Excluding OSC0 and $\overline{\text{RESET}}$
*2 Only for OSC0 and $\overline{\text{RESET}}$
*3 Excluding P4
*4 Only for P4
*5 Excluding $\overline{\text{RESET}}$
*6 Only for $\overline{\text{RESET}}$
*7 Including hardware stop mode
*8 Measured when OSC clock is stopped but LCD is operated without load
*9 Measured when OSC clock is stopped

DC Characteristics 2 (2.7V ≤ V_{DD} < 4.5V)

(GND = 0V, Ta = –20 to +70˚C)

Parameter	Symbol	Condition	Min.	Typ.	Max.	Unit
"H" Input Voltage 1 *1	V_{IH1}	CPUCLK=1MHz	$0.3V_{DD}$ +0.9	—	—	V
"H" Input Voltage 2 *2	V_{IH2}	CPUCLK=1MHz	$0.6V_{DD}$ +0.6 *10	—	—	
"L" Input Voltage	V_{IL}	CPUCLK=1MHz	—	—	$0.3V_{DD}$ –0.1 *11	
"H" Output Voltage 1 *3	V_{OH1}	I_{OH} = –10µA	$0.75V_{DD}$	—	—	
"H" Output Voltage 2 *4	V_{OH2}	I_{OH} = –20µA	$0.75V_{DD}$	—	—	
"L" Output Voltage 1 *3	V_{OL1}	I_{OL} = 10µA	—	—	0.1	
"L" Output Voltage 2 *4	V_{OL2}	I_{OL} = 20µA	—	—	0.1	
Segment and Common Driver Output Voltage	V_0	I = +10µA	—	—	0.4	
	V_1	V_{DD1} = 1.4V, I = ±10µA	V_{DD1}–0.4	—	V_{DD1}+0.4	
	V_2	V_{DD2} = 2.8V, I = ±10µA	V_{DD2}–0.4	—	V_{DD2}+0.4	
	V_3	V_{DD3} = 4.2V, I = –10µA	V_{DD3}–0.4	—	—	
Input Leakage Current *5	I_{LI2}	V_I = V_{DD}/0V	—	—	±10	µA
"L" Input Current *6	I_{IL}	V_I = 0V, V_{DD} = 3V	–40	–125	–250	
Input Capacitance	C_I	f = 1MHz, Ta = 25˚C	—	5	—	pF
Operating Current Consumption V_{DD} = 3V XT = 32kHz OSC = 5MHz	I_{DD1}	Stop mode, during LCD stop, no load *7	—	4	8	µA
	I_{DD2}	Stop mode, during LCD operation, no load *7	—	8	16	µA
	I_{DD3}	CPUCLK = 32kHz, HALT mode *8	—	15	30	µA
	I_{DD4}	CPUCLK = 32kHz, no load *9	—	45	90	µA
	I_{DD5}	CPUCLK = 5MHz, HALT mode	—	1.5	3	mA
	I_{DD6}	CPUCLK = 5MHz, no load	—	5	16	mA

*1 Excluding OSC0 and $\overline{\text{RESET}}$
*2 Only for OSC0 and $\overline{\text{RESET}}$
*3 Excluding P4
*4 Only for P4
*5 Excluding $\overline{\text{RESET}}$
*6 Only for $\overline{\text{RESET}}$
*7 Including hardware stop mode
*8 Measured when OSC clock is stopped but LCD is operated without load
*9 Measured when OSC clock is stopped
*10 More than 3.375V
*11 Less than 0.8V

AC Characteristics

• CPU control

(V_{DD} = 2.7 to 5.5V, GND = 0V, Ta = –20 to +70°C)

Parameter	Symbol	Condition	Min.	Max.	Unit
$\overline{\text{RESET}}$ Pulse Width	t_{RESW}	—	20	—	ns

• Peripheral control 1

(V_{DD} = 2.7 to 5.5V, GND = 0V, Ta = –20 to +70°C)

Parameter		Symbol	Condition	Min.	Max.	Unit
OSC	Clock Cycle	t_C	V_{DD} = 4.5 to 5.5V	100	—	ns
			2.7V ≤ V_{DD} < 4.5V	200	—	
	Clock "L" Pulse Width	t_{CLW}	—	0.45t_C	0.55t_C	
EXI	External Interrupt Pulse Width	t_{EXIW}	—	4CPUCLK *1	—	
T0	External Clock Pulse Width	t_{T0CW}		4CPUCLK *1	—	
	GATE Pulse Width	t_{T0GW}		4 t_{T0CLK} *2	—	

*1 CPUCLK : Supply clock to the CPU selected by SBYCON.

*2 t_{T0CLK} : Cycle time of timer 0 count clock selected by T0CON.

• Peripheral control 2

(V_{DD} = 2.7 to 5.5V, GND = 0V, Ta = –20 to +70°C)

Parameter		Symbol	Condition	MIN	MAX	Unit
OSC	Clock Cycle	t_C	V_{DD} = 4.5 to 5.5V	100	—	ns
			2.7V ≤ V_{DD} < 4.5V	200	—	
SFT0, 1	SFTCK Cycle	$t_{SFC0, 1}$	C_L = 100 pF	8CPUCLK *1	—	
	SFTCK "L" Pulse Width	$t_{SFCLW0, 1}$		4CPUCLK –20 *1	—	
	SFTCK "H" Pulse Width	$t_{SFCHW0, 1}$		4CPUCLK –20 *1	—	
	SFTO Setup Time	$t_{SFOS0, 1}$		$t_{SFCLW0, 1}$ –100	—	
	SFTO Hold Time	$t_{SFOH0, 1}$		$t_{SFCHW0, 1}$ –100	—	
	SFTI Setup Time	$t_{SFIS0, 1}$		100	—	
	SFTI Hold Time	$t_{SFIH0, 1}$		100	—	

*1 CPUCLK : Supply clock to the CPU selected by SBYCON.

See Timing Diagram.

A/D Converter Characteristics 1

(V_{DD} = AV_{DD} = V_{RH} = 4.5 to 5.5V, GND = AGND = 0V, Ta = –20 to +70°C)

Parameter	Symbol	Condition	Min.	Typ.	Max.	Unit
Resolution	n	Refer to recommended circuit. Analog input source impedance $R_I \leq 5k\Omega$	—	8	—	bit
Linearity Error	E_L		—	—	+1.5 –1.5	LSB
Differential Linearity Error	E_D		—	—	±0.5	LSB
Zero Scale Error	E_{ZS}		—	—	+1.5	LSB
Full Scale Error	E_{FS}		—	—	–1.5	LSB
Crosstalk	E_{CT}	Refer to measuring circuit.	—	—	±0.5	LSB
Conversion Time*	t_{CONV}	f_{OSC} = 10MHz	—	16	—	µs/CH

* The conversion time immediately after GO bit is set to "1" is 14.8µs/CH.

A/D Converter Characteristics 2

(V_{DD} = AV_{DD} = V_{RH}, 2.7V ≤ V_{DD} < 4.5V, GND = AGND = 0V, Ta = –20 to +70°C)

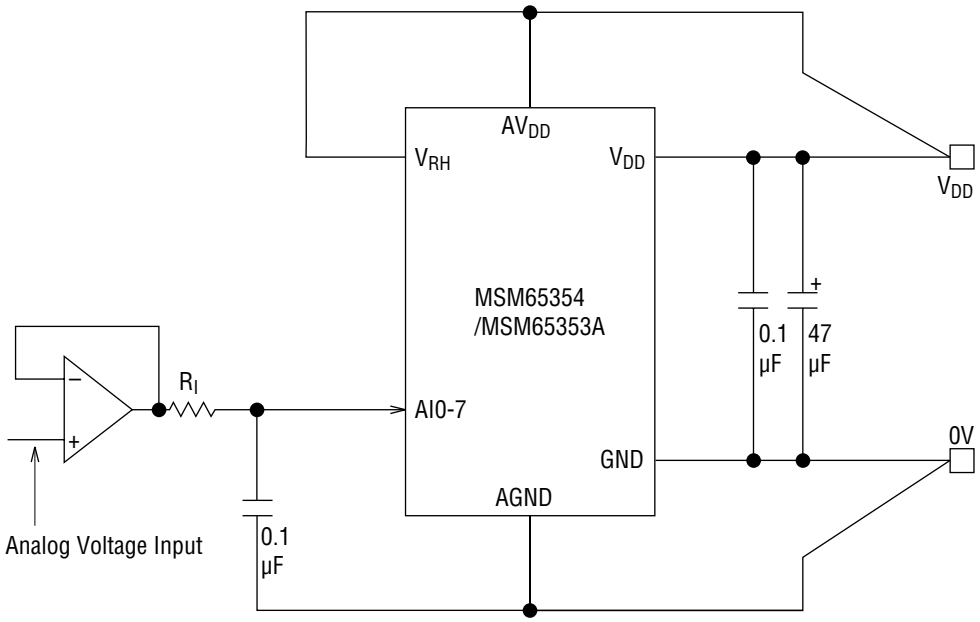
Parameter	Symbol	Condition	Min.	Typ.	Max.	Unit
Resolution	n	Refer to recommended circuit. Analog input source impedance $R_I \leq 5k\Omega$	—	8	—	bit
Linearity Error	E_L		—	—	+2 –2	LSB
Differential Linearity Error	E_D		—	—	±1	LSB
Zero Scale Error	E_{ZS}		—	—	+2	LSB
Full Scale Error	E_{FS}		—	—	–2	LSB
Crosstalk	E_{CT}	Refer to measuring circuit.	—	—	±1	LSB
Conversion Time*	t_{CONV}	f_{OSC} = 5MHz	—	32	—	µs/CH

* The conversion time immediately after GO bit is set to "1" is 29.6µs/CH.

Definition of Terms

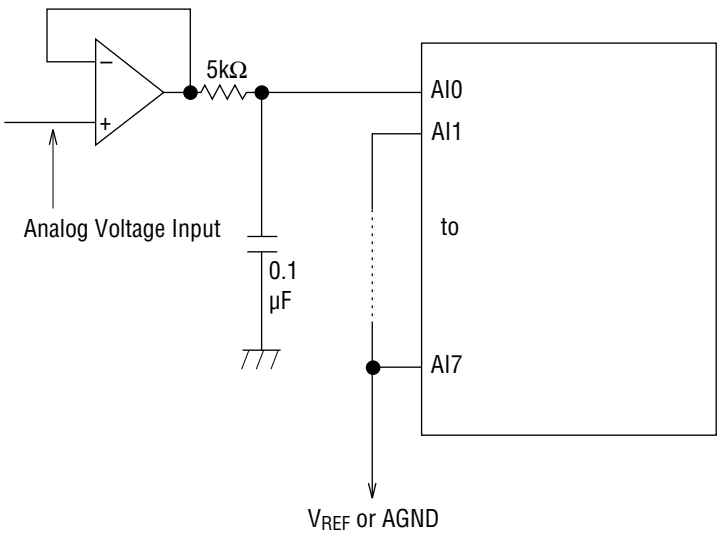
Resolution	Recognizable minimum input analog value. This can be resolved into $2^8 = 256$, that is $V_{RH} \div 256$
Linearity Error	Deviation between ideal conversion characteristics as an 8-bit A/D converter and actual conversion characteristics. (Not including quantization error.) Ideal conversion characteristics means a step which divides voltage between V_{RH} and AGND into 256.
Differential Linearity Error	Shows the smoothness of conversion characteristics. 1LSB = $V_{RH} \div 256$ is ideal for analog input voltage width corresponding to change per 1 bit of digital output. The differential linearity error is the deviation between this ideal bit size and a bit size at arbitrary point in conversion range.
Zero Scale Error	Deviation between ideal conversion characteristics of transfer point for digital outputs "000H" to "001H" and actual conversion characteristics.
Full Scale Error	Deviation between ideal conversion characteristics of transfer point for digital outputs "0FEH" to "0FFH" and actual conversion characteristics.

• **Recommended circuit**



R_I (Analog input source impedance) ≤ 5kΩ

• **Crosstalk measuring circuit**

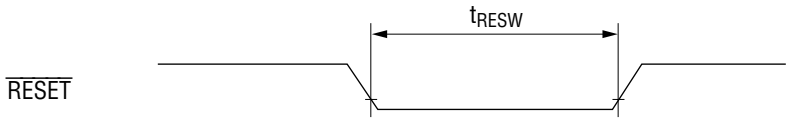


Crosstalk is defined as the difference of A/D conversion result between supplying the same voltage to AI0 to AI7 and supplying voltage shown in this left diagram.

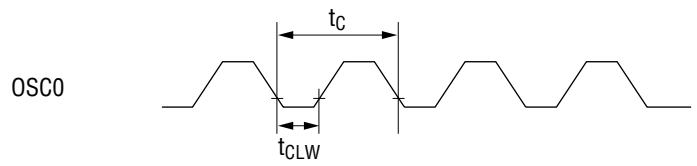
Timing Diagram

• CPU control

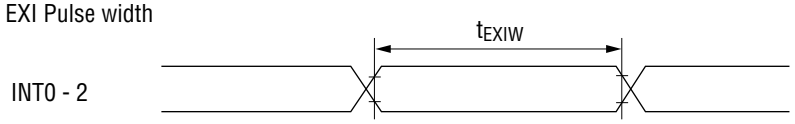
1) $\overline{\text{RESET}}$ Pulse width



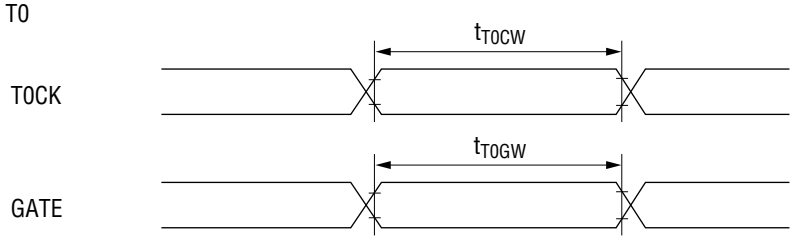
• Peripheral control 1



1) EXI Pulse width

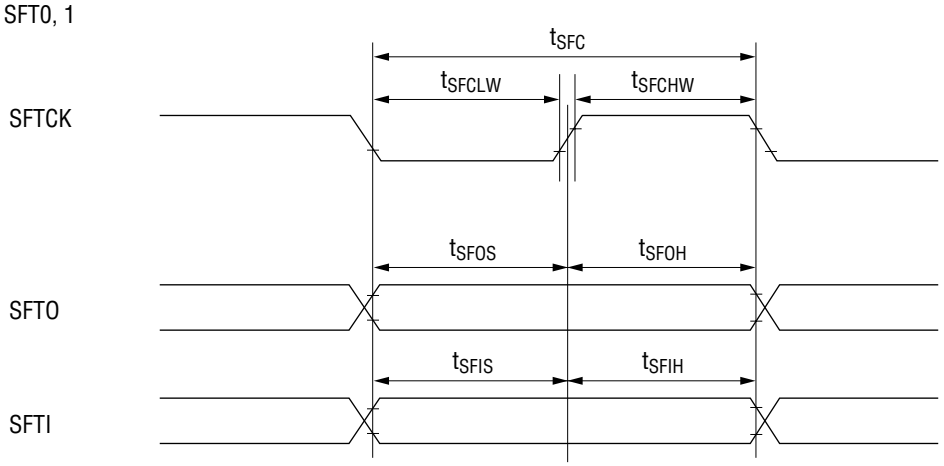


2) T0



• **Peripheral control 2**

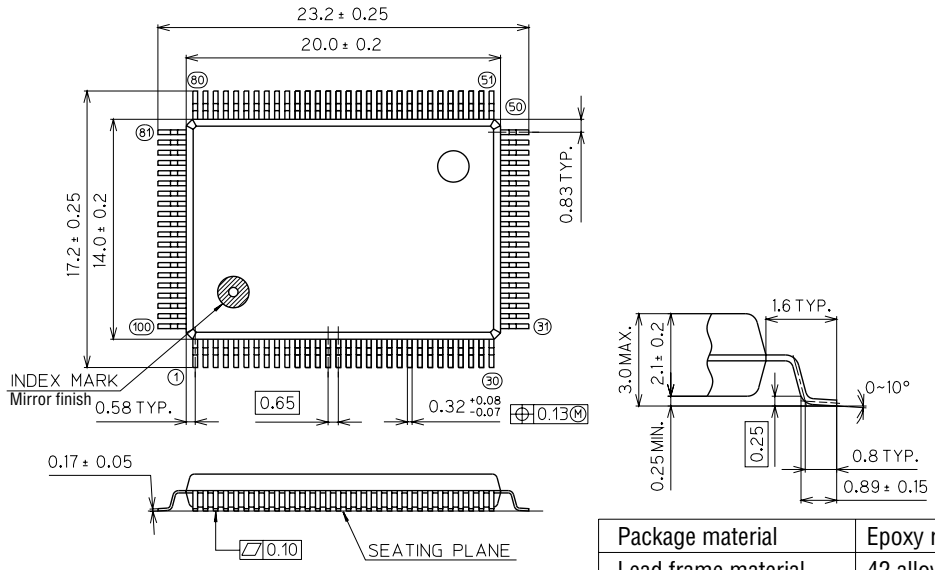
1) SFT0, 1



PACKAGE DIMENSIONS

(Unit : mm)

QFP100-P-1420-0.65-BK4



Package material	Epoxy resin
Lead frame material	42 alloy
Pin treatment	Solder plating
Solder plate thickness	5 μm or more
Package weight (g)	1.54 TYP.

Notes for Mounting the Surface Mount Type Package

The SOP, QFP, TSOP, SOJ, QFJ (PLCC), SHP and BGA are surface mount type packages, which are very susceptible to heat in reflow mounting and humidity absorbed in storage.
Therefore, before you perform reflow mounting, contact Oki's responsible sales person for the product name, package name, pin number, package code and desired mounting conditions (reflow method, temperature and times).