Digitally Controlled Potentiometer (XDCP™)

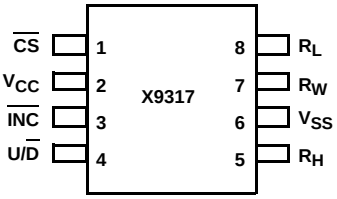
The Intersil X9317 is a digitally controlled potentiometer (XDCP™). The device consists of a resistor array, wiper switches, a control section, and nonvolatile memory. The wiper position is controlled by a 3-wire interface.

The potentiometer is implemented by a resistor array composed of 99 resistive elements and a wiper switching network. Between each element and at either end are tap points accessible to the wiper terminal. The position of the wiper element is controlled by the $\overline{CS}$, U/$\overline{D}$, and $\overline{INC}$ inputs. The position of the wiper can be stored in nonvolatile memory and then be recalled upon a subsequent power-up operation.

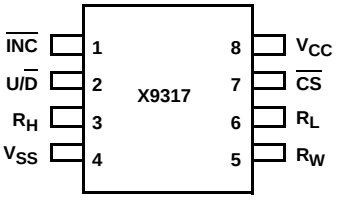
The device can be used as a three-terminal potentiometer for voltage control or as a two-terminal variable resistor for current control in a wide variety of applications.

Pinouts

X9317
(8 LD TSSOP)
TOP VIEW



X9317
(8 LD PDIP, 8 LD SOIC, 8 LD MSOP)
TOP VIEW



Features

- Solid-State Potentiometer
- 3-Wire Serial Up/Down Interface
- 100 Wiper Tap Points
  - Wiper Position Stored in Nonvolatile Memory and Recalled on Power-up
- 99 Resistive Elements
  - Temperature Compensated
  - End-to-end Resistance Range ±20%
- Low Power CMOS
  - V_{CC} = 2.7V to 5.5V, and 5V ±10%
  - Standby Current <5µA
- High Reliability
  - Endurance, 100,000 Data Changes per Bit
  - Register Data Retention, 100 years
- R_{TOTAL} Values = 1kΩ, 10kΩ, 50kΩ, 100kΩ
- Packages
  - 8 Ld SOIC, PDIP, TSSOP, and MSOP
- Pb-Free Available (RoHS Compliant)

Applications

- LCD Bias Control
- DC Bias Adjustment
- Gain and Offset Trim
- Laser Diode Bias Control
- Voltage Regulator Output Control

CAUTION: These devices are sensitive to electrostatic discharge; follow proper IC Handling Procedures.
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Ordering Information

PART NUMBER	PART MARKING	V_{CC} LIMITS (V)	R_{TOTAL} (kΩ)	TEMPERATURE RANGE (°C)	PACKAGE	PKG. DWG. #
X9317ZM8* (Note 2)	AFG	5 ±10%	1	0 to +70	8 Ld MSOP	M8.118
X9317ZM8Z* (Note 1)	DDA			0 to +70	8 Ld MSOP (Pb-free)	M8.118
X9317ZM8I* (Note 2)	AFI			-40 to +85	8 Ld MSOP	M8.118
X9317ZM8IZ* (Note 1)	DCY			-40 to +85	8 Ld MSOP (Pb-free)	M8.118
X9317ZP (Note 2)	X9317ZP			0 to +70	8 Ld PDIP	MDP0031
X9317ZS8* (Note 2)	X9317Z			0 to +70	8 Ld SOIC	M8.15E
X9317ZS8Z* (Note 1)	X9317Z Z			0 to +70	8 Ld SOIC (Pb-free)	M8.15E
X9317ZS8I* (Note 2)	9317W F			-40 to +85	8 Ld SOIC	M8.15E
X9317ZS8IZ* (Note 1)	X9317Z Z I			-40 to +85	8 Ld SOIC (Pb-free)	M8.15E
X9317ZV8* (Note 2)	9317Z			0 to +70	8 Ld TSSOP	M8.173
X9317ZV8Z* (Note 1)	9317Z Z			0 to +70	8 Ld TSSOP (Pb-free)	M8.173
X9317ZV8I* (Note 2)	317Z I			-40 to +85	8 Ld TSSOP	M8.173
X9317ZV8IZ* (Note 1)	9317Z IZ			-40 to +85	8 Ld TSSOP (Pb-free)	M8.173
X9317WM8T1 (Note 2)	ABF		10	0 to +70	8 Ld MSOP	M8.118
X9317WM8Z* (Note 1)	DCW			0 to +70	8 Ld MSOP (Pb-free)	M8.118
X9317WM8I*	ADS			-40 to +85	8 Ld MSOP	M8.118
X9317WM8 (Note 2)	ABF			-40 to +85	8 Ld MSOP	M8.118
X9317WM8IZ* (Note 1)	DCT			-40 to +85	8 Ld MSOP (Pb-free)	M8.118
X9317WP	X9317WP			0 to +70	8 Ld PDIP	MDP0031
X9317WPI (Note 2)	X9317WP I			-40 to +85	8 Ld PDIP	MDP0031
X9317WS8*	X9317W			0 to +70	8 Ld SOIC	M8.15E
X9317WS8Z* (Note 1)	X9317W Z			0 to +70	8 Ld SOIC (Pb-free)	M8.15E
X9317WS8I	X9317W I			-40 to +85	8 Ld SOIC	M8.15E
X9317WS8IT1 (Note 2)	X9317W I			-40 to +85	8 Ld SOIC	M8.15E
X9317WS8IZ* (Note 1)	X9317W ZI			-40 to +85	8 Ld SOIC (Pb-free)	M8.15E
X9317WV8	9317W			0 to +70	8 Ld TSSOP	M8.173
X9317WV8T1 (Note 2)	9317W			0 to +70	8 Ld TSSOP	M8.173
X9317WV8T2 (Note 2)	9317W			0 to +70	8 Ld TSSOP	M8.173
X9317WV8Z* (Note 1)	9317W Z			0 to +70	8 Ld TSSOP (Pb-free)	M8.173
X9317WV8I	317W I			-40 to +85	8 Ld TSSOP	M8.173
X9317WV8IT1 (Note 2)	317W I			-40 to +85	8 Ld TSSOP	M8.173
X9317WV8IZ* (Note 1)	9317W IZ			-40 to +85	8 Ld TSSOP (Pb-free)	M8.173
X9317UM8* (Note 2)	AEC			0 to +70	8 Ld MSOP	M8.118
X9317UM8Z* (Note 1)	DCS			0 to +70	8 Ld MSOP (Pb-free)	M8.118
X9317UM8I* (Note 2)	AFE			-40 to +85	8 Ld MSOP	M8.118
X9317UM8IZ* (Note 1)	DCR			-40 to +85	8 Ld MSOP (Pb-free)	M8.118
X9317UP (Note 2)	X9317UP		50	0 to +70	8 Ld PDIP	MDP0031
X9317UPI (Note 2)	X9317UP I			-40 to +85	8 Ld PDIP	MDP0031
X9317US8* (Note 2)	X9317U			0 to +70	8 Ld SOIC	M8.15E
X9317US8Z* (Note 1)	X9317U Z			0 to +70	8 Ld SOIC (Pb-free)	M8.15E
X9317US8I* (Note 2)	X9317U I			-40 to +85	8 Ld SOIC	M8.15E
X9317US8IZ* (Note 1)	X9317U ZI			-40 to +85	8 Ld SOIC (Pb-free)	M8.15E

Ordering Information (Continued)

PART NUMBER	PART MARKING	V_{CC} LIMITS (V)	R_{TOTAL} (kΩ)	TEMPERATURE RANGE (°C)	PACKAGE	PKG. DWG. #
X9317UV8* (Note 2)	9317U	5 ±10%	50	0 to +70	8 Ld TSSOP	M8.173
X9317UV8Z* (Note 1)	9317U Z			0 to +70	8 Ld TSSOP (Pb-free)	M8.173
X9317UV8I* (Note 2)	317U I			-40 to +85	8 Ld TSSOP	M8.173
X9317UV8IZ* (Note 1)	9317U IZ			-40 to +85	8 Ld TSSOP (Pb-free)	M8.173
X9317TM8*, ** (Note 2)	AGD		100	0 to +70	8 Ld MSOP	M8.118
X9317TM8Z* (Note 1)	DCN			0 to +70	8 Ld MSOP (Pb-free)	M8.118
X9317TM8I*, ** (Note 2)	AGF			-40 to +85	8 Ld MSOP	M8.118
X9317TM8IZ* (Note 1)	DCL			-40 to +85	8 Ld MSOP (Pb-free)	M8.118
X9317TP (Note 2)	X9317TP			0 to +70	8 Ld PDIP	MDP0031
X9317TPI (Note 2)	X9317TP I			-40 to +85	8 Ld PDIP	MDP0031
X9317TS8 (Note 2)	X9317T			0 to +70	8 Ld SOIC	M8.15E
X9317TS8Z (Note 1)	X9317T Z			0 to +70	8 Ld SOIC (Pb-free)	M8.15E
X9317TS8I (Note 2)	X9317T I			-40 to +85	8 Ld SOIC	M8.15E
X9317TS8IZ (Note 1)	X9317T ZI			-40 to +85	8 Ld SOIC (Pb-free)	M8.15E
X9317TV8*, ** (Note 2)	9317T			0 to +70	8 Ld TSSOP	M8.173
X9317TV8Z* (Note 1)	9317T Z			0 to +70	8 Ld TSSOP (Pb-free)	M8.173
X9317TV8I*, ** (Note 2)	317T I			-40 to +85	8 Ld TSSOP	M8.173
X9317TV8IZ* (Note 1)	9317T IZ			-40 to +85	8 Ld TSSOP (Pb-free)	M8.173
X9317ZM8-2.7* (Note 2)	AFH	2.7 to 5.5	1	0 to +70	8 Ld MSOP	M8.118
X9317ZM8Z-2.7* (Note 1)	AOA			0 to +70	8 Ld MSOP (Pb-free)	M8.118
X9317ZM8I-2.7* (Note 2)	AFJ			-40 to +85	8 Ld MSOP	M8.118
X9317ZM8IZ-2.7* (Note 1)	DCZ			-40 to +85	8 Ld MSOP (Pb-free)	M8.118
X9317ZS8-2.7* (Note 2)	X9317Z F			0 to +70	8 Ld SOIC	M8.15E
X9317ZS8Z-2.7* (Note 1)	X9317Z ZF			0 to +70	8 Ld SOIC (Pb-free)	M8.15E
X9317ZS8I-2.7* (Note 2)	X9317Z G			-40 to +85	8 Ld SOIC	M8.15E
X9317ZS8IZ-2.7* (Note 1)	X9317Z ZG			-40 to +85	8 Ld SOIC (Pb-free)	M8.15E
X9317ZV8-2.7* (Note 2)	317Z F			0 to +70	8 Ld TSSOP	M8.173
X9317ZV8Z-2.7* (Note 1)	9317Z FZ			0 to +70	8 Ld TSSOP (Pb-free)	M8.173
X9317ZV8I-2.7*, ** (Note 2)	317Z G			-40 to +85	8 Ld TSSOP	M8.173
X9317ZV8IZ-2.7* (Note 1)	9317Z GZ			-40 to +85	8 Ld TSSOP (Pb-free)	M8.173
X9317WM8-2.7* (Note 2)	ACZ		10	0 to +70	8 Ld MSOP	M8.118
X9317WM8Z-2.7* (Note 1)	DCX			0 to +70	8 Ld MSOP (Pb-free)	M8.118
X9317WM8I-2.7	ADT			-40 to +85	8 Ld MSOP	M8.118
X9317WM8I-2.7T1 (Note 2)	ADT			-40 to +85	8 Ld MSOP	M8.118
X9317WM8IZ-2.7* (Note 2)	DCU			-40 to +85	8 Ld MSOP (Pb-free)	M8.118
X9317WP-2.7 (Note 2)	X9317WP F			0 to +70	8 Ld PDIP	MDP0031
X9317WPI-2.7 (Note 2)	X9317WP G			-40 to +85	8 Ld PDIP	MDP0031
X9317WS8-2.7	X9317W F			0 to +70	8 Ld SOIC	M8.15E
X9317WS8-2.7T1 (Note 2)	X9317W F			0 to +70	8 Ld SOIC	M8.15E
X9317WS8Z-2.7* (Note 1)	X9317W ZF			0 to +70	8 Ld SOIC (Pb-free)	M8.15E
X9317WS8I-2.7** (Note 2)	X9317W G			-40 to +85	8 Ld SOIC	M8.15E
X9317WS8I-2.7T1	X9317W G			-40 to +85	8 Ld SOIC	M8.15E

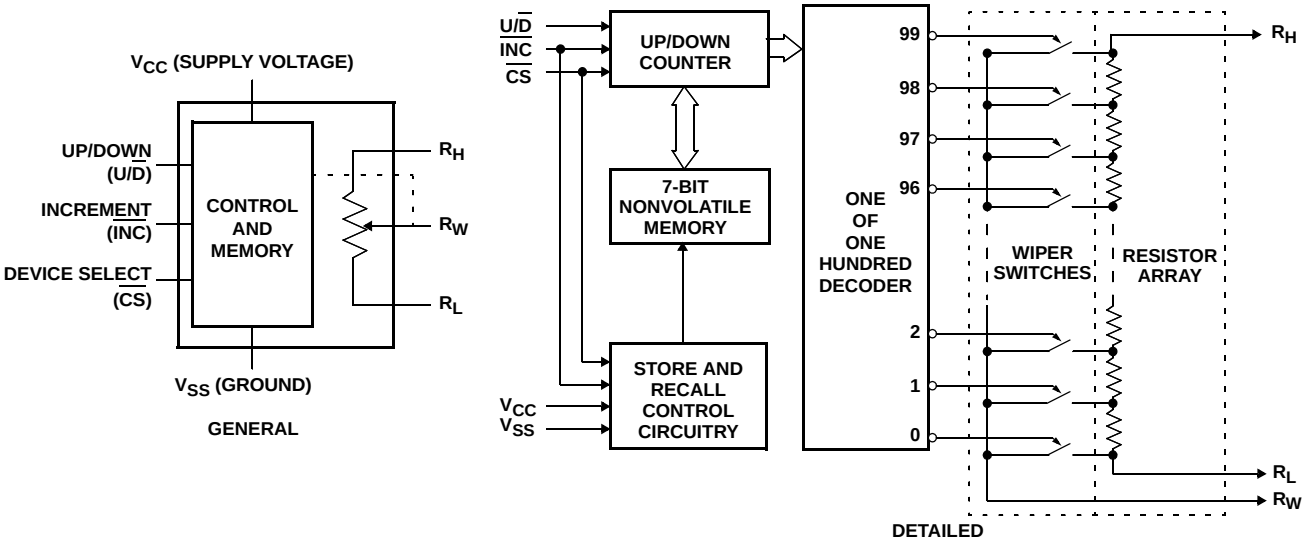
Ordering Information (Continued)

PART NUMBER	PART MARKING	V_{CC} LIMITS (V)	R_{TOTAL} (kΩ)	TEMPERATURE RANGE (°C)	PACKAGE	PKG. DWG. #
X9317WS8IZ-2.7* (Note 1)	X9317W ZG	2.7 to 5.5	10	-40 to +85	8 Ld SOIC (Pb-free)	M8.15E
X9317WV8-2.7* (Note 2)	317W F			0 to +70	8 Ld TSSOP	M8.173
X9317WV8Z-2.7* (Note 1)	9317W FZ			0 to +70	8 Ld TSSOP (Pb-free)	M8.173
X9317WV8I-2.7*, ** (Note 2)	317W G			-40 to +85	8 Ld TSSOP	M8.173
X9317WV8IZ-2.7* (Note)	AKZ			-40 to +85	8 Ld TSSOP (Pb-free)	M8.173
X9317UM8-2.7* (Note 2)	AED			0 to +70	8 Ld MSOP	M8.118
X9317UM8Z-2.7* (Note 1)	AOB			0 to +70	8 Ld MSOP (Pb-free)	M8.118
X9317UM8I-2.7*, ** (Note 2)	AFF			-40 to +85	8 Ld MSOP	M8.118
X9317UM8IZ-2.7* (Note 1)	AOH			-40 to +85	8 Ld MSOP (Pb-free)	M8.118
X9317US8-2.7* (Note 2)	X9317U F		50	0 to +70	8 Ld SOIC	M8.15E
X9317UP-2.7 (Note 2)	X9317UP F			0 to +70	8 Ld PDIP	MDP0031
X9317UPI-2.7 (Note 2)	X9317UP G			-40 to +85	8 Ld PDIP	MDP0031
X9317US8Z-2.7* (Note 1)	X9317U ZF			0 to +70	8 Ld SOIC (Pb-free)	M8.15E
X9317US8I-2.7*, ** (Note 2)	X9317U G			-40 to +85	8 Ld SOIC	M8.15E
X9317US8IZ-2.7* (Note 1)	X9317U ZG			-40 to +85	8 Ld SOIC (Pb-free)	M8.15E
X9317UV8-2.7* (Note 2)	317U F			0 to +70	8 Ld TSSOP	M8.173
X9317UV8Z-2.7* (Note 1)	9317U FZ			0 to +70	8 Ld TSSOP (Pb-free)	M8.173
X9317UV8I-2.7*, ** (Note 2)	317U G			-40 to +85	8 Ld TSSOP	M8.173
X9317UV8IZ-2.7* (Note 1)	9317U GZ			-40 to +85	8 Ld TSSOP (Pb-free)	M8.173
X9317TM8-2.7*, ** (Note 2)	AGE		100	0 to +70	8 Ld MSOP	M8.118
X9317TM8Z-2.7* (Note 1)	DCP			0 to +70	8 Ld MSOP (Pb-free)	M8.118
X9317TM8I-2.7*, ** (Note 2)	AGG			-40 to +85	8 Ld MSOP	M8.118
X9317TM8IZ-2.7* (Note 1)	DCM			-40 to +85	8 Ld MSOP (Pb-free)	M8.118
X9317TP-2.7 (Note 2)	X9317TP F			0 to +70	8 Ld PDIP	MDP0031
X9317TPI-2.7 (Note 2)	X9317TP G			-40 to +85	8 Ld PDIP	MDP0031
X9317TS8-2.7*, ** (Note 2)	X9317T F			0 to +70	8 Ld SOIC	M8.15E
X9317TS8Z-2.7* (Note 1)	X9317T ZF			0 to +70	8 Ld SOIC (Pb-free)	M8.15E
X9317TS8I-2.7*, ** (Note 2)	X9317T G			-40 to +85	8 Ld SOIC	M8.15E
X9317TS8IZ-2.7* (Note 1)	X9317T ZG			-40 to +85	8 Ld SOIC (Pb-free)	M8.15E
X9317TV8-2.7*, ** (Note 2)	317T F			0 to +70	8 Ld TSSOP	M8.173
X9317TV8Z-2.7* (Note 1)	9317T FZ			0 to +70	8 Ld TSSOP (Pb-free)	M8.173
X9317TV8I-2.7*, ** (Note 2)	317T G			-40 to +85	8 Ld TSSOP	M8.173
X9317TV8IZ-2.7* (Note 1)	9317T GZ			-40 to +85	8 Ld TSSOP (Pb-free)	M8.173

*Add "T1" suffix for tape and reel. Please refer to TB347 for details on reel specifications.
**Add "T2" suffix for tape and reel. Please refer to TB347 for details on reel specifications.
NOTES:

1. These Intersil Pb-free plastic packaged products employ special Pb-free material sets, molding compounds/die attach materials, and 100% matte tin plate plus anneal (e3 termination finish, which is RoHS compliant and compatible with both SnPb and Pb-free soldering operations). Intersil Pb-free products are MSL classified at Pb-free peak reflow temperatures that meet or exceed the Pb-free requirements of IPC/JEDEC J STD-020.
2. Not recommended for new designs.

Block Diagram



Pin Descriptions

PDIP/SOIC/MSOP	TSSOP	SYMBOL	BRIEF DESCRIPTION
1	3	$\overline{INC}$	**Increment** Toggling $\overline{INC}$ while $\overline{CS}$ is low moves the wiper either up or down.
2	4	U/$\overline{D}$	**Up/Down** The U/$\overline{D}$ input controls the direction of the wiper movement.
3	5	R_H	The high terminal is equivalent to one of the fixed terminals of a mechanical potentiometer.
4	6	V_{SS}	**Ground**
5	7	R_W	The wiper terminal is equivalent to the movable terminal of a mechanical potentiometer.
6	8	R_L	The low terminal is equivalent to one of the fixed terminals of a mechanical potentiometer.
7	1	$\overline{CS}$	**Chip Select** The device is selected when the $\overline{CS}$ input is LOW, and de-selected when $\overline{CS}$ is high.
8	2	V_{CC}	**Supply Voltage**

Absolute Maximum Ratings

I_W (10s) . . . . . ±8.8mA
R_H, R_W, R_L to Ground . . . . . +6V
Voltage on $\overline{CS}$, $\overline{INC}$, U/$\overline{D}$ and V_{CC}
with Respect to V_{SS} . . . . . -1V to +7V

Thermal Information

Junction Temperature Under Bias . . . . . -65°C to +135°C
Storage Temperature . . . . . -65°C to +150°C
Pb-free reflow profile . . . . . .see link below
http://www.intersil.com/pbfree/Pb-FreeReflow.asp

CAUTION: Do not operate at or near the maximum ratings listed for extended periods of time. Exposure to such conditions may adversely impact product reliability and result in failures not covered by warranty.

Potentiometer Specifications

V_{CC} = Full Range, T_A = Full Operating Temperature Range, unless otherwise stated.

SYMBOL	PARAMETER	TEST CONDITIONS/NOTES	MIN (Note 8)	TYP (Note 4)	MAX (Note 8)	UNIT
R_{TOTAL}	End-to-end Resistance Tolerance	See “Ordering Information” beginning on page 2 for values	-20		+20	%
$V_{RH}/_{RL}$	R_H/R_L Terminal Voltage	V_{SS} = 0V	V_{SS}		V_{CC}	V
	Power Rating	$R_{TOTAL} \geq 10k\Omega$			10	mW
		R_{TOTAL} = 1kΩ			25	mW
R_W	Wiper Resistance	$I_W = [V(R_H) - V(R_L)]/ R_{TOTAL}$, V_{CC} = 5V		200	400	Ω
		$I_W = [V(R_H) - V(R_L)]/ R_{TOTAL}$, V_{CC} = 2.7V		400	1000	Ω
I_W	Wiper Current (Note 5)	See “Test Circuit” on page 7	-4.4		+4.4	mA
	Noise (Note 7)	Ref: 1kHz		-120		dBV
	Resolution			1		%
	Absolute Linearity (Note 1)	$V(R_H) = V_{CC}$, $V(R_L)$ = 0V	-1		+1	MI (Note 3)
	Relative Linearity (Note 2)	$V(R_H) = V_{CC}$, $V(R_L)$ = 0V	-0.2		+0.2	MI (Note 3)
	R_{TOTAL} Temperature Coefficient (Note 5)	$V(R_H) = V_{CC}$, $V(R_L)$ = 0V		±300		ppm/°C
	Ratiometric Temperature Coefficient (Notes 5, 6)			±20		ppm/°C
$C_H/C_L/C_W$ (Note 5)	Potentiometer Capacitances	See “Equivalent Circuit” on page 7		10/10/25		pF
V_{CC}	Supply Voltage	X9317	4.5		5.5	V
		X9317-2.7	2.7		5.5	V

DC Electrical Specifications

V_{CC} = 5V ±10%, T_A = Full Operating Temperature Range, unless otherwise stated.

SYMBOL	PARAMETER	TEST CONDITIONS	MIN (Note 8)	TYP (Note 4)	MAX (Note 8)	UNIT
I_{CC1}	V_{CC} Active Current (Increment)	$\overline{CS}$ = V_{IL}, U/$\overline{D}$ = V_{IL} or V_{IH} and $\overline{INC}$ = V_{IL}/V_{IH} @ min. t_{CYC} R_L, R_H, R_W not connected			80	µA
I_{CC2}	V_{CC} Active Current (Store) (non-volatile write)	$\overline{CS}$ = V_{IH}, U/$\overline{D}$ = V_{IL} or V_{IH} and $\overline{INC}$ = V_{IL} or V_{IH}. R_L, R_H, R_W not connected			400	µA
I_{SB}	Standby Supply Current	$\overline{CS} \geq V_{IH}$, U/$\overline{D}$ and $\overline{INC}$ = V_{IL} R_L, R_H, R_W not connected			5	µA
I_{LI}	$\overline{CS}$, $\overline{INC}$, U/$\overline{D}$ Input Leakage Current	$V_{IN} = V_{SS}$ to V_{CC}	-10		+10	µA
V_{IH}	$\overline{CS}$, $\overline{INC}$, U/$\overline{D}$ Input HIGH Voltage		V_{CC} x 0.7		V_{CC} + 0.5	V
V_{IL}	$\overline{CS}$, $\overline{INC}$, U/$\overline{D}$ Input LOW Voltage		-0.5		V_{CC} x 0.1	V
C_{IN} (Note 5)	$\overline{CS}$, $\overline{INC}$, U/$\overline{D}$ Input Capacitance	V_{CC} = 5V, $V_{IN} = V_{SS}$, T_A = +25°C, f = 1MHz		10		pF

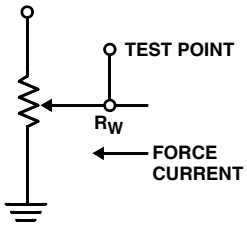
Endurance and Data Retention V_{CC} = 5V ±10%, T_A = Full Operating Temperature Range.

PARAMETER	MIN	UNIT
Minimum Endurance	100,000	Data changes per bit
Data Retention	100	Years

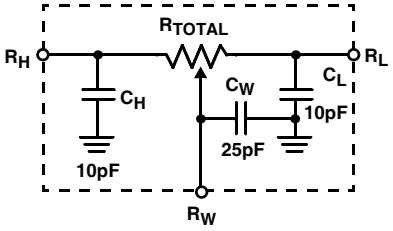
NOTES:

1. Absolute linearity is utilized to determine actual wiper voltage versus expected voltage = $[V(R_{W(n)(actual)})-V(R_{W(n)(expected)})]/MI$ $V(R_{W(n)(expected)}) = n(V(R_H)-V(R_L))/99 + V(R_L)$, with n from 0 to 99.
2. Relative linearity is a measure of the error in step size between taps = $[V(R_{W(n+1)})-(V(R_{W(n)}) - MI)]/MI$.
3. 1 MI = Minimum Increment = $[V(R_H)-V(R_L)]/99$.
4. Typical values are for T_A = +25°C and nominal supply voltage.
5. This parameter is not 100% tested.
6. Ratiometric temperature coefficient = $(V(R_W)_{T1(n)}-V(R_W)_{T2(n)})/[V(R_W)_{T1(n)}(T1-T2) \times 10^6]$, with T1 and T2 being 2 temperatures, and n from 0 to 99.
7. Measured with wiper at tap position 99, R_L grounded, using test circuit.
8. Parameters with MIN and/or MAX limits are 100% tested at +25°C, unless otherwise specified. Temperature limits established by characterization and are not production tested.

Test Circuit



Equivalent Circuit



AC Conditions of Test

Input pulse levels	0V to 3V
Input rise and fall times	10ns
Input reference levels	1.5V

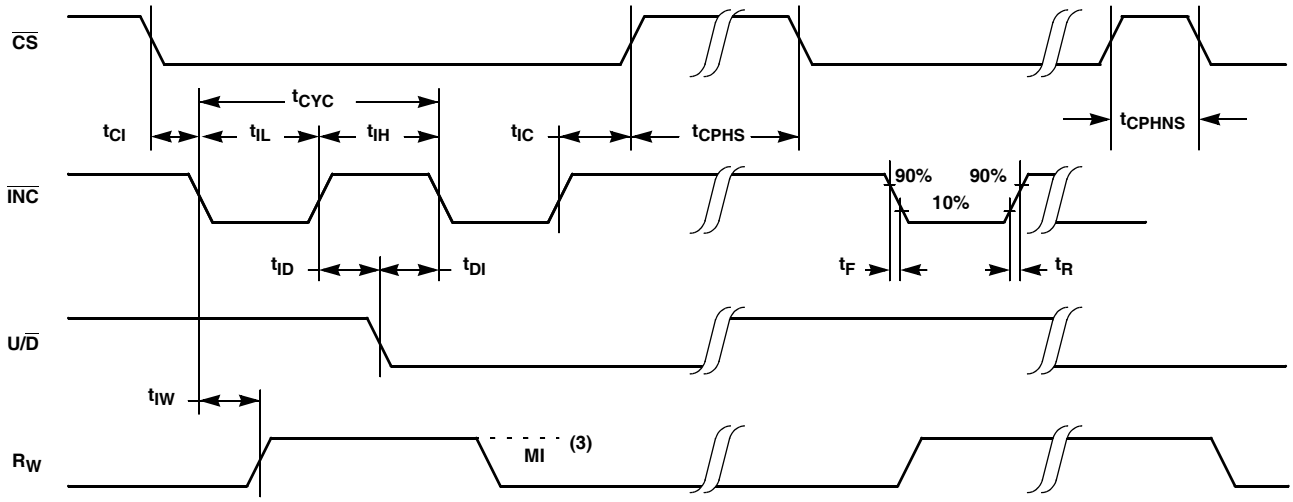
AC Electrical Specifications V_{CC} = 5V ±10%, T_A = Full Operating Temperature Range, unless otherwise stated.

SYMBOL	PARAMETER	MIN (Note 8)	TYP (Note 4)	MAX (Note 8)	UNIT
t_{CI}	$\overline{CS}$ to $\overline{INC}$ Setup	50			ns
t_{ID} (Note 5)	$\overline{INC}$ HIGH to U/$\overline{D}$ Change	100			ns
t_{DI} (Note 5)	U/$\overline{D}$ to $\overline{INC}$ Setup	1			µs
t_{IL}	$\overline{INC}$ LOW Period	960			ns
t_{IH}	$\overline{INC}$ HIGH Period	960			ns
t_{IC}	$\overline{INC}$ Inactive to $\overline{CS}$ Inactive	1			µs
t_{CPHS}	$\overline{CS}$ Deselect Time (STORE)	10			ms
t_{CPHNS} (Note 5)	$\overline{CS}$ Deselect Time (NO STORE)	100			ns
t_{IW}	$\overline{INC}$ to R_W Change		1	5	µs
t_{CYC}	$\overline{INC}$ Cycle Time	2			µs
t_R, t_F (Note 5)	$\overline{INC}$ Input Rise and Fall Time			500	µs
t_{PU} (Note 5)	Power-up to Wiper Stable			5	µs
t_R V_{CC} (Note 5)	V_{CC} Power-up Rate	0.2		50	V/ms
t_{WR}	Store Cycle		5	10	ms

Power-up and Down Requirements

The recommended power-up sequence is to apply V_{CC}/V_{SS} first, then the potentiometer voltages. During power-up, the data sheet parameters for the DCP do not fully apply until 1ms after V_{CC} reaches its final value. The V_{CC} ramp spec is always in effect. In order to prevent unwanted tap position changes, or an inadvertent store, bring the $\overline{CS}$ and $\overline{INC}$ high before or concurrently with the V_{CC} pin on power-up.

AC Timing



Typical Performance Characteristic

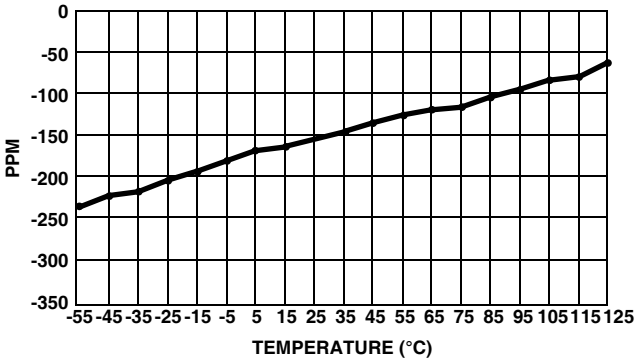


FIGURE 1. TYPICAL TOTAL RESISTANCE TEMPERATURE COEFFICIENT

Pin Descriptions

R_H AND R_L

The high (R_H) and low (R_L) terminals of the X9317 are equivalent to the fixed terminals of a mechanical potentiometer. The terminology of R_L and R_H references the relative position of the terminal in relation to wiper movement direction selected by the U/$\overline{D}$ input and not the voltage potential on the terminal.

R_W

R_W is the wiper terminal and is equivalent to the movable terminal of a mechanical potentiometer. The position of the wiper within the array is determined by the control inputs. The wiper terminal series resistance is typically 200Ω.

UP/DOWN (U/$\overline{D}$)

The U/$\overline{D}$ input controls the direction of the wiper movement and whether the counter is incremented or decremented.

INCREMENT ($\overline{INC}$)

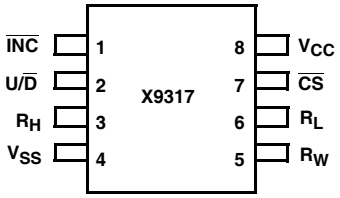
The $\overline{INC}$ input is negative-edge triggered. Toggling $\overline{INC}$ will move the wiper and either increment or decrement the counter in the direction indicated by the logic level on the U/$\overline{D}$ input.

CHIP SELECT ($\overline{CS}$)

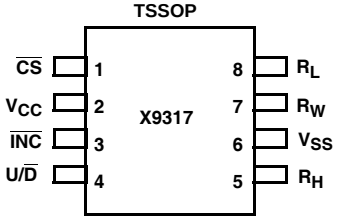
The device is selected when the $\overline{CS}$ input is LOW. The current counter value is stored in nonvolatile memory when $\overline{CS}$ is returned HIGH while the $\overline{INC}$ input is also HIGH. After the store operation is complete, the X9317 will be placed in the low power standby mode until the device is selected once again.

Pin Configuration

DIP/SOIC/MSOP



TSSOP



Pin Names

SYMBOL	DESCRIPTION
R_H	High terminal
R_W	Wiper terminal
R_L	Low terminal
V_{SS}	Ground
V_{CC}	Supply voltage
U/$\overline{D}$	Up/Down control input
$\overline{INC}$	Increment control input
$\overline{CS}$	Chip select control input

Principles of Operation

There are three sections of the X9317: the control section, the nonvolatile memory, and the resistor array. The control section operates just like an up/down counter. The output of this counter is decoded to turn on a single electronic switch connecting a point on the resistor array to the wiper output. The contents of the counter can be stored in nonvolatile memory and retained for future use. The resistor array is comprised of 99 individual resistors connected in series. Electronic switches at either end of the array and between each resistor provide an electrical connection to the wiper pin, R_W.

The wiper acts like its mechanical equivalent and does not move beyond the first or last position. That is, the counter does not wrap around when clocked to either extreme.

The electronic switches on the device operate in a “make before break” mode when the wiper changes tap positions. If the wiper is moved several positions, multiple taps are connected to the wiper for t_{IW} ($\overline{INC}$ to V_W change). The R_{TOTAL} value for the device can temporarily be reduced by a significant amount if the wiper is moved several positions.

When the device is powered-down, the last wiper position stored will be maintained in the nonvolatile memory. When power is restored, the contents of the memory are recalled and the wiper is set to the value last stored.

Instructions and Programming

The $\overline{INC}$, U/$\overline{D}$ and $\overline{CS}$ inputs control the movement of the wiper along the resistor array. With $\overline{CS}$ set LOW, the device is selected and enabled to respond to the U/$\overline{D}$ and $\overline{INC}$ inputs. HIGH to LOW transitions on $\overline{INC}$ will increment or decrement (depending on the state of the U/$\overline{D}$ input) a 7-bit counter. The output of this counter is decoded to select one of one hundred wiper positions along the resistive array.

The value of the counter is stored in nonvolatile memory whenever $\overline{CS}$ transitions HIGH while the $\overline{INC}$ input is also HIGH.

The system may select the X9317, move the wiper and deselect the device without having to store the latest wiper position in nonvolatile memory. After the wiper movement is performed as previously described and once the new position is reached, the system must keep $\overline{INC}$ LOW while taking $\overline{CS}$ HIGH. The new wiper position will be maintained until changed by the system or until a power-up/down cycle recalls the previously stored data.

This procedure allows the system to always power-up to a preset value stored in nonvolatile memory; then during system operation minor adjustments could be made. The adjustments might be based on user preference, system parameter changes due to temperature drift, etc.

The state of U/$\overline{D}$ may be changed while $\overline{CS}$ remains LOW. This allows the host system to enable the device and then move the wiper up and down until the proper trim is attained.

Mode Selection

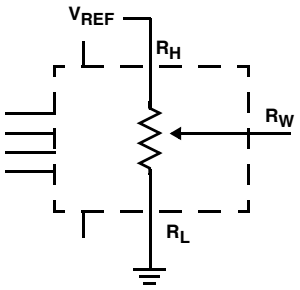
$\overline{CS}$	$\overline{INC}$	U/$\overline{D}$	MODE
L		H	Wiper up
L		L	Wiper down
	H	X	Store wiper position to nonvolatile memory
H	X	X	Standby
	L	X	No store, return to standby
	L	H	Wiper Up (not recommended)
	L	L	Wiper Down (not recommended)

Applications Information

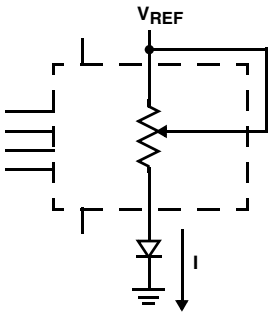
Electronic digitally controlled (XDCP) potentiometers provide three powerful application advantages:

1. the variability and reliability of a solid-state potentiometer,
2. the flexibility of computer-based digital controls, and
3. the retentivity of nonvolatile memory used for the storage of multiple potentiometer settings or data.

Basic Configurations of Electronic Potentiometers



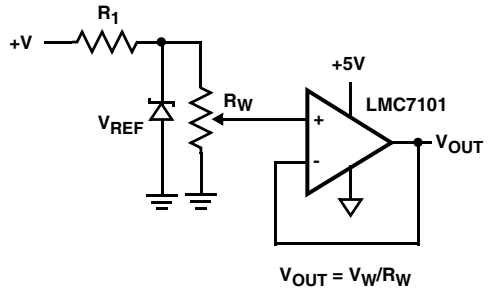
THREE TERMINAL POTENTIOMETER;
VARIABLE VOLTAGE DIVIDER



TWO TERMINAL VARIABLE RESISTOR;
VARIABLE CURRENT

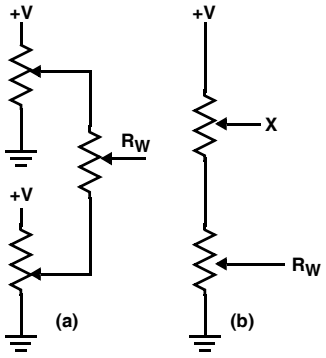
Basic Circuits

BUFFERED REFERENCE VOLTAGE

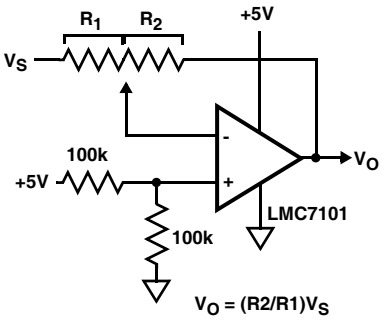


$V_{OUT} = V_W/R_W$

CASCADING TECHNIQUES

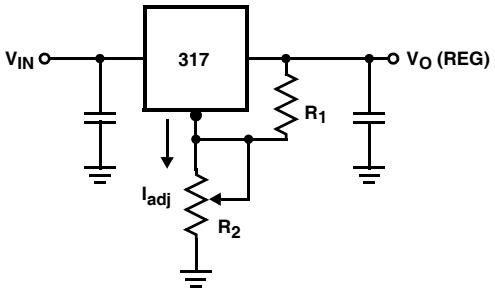


SINGLE SUPPLY INVERTING AMPLIFIER



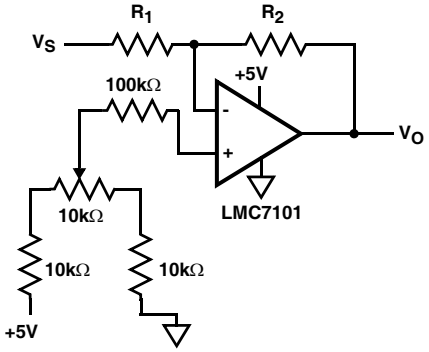
$V_O = (R2/R1)V_S$

VOLTAGE REGULATOR

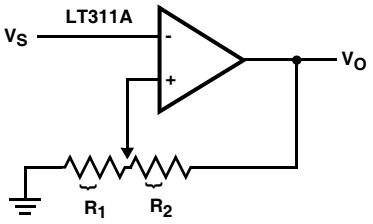


V_O (REG) = 1.25V $(1+R_2/R_1)+I_{adj}$ R_2

OFFSET VOLTAGE ADJUSTMENT

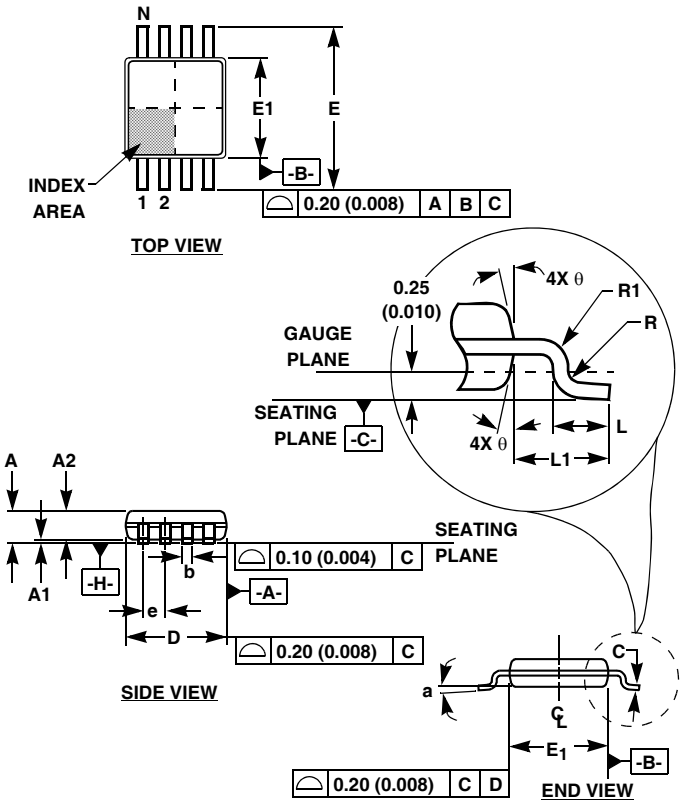


COMPARATOR WITH HYSTERESIS



$V_{UL} = \{R_1/(R_1+R_2)\}$ V_O(max)
$V_{LL} = \{R_1/(R_1+R_2)\}$ V_O(min)

Mini Small Outline Plastic Packages (MSOP)



NOTES:

1. These package dimensions are within allowable dimensions of JEDEC MO-187BA.
2. Dimensioning and tolerancing per ANSI Y14.5M-1994.
3. Dimension “D” does not include mold flash, protrusions or gate burrs and are measured at Datum Plane. Mold flash, protrusion and gate burrs shall not exceed 0.15mm (0.006 inch) per side.
4. Dimension “E1” does not include interlead flash or protrusions and are measured at Datum Plane. [- H -] Interlead flash and protrusions shall not exceed 0.15mm (0.006 inch) per side.
5. Formed leads shall be planar with respect to one another within 0.10mm (0.004) at seating Plane.
6. “L” is the length of terminal for soldering to a substrate.
7. “N” is the number of terminal positions.
8. Terminal numbers are shown for reference only.
9. Dimension “b” does not include dambar protrusion. Allowable dambar protrusion shall be 0.08mm (0.003 inch) total in excess of “b” dimension at maximum material condition. Minimum space between protrusion and adjacent lead is 0.07mm (0.0027 inch).
10. Datums [-A -] and [- B -] to be determined at Datum plane [- H -].
11. Controlling dimension: MILLIMETER. Converted inch dimensions are for reference only.

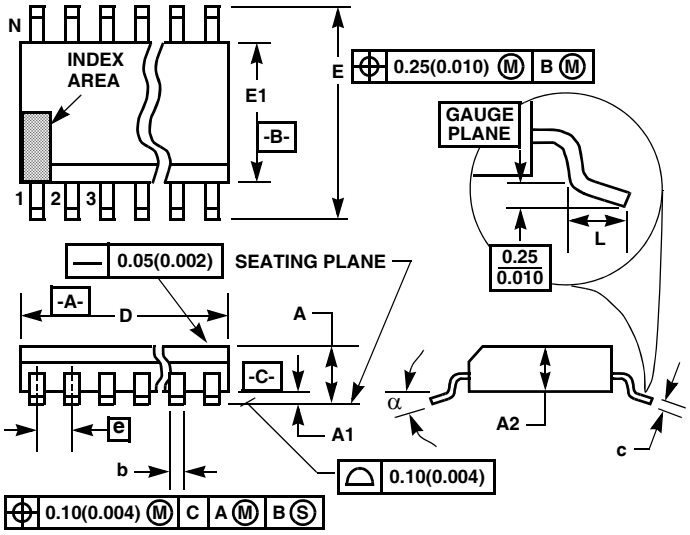
M8.118 (JEDEC MO-187AA)

8 LEAD MINI SMALL OUTLINE PLASTIC PACKAGE

SYMBOL	INCHES		MILLIMETERS		NOTES
	MIN	MAX	MIN	MAX	
A	0.037	0.043	0.94	1.10	-
A1	0.002	0.006	0.05	0.15	-
A2	0.030	0.037	0.75	0.95	-
b	0.010	0.014	0.25	0.36	9
c	0.004	0.008	0.09	0.20	-
D	0.116	0.120	2.95	3.05	3
E1	0.116	0.120	2.95	3.05	4
e	0.026 BSC		0.65 BSC		-
E	0.187	0.199	4.75	5.05	-
L	0.016	0.028	0.40	0.70	6
L1	0.037 REF		0.95 REF		-
N	8		8		7
R	0.003	-	0.07	-	-
R1	0.003	-	0.07	-	-
0	5^o	15^o	5^o	15^o	-
α	0^o	6^o	0^o	6^o	-

Rev. 2 01/03

Thin Shrink Small Outline Plastic Packages (TSSOP)



NOTES:

1. These package dimensions are within allowable dimensions of JEDEC MO-153-AC, Issue E.
2. Dimensioning and tolerancing per ANSI Y14.5M-1982.
3. Dimension “D” does not include mold flash, protrusions or gate burrs. Mold flash, protrusion and gate burrs shall not exceed 0.15mm (0.006 inch) per side.
4. Dimension “E1” does not include interlead flash or protrusions. Interlead flash and protrusions shall not exceed 0.15mm (0.006 inch) per side.
5. The chamfer on the body is optional. If it is not present, a visual index feature must be located within the crosshatched area.
6. “L” is the length of terminal for soldering to a substrate.
7. “N” is the number of terminal positions.
8. Terminal numbers are shown for reference only.
9. Dimension “b” does not include dambar protrusion. Allowable dambar protrusion shall be 0.08mm (0.003 inch) total in excess of “b” dimension at maximum material condition. Minimum space between protrusion and adjacent lead is 0.07mm (0.0027 inch).
10. Controlling dimension: MILLIMETER. Converted inch dimensions are not necessarily exact. (Angles in degrees)

M8.173

8 LEAD THIN SHRINK NARROW BODY SMALL OUTLINE PLASTIC PACKAGE

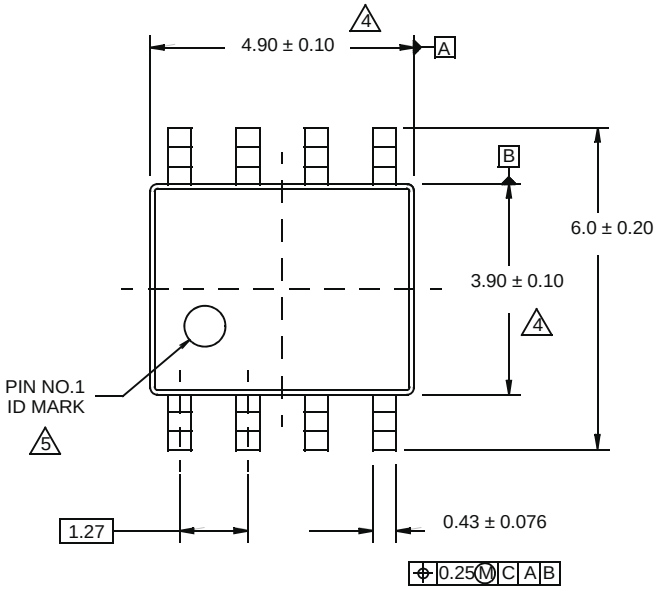
SYMBOL	INCHES		MILLIMETERS		NOTES
	MIN	MAX	MIN	MAX	
A	-	0.047	-	1.20	-
A1	0.002	0.006	0.05	0.15	-
A2	0.031	0.051	0.80	1.05	-
b	0.0075	0.0118	0.19	0.30	9
c	0.0035	0.0079	0.09	0.20	-
D	0.116	0.120	2.95	3.05	3
E1	0.169	0.177	4.30	4.50	4
e	0.026 BSC		0.65 BSC		-
E	0.246	0.256	6.25	6.50	-
L	0.0177	0.0295	0.45	0.75	6
N	8		8		7
α	0^o	8^o	0^o	8^o	-

Rev. 1 12/00

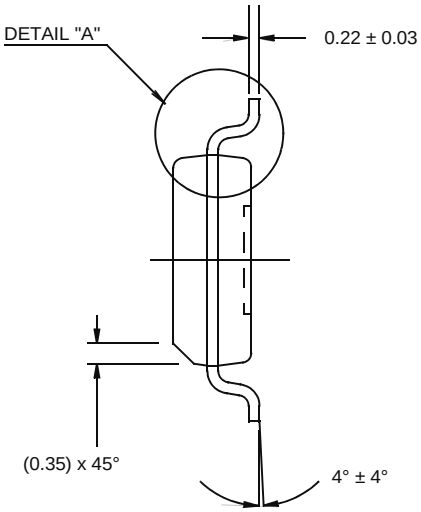
Package Outline Drawing

M8.15E

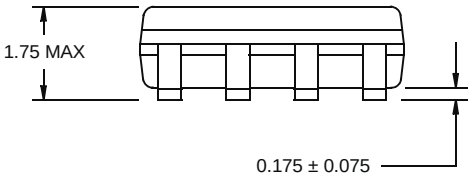
8 LEAD NARROW BODY SMALL OUTLINE PLASTIC PACKAGE
Rev 0, 08/09



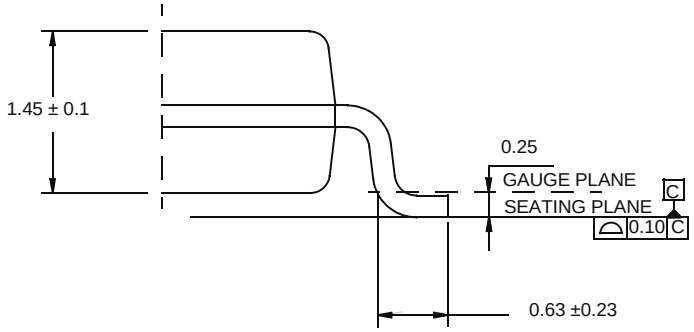
TOP VIEW



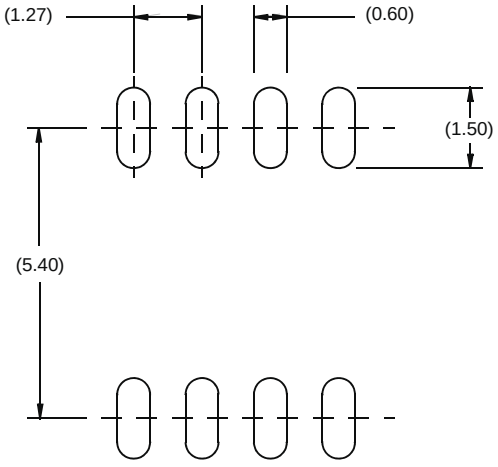
SIDE VIEW “B”



SIDE VIEW “A”



DETAIL "A"

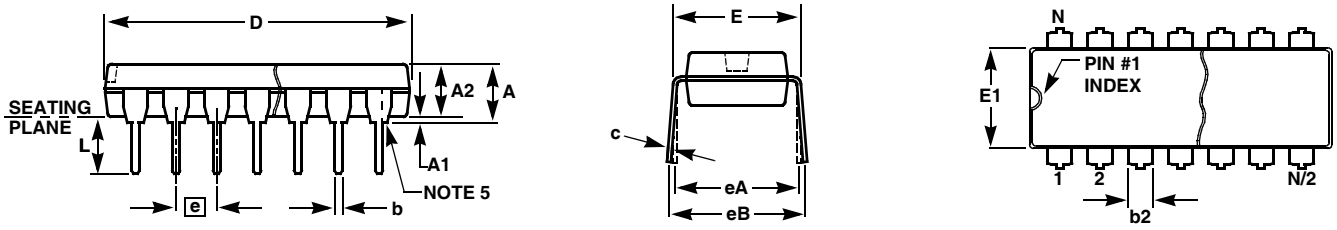


TYPICAL RECOMMENDED LAND PATTERN

NOTES:

1. Dimensions are in millimeters.
   Dimensions in ( ) for Reference Only.
2. Dimensioning and tolerancing conform to AMSE Y14.5m-1994.
3. Unless otherwise specified, tolerance : Decimal ± 0.05
4. Dimension does not include interlead flash or protrusions.
   Interlead flash or protrusions shall not exceed 0.25mm per side.
5. The pin #1 identifier may be either a mold or mark feature.
6. Reference to JEDEC MS-012.

Plastic Dual-In-Line Packages (PDIP)



MDP0031

PLASTIC DUAL-IN-LINE PACKAGE

SYMBOL	INCHES					TOLERANCE	NOTES
	PDIP8	PDIP14	PDIP16	PDIP18	PDIP20		
A	0.210	0.210	0.210	0.210	0.210	MAX	
A1	0.015	0.015	0.015	0.015	0.015	MIN	
A2	0.130	0.130	0.130	0.130	0.130	±0.005	
b	0.018	0.018	0.018	0.018	0.018	±0.002	
b2	0.060	0.060	0.060	0.060	0.060	+0.010/-0.015	
c	0.010	0.010	0.010	0.010	0.010	+0.004/-0.002	
D	0.375	0.750	0.750	0.890	1.020	±0.010	1
E	0.310	0.310	0.310	0.310	0.310	+0.015/-0.010	
E1	0.250	0.250	0.250	0.250	0.250	±0.005	2
e	0.100	0.100	0.100	0.100	0.100	Basic	
eA	0.300	0.300	0.300	0.300	0.300	Basic	
eB	0.345	0.345	0.345	0.345	0.345	±0.025	
L	0.125	0.125	0.125	0.125	0.125	±0.010	
N	8	14	16	18	20	Reference	

Rev. C 2/07

NOTES:

1. Plastic or metal protrusions of 0.010” maximum per side are not included.
2. Plastic interlead protrusions of 0.010” maximum per side are not included.
3. Dimensions E and eA are measured with the leads constrained perpendicular to the seating plane.
4. Dimension eB is measured with the lead tips unconstrained.
5. 8 and 16 lead packages have half end-leads as shown.

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Intersil Corporation’s quality certifications can be viewed at www.intersil.com/design/quality

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