PRELIMINARY

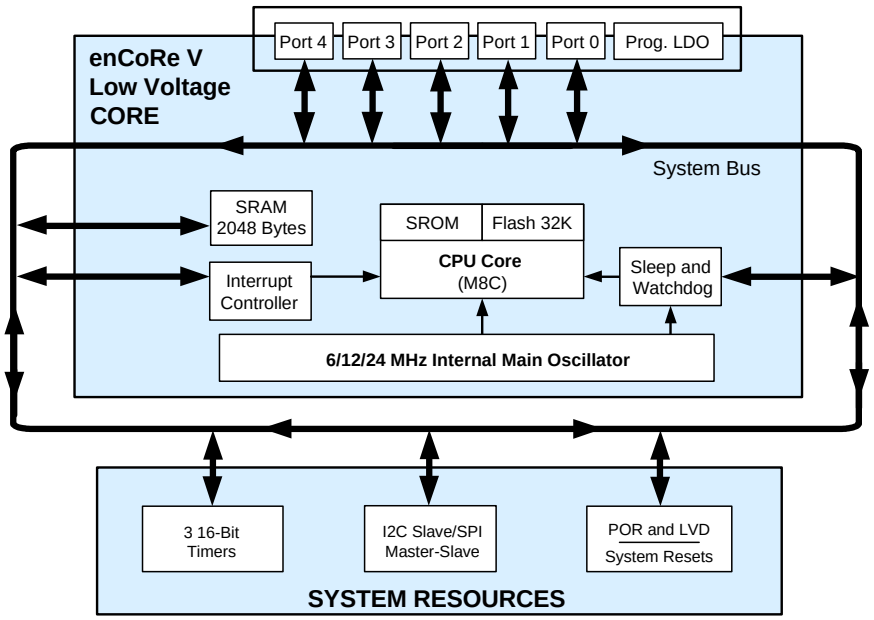
CY7C60445, CY7C6045x

enCoRe™ V Low Voltage Microcontroller

Features

- Powerful Harvard Architecture Processor
  - M8C Processor speeds running up to 24 MHz
  - Low power at high processing speeds
  - Interrupt controller
  - 1.71V to 3.6V operating voltage
  - Temperature range: 0°C to 70°C
- Flexible On-Chip Memory
  - Up to 32K Flash program storage 50,000 Erase/write cycles
  - Up to 2048 bytes SRAM data storage
  - Flexible protection modes
  - In-System Serial Programming (ISSP)
- Complete Development Tools
  - Free development tool (PSoC Designer™)
  - Full-featured, in-circuit emulator and programmer
  - Full-speed emulation
  - Complex breakpoint structure
  - 128K Trace memory
- Precision, Programmable Clocking
  - Crystal-less oscillator with support for an external crystal or resonator
  - Internal ±5.0% 6/12/24 MHz main oscillator
  - Internal Low speed oscillator at 32 kHz for watchdog and sleep.The frequency range is 19-50 kHz with a 32 kHz typical value.
- Programmable Pin Configurations
  - 25 mA Sink current on all GPIO
  - Pull up, high Z, open drain, CMOS drive modes on all GPIO
  - Configurable inputs on all GPIO
  - Low-dropout voltage regulator for Port1 pins. Programmable to output 3.0, 2.5 or 1.8V at the I/O pins.
  - Selectable, regulated digital IO on Port 1
    - Configurable Input Threshold for Port 1
    - 3.0V, 20 mA Total Port 1 source current
    - Hot-Swappable
  - 5 mA Strong drive mode on Ports 0 and 1
- Additional System Resources
  - Configurable communication speeds
  - I^2C™ Slave
    - Selectable to 50 kHz, 100 kHz, or 400 kHz
    - Implementation requires no clock stretching
    - Implementation during sleep modes with less than 100 mA
    - Hardware address detection
  - SPI master and SPI slave
    - Configurable between 46.9 kHz–3 MHz
  - Three 16-bit timers
  - 10-bit ADC for monitoring battery voltage or other signals
  - Watchdog and sleep timers
  - Integrated supervisory circuit

enCoRe V LV - Block Diagram



Functional Overview

The enCoRe V LV family of devices are designed to replace multiple traditional low voltage microcontroller system components with one, low cost single-chip programmable component. Communication peripherals (I2C/SPI), a fast CPU, Flash program memory, SRAM data memory, and configurable IO are included in a range of convenient pinouts.

The architecture for this device family, as illustrated (enCoRe V LV - Block Diagram), is comprised of two main areas: the CPU core and the system resources. Depending on the enCoRe V LV package, up to 36 general purpose IO (GPIO) are also included.

Enhancements over the Cypress' legacy low voltage microcontrollers include faster CPU at lower voltage operation, lower current consumption, twice the RAM and Flash, hot-swapable IOs, I2C hardware address recognition, new very low current sleep mode, and new package options.

The enCoRe V LV Core

The enCoRe V LV Core is a powerful engine that supports a rich instruction set. It encompasses SRAM for data storage, an interrupt controller, sleep and watchdog timers, and IMO (internal main oscillator) and ILO (internal low speed oscillator). The CPU core, called the M8C, is a powerful processor with speeds up to 24 MHz. The M8C is a four-MIPS, 8-bit Harvard architecture microprocessor.

System Resources provide additional capability, such as a configurable I2C slave/SPI master-slave communication interface and various system resets supported by the M8C.

Additional System Resources

System Resources, some of which have been previously listed, provide additional capability useful to complete systems. Additional resources include low voltage detection and power on reset. Brief statements describing the merits of each system resource are presented below.

- 10-bit on-chip ADC shared between System Performance manager (used to calculate parameters based on temperature for flash write operations) and the user.
- The I2C slave/SPI master-slave module provides 50/100/400 kHz communication over two wires. SPI communication over 3 or 4 wires runs at speeds of 46.9 kHz to 3 MHz (lower for a slower system clock).
  - In I2C Slave mode the hardware address recognition feature reduces the already low power consumption by eliminating the need for CPU intervention until a packet addressed to the target device has been received.
- Low Voltage Detection (LVD) interrupts can signal the application of falling voltage levels, while the advanced POR (Power On Reset) circuit eliminates the need for a system supervisor.
- The 5V maximum input, 1.8/2.5/3V-selectable output, low-dropout regulator (LDO) provides regulation for IOs. A register-controlled bypass mode allows the user to disable the LDO.
- Standard Cypress PSoC IDE tools are available for debugging the enCoRe V LV family of parts.

Getting Started

The quickest path to understanding the enCoRe V LV silicon is by reading this data sheet and using the PSoC Designer Integrated Development Environment (IDE). This data sheet is an overview of the enCoRe V LV integrated circuit and presents specific pin, register, and electrical specifications.

For up-to-date Ordering, Packaging, and Electrical Specification information, reference the latest enCoRe V LV device data sheet on the web at http://www.cypress.com.

Development Kits

Development Kits are available from the following distributors: Digi-Key, Avnet, Arrow, and Future. The Cypress Online Store contains development kits, **C** compilers, and all accessories for PSoC development. Go to the Cypress Online Store web site at http://www.cypress.com, click the Online Store shopping cart icon at the bottom of the web page, and click *USB (Universal Serial Bus)* to view a current list of available items.

Technical Training

Free enCoRe V LV microcontrollers technical training is available for beginners and is taught by a marketing or application engineer over the phone. Low-Voltage microcontroller training classes cover designing, debugging, analog, as well as application-specific classes covering topics such as PSoC, USB and the LIN bus. Go to http://www.cypress.com, click on Design Support located on the left side of the web page, and select Technical Training for more details.

Consultants

Certified Cypress consultants offer everything from technical assistance to completed microcontroller designs. To contact or become a Cypress PSoC/USB/microcontroller consultant go to http://www.cypress.com, click on Design Support located on the left side of the web page, and select CYPros Consultants.

Technical Support

Cypress application engineers take pride in fast and accurate response. They can be reached with a 4-hour guaranteed response at http://www.cypress.com/support/login.cfm.

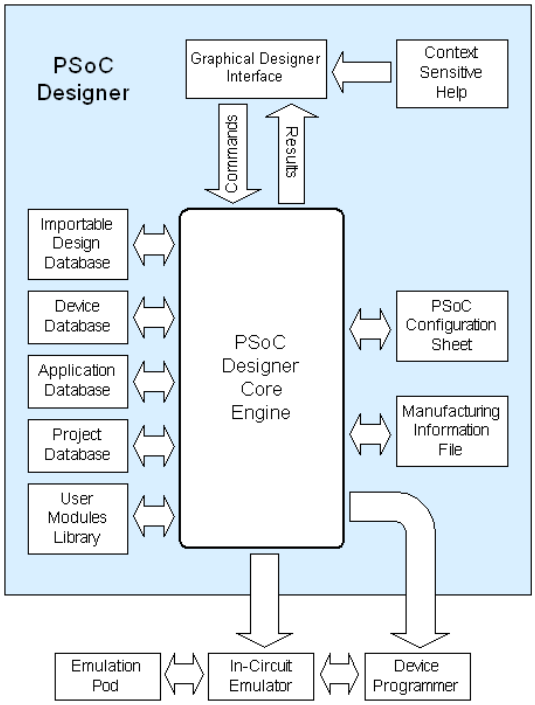
Development Tools

PSoC Designer is a Microsoft® Windows-based, integrated development environment for the Programmable System-on-Chip (PSoC) devices. The PSoC Designer IDE and application runs on Windows NT 4.0, Windows 2000, Windows Millennium (Me), or Windows XP. (Reference the PSoC Designer Functional Flow diagram below.)

PSoC Designer helps the customer to select an operating configuration for the microcontroller, write application code that uses its resources, and debug the application. This system provides design database management by project, an integrated debugger with In-Circuit Emulator, in-system programming support, and the CYASM macro assembler for the CPUs.

PSoC Designer also supports a high-level C language compiler developed specifically for the devices in the family.

Figure 1. PSoC Designer Subsystems



PSoC Designer Software Subsystems

Device Editor

The device editor subsystem allows the user to select different onboard analog and digital components called user modules using the enCoRe V LV device blocks. Examples of user modules are timers, 10-bit ADC, SPI/I2C etc.

The device editor also supports easy development of multiple configurations and dynamic reconfiguration. Dynamic reconfiguration allows for changing configurations at run time.

PSoC Designer sets up power-on initialization tables for selected enCoRe V LV block configurations and creates source code for an application framework. The framework contains software to operate the selected components and, if the project uses more than one operating configuration, contains routines to switch between different sets of enCoRe V LV block configurations at run time. PSoC Designer can print out a configuration sheet for a given project configuration for use during application programming in conjunction with the Device Data Sheet. Once the framework is generated, the user can add application-specific code to flesh out the framework. It's also possible to change the selected components and regenerate the framework.

Application Editor

In the Application Editor you can edit your C language and Assembly language source code. You can also assemble, compile, link, and build.

Assembler. The macro assembler allows the assembly code to be merged seamlessly with C code. The link libraries automatically use absolute addressing or can be compiled in relative mode, and linked with other software modules to get absolute addressing.

C Language Compiler. A C language compiler is available that supports the enCoRe V LV family of devices. Even if you have never worked in the C language before, the product quickly allows you to create complete C programs for the enCoRe V LV family devices.

The embedded, optimizing C compiler provides all the features of C tailored to the enCoRe V LV architecture. It comes complete with embedded libraries providing port and bus operations, standard keypad and display support, and extended math functionality.

Debugger

The PSoC Designer Debugger subsystem provides hardware in-circuit emulation, allowing the designer to test the program in a physical system while providing an internal view of the PSoC device. Debugger commands allow the designer to read the program and read and write data memory, read and write IO registers, read and write CPU registers, set and clear breakpoints, and provide program run, halt, and step control. The debugger also allows the designer to create a trace buffer of registers and memory locations of interest.

Online Help System

The online help system displays online, context-sensitive help for the user. Designed for procedural and quick reference, each functional subsystem has its own context-sensitive help. This system also provides tutorials and links to FAQs and an Online Support Forum to aid the designer in getting started.

Hardware Tools

In-Circuit Emulator

A low cost, high functionality ICE (In-Circuit Emulator) is available for development support. This hardware has the capability to program single devices.

The emulator consists of a base unit that connects to the PC by way of a USB port. The base unit is universal and operates with most Cypress USB devices and all PSoC devices. Emulation pods for each device family are available separately. The emulation pod takes the place of the enCoRe V LV in the target board and performs full speed (24 MHz) operation.

Designing with User Modules

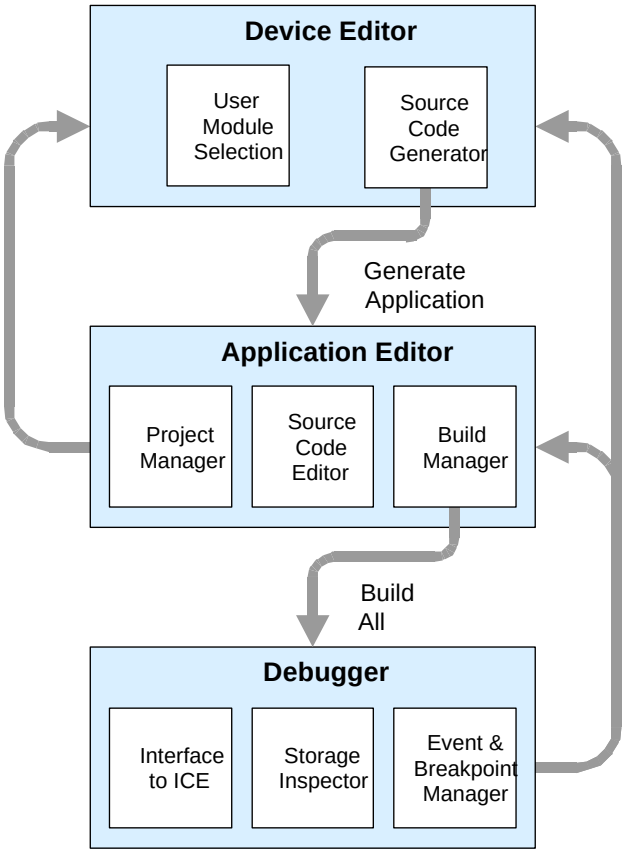
To speed the development process, the PSoC Designer Integrated Development Environment (IDE) provides a feature where the resources of the part can be selected as user modules. For example, the timers, I2C, SPI resources are available as user modules. User modules make selecting and implementing peripheral devices simple and easy.

Each user module establishes the basic register settings that implement the selected function. It also provides parameters that allow you to tailor its precise configuration to your particular application. User modules also provide tested software to cut your development time. The user module application programming interface (API) provides high-level functions to control and respond to hardware events at run time. The API also provides optional interrupt service routines that you can adapt as needed.

The API functions are documented in user module data sheets that are viewed directly in the PSoC Designer IDE. These data sheets explain the internal operation of the user module and provide performance specifications. Each data sheet describes the use of each user module parameter and documents the setting of each register controlled by the user module.

The development process starts when you open a new project and bring up the Device Editor, a graphical user interface (GUI) for configuring the hardware. You pick and place the user modules you need for your project. The tool automatically builds signal chains by connecting user modules to the default IO pins or as required. At this stage, you also configure the clock source connections and enter parameter values directly or by selecting values from drop-down menus. When you are ready to test the hardware configuration or move on to developing code for the project, you perform the “Generate Application” step. This causes PSoC Designer to generate source code that automatically configures the device to your specification and provides the high-level user module API functions.

Figure 2. User Module and Source Code Development Flows



The next step is to write your main program, and any sub-routines using PSoC Designer’s Application Editor subsystem. The Application Editor includes a Project Manager that allows you to open the project source code files (including all generated code files) from a hierarchal view. The source code editor provides syntax coloring and advanced edit features for both C and assembly language. File search capabilities include simple string searches and recursive “grep-style” patterns. A single mouse click invokes the Build Manager. It employs a professional-strength “makefile” system to automatically analyze all file dependencies and run the compiler and assembler as necessary. Project-level options control optimization strategies used by the compiler and linker. Syntax errors are displayed in a console window. Double clicking the error message takes you directly to the offending line of source code. When all is correct, the linker builds a HEX file image suitable for programming.

The last step in the development process takes place inside the PSoC Designer’s Debugger subsystem. The Debugger downloads the HEX image to the In-Circuit Emulator (ICE) where it runs at full speed. Debugger capabilities rival those of systems costing many times more. In addition to traditional single-step, run-to-breakpoint and watch-variable features, the Debugger provides a large trace buffer and allows you define complex breakpoint events that include monitoring address and data bus values, memory locations and external signals.

Document Conventions

Acronyms Used

The following table lists the acronyms that are used in this document.

Acronym	Description
API	application programming interface
CPU	central processing unit
GPIO	general purpose IO
GUI	graphical user interface
ICE	in-circuit emulator
ILO	internal low speed oscillator
IMO	internal main oscillator
IO	input/output
LSb	least-significant bit
LVD	low voltage detect
MSb	most-significant bit
POR	power on reset
PPOR	precision power on reset
PSoC®	Programmable System-on-Chip™
SLIMO	slow IMO
SRAM	static random access memory

Units of Measure

A units of measure table is located in the Electrical Specifications section. Table 4 on page 14 lists all the abbreviations used to measure the enCoRe V LV devices.

Numeric Naming

Hexidecimal numbers are represented with all letters in uppercase with an appended lowercase ‘h’ (for example, ‘14h’ or ‘3Ah’). Hexidecimal numbers may also be represented by a ‘0x’ prefix, the C coding convention. Binary numbers have an appended lowercase ‘b’ (e.g., 01010100b’ or ‘01000011b’). Numbers not indicated by an ‘h’, ‘b’, or 0x are decimal.

Pin Configuration

32-Pin Part Pinout

Figure 3. CY7C60445 32-Pin enCoRe V LV Device

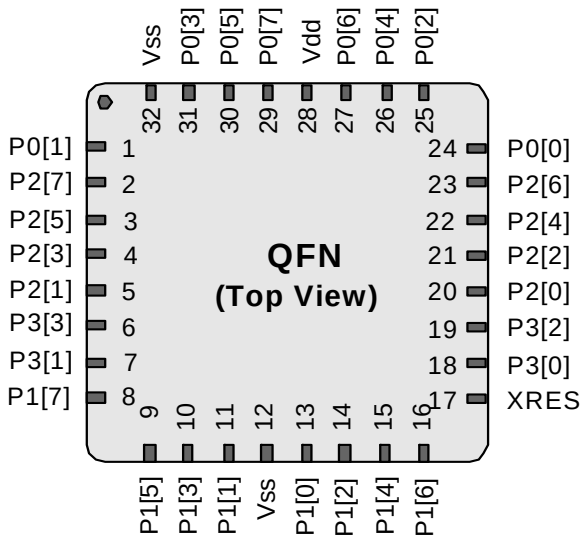


Table 1. 32-Pin Part Pinout (QFN)

Pin No.	Type	Name	Description
1	IOH	P0[1]	Digital IO
2	IO	P2[7]	Digital IO
3	IO	P2[5]	Digital IO, Crystal Out (Xout)
4	IO	P2[3]	Digital IO, Crystal In (Xin)
5	IO	P2[1]	Digital IO
6	IO	P3[3]	Digital IO
7	IO	P3[1]	Digital IO
8	IOHR	P1[7]	Digital IO, I2C SCL, SPI SS
9	IOHR	P1[5]	Digital IO, I2C SDA, SPI MISO
10	IOHR	P1[3]	Digital IO, SPI CLK
11	IOHR	P1[1](1)	Digital IO, ISSP CLK, I2C SCL, SPI MOSI
12	Power	Vss	Ground connection
13	IOHR	P1[0](1)	Digital IO, ISSP DATA, I2C SDA, SPI CLK
14	IOHR	P1[2]	Digital IO

Note
1. These are the in-system serial programming (ISSP) pins, that are not High Z at power on reset (POR).

Table 1. 32-Pin Part Pinout (QFN) (continued)

Pin No.	Type	Name	Description
15	IOHR	P1[4]	Digital IO, optional external clock input (EXTCLK)
16	IOHR	P1[6]	Digital IO
17	Reset Input	XRES	Active high external reset with internal pull down
18	IO	P3[0]	Digital IO
19	IO	P3[2]	Digital IO
20	IO	P2[0]	Digital IO
21	IO	P2[2]	Digital IO
22	IO	P2[4]	Digital IO
23	IO	P2[6]	Digital IO
24	IOH	P0[0]	Digital IO
25	IOH	P0[2]	Digital IO
26	IOH	P0[4]	Digital IO
27	IOH	P0[6]	Digital IO
28	Power	Vdd	Supply voltage
29	IOH	P0[7]	Digital IO
30	IOH	P0[5]	Digital IO
31	IOH	P0[3]	Digital IO
32	Power	Vss	Ground connection
CP	Power	Vss	Center pad must be connected to ground

LEGEND I = Input, O = Output, OH = 5 mA High Output Drive, R = Regulated Output.

48-Pin Part Pinout

Figure 4. CY7C60455/CY7C60456 48-Pin enCoRe V LV Device

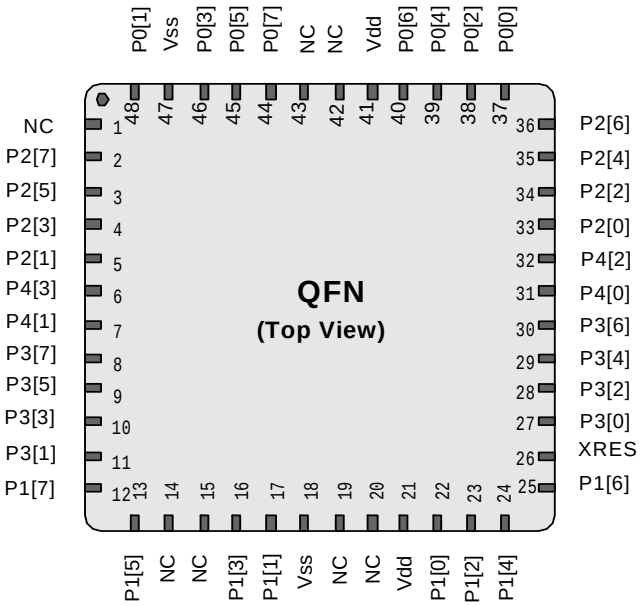


Table 2. 48-Pin Part Pinout (QFN)

Pin No.	Type	Name	Description
1	NC	NC	No connection
2	IO	P2[7]	Digital I/O
3	IO	P2[5]	Digital I/O, Crystal Out (Xout)
4	IO	P2[3]	Digital I/O, Crystal In (Xin)
5	IO	P2[1]	Digital I/O
6	IO	P4[3]	Digital I/O
7	IO	P4[1]	Digital I/O
8	IO	P3[7]	Digital I/O
9	IO	P3[5]	Digital I/O
10	IO	P3[3]	Digital I/O
11	IO	P3[1]	Digital I/O
12	IOHR	P1[7]	Digital I/O, I2C SCL, SPI SS
13	IOHR	P1[5]	Digital I/O, I2C SDA, SPI MISO
14	NC	NC	No connection
15	NC	NC	No connection

Table 2. 48-Pin Part Pinout (QFN) (continued)

Pin No.	Type	Name	Description
16	IOHR	P1[3]	Digital I/O, SPI CLK
17	IOHR	P1[1][2]	Digital I/O, ISSP CLK, I2C SCL, SPI MOSI
18	Power	Vss	Supply ground
19	NC	NC	No connection
20	NC	NC	No connection
21	Power	Vdd	Supply voltage
22	IOHR	P1[0][2]	Digital I/O, ISSP DATA, I2C SDA, SPI CLK
23	IOHR	P1[2]	Digital I/O
24	IOHR	P1[4]	Digital I/O, optional external clock input (EXTCLK)
25	IOHR	P1[6]	Digital I/O
26	XRES	Ext Reset	Active high external reset with internal pull down
27	IO	P3[0]	Digital I/O
28	IO	P3[2]	Digital I/O
29	IO	P3[4]	Digital I/O
30	IO	P3[6]	Digital I/O
31	IO	P4[0]	Digital I/O
32	IO	P4[2]	Digital I/O
33	IO	P2[0]	Digital I/O
34	IO	P2[2]	Digital I/O
35	IO	P2[4]	Digital I/O
36	IO	P2[6]	Digital I/O
37	IOH	P0[0]	Digital I/O
38	IOH	P0[2]	Digital I/O
39	IOH	P0[4]	Digital I/O
40	IOH	P0[6]	Digital I/O
41	Power	Vdd	Supply voltage
42	NC	NC	No connection
43	NC	NC	No connection
44	IOH	P0[7]	Digital I/O
45	IOH	P0[5]	Digital I/O
46	IOH	P0[3]	Digital I/O
47	Power	Vss	Supply ground
48	IOH	P0[1]	Digital I/O
CP	Power	Vss	Center pad must be connected to ground

LEGEND I = Input, O = Output, OH = 5 mA High Output Drive, R = Regulated Output.

Note
2. These are the in-system serial programming (ISSP) pins, that are not High Z at power on reset (POR).

Register Reference

The section discusses the registers of the enCoRe V LV device. It lists all the registers in mapping tables, in address order.

Register Conventions

The register conventions specific to this section and the Register Reference chapter are listed in the following table.

Table 3. Register Conventions

Convention	Description
R	Read register or bits
W	Write register or bits
O	Only a read/write register or bits
L	Logical register or bits
C	Clearable register or bits
#	Access is bit specific

Register Mapping Tables

The enCoRe V LV device has a total register address space of 512 bytes. The register space is also referred to as IO space and is broken into two parts: Bank 0 (user space) and Bank 1 (configuration space). The XIO bit in the Flag register (CPU_F) determines which bank the user is currently in. When the XIO bit is set, the user is said to be in the “extended” address space or the “configuration” registers.

Register Map Bank 0 Table: User Space

Name	Addr (0,Hex)	Access	Name	Addr (0,Hex)	Access	Name	Addr (0,Hex)	Access	Name	Addr (0,Hex)	Access
PRT0DR	00	RW		40			80			C0	
PRT0IE	01	RW		41			81			C1	
	02			42			82			C2	
	03			43			83			C3	
PRT1DR	04	RW		44			84			C4	
PRT1IE	05	RW		45			85			C5	
	06			46			86			C6	
	07			47			87			C7	
PRT2DR	08	RW		48			88		I2C_XCFG	C8	RW
PRT2IE	09	RW		49			89		I2C_XSTAT	C9	R
	0A			4A			8A		I2C_ADDR	CA	RW
	0B			4B			8B		I2C_BP	CB	R
PRT3DR	0C	RW		4C			8C		I2C_CP	CC	R
PRT3IE	0D	RW		4D			8D		CPU_BP	CD	RW
	0E			4E			8E		CPU_CP	CE	R
	0F			4F			8F		I2C_BUF	CF	RW
PRT4DR	10	RW		50			90		CUR_PP	D0	RW
PRT4IE	11	RW		51			91		STK_PP	D1	RW
	12			52			92			D2	
	13			53			93		IDX_PP	D3	RW
	14			54			94		MVR_PP	D4	RW
	15			55			95		MVW_PP	D5	RW
	16			56			96		I2C_CFG	D6	RW
	17			57			97		I2C_SCR	D7	#
	18			58			98		I2C_DR	D8	RW
	19			59			99			D9	
	1A			5A			9A		INT_CLR0	DA	RW
	1B			5B			9B		INT_CLR1	DB	RW
	1C			5C			9C		INT_CLR2	DC	RW
	1D			5D			9D		INT_CLR3	DD	RW
	1E			5E			9E		INT_MSK2	DE	RW
	1F			5F			9F		INT_MSK1	DF	RW
	20			60			A0		INT_MSK0	E0	RW
	21			61			A1		INT_SW_EN	E1	RW
	22			62			A2		INT_VC	E2	RC
	23			63			A3		RES_WDT	E3	W

Gray fields are reserved and should not be accessed. # Access is bit specific.

Name	Addr (0,Hex)	Access	Name	Addr (0,Hex)	Access	Name	Addr (0,Hex)	Access	Name	Addr (0,Hex)	Access
	24			64			A4		INT_MSK3	E4	RW
	25			65			A5			E5	
	26			66			A6			E6	
	27			67			A7			E7	
	28			68			A8			E8	
SPI_TXR	29	W		69			A9			E9	
SPI_RXR	2A	R		6A			AA			EA	
SPI_CR	2B	#		6B			AB			EB	
	2C			6C			AC			EC	
	2D			6D			AD			ED	
	2E			6E			AE			EE	
	2F			6F			AF			EF	
	30			70		PT0_CFG	B0	RW		F0	
	31			71		PT0_DATA1	B1	RW		F1	
	32			72		PT0_DATA0	B2	RW		F2	
	33			73		PT1_CFG	B3	RW		F3	
	34			74		PT1_DATA1	B4	RW		F4	
	35			75		PT1_DATA0	B5	RW		F5	
	36			76		PT2_CFG	B6	RW		F6	
	37			77		PT2_DATA1	B7	RW	CPU_F	F7	RL
	38			78		PT2_DATA0	B8	RW		F8	
	39			79			B9			F9	
	3A			7A			BA			FA	
	3B			7B			BB			FB	
	3C			7C			BC			FC	
	3D			7D			BD			FD	
	3E			7E			BE		CPU_SCR1	FE	#
	3F			7F			BF		CPU_SCR0	FF	#

Gray fields are reserved and should not be accessed. # Access is bit specific.

Register Map Bank 1 Table: Configuration Space

Name	Addr (1,Hex)	Access	Name	Addr (1,Hex)	Access	Name	Addr (1,Hex)	Access	Name	Addr (1,Hex)	Access
PRT0DM0	00	RW		40			80			C0	
PRT0DM1	01	RW		41			81			C1	
	02			42			82			C2	
	03			43			83			C3	
PRT1DM0	04	RW		44			84			C4	
PRT1DM1	05	RW		45			85			C5	
	06			46			86			C6	
	07			47			87			C7	
PRT2DM0	08	RW		48			88			C8	
PRT2DM1	09	RW		49			89			C9	
	0A			4A			8A			CA	
	0B			4B			8B			CB	
PRT3DM0	0C	RW		4C			8C			CC	
PRT3DM1	0D	RW		4D			8D			CD	
	0E			4E			8E			CE	
	0F			4F			8F			CF	
PRT4DM0	10	RW		50			90			D0	
PRT4DM1	11	RW		51			91			D1	
	12			52			92			D2	
	13			53			93			D3	
	14			54			94			D4	
	15			55			95			D5	
	16			56			96			D6	
	17			57			97			D7	
	18			58			98			D8	
	19			59			99			D9	
	1A			5A			9A			DA	
	1B			5B			9B			DB	
	1C			5C			9C		IO_CFG	DC	RW
	1D			5D			9D		OUT_P1	DD	RW
	1E			5E			9E			DE	
	1F			5F			9F			DF	
	20			60			A0		OSC_CR0	E0	RW
	21			61			A1		ECO_CFG	E1	#
	22			62			A2		OSC_CR2	E2	RW
	23			63			A3		VLT_CR	E3	RW
	24			64			A4		VLT_CMP	E4	R
	25			65			A5			E5	
	26			66			A6			E6	
	27			67			A7			E7	
	28			68			A8		IMO_TR	E8	W
SPI_CFG	29	RW		69			A9		ILO_TR	E9	W
	2A			6A			AA			EA	
	2B			6B			AB		SLP_CFG	EB	RW
	2C		TMP_DR0	6C	RW		AC		SLP_CFG2	EC	RW
	2D		TMP_DR1	6D	RW		AD		SLP_CFG3	ED	RW
	2E		TMP_DR2	6E	RW		AE			EE	
	2F		TMP_DR3	6F	RW		AF			EF	
	30			70			B0			F0	
	31			71			B1			F1	
	32			72			B2			F2	
	33			73			B3			F3	
	34			74			B4			F4	
	35			75			B5			F5	
	36			76			B6			F6	
	37			77			B7		CPU_F	F7	RL
	38			78			B8			F8	
	39			79			B9			F9	

Gray fields are reserved and should not be accessed. # Access is bit specific.

Name	Addr (1,Hex)	Access	Name	Addr (1,Hex)	Access	Name	Addr (1,Hex)	Access	Name	Addr (1,Hex)	Access
	3A			7A			BA			FA	
	3B			7B			BB			FB	
	3C			7C			BC			FC	
	3D			7D			BD			FD	
	3E			7E			BE			FE	
	3F			7F			BF			FF	

Gray fields are reserved and should not be accessed. # Access is bit specific.

Electrical Specifications

This chapter presents the DC and AC electrical specifications of the enCoRe V LV devices. For the most up to date electrical specifications, verify that you have the most recent data sheet available by visiting the company web site at http://www.cypress.com

Figure 5. Voltage versus CPU Frequency

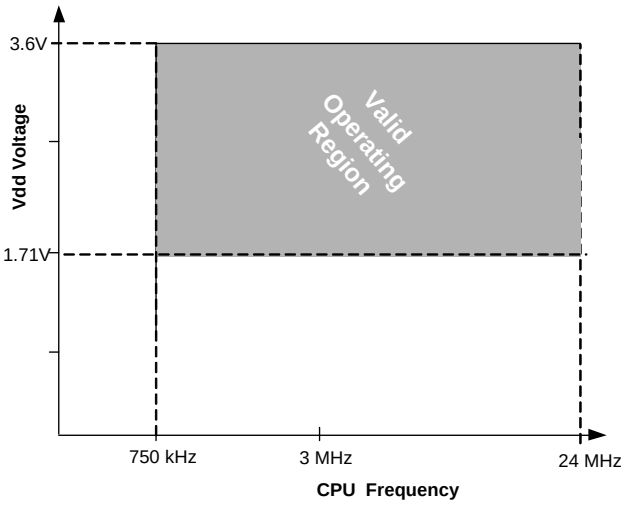
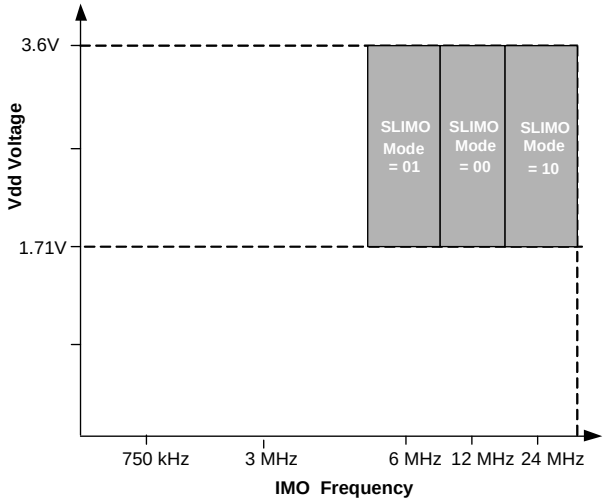


Figure 6. IMO Frequency Trim Options



The following table lists the units of measure that are used in this chapter.

Table 4. Units of Measure

Symbol	Unit of Measure
°C	degree Celsius
dB	decibels
fF	femto farad
Hz	hertz
KB	1024 bytes
Kbit	1024 bits
kHz	kilohertz
kΩ	kilohm
MHz	megahertz
MΩ	megaohm
µA	microampere
µF	microfarad
µH	microhenry
µs	microsecond
µV	microvolts
µVrms	microvolts root-mean-square
µW	microwatts
mA	milli-ampere
ms	milli-second
mV	milli-volts
nA	nanoampere
ns	nanosecond
nV	nanovolts
W	ohm
pA	picoampere
pF	picofarad
pp	peak-to-peak
ppm	parts per million
ps	picosecond
sps	samples per second
s	sigma: one standard deviation
V	volts

Electrical Characteristics

Absolute Maximum Ratings

Storage Temperature (T_{STG}) [3] ..... -55°C to 125°C (Typical +25°C)
Supply Voltage Relative to Vss (Vdd) ..... -0.5V to +4.0V
DC Input Voltage (V_{IO}) ..... Vss - 0.5V to Vdd + 0.5V
DC Voltage Applied to Tri-state (V_{IOZ}) ..... Vss - 0.5V to Vdd + 0.5V
Maximum Current into any Port Pin (I_{MIO}) ..... -25mA to +50mA
Electro Static Discharge Voltage (ESD) [4] 2000V
Latch-up Current (LU) [5] 200mA

Operating Conditions

Ambient Temperature (T_A) ..... 0°C to 70°C
Operational Die Temperature (T_J)[6] ..... 0°C to 85°C

DC Electrical Characteristics

DC Chip-Level Specifications

The following table lists guaranteed maximum and minimum specifications for the entire voltage and temperature ranges.

Parameter	Description	Conditions	Min	Typ	Max	Units
Vdd	Supply Voltage	See table titled DC POR and LVD Specifications on page 19.	1.71	–	3.6	V
I_{DD24}	Supply Current, IMO = 24 MHz	Conditions are Vdd = 3.0V, T_A = 25°C, CPU = 24 MHz No I2C/SPI	–	–	2.15	mA
I_{DD12}	Supply Current, IMO = 12 MHz	Conditions are Vdd = 3.0V, T_A = 25°C, CPU = 12 MHz No I2C/SPI	–	–	1.45	mA
I_{DD6}	Supply Current, IMO = 6 MHz	Conditions are Vdd = 3.0V, T_A = 25°C, CPU = 6 MHz No I2C/SPI	–	–	1.1	mA
I_{SB0}	Deep Sleep Current	Vdd = 3.0V, T_A = 25°C, IO regulator turned off	–	0.1	–	µA
I_{SB1}	Standby Current with POR, LVD and Sleep Timer	Vdd = 3.0V, T_A = 25°C, IO regulator turned off	–	–	1.5	µA

Notes
3. Higher storage temperatures reduce data retention time. Recommended Storage Temperature is +25°C ± 25°C. Extended duration storage temperatures above 85°C degrade reliability.
4. Human Body Model ESD.
5. Per JESD78 standard.
6. The temperature rise from ambient to junction is package specific. See "Package Diagram" on page 23 for Thermal Impedances. The user must limit the power consumption to comply with this requirement.

DC General Purpose IO Specifications

The following tables list guaranteed maximum and minimum specifications for the voltage and temperature ranges: 1.71V to 3.6V and 0°C ≤ T_A ≤ 70°C. Typical parameters apply to 3.3V at 25°C and are for design guidance only.

Table 5. 3.0V to 3.6V DC GPIO Specifications

Symbol	Description	Conditions	Min	Typ	Max	Units
R_{PU}	Pull up Resistor		4	5.6	8	kΩ
V_{OH1}	High Output Voltage Port 2 or 3 Pins	IOH ≤ 10 µA, maximum of 10 mA source current in all IOs	Vdd - 0.2	–	–	V
V_{OH2}	High Output Voltage Port 2 or 3 Pins	IOH = 1 mA, maximum of 20 mA source current in all IOs	Vdd - 0.9	–	–	V
V_{OH3}	High Output Voltage Port 0 or 1 Pins with LDO Regulator Disabled for Port 1	IOH < 10 µA, maximum of 10 mA source current in all IOs	Vdd - 0.2	–	–	V
V_{OH4}	High Output Voltage Port 0 or 1 Pins with LDO Regulator Disabled for Port 1	IOH = 5 mA, maximum of 20 mA source current in all IOs	Vdd - 0.9	–	–	V
V_{OH5}	High Output Voltage Port 1 Pins with LDO Regulator Enabled for 3V Out	IOH < 10 µA, Vdd > 3.1V, maximum of 4 IOs all sourcing 5 mA	2.85	3.00	3.15	V
V_{OH6}	High Output Voltage Port 1 Pins with LDO Regulator Enabled for 3V Out	IOH = 5 mA, Vdd > 3.1V, maximum of 20 mA source current in all IOs	2.20	–	–	V
V_{OH7}	High Output Voltage Port 1 Pins with LDO Enabled for 2.5V Out	IOH < 10 µA, Vdd > 2.7V, maximum of 20 mA source current in all IOs	2.35	2.50	2.65	V
V_{OH8}	High Output Voltage Port 1 Pins with LDO Enabled for 2.5V Out	IOH = 2 mA, Vdd > 2.7V, maximum of 20 mA source current in all IOs	1.90	–	–	V
V_{OH9}	High Output Voltage Port 1 Pins with LDO Enabled for 1.8V Out	IOH < 10 µA, Vdd > 2.7V, maximum of 20 mA source current in all IOs	1.60	1.80	2.00	V
V_{OH10}	High Output Voltage Port 1 Pins with LDO Enabled for 1.8V Out	IOH = 1 mA, Vdd > 2.7V, maximum of 20 mA source current in all IOs	1.20	–	–	V
V_{OL}	Low Output Voltage	IOL = 25 mA, Vdd > 3.3V, maximum of 60 mA sink current on even port pins (for example, P0[2] and P1[4]) and 60 mA sink current on odd port pins (for example, P0[3] and P1[5])	–	–	0.75	V
V_{IL}	Input Low Voltage		–	–	0.80	V
V_{IH}	Input High Voltage		2.00	–		V
V_H	Input Hysteresis Voltage		–	80	–	mV
I_{IL}	Input Leakage (Absolute Value)		–	1	25	nA
C_{IN}	Capacitive Load on Pins as Input	Package and pin dependent Temp = 25°C	0.5	1.7	5	pF
C_{OUT}	Capacitive Load on Pins as Output	Package and pin dependent Temp = 25°C	0.5	1.7	5	pF

Table 6. 2.4V to 3.0V DC GPIO Specifications

Symbol	Description	Conditions	Min	Typ	Max	Units
R_{PU}	Pull up Resistor		4	5.6	8	kΩ
V_{OH1}	High Output Voltage Port 2 or 3 Pins	IOH < 10 µA, maximum of 10 mA source current in all IOs	Vdd - 0.2	–	–	V
V_{OH2}	High Output Voltage Port 2 or 3 Pins	IOH = 0.2 mA, maximum of 10 mA source current in all IOs	Vdd - 0.4	–	–	V
V_{OH3}	High Output Voltage Port 0 or 1 Pins with LDO Regulator Disabled for Port 1	IOH < 10 µA, maximum of 10 mA source current in all IOs	Vdd - 0.2	–	–	V
V_{OH4}	High Output Voltage Port 0 or 1 Pins with LDO Regulator Disabled for Port 1	IOH = 2 mA, maximum of 10 mA source current in all IOs	Vdd - 0.5	–	–	V
V_{OH5A}	High Output Voltage Port 1 Pins with LDO Enabled for 1.8V Out	IOH < 10 µA, Vdd > 2.4V, maximum of 20 mA source current in all IOs.	1.50	1.80	2.00	V
V_{OH6A}	High Output Voltage Port 1 Pins with LDO Enabled for 1.8V Out	IOH = 1 mA, Vdd > 2.4V, maximum of 20 mA source current in all IOs	1.20	–	–	V
V_{OL}	Low Output Voltage	IOL = 10 mA, maximum of 30 mA sink current on even port pins (for example, P0[2] and P1[4]) and 30 mA sink current on odd port pins (for example, P0[3] and P1[5])	–	–	0.75	V
V_{IL}	Input Low Voltage		–	–	0.72	V
V_{IH}	Input High Voltage		2.0	–		V
V_H	Input Hysteresis Voltage		–	80	–	mV
I_{IL}	Input Leakage (Absolute Value)	Gross tested to 1 µA.	–	1	–	nA
C_{IN}	Capacitive Load on Pins as Input	Package and pin dependent Temp = 25°C	0.5	1.7	5	pF
C_{OUT}	Capacitive Load on Pins as Output	Package and pin dependent Temp = 25°C	0.5	1.7	5	pF

Table 7. 1.71V to 2.4V DC GPIO Specifications

Symbol	Description	Conditions	Min	Typ	Max	Units
R_{PU}	Pull up Resistor		4	5.6	8	kΩ
V_{OH1}	High Output Voltage Port 2 or 3 Pins	IOH = 10 µA, maximum of 10 mA source current in all IOs	Vdd - 0.2	–	–	V
V_{OH2}	High Output Voltage Port 2 or 3 Pins	IOH = 0.5 mA, maximum of 10 mA source current in all IOs	Vdd - 0.5	–	–	V
V_{OH3}	High Output Voltage Port 0 or 1 Pins with LDO Regulator Disabled for Port 1	IOH = 100 µA, maximum of 10 mA source current in all IOs	Vdd - 0.2	–	–	V
V_{OH4}	High Output Voltage Port 0 or 1 Pins with LDO Regulator Disabled for Port 1	IOH = 2 mA, maximum of 10 mA source current in all IOs	Vdd - 0.5	–	–	V
V_{OL}	Low Output Voltage	IOL = 5 mA, maximum of 20 mA sink current on even port pins (for example, P0[2] and P1[4]) and 30 mA sink current on odd port pins (for example, P0[3] and P1[5])	–	–	0.4	V
V_{IL}	Input Low Voltage		–	–	0.3 x Vdd	V
V_{IH}	Input High Voltage		0.65 x Vdd	–		V
V_H	Input Hysteresis Voltage		–	80	–	mV
I_{IL}	Input Leakage (Absolute Value)		–	1	50	nA
C_{IN}	Capacitive Load on Pins as Input	Package and pin dependent. Temp = 25°C	0.5		5	pF
C_{OUT}	Capacitive Load on Pins as Output	Package and pin dependent Temp = 25°C	0.5		5	pF

DC POR and LVD Specifications

The following table lists guaranteed maximum and minimum specifications for the entire voltage and temperature ranges.

Table 8. DC POR and LVD Specifications

Symbol	Description	Min	Typ	Max	Units
	Vdd Value for PPOR Trip[7]				
V_{PPOR0}	PORLEV[1:0] = 00b, HPOR = 0	1.61	1.66	1.71	V
V_{PPOR1}	PORLEV[1:0] = 00b, HPOR = 1		2.36	2.40	V
V_{PPOR2}	PORLEV[1:0] = 01b, HPOR = 1		2.60	2.65	V
V_{PPOR3}	PORLEV[1:0] = 10b, HPOR = 1		2.82	2.95	V
	Vdd Value for LVD Trip				
V_{LVD0}	VM[2:0] = 000b[8]	2.40	2.45	2.51	V
V_{LVD1}	VM[2:0] = 001b[9]	2.64	2.71	2.78	V
V_{LVD2}	VM[2:0] = 010b[10]	2.85	2.92	2.99	V
V_{LVD3}	VM[2:0] = 011b	2.95	3.02	3.09	V
V_{LVD4}	VM[2:0] = 100b	3.06	3.13	3.20	
V_{LVD5}	VM[2:0] = 101b	–	1.9	–	
V_{LVD6}	VM[2:0] = 110b[11]	–	1.8	–	

DC Programming Specifications

The following table lists guaranteed maximum and minimum specifications for the entire voltage and temperature ranges.

Table 9. DC Programming Specifications

Symbol	Description	Min	Typ	Max	Units
Vdd_{IWRITE}	Supply Voltage for Flash Write Operations	1.71	–	–	V
I_{DDP}	Supply Current During Programming or Verify	–	5	25	mA
V_{ILP}	Input Low Voltage During Programming or Verify	–	–	V_{IL}	V
V_{IHP}	Input High Voltage During Programming or Verify	V_{IH}	–	–	V
I_{ILP}	Input Current when Applying Vilp to P1[0] or P1[1] During Programming or Verify[12]	–	–	0.2	mA
I_{IHP}	Input Current when Applying Vihp to P1[0] or P1[1] During Programming or Verify[13]	–	–	1.5	mA
V_{OLV}	Output Low Voltage During Programming or Verify	–	–	Vss + 0.75	V
V_{OHV}	Output High Voltage During Programming or Verify	Vdd - 1.0	–	Vdd	V
$Flash_{ENPB}$	Flash Write Endurance[14]	50,000	–	–	Cycles
$Flash_{DR}$	Flash Data Retention[15]	10	20	–	Years

Notes

7. Vdd must be greater than or equal to 1.71V during startup, reset from the XRES pin, or reset from Watchdog.
8. Always greater than 50 mV above V_{PPOR1} for falling supply.
9. Always greater than 50 mV above V_{PPOR2} for falling supply.
10. Always greater than 50 mV above V_{PPOR3} for falling supply.
11. Always greater than 50 mV above V_{PPOR0} voltage for falling supply.
12. Driving internal pull down resistor.
13. Driving internal pull down resistor.
14. Erase/write cycles per block.
15. Following maximum Flash write cycles.

AC Electrical Characteristics

AC Chip-Level Specifications

The following table lists guaranteed maximum and minimum specifications for the entire voltage and temperature ranges.

Table 10. AC Chip-Level Specifications

Symbol	Description	Min	Typ	Max	Units
F_{MAX}	Maximum Operating Frequency[16]	24	–	–	MHz
F_{CPU}	Maximum Processing Frequency[17]	24	–	–	MHz
F_{32K1}	Internal Low Speed Oscillator Frequency	30.4	32	33.6	kHz
F_{IMO24}	Internal Main Oscillator Stability for 24 MHz ± 5%[18]	22.8	24	25.2	MHz
F_{IMO12}	Internal Main Oscillator Stability for 12 MHz[19]	11.4	12	12.6	MHz
F_{IMO6}	Internal Main Oscillator Stability for 6 MHz[20]	5.7	6.0	6.3	MHz
DC_{IMO}	Duty Cycle of IMO	40	50	60	%
T_{RAMP}	Supply Ramp Time	0	–	–	µs

AC General Purpose IO Specifications

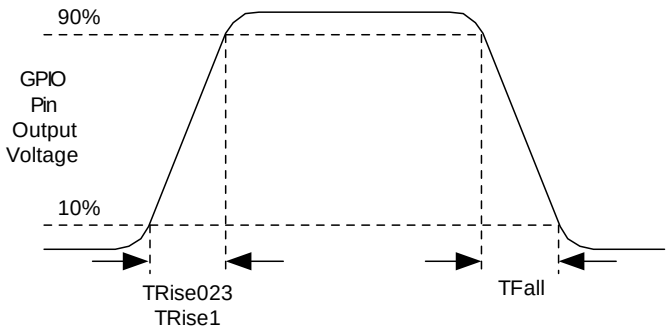
The following table lists guaranteed maximum and minimum specifications for the entire voltage and temperature ranges.

Table 11. AC GPIO Specifications

Symbol	Description	Conditions	Min	Typ	Max	Units
F_{GPIO}	GPIO Operating Frequency	Normal Strong Mode, Port 1	0	–	6 MHz for 1.8V<Vdd<2.4V 12 MHz for 2.4V<Vdd<3.6V	MHz
TRise023	Rise Time, Strong Mode, Cload = 50 pF Ports 2 or 3	Vdd = 3.0 to 3.6V, 10% – 90%	15	–	80	ns
TRise023L	Rise Time, Strong Mode Low Supply, Cload = 50 pF Ports 2 or 3	Vdd = 1.71 to 3.0V, 10% – 90%	15	–	80	ns
TRise1	Rise Time, Strong Mode, Cload = 50 pF Ports 0 or 1	Vdd = 3.0 to 3.6V, 10% – 90% LDO enabled or disabled.	7	–	50	ns
TRise1L	Rise Time, Strong Mode Low Supply, Cload = 50 pF Ports 0 or 1	Vdd = 1.71 to 3.0V, 10% – 90% LDO enabled or disabled	8	–	80	ns
TFall	Fall Time, Strong Mode, Cload = 50 pF All Ports	Vdd = 3.0 to 3.6V, 10% – 90%	7	–	50	ns
TFallL	Fall Time, Strong Mode Low Supply, Cload = 50 pF All Ports	Vdd = 1.71 to 3.0V, 10% – 90%	9	–	70	ns

Notes
16. Digital clocking functions.
17. CPU speed.
18. Trimmed using factory trim values.
19. Trimmed using factory trim values.
20. Trimmed using factory trim values.

Figure 7. GPIO Timing Diagram



AC External Clock Specifications

The following table lists guaranteed maximum and minimum specifications for the entire voltage and temperature ranges.

Table 12. AC External Clock Specifications

Symbol	Description	Min	Typ	Max	Units
F_{OSCEXT}	Frequency	0.750	–	25.2	MHz
–	High Period	20.6	–	5300	ns
–	Low Period	20.6	–	–	ns
–	Power Up IMO to Switch	150	–	–	µs

AC Programming Specifications

The following table lists guaranteed maximum and minimum specifications for the entire voltage and temperature ranges.

Table 13. AC Programming Specifications

Symbol	Description	Min	Typ	Max	Units
T_{RSCLK}	Rise Time of SCLK	1	–	20	ns
T_{FSCLK}	Fall Time of SCLK	1	–	20	ns
T_{SSCLK}	Data Set up Time to Falling Edge of SCLK	40	–	–	ns
T_{HSCLK}	Data Hold Time from Falling Edge of SCLK	40	–	–	ns
F_{SCLK}	Frequency of SCLK	0	–	8	MHz
T_{ERASEB}	Flash Erase Time (Block)	–	–	18	ms
T_{WRITE}	Flash Block Write Time	–	–	25	ms
T_{DSCLK}	Data Out Delay from Falling Edge of SCLK	–	–	45	ns
T_{DSCLK3}	Data Out Delay from Falling Edge of SCLK	–	–	50	ns
T_{DSCLK2}	Data Out Delay from Falling Edge of SCLK	–	–	70	ns

AC SPI Specifications

The following table lists guaranteed maximum and minimum specifications for the entire voltage and temperature ranges.

Table 14. AC SPI Specifications

Symbol	Description	Min	Typ	Max	Units
F_{SPIM}	Maximum Input Clock Frequency Selection, Master[21]	–	–	8.2	MHz
F_{SPIS}	Maximum Input Clock Frequency Selection, Slave	–	–	4.1	MHz
T_{SS}	Width of SS_ Negated Between Transmissions	50	–	–	ns

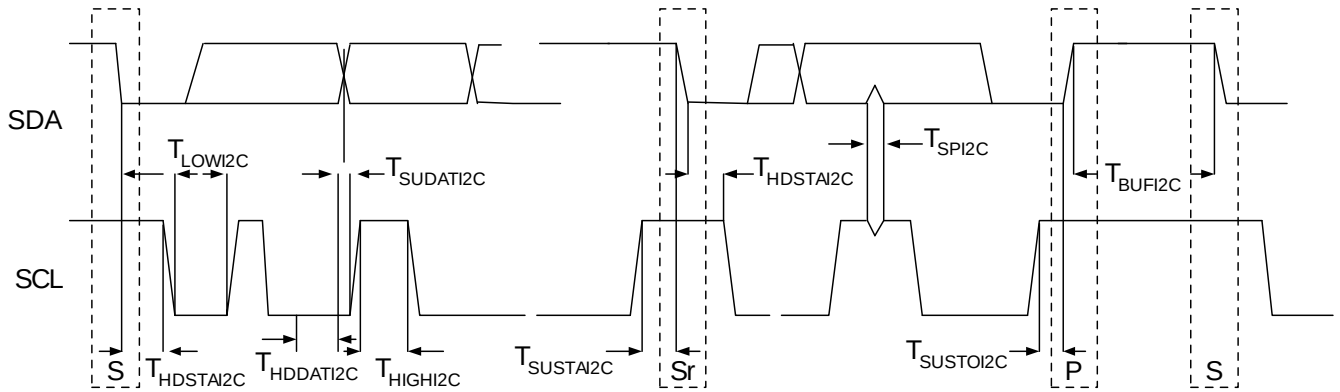
AC I²C Specifications

The following table lists guaranteed maximum and minimum specifications for the entire voltage and temperature ranges.

Table 15. AC Characteristics of the I²C SDA and SCL Pins

Symbol	Description	Standard Mode		Fast Mode		Units
		Min	Max	Min	Max	
F_{SCLI2C}	SCL Clock Frequency	0	100	0	400	kHz
$T_{HDSTAI2C}$	Hold Time (repeated) START Condition. After this period, the first clock pulse is generated.	4.0	–	0.6	–	µs
T_{LOWI2C}	LOW Period of the SCL Clock	4.7	–	1.3	–	µs
$T_{HIGHI2C}$	HIGH Period of the SCL Clock	4.0	–	0.6	–	µs
$T_{SUSTAI2C}$	Set-up Time for a Repeated START Condition	4.7	–	0.6	–	µs
$T_{HDDATI2C}$	Data Hold Time	0	–	0	–	µs
$T_{SUDATI2C}$	Data Set-up Time	250	–	100[22]	–	ns
$T_{SUSTOI2C}$	Set-up Time for STOP Condition	4.0	–	0.6	–	µs
T_{BUFI2C}	Bus Free Time Between a STOP and START Condition	4.7	–	1.3	–	µs
T_{SPI2C}	Pulse Width of spikes are suppressed by the input filter	–	–	0	50	ns

Figure 8. Definition for Timing for Fast/Standard Mode on the I²C Bus



Notes

21. Output clock frequency is half of input clock rate.
22. A Fast-Mode I2C-bus device can be used in a Standard-Mode I2C-bus system, but the requirement $t_{SU;DAT}$ Š 250 ns must then be met. This is automatically the case if the device does not stretch the LOW period of the SCL signal. If such device does stretch the LOW period of the SCL signal, it must output the next data bit to the SDA line $t_{rmax} + t_{SU;DAT}$ = 1000 + 250 = 1250 ns (according to the Standard-Mode I2C-bus specification) before the SCL line is released.

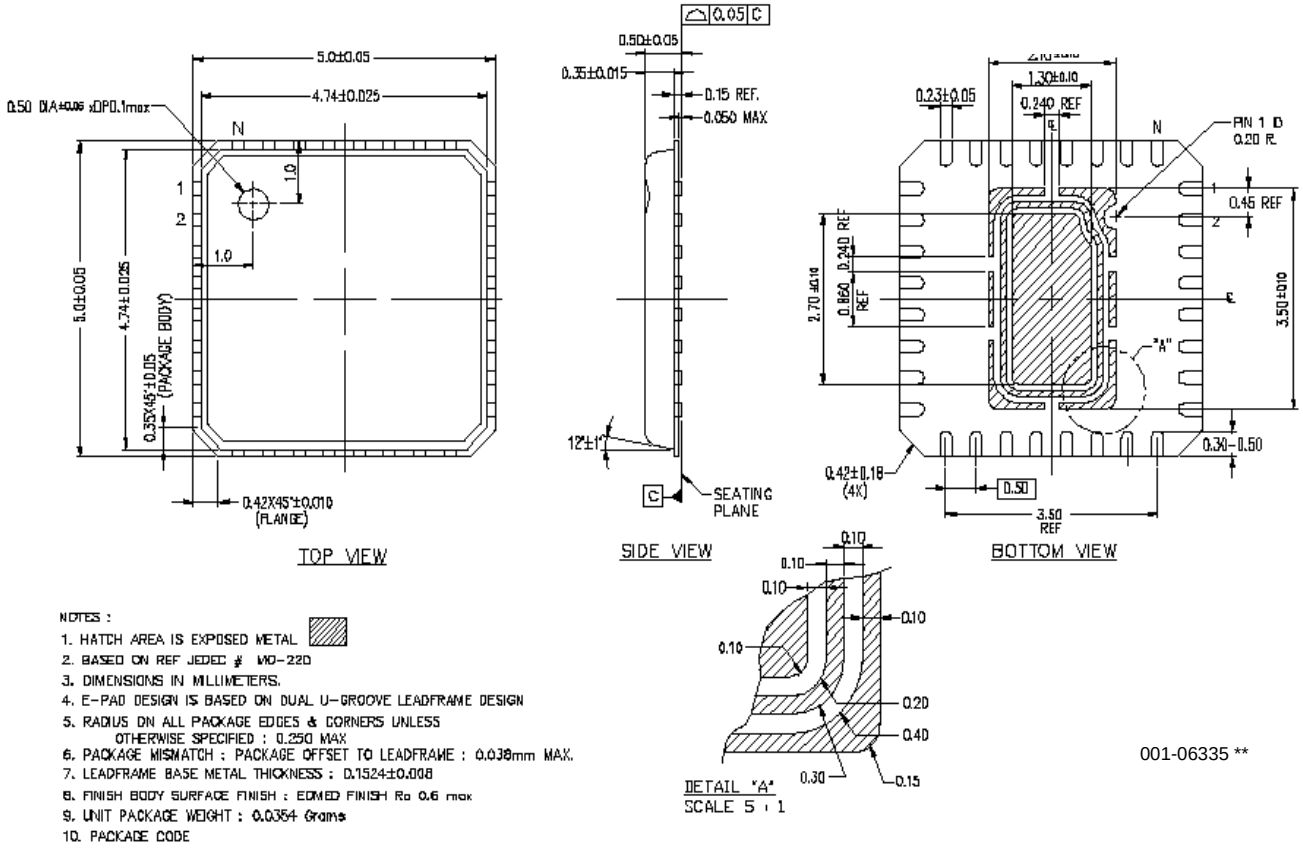
Package Diagram

This chapter illustrates the packaging specifications for the enCoRe V LV device, along with the thermal impedances for each package.

Important Note Emulation tools may require a larger area on the target PCB than the chip's footprint. For a detailed description of the enCoRe V LV emulation tools and their dimensions, refer to the development kit.

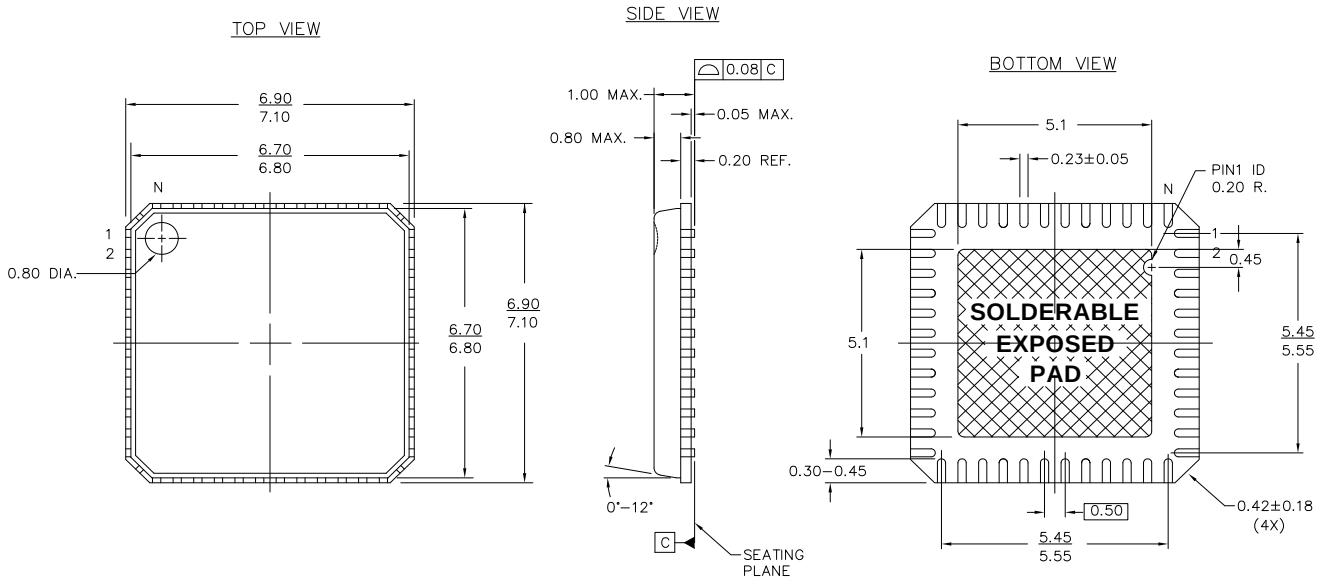
Packaging Dimensions

Figure 9. 32-Lead (5x5 x 0.6 mm) QFN



NOTES :
1. HATCH AREA IS EXPOSED METAL
2. BASED ON REF JEDEC # MO-220
3. DIMENSIONS IN MILLIMETERS.
4. E-PAD DESIGN IS BASED ON DUAL U-GROOVE LEADFRAME DESIGN
5. RADIUS ON ALL PACKAGE EDGES & CORNERS UNLESS OTHERWISE SPECIFIED : 0.250 MAX
6. PACKAGE MISMATCH : PACKAGE OFFSET TO LEADFRAME : 0.038mm MAX.
7. LEADFRAME BASE METAL THICKNESS : 0.1524±0.008
8. FINISH BODY SURFACE FINISH : EDMED FINISH Ra 0.6 max
9. UNIT PACKAGE WEIGHT : 0.0364 Grams
10. PACKAGE CODE

Figure 10. 48-Lead (7x7 x 1mm) QFN



NOTES:

1. HATCH AREA IS SOLDERABLE EXPOSED METAL.
2. REFERENCE JEDEC#: MO-220
3. PACKAGE WEIGHT: 0.13g
4. ALL DIMENSIONS ARE IN MM [MIN/MAX]
5. PACKAGE CODE

PART #	DESCRIPTION
LF48A	STANDARD
LY48A	LEAD FREE

001-12919 *A

Thermal Impedances

Table 16. Thermal Impedances per Package

Package	Typical θ_{JA} *
32 QFN**	14.5 °C/W
48 QFN**	28 °C/W

* $T_J = T_A + \text{Power} \times \theta_{JA}$
** To achieve the thermal impedance specified for the ** package, solder the center thermal pad to the PCB ground plane.

Solder Reflow Peak Temperature

Following is the minimum solder reflow peak temperature to achieve good solderability.

Table 17. Solder Reflow Peak Temperature

Package	Minimum Peak Temperature*	Maximum Peak Temperature
32 QFN	240°C	260°C
48 QFN	240°C	260°C

*Higher temperatures may be required based on the solder melting point. Typical temperatures for solder are 220 ± 5°C with Sn-Pb or 245 ± 5°C with Sn-Ag-Cu paste. Refer to the solder manufacturer specifications.

Ordering Information

Ordering Code	Package Information	Flash	SRAM	No. of GPIOs	Target Applications
CY7C60445-32LKXC	32-lead QFN (5x5x0.6mm)	16K	1K	28	Feature-Rich Wireless Mouse
CY7C60455-48LFXC	48-lead QFN (7x7x1mm)	16K	1K	36	Mid-Tier Wireless Keyboard
CY7C60456-48LFXC	48-lead QFN (7x7x1mm)	32K	2K	36	Feature-Rich Wireless Keyboard

Document History Page

Document Title: CY7C60445, CY7C6045x enCoRe™ V Low Voltage Microcontroller Document Number: 001-12395				
REV.	**ECN.**	**Issue Date**	**Orig. of Change**	**Description of Change**
**	626516	See ECN	TYJ	New data sheet
*A	735721	See ECN	TYJ/ARI	Added new block diagram, replaced TBDs, corrected values, updated pinout information, changed part number to reflect new specifications.
*B	1120504	See ECN	ARI	Corrected the description to pin 29 on Table 1, the Typ/Max values for I_{SB0} on the DC chip-level specifications, and the Min voltage value for Vdd_{IWRITE} in the DC Programming Specifications table. Corrected Flash Write Endurance minimum value in the DC Programming Specifications table. Corrected the Flash Erase Time max value and the Flash Block Write Time max value in the AC Programming Specifications table. Implemented new latest template.
*C	1225864	See ECN	AESA/ARI	Corrected the description to pin 13, 29 on Table 1 and 22,44 on Table 2. Added sections Register Reference, Register Conventions and Register Mapping Tables. Corrected Max values on the DC Chip-Level Specifications table.
*D	1446763	See ECN	AESA	Changed T_{ERASEB} parameter, max value to 18ms in Table 13, AC Programming Specification.
*E	1639963	See ECN	AESA	Post to www.cypress.com