

Single, Dual, Quad General Purpose Micropower, RRIO Operational Amplifiers

ISL28114, ISL28214, ISL28414

The ISL28114, ISL28214, and ISL28414 are single, dual, and quad channel general purpose micropower, rail-to-rail input and output operational amplifiers with supply voltage range of 1.8V to 5.5V. Key features are a low supply current of 360µA maximum per channel at room temperature, a low bias current and a wide input voltage range, which enables the ISL28x14 devices to be excellent general purpose op-amps for a wide range of applications.

The ISL28114 is available in the SC70-5 and SOT23-5 packages, the ISL28214 is in the MSOP8, S08 packages, and the ISL28414 is in the TSSOP14, SOIC14 packages. All devices operate over the extended temperature range of -40°C to +125°C.

Related Literature

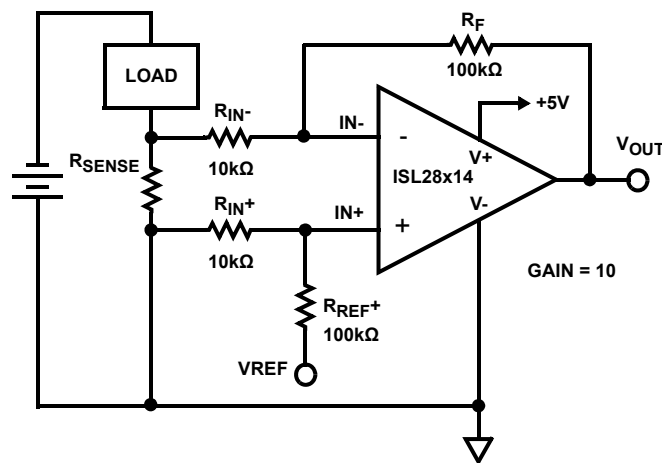
- See [AN1519](#) for “ISL28213/14SOICEVAL2Z Evaluation Board User’s Guide”
- See [AN1520](#) for “ISL28113/14SOT23EVAL1Z Evaluation Board User’s Guide”
- See [AN1542](#) for “ISL28213/14MSOPEVAL2Z Evaluation Board User’s Guide”
- See [AN1547](#) for “ISL28414TSSOPEVAL1Z Evaluation Board User’s Guide”

Features

- Low Current Consumption 360µA
- Wide Supply Range 1.8V to 5.5V
- Gain Bandwidth Product 5MHz
- Input Bias Current 20pA, Max.
- Operating Temperature Range -40°C to +125°C
- Packages
 - ISL28114 (Single) SC70-5, SOT23-5
 - ISL28214 (Dual) MSOP8, S08
 - ISL28414 (Quad) SOIC14, TSSOP14

Applications

- Power Supply Control/Regulation
- Process Control
- Signal Ban/Buffers
- Active Filters
- Current Shunt Sensing
- Trans-impedance Amp



SINGLE-SUPPLY, LOW-SIDE CURRENT SENSE AMPLIFIER

FIGURE 1. TYPICAL APPLICATION

ISL28114, ISL28214, ISL28414

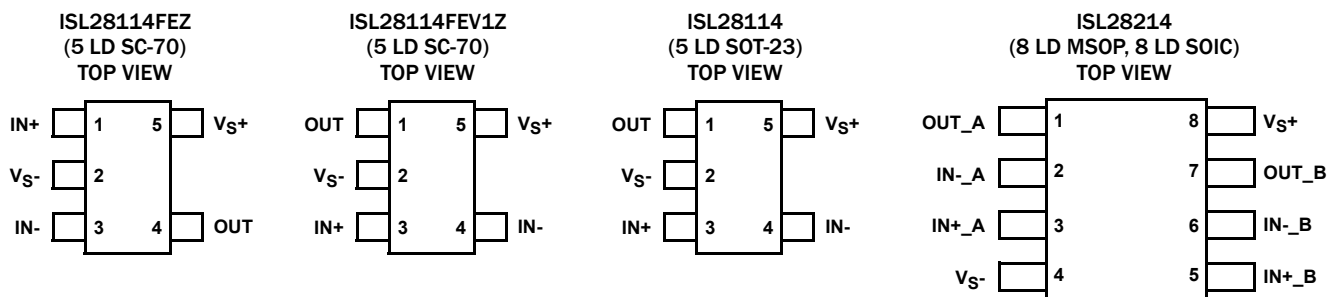
Ordering Information

| PART NUMBER (Notes 2, 3) | PART MARKING | PACKAGE (Pb-Free) | PKG. DWG. # |
|---|------------------|----------------------|----------------|
| ISL28114FEZ-T7 (Note 1) | BKA (Note 4) | 5 Ld SC-70 | P5.049 |
| ISL28114FEZ-T7A (Note 1) | BKA (Note 4) | 5 Ld SC-70 | P5.049 |
| Coming Soon ISL28114FEV1Z-T7 (Note 1) | BMA (Note 4) | 5 Ld SC-70 | P5.049 |
| Coming Soon ISL28114FEV1Z-T7A (Note 1) | BMA (Note 4) | 5 Ld SC-70 | P5.049 |
| ISL28114FHZ-T7 (Note 1) | BDBA (Note 4) | 5 Ld SOT-23 | P5.064A |
| ISL28114FHZ-T7A (Note 1) | BDBA (Note 4) | 5 Ld SOT-23 | P5.064A |
| ISL28214FUZ | 8214Z | 8 Ld MSOP | M8.118A |
| ISL28214FUZ-T7 (Note 1) | 8214Z | 8 Ld MSOP | M8.118A |
| ISL28214FBZ | 28214 FBZ | 8 Ld SOIC | M8.15E |
| ISL28214FBZ-T7 (Note 1) | 28214 FBZ | 8 Ld SOIC | M8.15E |
| ISL28214FBZ-T13 (Note 1) | 28214 FBZ | 8 Ld SOIC | M8.15E |
| ISL28414FVZ | 28414 FVZ | 14 Ld TSSOP | MDP0044 |
| ISL28414FVZ-T7 (Note 1) | 28414 FVZ | 14 Ld TSSOP | MDP0044 |
| ISL28414FVZ-T13 (Note 1) | 28414 FVZ | 14 Ld TSSOP | MDP0044 |
| ISL28414FBZ | 28414 FBZ | 14 Ld SOIC | MDP0027 |
| ISL28414FBZ-T7 (Note 1) | 28414 FBZ | 14 Ld SOIC | MDP0027 |
| ISL28414FBZ-T13 (Note 1) | 28414 FBZ | 14 Ld SOIC | MDP0027 |
| ISL28114SOT23EVAL1Z | Evaluation Board | | |
| ISL28214MSOPEVAL2Z | Evaluation Board | | |
| ISL28214SOICEVAL2Z | Evaluation Board | | |
| ISL28414TSSOPEVAL1Z | Evaluation Board | | |

NOTES:

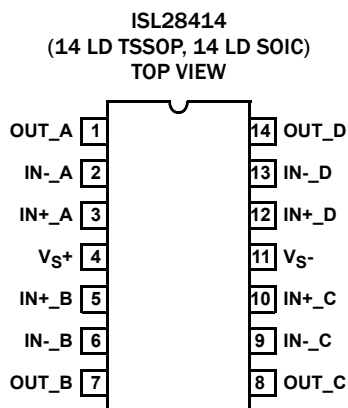
1. Please refer to [TB347](#) for details on reel specifications.
2. These Intersil Pb-free plastic packaged products employ special Pb-free material sets, molding compounds/die attach materials, and 100% matte tin plate plus anneal (e3 termination finish, which is RoHS compliant and compatible with both SnPb and Pb-free soldering operations). Intersil Pb-free products are MSL classified at Pb-free peak reflow temperatures that meet or exceed the Pb-free requirements of IPC/JEDEC J STD-020.
3. For Moisture Sensitivity Level (MSL), please see device information page for [ISL28114](#), [ISL28214](#), [ISL28414](#). For more information on MSL please see Tech Brief [TB363](#).
4. The part marking is located on the bottom of the part.

Pin Configurations



ISL28114, ISL28214, ISL28414

Pin Configurations (Continued)



Pin Descriptions

| PIN NAME | PIN NO. | | | | | DESCRIPTION | |
|---|--------------------|----------------------|---------|-----------|--------------------|-------------------------|--|
| | ISL28114FEZ SC70-5 | ISL28114FEV1Z SC70-5 | SOT23-5 | MSOP8 S08 | TSSOP14 14 LD SOIC | | |
| OUT OUT_A OUT_B OUT_C OUT_D | 4 | 1 | 1 | 1 7 | 1 7 8 14 | Output | <p style="text-align: center;">CIRCUIT 1</p> |
| VS- | 2 | 2 | 2 | 4 | 11 | Negative supply voltage | <p style="text-align: center;">CIRCUIT 2</p> |
| IN+ IN+_A IN+_B IN+_C IN+_D | 1 | 3 | 3 | 3 5 | 3 5 10 12 | Positive Input | <p style="text-align: center;">CIRCUIT 3</p> |
| IN- IN-_A IN-_B IN-_C IN-_D | 3 | 4 | 4 | 2 6 | 2 6 9 13 | Negative Input | |
| VS+ | 5 | 5 | 5 | 8 | 4 | Positive supply voltage | See "CIRCUIT 2" |

ISL28114, ISL28214, ISL28414

Absolute Maximum Ratings (T_A = +25°C)

| | |
|------------------------------------|--|
| Supply Voltage | 6.5V |
| Supply Turn-on Voltage Slew Rate | 1V/μs |
| Differential Input Current | 20mA |
| Differential Input Voltage | V ₋ - 0.5V to V ₊ + 0.5V |
| Input Voltage | V ₋ - 0.5V to V ₊ + 0.5V |
| ESD Rating | |
| Human Body Model | 4000V |
| Machine Model (ISL28114, ISL28214) | 350V |
| Machine Model (ISL28414) | 400V |
| Charged Device Model | 2000V |

Thermal Information

| | | |
|-------------------------------------|---|------------------------|
| Thermal Resistance (Typical) | θ _{JA} (°C/W) | θ _{JC} (°C/W) |
| 5 Ld SC-70 (Notes 5, 6) | 250 | N/A |
| 5 Ld SOT-23 (Notes 5, 6) | 225 | N/A |
| 8 Ld MSOP (Notes 5, 6) | 180 | 100 |
| 8 Ld SOIC Package (Notes 5, 6) | 126 | 90 |
| 14 Ld TSSOP Package (Notes 5, 6) | 120 | 40 |
| 14 Ld SOIC Package (Notes 5, 6) | 90 | 50 |
| Ambient Operating Temperature Range | -40°C to +125°C | |
| Storage Temperature Range | -65°C to +150°C | |
| Operating Junction Temperature | +125°C | |
| Pb-Free Reflow Profile | see link below | |
| | http://www.intersil.com/pbfree/Pb-FreeReflow.asp | |

CAUTION: Do not operate at or near the maximum ratings listed for extended periods of time. Exposure to such conditions may adversely impact product reliability and result in failures not covered by warranty.

NOTES:

- θ_{JA} is measured with the component mounted on a high effective thermal conductivity test board in free air. See Tech Brief TB379 for details.
- For θ_{JC}, the “case temp” location is taken at the package top center.

Electrical Specifications V_{S+} = 5V, V_{S-} = 0V, R_L = Open, V_{CM} = V_S/2, T_A = +25°C, unless otherwise specified. **Boldface limits apply over the operating temperature range, -40°C to +125°C, unless otherwise specified.**

| PARAMETER | DESCRIPTION | CONDITIONS | MIN (Note 7) | TYP | MAX (Note 7) | UNIT |
|---------------------------------|--|--|-----------------|----------|-----------------|-------|
| DC SPECIFICATIONS | | | | | | |
| V _{OS} | Input Offset Voltage | | -5 | 0.5 | 5 | mV |
| | | -40°C to +125°C | -6 | | 6 | mV |
| TCV _{OS} | Input Offset Voltage Temperature Coefficient | -40°C to +125°C | | 2 | 10 | μV/°C |
| I _{OS} | Input Offset Current | | | 1 | 30 | μA |
| I _B | Input Bias Current | ISL28114 | -20 | 3 | 20 | μA |
| | | | -100 | | 100 | μA |
| | | ISL28214, ISL28414 | -20 | 3 | 20 | μA |
| | | | -50 | | 50 | μA |
| Common Mode Input Voltage Range | | | -0.1 | | 5.1 | V |
| CMRR | Common Mode Rejection Ratio | V _{CM} = -0.1V to 5.1V | | 72 | | dB |
| | | -40°C to +125°C | | 70 | | dB |
| PSRR | Power Supply Rejection Ratio | V _S = 1.8V to 5.5V | | 71 | | dB |
| | | -40°C to +125°C | | 70 | | dB |
| V _{OH} | Output Voltage Swing, High | R _L = 10kΩ | 4.985 | 4.993 | | V |
| | | | 4.98 | | | V |
| V _{OL} | Output Voltage Swing, Low | R _L = 10kΩ | | 13 | 15 | mV |
| | | | | | 20 | mV |
| V ₊ | Supply Voltage | | 1.8 | | 5.5 | V |
| I _S | Supply Current per Amplifier | R _L = OPEN | | 300 | 360 | μA |
| | | | | | 400 | μA |
| I _{SC+} | Output Source Short Circuit Current | R _L = 10Ω to V ₋ | | -31 | | mA |
| I _{SC-} | Output Sink Short Circuit Current | R _L = 10Ω to V ₊ | | 26 | | mA |

ISL28114, ISL28214, ISL28414

Electrical Specifications $V_{S+} = 5V$, $V_{S-} = 0V$, $R_L = \text{Open}$, $V_{CM} = V_S/2$, $T_A = +25^\circ\text{C}$, unless otherwise specified. **Boldface limits apply over the operating temperature range, -40°C to $+125^\circ\text{C}$, unless otherwise specified. (Continued)**

| PARAMETER | DESCRIPTION | CONDITIONS | MIN (Note 7) | TYP | MAX (Note 7) | UNIT |
|------------------------------|--|---|-----------------|-----------|-----------------|------------------------------|
| AC SPECIFICATIONS | | | | | | |
| GBWP | Gain Bandwidth Product | $V_S = \pm 2.5V$ $A_V = 100$, $R_F = 100k\Omega$, $R_G = 1k\Omega$, $R_L = 10k\Omega$ to V_{CM} | | 5 | | MHz |
| $e_N V_{P-P}$ | Peak-to-Peak Input Noise Voltage | $V_S = \pm 2.5V$ $f = 0.1\text{Hz}$ to 10Hz | | 12 | | μV_{P-P} |
| e_N | Input Noise Voltage Density | $V_S = \pm 2.5V$ $f = 1\text{kHz}$ | | 40 | | $\text{nV}/\sqrt{\text{Hz}}$ |
| i_N | Input Noise Current Density | $V_S = \pm 2.5V$ $f = 1\text{kHz}$ | | 8 | | $\text{fA}/\sqrt{\text{Hz}}$ |
| Z_{IN} | Input Impedance | | | 10^{12} | | Ω |
| C_{in} | Differential Input Capacitance | $V_S = \pm 2.5V$ $f = 1\text{MHz}$ | | 1.0 | | pF |
| | Common Mode Input Capacitance | | | 1.3 | | pF |
| TRANSIENT RESPONSE | | | | | | |
| SR | Slew Rate | $V_{OUT} = 0.5V$ to $4.5V$ | | 2.5 | | $V/\mu\text{s}$ |
| t_r , t_f , Small Signal | Rise Time, t_r 10% to 90% | $V_S = \pm 2.5V$ $A_V = +1$, $V_{OUT} = 0.05V_{P-P}$, $R_F = 0\Omega$, $R_L = 10k\Omega$, $C_L = 15\text{pF}$ | | 37 | | ns |
| | Fall Time, t_f 10% to 90% | | | 42 | | ns |
| t_s | Settling Time to 0.1%, $4V_{P-P}$ Step | $V_S = \pm 2.5V$ $A_V = +1$, $R_F = 0\Omega$, $R_L = 10k\Omega$, $C_L = 1.2\text{pF}$ | | 5.6 | | μs |

NOTE:

7. Compliance to datasheet limits is assured by one or more methods: production test, characterization and/or design.

Typical Performance Curves $V_S = \pm 2.5V, V_{CM} = 0V, R_L = \text{Open}$, unless otherwise specified.

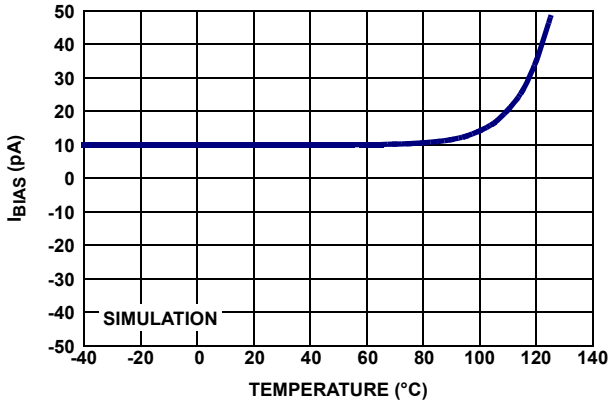


FIGURE 2. INPUT BIAS CURRENT vs TEMPERATURE

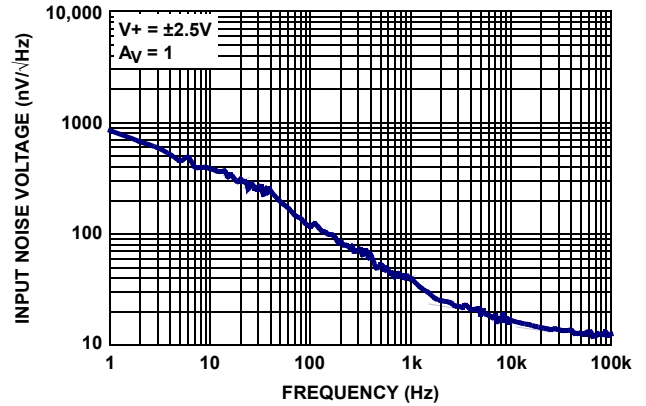


FIGURE 3. INPUT NOISE VOLTAGE SPECTRAL DENSITY

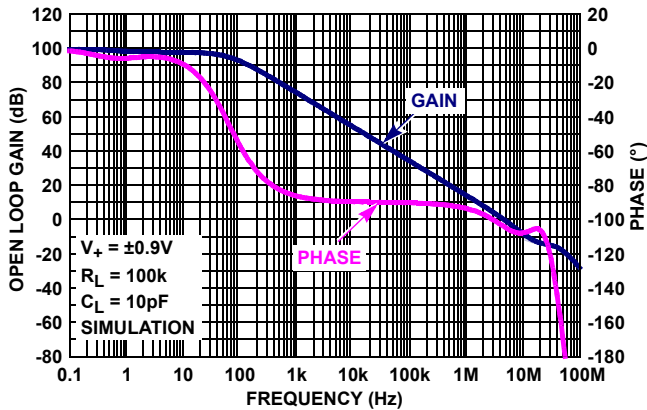


FIGURE 4. OPEN-LOOP GAIN, PHASE vs FREQUENCY, $R_L = 100k\Omega, C_L = 10pF, V_S = \pm 0.9V$

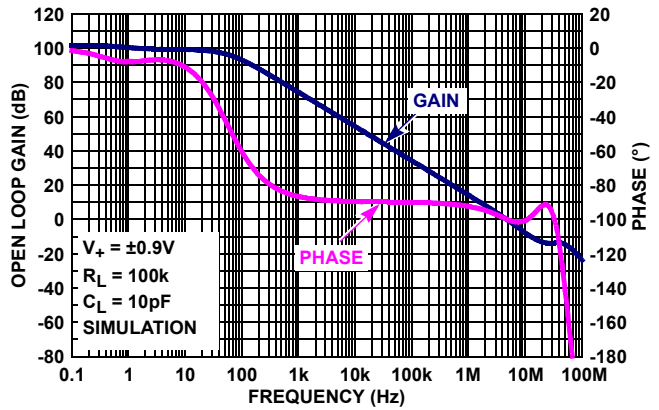


FIGURE 5. OPEN-LOOP GAIN, PHASE vs FREQUENCY, $R_L = 100k\Omega, C_L = 10pF, V_S = \pm 2.5V$

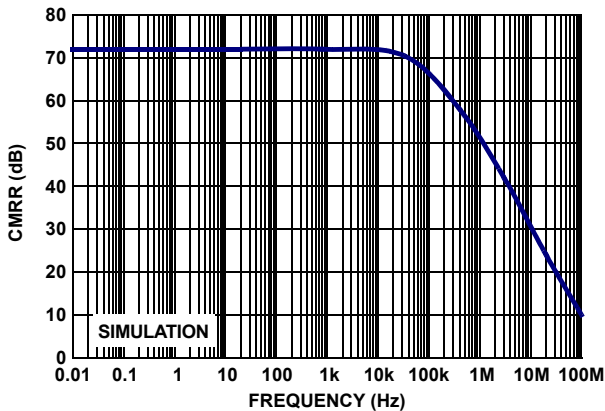


FIGURE 6. CMRR vs FREQUENCY (SIMULATED DATA)

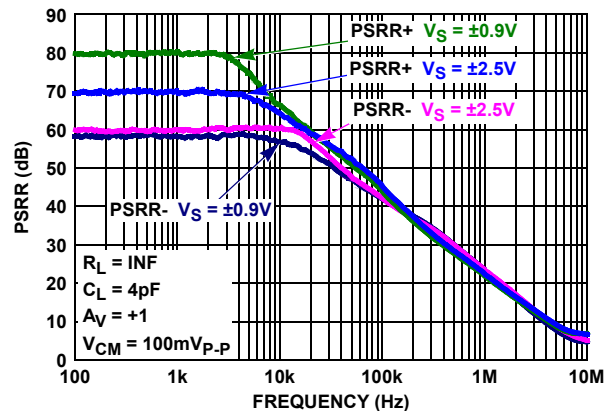


FIGURE 7. PSRR vs FREQUENCY, $V_S = \pm 0.9V, \pm 2.5V$

Typical Performance Curves $V_S = \pm 2.5V, V_{CM} = 0V, R_L = \text{Open}$, unless otherwise specified. (Continued)

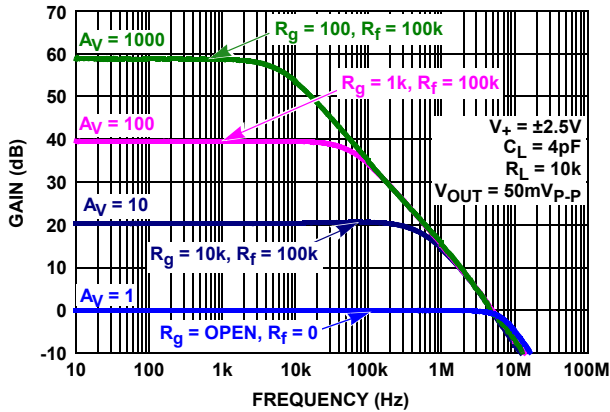


FIGURE 8. FREQUENCY RESPONSE vs CLOSED LOOP GAIN

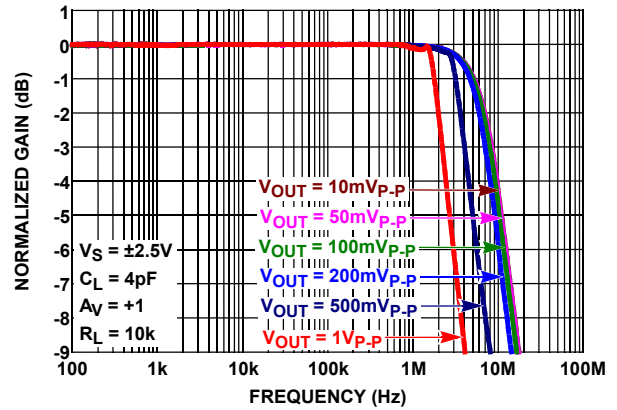


FIGURE 9. FREQUENCY RESPONSE vs V_{OUT}

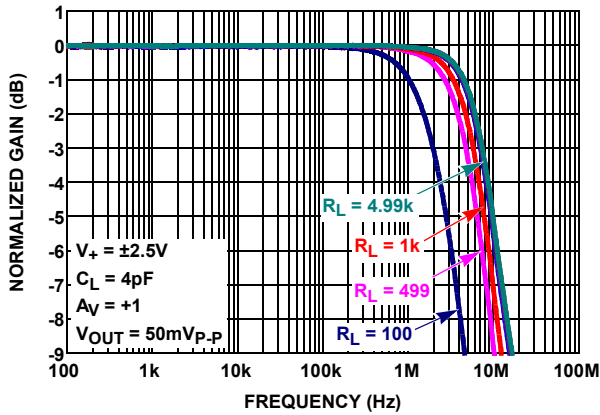


FIGURE 10. GAIN vs FREQUENCY vs R_L

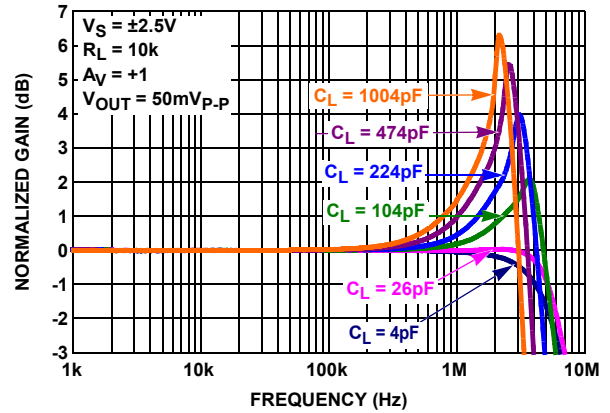


FIGURE 11. GAIN vs FREQUENCY vs C_L

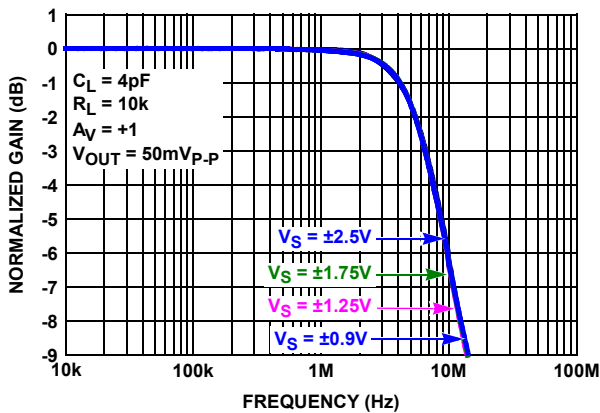


FIGURE 12. GAIN vs FREQUENCY vs SUPPLY VOLTAGE

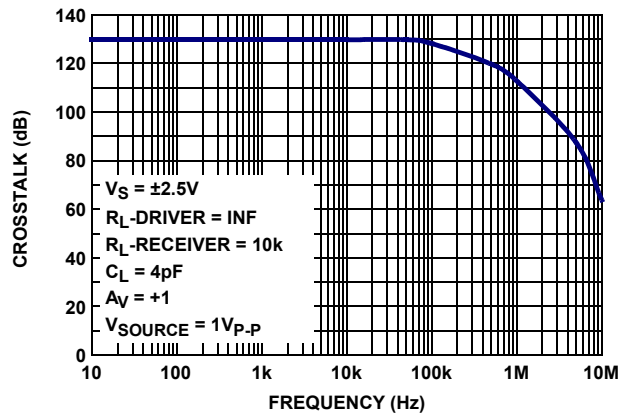


FIGURE 13. CROSSTALK, $V_S = \pm 2.5V$

Typical Performance Curves $V_S = \pm 2.5V, V_{CM} = 0V, R_L = \text{Open}$, unless otherwise specified. (Continued)

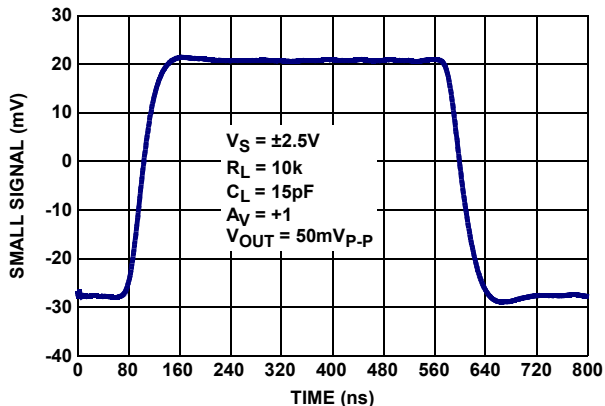


FIGURE 14. SMALL SIGNAL TRANSIENT RESPONSE, $V_S = \pm 2.5V$

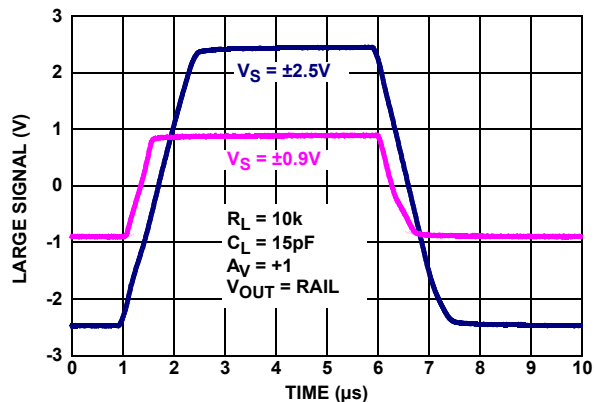


FIGURE 15. LARGE SIGNAL TRANSIENT RESPONSE vs $R_L, V_S = \pm 0.9V, \pm 2.5V$

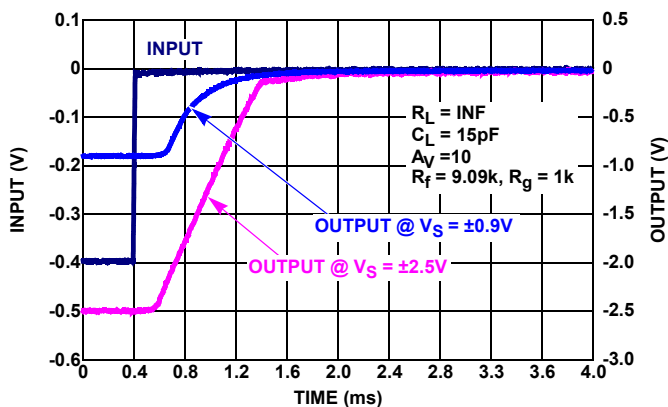


FIGURE 16. NEGATIVE OUTPUT OVERLOAD RESPONSE TIME, $V_S = \pm 0.9V, \pm 2.5V$

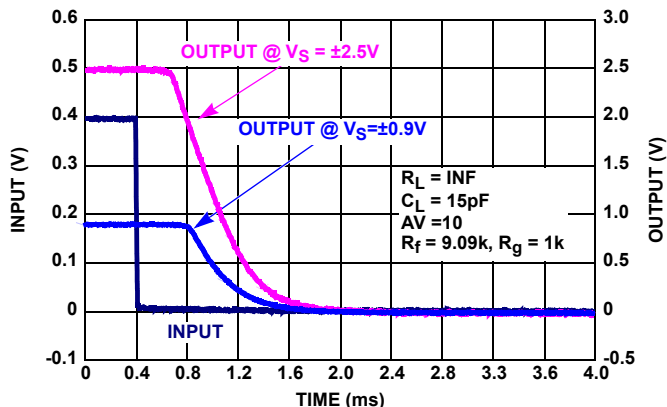


FIGURE 17. POSITIVE OUTPUT OVERLOAD RESPONSE TIME, $V_S = \pm 0.9V, \pm 2.5V$

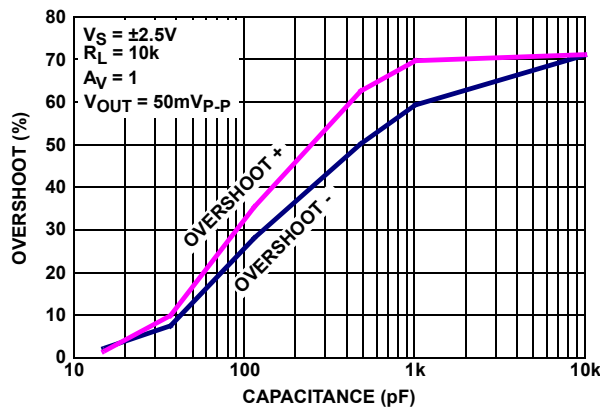


FIGURE 18. % OVERSHOOT vs LOAD CAPACITANCE, $V_S = \pm 2.5V$

Applications Information

Functional Description

The ISL28114, ISL28214 and ISL28414 are single dual and quad, CMOS rail-to-rail input, output (RRIO) micropower operational amplifiers. They are designed to operate from single supply (1.8V to 5.5V) or dual supply ($\pm 0.9V$ to $\pm 2.75V$). The parts have an input common mode range that extends 100mV above and below the power supply voltage rails. The output stage can swing to within 15mV of the supply rails with a 10k Ω load.

Input ESD Diode Protection

All input terminals have internal ESD protection diodes to both positive and negative supply rails, limiting the input voltage to within one diode beyond the supply rails. For applications where the input differential voltage is expected to exceed 0.5V, an external series resistor must be used to ensure the input currents never exceed 20mA (see Figure 19).

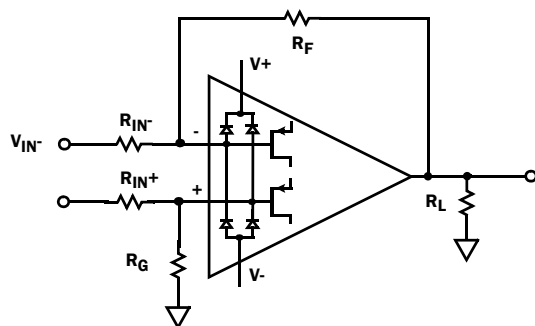


FIGURE 19. INPUT ESD DIODE CURRENT LIMITING

Output Phase Reversal

Output phase reversal is a change of polarity in the amplifier transfer function when the input voltage exceeds the supply voltage. The ISL28114, ISL28214 and ISL28414 are immune to output phase reversal, even when the input voltage is 1V beyond the supplies.

Unused Channels

If the application requires less than all amplifiers one channel, the user must configure the unused channel(s) to prevent it from oscillating. The unused channel(s) will oscillate if the input and output pins are floating. This will result in higher than expected supply currents and possible noise injection into the channel being used. The proper way to prevent this oscillation is to short the output to the inverting input and ground the positive input (as shown in Figure 20).

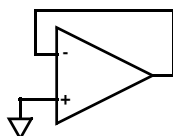


FIGURE 20. PREVENTING OSCILLATIONS IN UNUSED CHANNELS

Power Dissipation

It is possible to exceed the +125°C maximum junction temperatures under certain load, power supply conditions and ambient temperature conditions. It is therefore important to calculate the maximum junction temperature (T_{JMAX}) for all applications to determine if power supply voltages, load conditions, or package type need to be modified to remain in the safe operating area. These parameters are related using Equation 1:

$$T_{JMAX} = T_{MAX} + \theta_{JA} \times PD_{MAXTOTAL} \quad (EQ. 1)$$

where:

- $PD_{MAXTOTAL}$ is the sum of the maximum power dissipation of each amplifier in the package (PD_{MAX})
- PD_{MAX} for each amplifier can be calculated using Equation 2:

$$PD_{MAX} = V_S \times I_{qMAX} + (V_S - V_{OUTMAX}) \times \frac{V_{OUTMAX}}{R_L} \quad (EQ. 2)$$

where:

- T_{MAX} = Maximum ambient temperature
- θ_{JA} = Thermal resistance of the package
- PD_{MAX} = Maximum power dissipation of 1 amplifier
- V_S = Total supply voltage
- I_{qMAX} = Maximum quiescent supply current of 1 amplifier
- V_{OUTMAX} = Maximum output voltage swing of the application
- R_L = Load resistance

ISL28114, ISL28214 and ISL28414 SPICE Model

Figure 21 shows the SPICE model schematic and Figure 22 shows the net list for the SPICE model. The model is a simplified version of the actual device and simulates important AC and DC parameters. AC parameters incorporated into the model are: 1/f and flatband noise, Slew Rate, CMRR, Gain and Phase. The DC parameters are IOS, total supply current and output voltage swing. The model uses typical parameters given in the "Electrical Specifications" Table beginning on page 4. The AVOL is adjusted for 90dB with the dominate pole at 125Hz. The CMRR is set 72dB, $f = 80kHz$. The input stage models the actual device to present an accurate AC representation. The model is configured for ambient temperature of +25°C.

Figures 23 through 30 show the characterization vs simulation results for the Noise Voltage, Closed Loop Gain vs Frequency, Large Signal 5V Step Response and CMRR and Open Loop Gain Phase.

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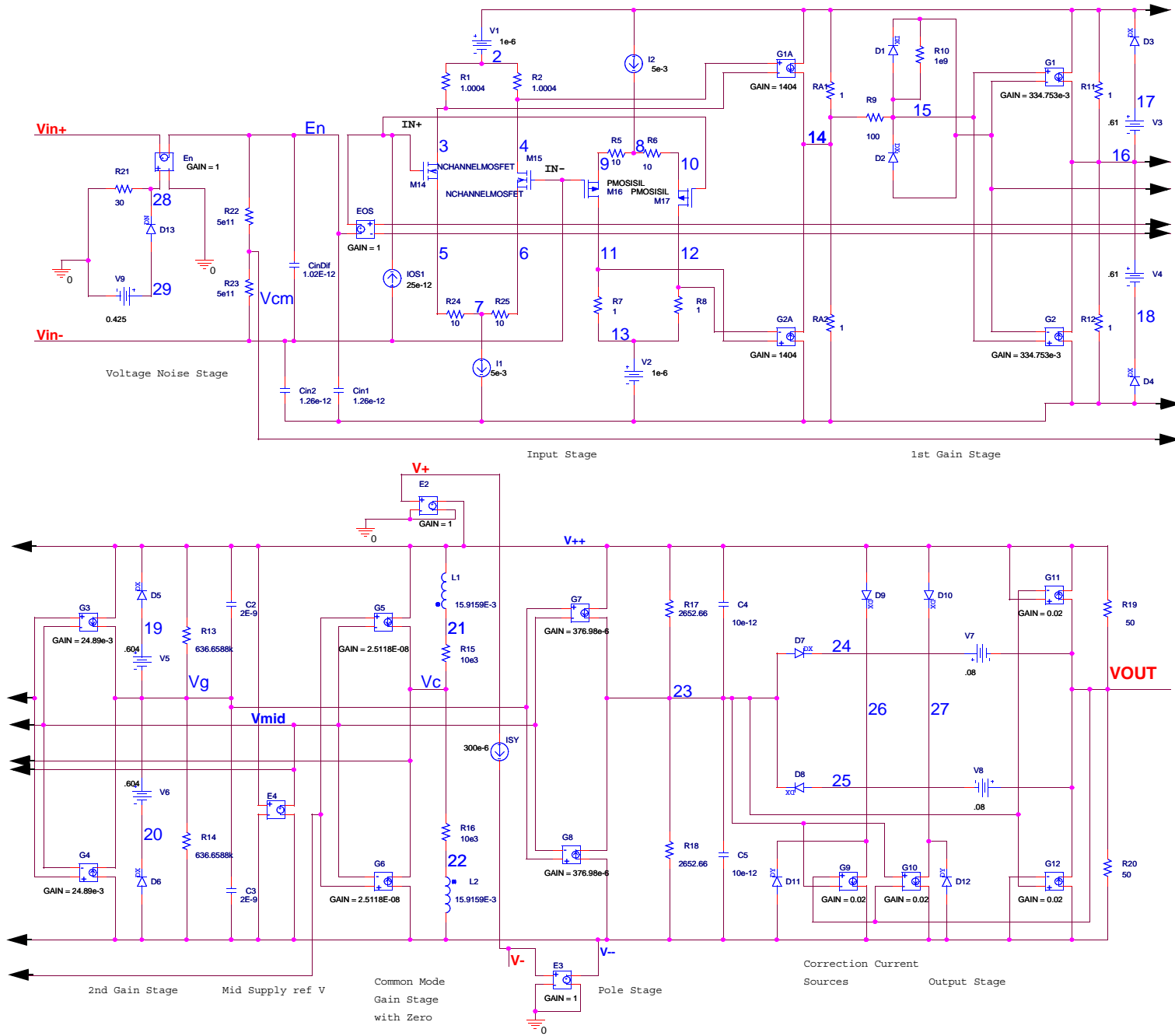


FIGURE 21. SPICE SCHEMATIC

ISL28114, ISL28214, ISL28414

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*ISL28114 Macromodel - covers following
*products
*ISL28114
*ISL28214
*ISL28414
*
*Revision History:
*Revision B, LaFontaine March 25th 2011
*Model for Noise, quiescent supply currents,
*CMRR 72dB
*fcm=100kHz ,AVOL 90dB f=125Hz SR =
*2.5V/us, GBWP 5MHz, 2nd pole 6Mhz
output *voltage clamp and short ckt current
limit.
*
*Copyright 2011 by Intersil Corporation
*Refer to data sheet "LICENSE
STATEMENT" *Use of this model indicates
your acceptance *with the terms and
provisions in the License *Statement.
*
*Intended use:
*This Pspice Macromodel is intended to give
*typical DC and AC performance
*characteristics under a wide range of
external *circuit configurations using
compatible *simulation platforms - such as
iSim PE.
*
*Device performance features supported by
this *model
*Typical, room temp., nominal power supply
*voltages used to produce the following
*characteristics:
*Open and closed loop I/O impedances
*Open loop gain and phase
*Closed loop bandwidth and frequency
*response
*Loading effects on closed loop frequency
*response
*Input noise terms including 1/f effects
*Slew rate
*Input and Output Headroom limits to I/O
*voltage swing
*Supply current at nominal specified supply
*voltages
*
*Device performance features NOT
supported *by this model
*Harmonic distortion effects
*Disable operation (if any)
*Thermal effects and/or over temperature
*parameter variation
*Limited performance variation vs. supply
*voltage is modeled
*Part to part performance variation due to
*normal process parameter spread
*Any performance difference arising from
*different packaging
* source
* Connections:  +input
*               |
*               | -input
*               | | +Vsupply
*               | | |
*               | | | -Vsupply
*               | | | |
*               | | | | output
*               | | | | |
*               | | | | |
*
.subckt ISL28114 Vin+ Vin-V+ V- VOUT
* source ISL28114_DS rev1
*
*Voltage Noise
E_En  VIN+ EN 28 0 1
D_D13 29 28 DN
V_V9 29 0 0.425
R_R21 28 0 30
*
*Input Stage
M_M14 3 1 5 5 NCHANNELMOSFET
M_M15 4 VIN- 6 6 NCHANNELMOSFET
*
M_M16 11 VIN- 9 9 PMOSISIL
M_M17 12 1 10 10 PMOSISIL
L_L1 7 V-- DC 5e-3
L_L2 22 V-- DC 5e-3
L_IOS VIN- 1 DC 25e-12
G_G1A V++ 14 4 3 1404
G_G2A V-- 14 11 12 1404
V_V1 V++ 2 1e-6
V_V2 13 V-- 1e-6
R_R1 3 2 1.0004
R_R2 4 2 1.0004
R_R3 5 7 10
R_R4 7 6 10
R_R5 9 8 10
R_R6 8 10 10
R_R7 13 11 1
R_R8 13 12 1
R_RA1 14 V++ 1
R_RA2 V-- 14 1
C_CinDif VIN- EN 1.02E-12
C_Cin1 V-- EN 1.26e-12
C_Cin2 V-- VIN- 1.26e-12
*
*1st Gain Stage
G_G1 V++ 16 15 VMID 334.753e-3
G_G2 V-- 16 15 VMID 334.753e-3
V_V3 17 16 .61
V_V4 16 18 .61
D_D1 15 VMID DX
D_D2 VMID 15 DX
D_D3 17 V++ DX
D_D4 V-- 18 DX
R_R9 15 14 100
R_R10 15 VMID 1e9
R_R11 16 V++ 1
R_R12 V-- 16 1
*
*2nd Gain Stage
G_G3 V++ VG 16 VMID 24.893e-3
G_G4 V-- VG 16 VMID 24.893e-3
V_V5 19 VG .604
V_V6 VG 20 .604
D_D5 19 V++ DX
D_D6 V-- 20 DX
R_R13 VG V++ 636.658e3
R_R14 V-- VG 636.658e3
C_C2 VG V++ 2E-09
C_C3 V-- VG 2E-09
*
*Mid supply Ref
E_E4 VMID V-- V++ V-- 0.5
E_E2 V++ 0 V+ 0 1
E_E3 V-- 0 V- 0 1
L_ISY V+ V- DC 300e-6
*
*Common Mode Gain Stage with Zero
G_G5 V++ VC VCM VMID 2.5118E-8
G_G6 V-- VC VCM VMID 2.5118E-8
E_EOS 1 EN VC VMID 1
R_R15 VC 21 10e3
R_R16 22 VC 10e3
R_R22 EN VCM 5e11
R_R23 VCM VIN- 5e11
L_L1 21 V++ 15.9159e-3
L_L2 22 V-- 15.9159e-3
*
*Pole Stage
G_G7 V++ 23 VG VMID 376.98e-6
G_G8 V-- 23 VG VMID 376.98e-6
R_R17 23 V++ 2652.66
R_R18 V-- 23 2652.66
C_C4 23 V++ 10e-12
C_C5 V-- 23 10e-12
*
*Output Stage with Correction Current
Sources
G_G9 26 V-- VOUT 23 0.02
G_G10 27 V-- 23 VOUT 0.02
G_G11 VOUT V++ V++ 23 0.02
G_G12 V-- VOUT 23 V-- 0.02
V_V7 24 VOUT .08
V_V8 VOUT 25 .08
D_D7 23 24 DX
D_D8 25 23 DX
D_D9 V++ 26 DX
D_D10 V++ 27 DX
D_D11 V-- 26 DY
D_D12 V-- 27 DY
R_R19 VOUT V++ 50
R_R20 V-- VOUT 50
.model pmosil pmos (kp=16e-3 vto=-0.6)
.model NCHANNELMOSFET nmos (kp=3e-3
vto=0.6)
.model DN D(KF=6.69e-9 AF=1)
.MODEL DX D(IS=1E-12 Rs=0.1)
.MODEL DY D(IS=1E-15 BV=50 Rs=1)
.ends ISL28114

```

FIGURE 22. SPICE NET LIST

Characterization vs Simulation Results

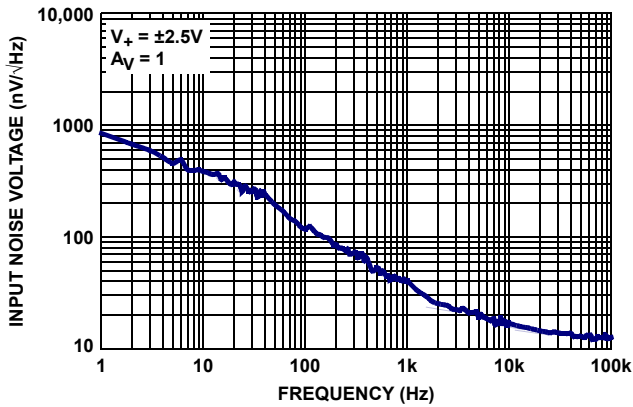


FIGURE 23. CHARACTERIZED INPUT NOISE VOLTAGE

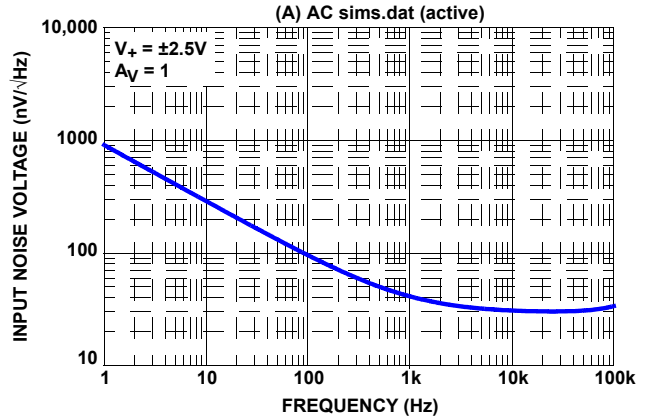


FIGURE 24. SIMULATED INPUT NOISE VOLTAGE

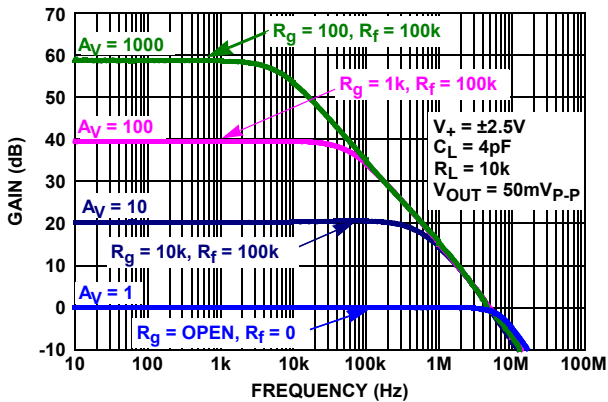


FIGURE 25. CHARACTERIZED CLOSED LOOP GAIN vs FREQUENCY

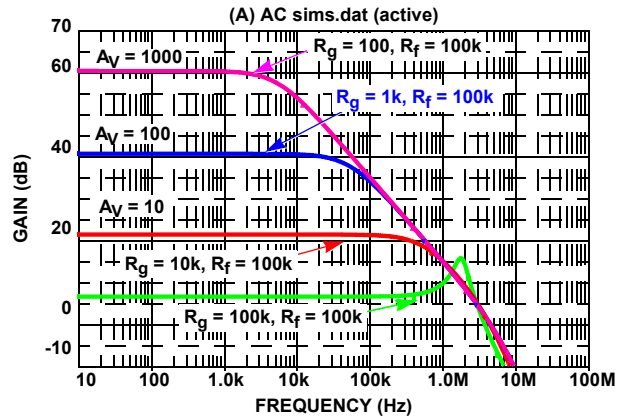


FIGURE 26. SIMULATED CLOSED LOOP GAIN vs FREQUENCY

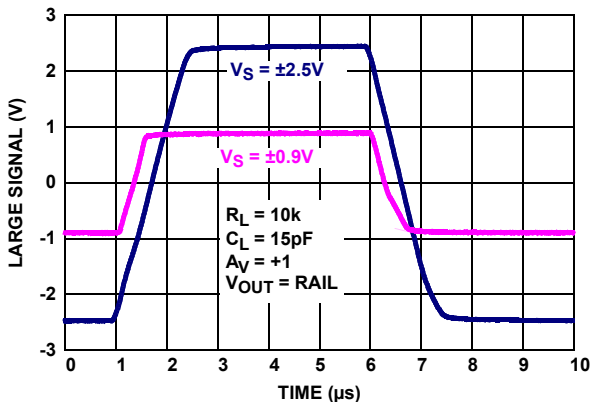


FIGURE 27. CHARACTERIZED LARGE SIGNAL TRANSIENT RESPONSE vs R_L , $V_S = \pm 0.9V, \pm 2.5V$

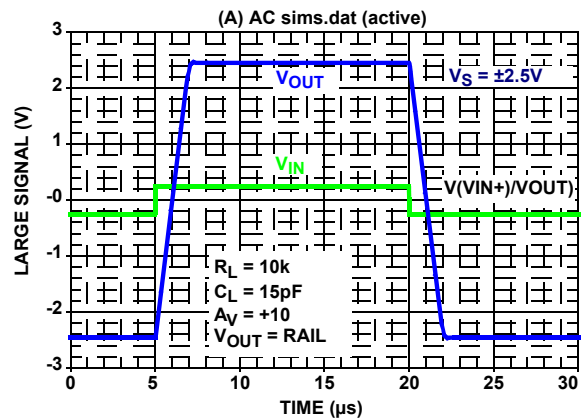


FIGURE 28. SIMULATED LARGE SIGNAL TRANSIENT RESPONSE vs R_L , $V_S = \pm 0.9V, \pm 2.5V$

Characterization vs Simulation Results (Continued)

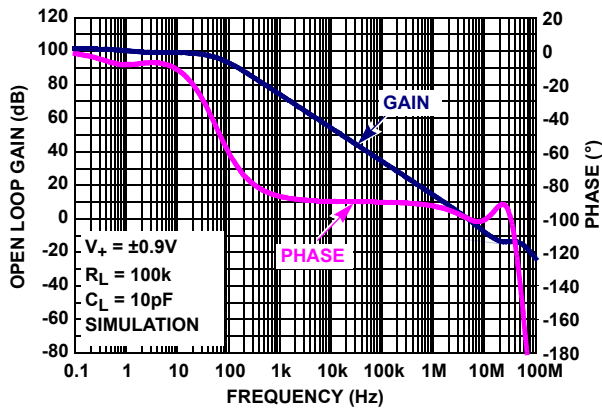


FIGURE 29. SIMULATED (DESIGN) OPEN-LOOP GAIN, PHASE vs FREQUENCY

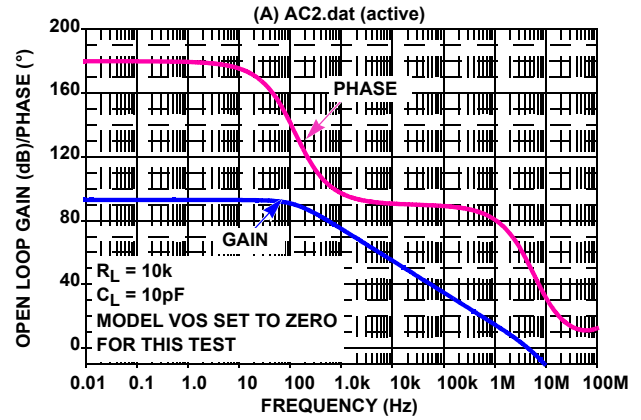


FIGURE 30. SIMULATED (SPICE) OPEN-LOOP GAIN, PHASE vs FREQUENCY

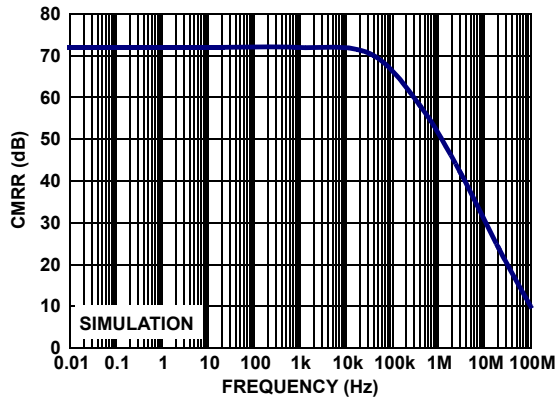


FIGURE 31. SIMULATED (DESIGN) CMRR

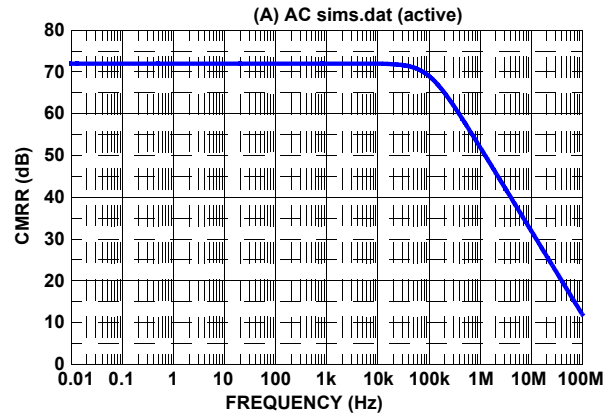


FIGURE 32. SIMULATED (SPICE) CMRR

ISL28114, ISL28214, ISL28414

Revision History

The revision history provided is for informational purposes only and is believed to be accurate, but not warranted. Please go to Web to make sure you have the latest Rev.

| DATE | REVISION | CHANGE |
|----------|----------|--|
| 5/18/11 | FN6800.5 | <ul style="list-style-type: none"> - On page 3, Pin Descriptions: Circuit 3 diagram, removed anti-parallel diodes from the IN+ to IN- terminals. - On page 4, Absolute Maximum Ratings: changed Differential Input Voltage from "0.5V" to "V- - 0.5V to V+ + 0.5V" - On page 4, updated CMRR and PSRR parameters in Electrical Specifications table with test condition specifying -40°C to 125°C typical parameter. - On page 5, updated Note 7, referenced in MIN and MAX column headings of Electrical Specifications table, from "Parameters with MIN and/or MAX limits are 100% tested at +25°C, unless otherwise specified. Temperature limits established by characterization and are not production tested." to new standard "Compliance to datasheet limits is assured by one or more methods: production test, characterization and/or design." - On page 9, under "Input ESD Diode Protection," removed "They also contain back to-back diodes across the input terminals." Removed "Although the amplifier is fully protected, high input slew rates that exceed the amplifier slew rate ($\pm 2.5V/\mu s$) may cause output distortion." - On page 9, Figure 19: updated circuit schematic by removing back-to-back input protection diodes. - On page 11 replaced SPICE schematic (Figure 21) - On page 12 replaced SPICE Netlist (Figure 22) - On page 13 replaced Figure 24 - On page 14 replaced Figure 32 |
| 9/23/10 | FN6800.4 | <p>Added new SC70 pinout package extension as follows: Added to Related Literature on page 1 "See AN1547 for "ISL28414TSSOPEVAL1Z Evaluation Board User's Guide". Added to ordering information ISL28114FEV1Z-T7 and ISL28114FEV1Z-T7A and Evaluation boards. Added to Pin Configurations new pinout for ISL28114FEV1Z. Added in Pin Descriptions ISL28114FEV1Z SC70 pin description column.</p> |
| 7/28/10 | | <p>Changed Note 6 on page page 4 from "For θ_{JC}, the "case temp" location is the center of the exposed metal pad on the package underside." to "For θ_{JC}, the "case temp" location is taken at the package top center."</p> |
| 5/13/10 | | <p>Added "Related Literature" on page 1. Changed package outline drawing from MDP0038 to P5.064A on page 2 and page 18. MDP0038 package contained 2 packages for both the 5 and 6 Ld SOT-23. MDP0038 was obsoleted and the packages were separated and made into 2 separate package outline drawings; P5.064A and P6.064A. Changes to the 5 Ld SOT-23 were to move dimensions from table onto drawing, add land pattern and add JEDEC reference number. Added Note 4 to "Ordering Information" on page 2.</p> |
| 12/16/09 | FN6800.3 | <p>Removed "Coming Soon" from MSOP package options in the "Ordering Information" on page 2. Updated the Theta JA for the MSOP package option from 170°C/W to 180°C/W on page 4.</p> |
| 11/17/09 | FN6800.2 | <p>Removed "Coming Soon" from SC70 and SOT-23 package options in the "Ordering Information" on page 2.</p> |
| 11/12/09 | FN6800.1 | <p>Changed theta Ja to 250 from 300. Added license statement (page 10) and reference in spice model (page 12).</p> |
| 10/23/09 | FN6800.0 | <p>Initial Release</p> |

ISL28114, ISL28214, ISL28414

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*For a complete listing of Applications, Related Documentation and Related Parts, please see the respective device information page on intersil.com: [ISL28114](#), [ISL28214](#), [ISL28414](#)

To report errors or suggestions for this datasheet, please go to www.intersil.com/askourstaff

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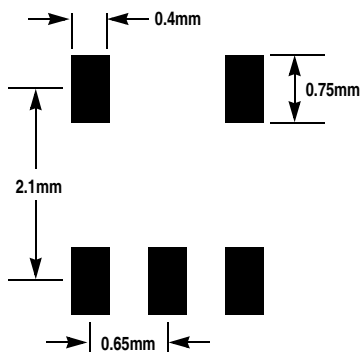
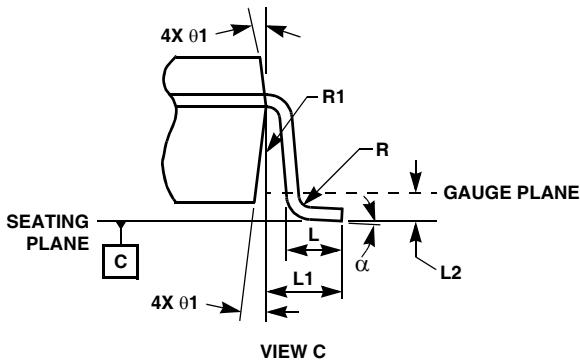
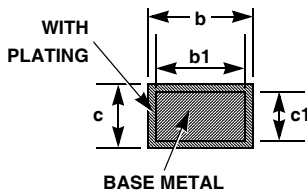
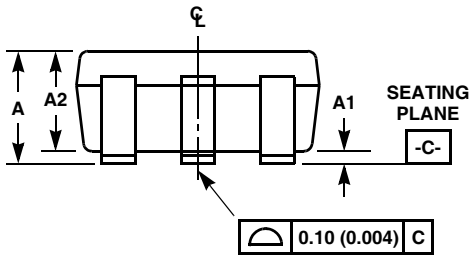
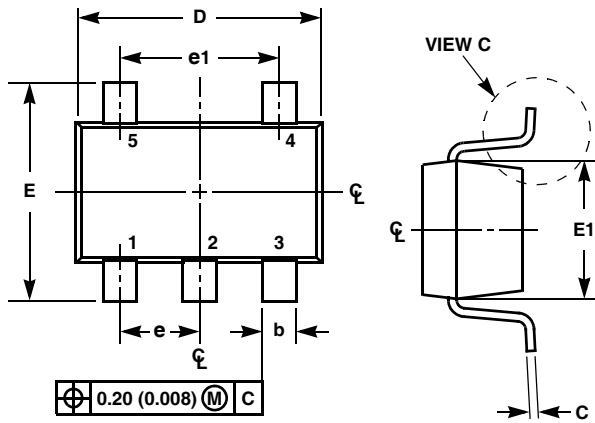
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ISL28114, ISL28214, ISL28414

Small Outline Transistor Plastic Packages (SC70-5)



TYPICAL RECOMMENDED LAND PATTERN

P5.049

5 LEAD SMALL OUTLINE TRANSISTOR PLASTIC PACKAGE

| SYMBOL | INCHES | | MILLIMETERS | | NOTES |
|--------|------------|-------|-------------|------|-------|
| | MIN | MAX | MIN | MAX | |
| A | 0.031 | 0.043 | 0.80 | 1.10 | - |
| A1 | 0.000 | 0.004 | 0.00 | 0.10 | - |
| A2 | 0.031 | 0.039 | 0.80 | 1.00 | - |
| b | 0.006 | 0.012 | 0.15 | 0.30 | - |
| b1 | 0.006 | 0.010 | 0.15 | 0.25 | - |
| c | 0.003 | 0.009 | 0.08 | 0.22 | 6 |
| c1 | 0.003 | 0.009 | 0.08 | 0.20 | 6 |
| D | 0.073 | 0.085 | 1.85 | 2.15 | 3 |
| E | 0.071 | 0.094 | 1.80 | 2.40 | - |
| E1 | 0.045 | 0.053 | 1.15 | 1.35 | 3 |
| e | 0.0256 Ref | | 0.65 Ref | | - |
| e1 | 0.0512 Ref | | 1.30 Ref | | - |
| L | 0.010 | 0.018 | 0.26 | 0.46 | 4 |
| L1 | 0.017 Ref. | | 0.420 Ref. | | - |
| L2 | 0.006 BSC | | 0.15 BSC | | - |
| α | 0° | 8° | 0° | 8° | - |
| N | 5 | | 5 | | 5 |
| R | 0.004 | - | 0.10 | - | - |
| R1 | 0.004 | 0.010 | 0.15 | 0.25 | - |

Rev. 3 7/07

NOTES:

1. Dimensioning and tolerances per ASME Y14.5M-1994.
2. Package conforms to EIAJ SC70 and JEDEC MO-203AA.
3. Dimensions D and E1 are exclusive of mold flash, protrusions, or gate burrs.
4. Footlength L measured at reference to gauge plane.
5. "N" is the number of terminal positions.
6. These Dimensions apply to the flat section of the lead between 0.08mm and 0.15mm from the lead tip.
7. Controlling dimension: MILLIMETER. Converted inch dimensions are for reference only.

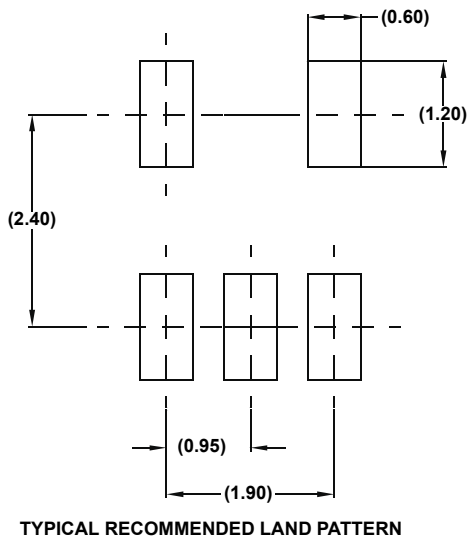
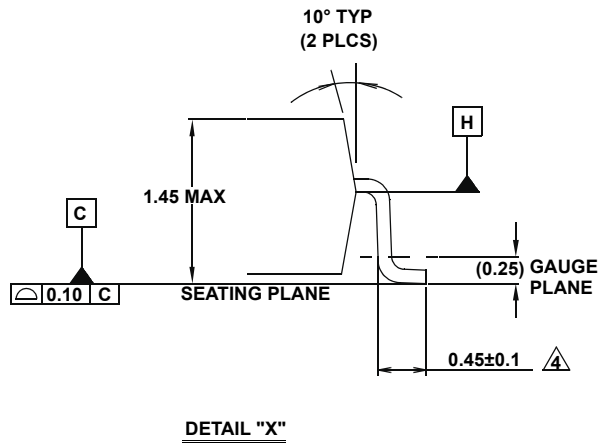
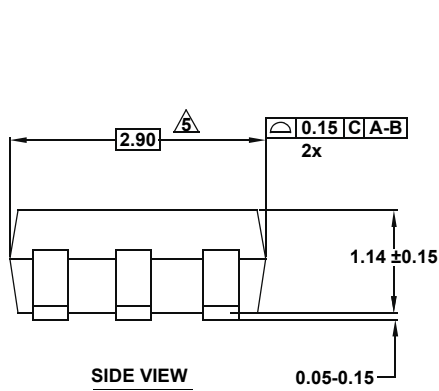
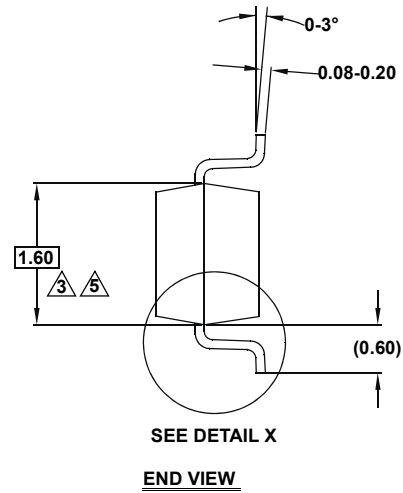
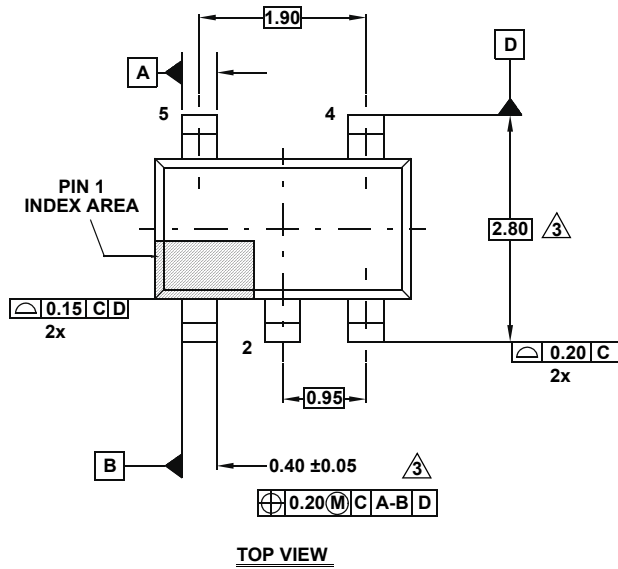
ISL28114, ISL28214, ISL28414

Package Outline Drawing

P5.064A

5 LEAD SMALL OUTLINE TRANSISTOR PLASTIC PACKAGE

Rev 0, 2/10



NOTES:

1. Dimensions are in millimeters.
Dimensions in () for Reference Only.
2. Dimensioning and tolerancing conform to ASME Y14.5M-1994.
3. Dimension is exclusive of mold flash, protrusions or gate burrs.
4. Foot length is measured at reference to gauge plane.
5. This dimension is measured at Datum "H".
6. Package conforms to JEDEC MO-178AA.

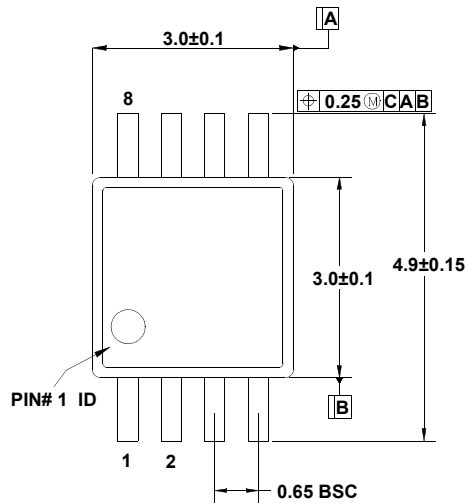
ISL28114, ISL28214, ISL28414

Package Outline Drawing

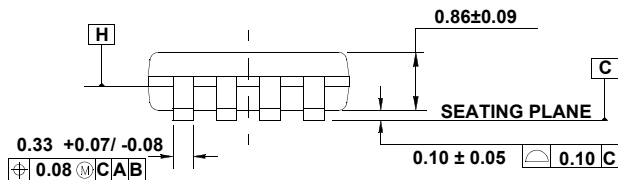
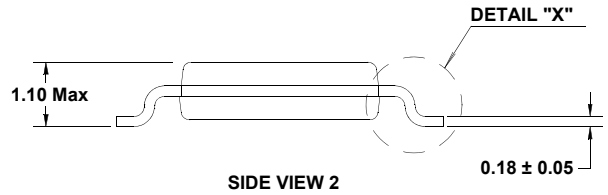
M8.118A

8 LEAD MINI SMALL OUTLINE PLASTIC PACKAGE (MSOP)

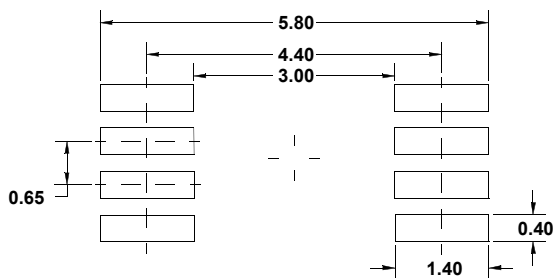
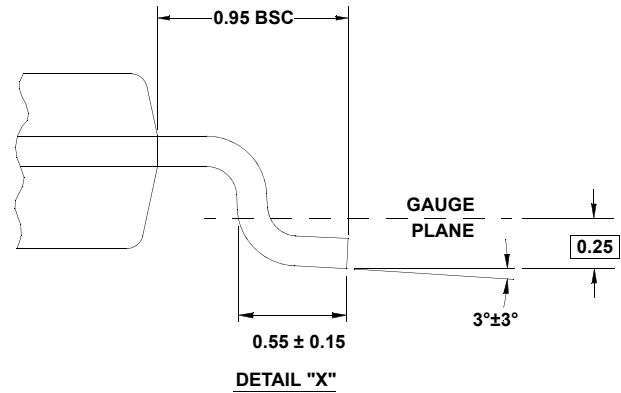
Rev 0, 9/09



TOP VIEW



SIDE VIEW 1



TYPICAL RECOMMENDED LAND PATTERN

NOTES:

1. Dimensions are in millimeters.
2. Dimensioning and tolerancing conform to JEDEC MO-187-AA and AMSE Y14.5m-1994.
3. Plastic or metal protrusions of 0.15mm max per side are not included.
4. Plastic interlead protrusions of 0.25mm max per side are not included.
5. Dimensions "D" and "E1" are measured at Datum Plane "H".
6. This replaces existing drawing # MDP0043 MSOP 8L.

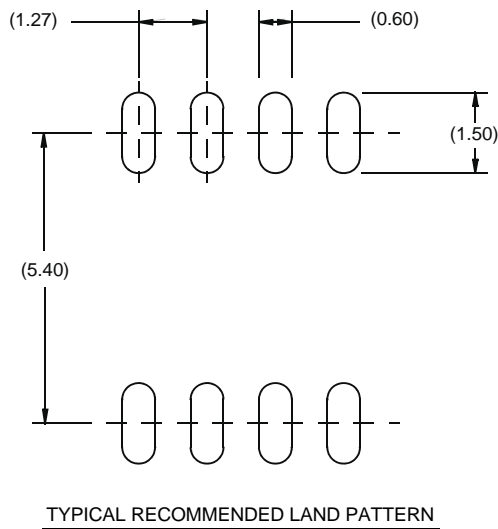
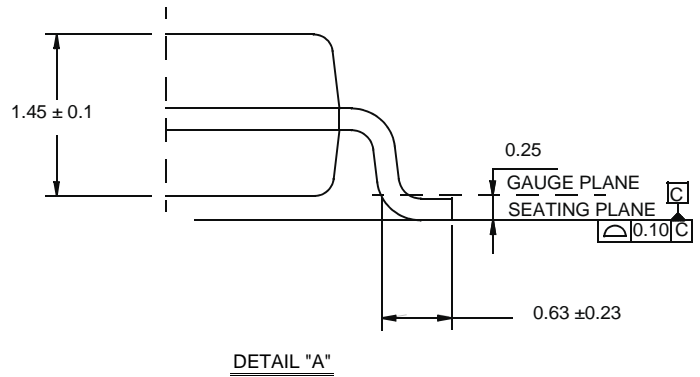
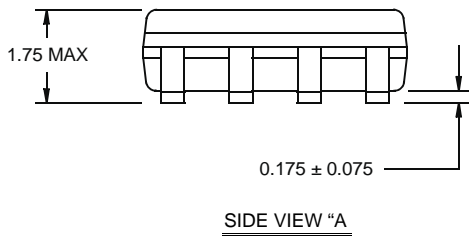
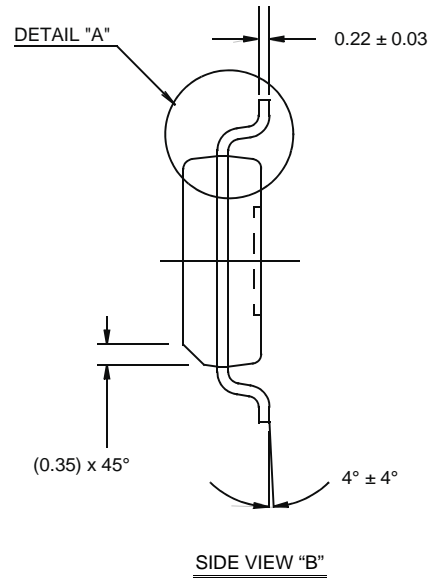
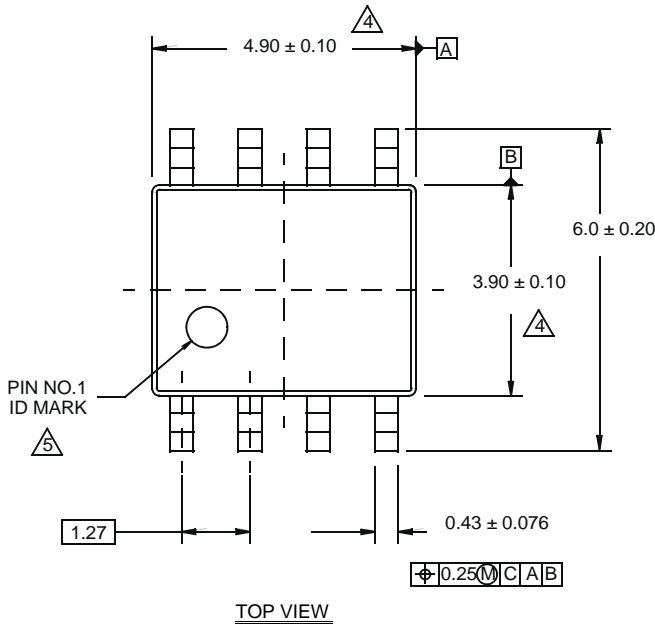
ISL28114, ISL28214, ISL28414

Package Outline Drawing

M8.15E

8 LEAD NARROW BODY SMALL OUTLINE PLASTIC PACKAGE

Rev 0, 08/09

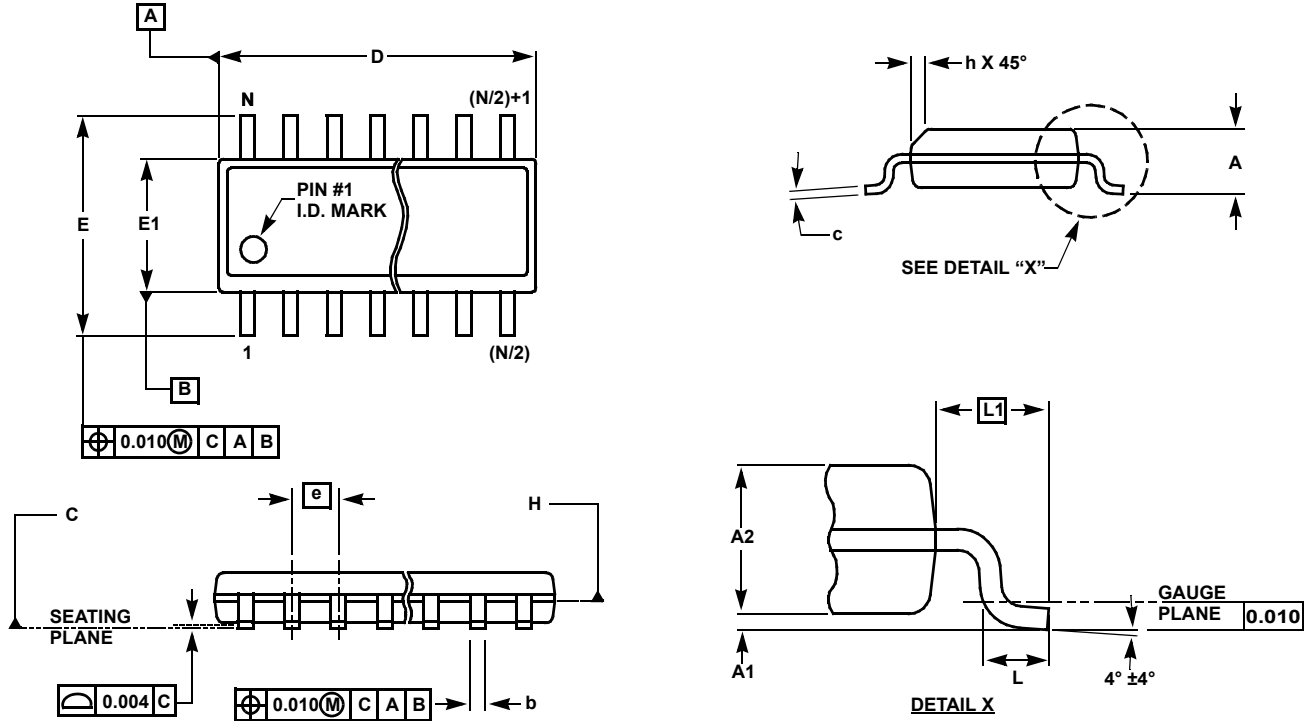


NOTES:

1. Dimensions are in millimeters.
Dimensions in () for Reference Only.
2. Dimensioning and tolerancing conform to AMSE Y14.5m-1994.
3. Unless otherwise specified, tolerance : Decimal ± 0.05
4. Dimension does not include interlead flash or protrusions.
Interlead flash or protrusions shall not exceed 0.25mm per side.
5. The pin #1 identifier may be either a mold or mark feature.
6. Reference to JEDEC MS-012.

ISL28114, ISL28214, ISL28414

Small Outline Package Family (SO)



MDP0027

SMALL OUTLINE PACKAGE FAMILY (SO)

| SYMBOL | INCHES | | | | | | | TOLERANCE | NOTES |
|--------|--------|-------|------------------|---------------------------|------------------|------------------|------------------|-----------|-------|
| | SO-8 | SO-14 | SO16 (0.150") | SO16 (0.300") (SOL-16) | SO20 (SOL-20) | SO24 (SOL-24) | SO28 (SOL-28) | | |
| A | 0.068 | 0.068 | 0.068 | 0.104 | 0.104 | 0.104 | 0.104 | MAX | - |
| A1 | 0.006 | 0.006 | 0.006 | 0.007 | 0.007 | 0.007 | 0.007 | ±0.003 | - |
| A2 | 0.057 | 0.057 | 0.057 | 0.092 | 0.092 | 0.092 | 0.092 | ±0.002 | - |
| b | 0.017 | 0.017 | 0.017 | 0.017 | 0.017 | 0.017 | 0.017 | ±0.003 | - |
| c | 0.009 | 0.009 | 0.009 | 0.011 | 0.011 | 0.011 | 0.011 | ±0.001 | - |
| D | 0.193 | 0.341 | 0.390 | 0.406 | 0.504 | 0.606 | 0.704 | ±0.004 | 1, 3 |
| E | 0.236 | 0.236 | 0.236 | 0.406 | 0.406 | 0.406 | 0.406 | ±0.008 | - |
| E1 | 0.154 | 0.154 | 0.154 | 0.295 | 0.295 | 0.295 | 0.295 | ±0.004 | 2, 3 |
| e | 0.050 | 0.050 | 0.050 | 0.050 | 0.050 | 0.050 | 0.050 | Basic | - |
| L | 0.025 | 0.025 | 0.025 | 0.030 | 0.030 | 0.030 | 0.030 | ±0.009 | - |
| L1 | 0.041 | 0.041 | 0.041 | 0.056 | 0.056 | 0.056 | 0.056 | Basic | - |
| h | 0.013 | 0.013 | 0.013 | 0.020 | 0.020 | 0.020 | 0.020 | Reference | - |
| N | 8 | 14 | 16 | 16 | 20 | 24 | 28 | Reference | - |

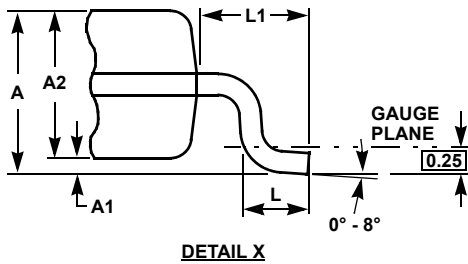
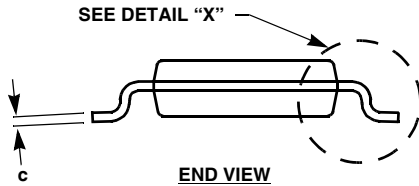
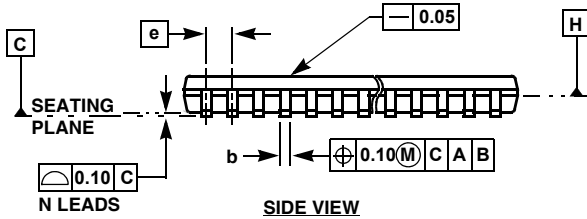
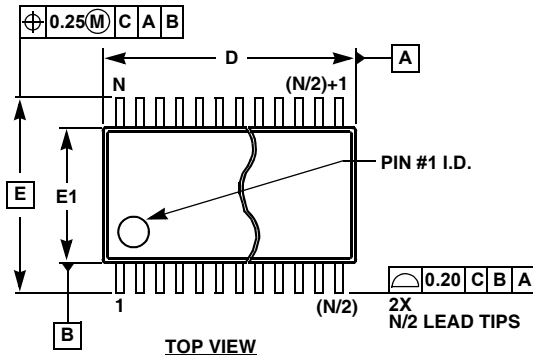
Rev. M 2/07

NOTES:

1. Plastic or metal protrusions of 0.006" maximum per side are not included.
2. Plastic interlead protrusions of 0.010" maximum per side are not included.
3. Dimensions "D" and "E1" are measured at Datum Plane "H".
4. Dimensioning and tolerancing per ASME Y14.5M-1994

ISL28114, ISL28214, ISL28414

Thin Shrink Small Outline Package Family (TSSOP)



MDP0044

THIN SHRINK SMALL OUTLINE PACKAGE FAMILY

| SYMBOL | MILLIMETERS | | | | | TOLERANCE |
|--------|-------------|-------|-------|-------|-------|-------------|
| | 14 LD | 16 LD | 20 LD | 24 LD | 28 LD | |
| A | 1.20 | 1.20 | 1.20 | 1.20 | 1.20 | Max |
| A1 | 0.10 | 0.10 | 0.10 | 0.10 | 0.10 | ±0.05 |
| A2 | 0.90 | 0.90 | 0.90 | 0.90 | 0.90 | ±0.05 |
| b | 0.25 | 0.25 | 0.25 | 0.25 | 0.25 | +0.05/-0.06 |
| c | 0.15 | 0.15 | 0.15 | 0.15 | 0.15 | +0.05/-0.06 |
| D | 5.00 | 5.00 | 6.50 | 7.80 | 9.70 | ±0.10 |
| E | 6.40 | 6.40 | 6.40 | 6.40 | 6.40 | Basic |
| E1 | 4.40 | 4.40 | 4.40 | 4.40 | 4.40 | ±0.10 |
| e | 0.65 | 0.65 | 0.65 | 0.65 | 0.65 | Basic |
| L | 0.60 | 0.60 | 0.60 | 0.60 | 0.60 | ±0.15 |
| L1 | 1.00 | 1.00 | 1.00 | 1.00 | 1.00 | Reference |

Rev. F 2/07

NOTES:

1. Dimension "D" does not include mold flash, protrusions or gate burrs. Mold flash, protrusions or gate burrs shall not exceed 0.15mm per side.
2. Dimension "E1" does not include interlead flash or protrusions. Interlead flash and protrusions shall not exceed 0.25mm per side.
3. Dimensions "D" and "E1" are measured at dAtum Plane H.
4. Dimensioning and tolerancing per ASME Y14.5M-1994.