**Revision History :**

Revision 1.0 (Jul. 5, 2007)
- Original

# PSRAM 8-Mbit (512K x 16) Pseudo Static RAM

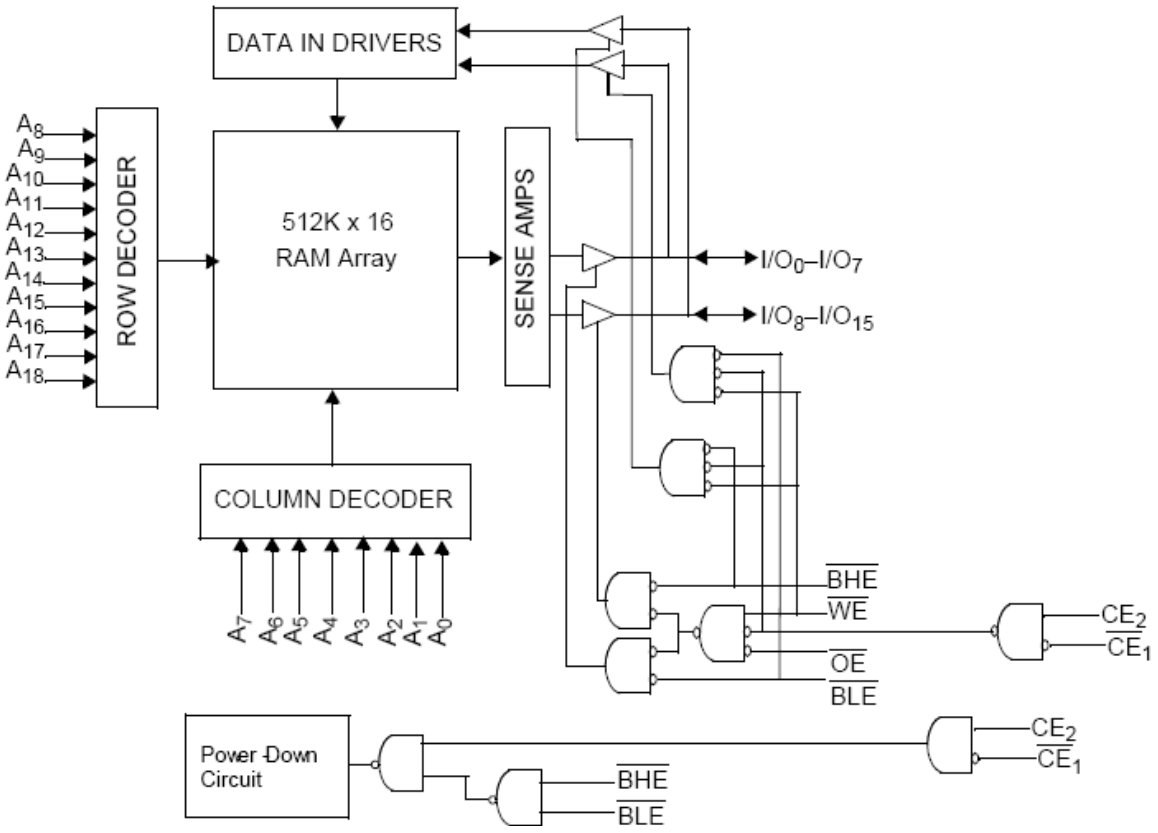
## Features

- Wide voltage range: 1.7V–1.95V
- Access Time: 55 ns, 70 ns
- Ultra-low active power
— Typical active current: 3 mA @ f = 1 MHz
— Typical active current: 20 mA @ f = fmax
- Ultra low standby power
- Automatic power-down when deselected
- CMOS for optimum speed/power
- Offered in a 48-ball BGA Package
- Operating Temperature: –40°C to +85°C

## Functional Description[1]

The M24D816512DA is a high-performance CMOS Pseudo Static RAM organized as 512K words by 16 bits that supports an asynchronous memory interface. This device features advanced circuit design to provide ultra-low active current. This is ideal for portable applications such as cellular telephones. The device can be put into standby mode when deselected ( $\overline{CE}$1 HIGH or CE2 LOW or both $\overline{BHE}$ and $\overline{BLE}$ are HIGH). The input/output pins (I/O0 through $I/O_{15}$) are placed in a high-impedance state when: deselected ( $\overline{CE}$1 HIGH or CE2 LOW), outputs are disabled ( $\overline{OE}$ HIGH), both Byte High Enable and Byte Low Enable are disabled ( $\overline{BHE}$ , $\overline{BLE}$ HIGH), or during a write operation ( $\overline{CE}$1 LOW and CE2 HIGH and $\overline{WE}$ LOW). Writing to the device is accomplished by taking Chip Enable( $\overline{CE}$1 LOW and CE2 HIGH) and Write Enable ( $\overline{WE}$ ) input LOW. If Byte Low Enable ( $\overline{BLE}$ ) is LOW, then data from I/O pins (I/O0through I/O7), is written into the location specified on the address pins (A0 through A18). If Byte High Enable ( $\overline{BHE}$ ) is LOW, then data from I/O pins ($I/O_8$ through $I/O_{15}$) is written in to the location specified on the address pins ($A_0$ through $A_{18}$).Reading from the device is accomplished by taking Chip Enables ( $\overline{CE}$1 LOW and CE2 HIGH) and Output Enable ( $\overline{OE}$ )LOW while forcing the Write Enable ( $\overline{WE}$ ) HIGH. If Byte Low Enable ( $\overline{BLE}$ ) is LOW, then data from the memory location specified by the address pins will appear on $I/O_0$ to $I/O_7$. If Byte High Enable ( $\overline{BHE}$ ) is LOW, then data from memory will appear on $I/O_8$ to $I/O_{15}$. Refer to the truth table for a complete description of read and write modes..

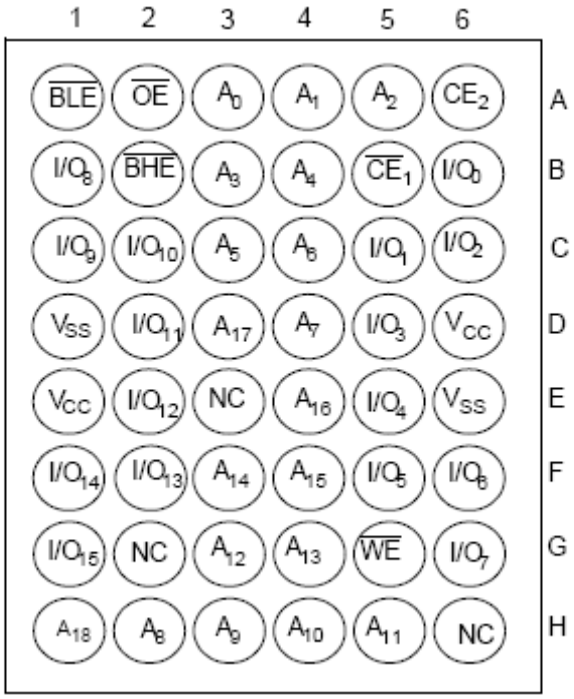
## Logic Block Diagram



Pin Configuration[2, 3]

48-Ball VFBGA

Top View



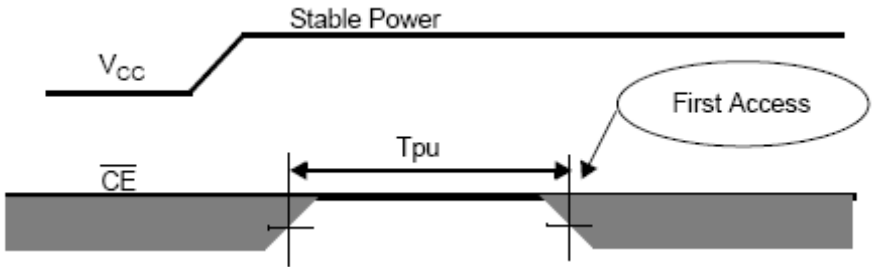

Product Portfolio [4]

| Product | $V_{CC}$ Range (V) | | | Speed(ns) | Power Dissipation | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|
| | | | | | Operating $I_{CC}$(Ma) | | | | Standby ISB2(μA) | |
| | | | | | f = 1MHz | | f = fmax | | | |
| | Min. | Typ.[4] | Max. | | .Typ.[4] | Max. | .Typ.[4] | Max. | .Typ. [4] | Max. |
| M24D816512DA | 1.7 | 1.8 | 1.95 | 55 | 3 | 5 | 20 | 35 | 32 | 70 |
| | | | | 70 | | | 18 | 25 | | |

Note:
2.Ball G2, H6 and E3 can be used to upgrade to a 16-Mbit, 32-Mbit and a 64-Mbit density, respectively.
3.NC “no connect” - not connected internally to the die.
4.Typical values are included for reference only and are not guaranteed or tested. Typical values are measured at $V_{CC}$ = $V_{CC}$ (typ) and $T_A$ = 25°C. Tested initially and after design changes that may affect the parameters.

## Power-up Characteristics

The initialization sequence is shown in Figure1. Chip Select should be $\overline{CE}1$ HIGH or CE2 LOW for at least 200 µs after $V_{CC}$ has reached a stable value. No access must be attempted during this period of 200 µs.




| Parameter | Description | Min. | Typ. | Max. | Unit |
|---|---|---|---|---|---|
| Tpu | $\overline{CE}1$ LOW and CE2 HIGH After Stable $V_{CC}$ | 200 | | | µs |

## Maximum Ratings

(Above which the useful life may be impaired. For user guide-lines, not tested.)
Storage Temperature .....–65°C to +150°C
Ambient Temperature with
Power Applied .....–55°C to +125°C
Supply Voltage to
Ground Potential . .....−0.2V to $V_{CCMAX}$ + 0.3V
DC Voltage Applied to Outputs
in High-Z State[5, 6, 7] ..... −0.2V to $V_{CCMAX}$ + 0.3V
DC Input Voltage[5, 6, 7]..... −0.2V to $V_{CCMAX}$ + 0.3V
Output Current into Outputs (LOW) .....20 mA

Static Discharge Voltage ..... >2001V
(per MIL-STD-883, Method 3015)
Latch-up Current .....> 200 mA

## Operating Range

| Range | Ambient Temperature ($T_A$) | $V_{CC}$ |
|---|---|---|
| Industrial | −40°C to +85°C | 1.7V to 1.95V |

## DC Electrical Characteristics (Over the Operating Range)[5,6,7]

| Parameter | Description | Test Conditions | | -55 | | | -70 | | | Unit |
|---|---|---|---|---|---|---|---|---|---|---|
| | | | | Min. | Typ .[4] | Max. | Min. | Typ. [4] | Max. | |
| $V_{CC}$ | Supply Voltage | | | 2.7 | 1.8 | 1.95 | 1.7 | 1.8 | 1.95 | V |
| $V_{OH}$ | Output HIGH Voltage | $I_{OH}$ = −0.1 mA<br>$V_{CC}$ = 1.7V to 1.95V | | $V_{CC}$-0.2 | | | $V_{CC}$-0.2 | | | V |
| $V_{OL}$ | Output LOW Voltage | $I_{OL}$ = 0.1 mA<br>$V_{CC}$ = 1.7V to 1.95V | | | | 0.2 | | | 0.2 | V |
| $V_{IH}$ | Input HIGH Voltage | $V_{CC}$ = 1.7V to 1.95V | | 0.8* $V_{CC}$ | | $V_{CC}$+ 0.3V | 0.8* $V_{CC}$ | | $V_{CC}$ +0.3V | V |
| $V_{IL}$ | Input LOW Voltage | $V_{CC}$ = 1.7V to 1.95V | | -0.2 | | 0.2* $V_{CC}$ | -0.2 | | 0.2* $V_{CC}$ | V |
| $I_{IX}$ | Input Leakage Current | GND ≤$V_{IN}$ ≤ $V_{CC}$ | | -1 | | +1 | -1 | | +1 | µA |
| $I_{OZ}$ | Output Leakage Current | GND ≤ $V_{OUT}$ ≤ $V_{CC}$ | | -1 | | +1 | -1 | | +1 | µA |
| $I_{CC}$ | $V_{CC}$ Operating Supply Current | f = $f_{MAX}$ = 1/$t_{RC}$ | $V_{CC}$ = $V_{CCMAX}$<br>$I_{OUT}$ = 0mA<br>CMOS levels | | 20 | 35 | | 18 | 25 | mA |
| | | f = 1 MHz | | | 3 | 5 | | 3 | 5 | mA |
| $I_{SB2}$ | Automatic CE Power-Down Current —CMOS Inputs | $\overline{CE1}$ ≥ $V_{CC}$−0.2V or CE2 ≤ 0.2V<br>$V_{IN}$ ≥ $V_{CC}$ − 0.2V or $V_{IN}$ ≤ 0.2V,<br>f = 0, $V_{CC}$ = $V_{CCMAX}$ | | | 32 | 40 | | 32 | 40 | µA |

## Capacitance[8]

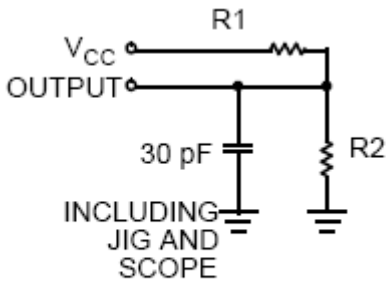
| Parameter | Description | Test Conditions | Max. | Unit |
|---|---|---|---|---|
| $C_{IN}$ | Input Capacitance | TA = 25°C, f = 1 MHz | 8 | pF |
| $C_{OUT}$ | Output Capacitance | $V_{CC}$ = $V_{CC(typ)}$ | 8 | pF |

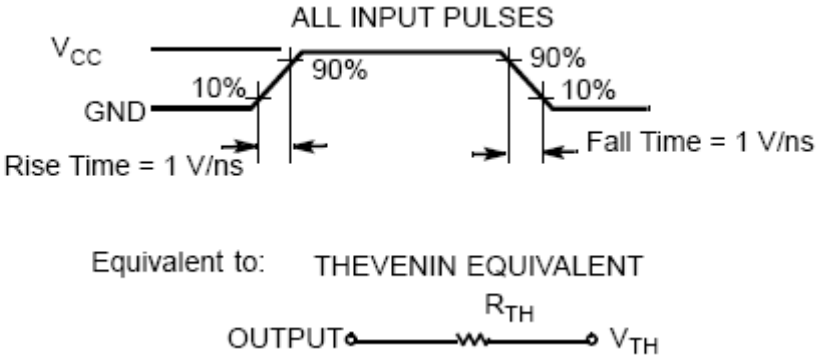
## Thermal Resistance[8]

| Parameter | Description | Test Conditions | BGA | Unit |
|---|---|---|---|---|
| ΘJA | Thermal Resistance(Junction to Ambient) | Test conditions follow standard test methods and procedures for measuring thermal impedance, per EIA/ JESD51. | 56 | °C/W |
| ΘJC | Thermal Resistance (Junction to Case) | | 11 | °C/W |

Notes:
5.$V_{IL(MIN)}$ = –0.5V for pulse durations less than 20 ns.
6.$V_{IH(Max)}$ = $V_{CC}$ + 0.5V for pulse durations less than 20 ns.
7.Overshoot and undershoot specifications are characterized and are not 100% tested.
8.Tested initially and after any design or process changes that may affect these parameters.

AC Test Loads and Waveforms




| Parameters | 1.8V ($V_{CC}$) | Unit |
|---|---|---|
| R1 | 14000 | Ω |
| R2 | 14000 | Ω |
| $R_{TH}$ | 7000 | Ω |
| $V_{TH}$ | 0.90 | V |

Switching Characteristics Over the Operating Range [9, 10, 11, 12]

| Parameter | Description | -55 | | -70 | | Unit |
|---|---|---|---|---|---|---|
| | | Min. | Max. | Min. | Max. | |
| Read Cycle | | | | | | |
| $t_{RC}$[14] | Read Cycle Time | 55 | 80000 | 70 | 80000 | ns |
| $t_{CD}$ [15] | Chip Deselect Time $\overline{CE1}$ = HIGH orCE2 = LOW, $\overline{BLE}$ / $\overline{BHE}$ High Pulse Time | 5 | | 5 | | ns |
| $t_{AA}$ | Address to Data Valid | | 55 | | 70 | ns |
| $t_{OHA}$ | Data Hold from Address Change | 5 | | 5 | | ns |
| $t_{ACE}$ | $\overline{CE1}$ LOW and CE2 HIGH to Data Valid | | 55 | | 70 | ns |
| $t_{DOE}$ | $\overline{OE}$ LOW to Data Valid | | 25 | | 35 | ns |
| $t_{LZOE}$ | $\overline{OE}$ LOW to Low Z[10, 11, 13] | 5 | | 5 | | ns |
| $t_{HZOE}$ | $\overline{OE}$ HIGH to High Z[10, 11, 13] | | 20 | | 25 | ns |
| $t_{LZCE}$ | $\overline{CE1}$ LOW and CE2 HIGH to Low Z[10, 11, 13] | 10 | | 10 | | ns |
| $t_{HZCE}$ | $\overline{CE1}$ HIGH or CE2 LOW to High Z[10, 11, 13] | | 20 | | 25 | ns |
| $t_{DBE}$ | $\overline{BLE}$ / $\overline{BHE}$ LOW to Data Valid | | 55 | | 70 | ns |
| $t_{LZBE}$ | $\overline{BLE}$ / $\overline{BHE}$ LOW to Low Z[10, 11, 13] | 5 | | 5 | | ns |
| $t_{HZBE}$ | $\overline{BLE}$ / $\overline{BHE}$ HIGH to Low Z[10, 11, 13] | | 20 | | 25 | ns |

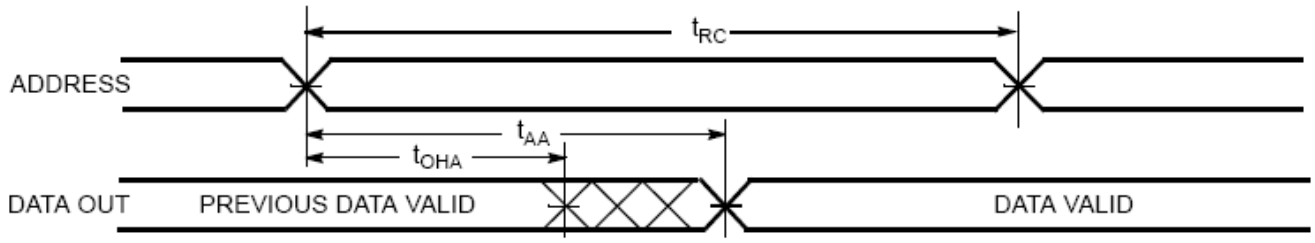
Notes:

9. Test conditions for all parameters other than tri-state parameters assume signal transition time of 1 ns/V, timing reference levels of $V_{CC(typ.)}/2$, input pulse levels of 0V to $V_{CC}$, and output loading of the specified $I_{OL}/I_{OH}$ as shown in the "AC Test Loads and Waveforms" section.
10. At any given temperature and voltage conditions $t_{HZCE}$ is less than $t_{LZCE}$, $t_{HZBE}$ is less than $t_{LZBE}$, $t_{HZOE}$ is less than $t_{LZOE}$, and $t_{HZWE}$ is less than $t_{LZWE}$ for any given device. All low-Z parameters will be measured with a load capacitance of 30 pF (3V)
11. $t_{HZOE}$, $t_{HZCE}$, $t_{HZBE}$, and $t_{HZWE}$ transitions are measured when the outputs enter a high-impedance state.
12. The internal Write time of the memory is defined by the overlap of $\overline{WE}$, $\overline{CE1}$ = $V_{IL}$ and CE2 = $V_{IH}$, $\overline{BHE}$ and/or $\overline{BLE}$ = $V_{IL}$. All signals must be ACTIVE to initiate a write and any of these signals can terminate a write by going INACTIVE. The data input set-up and hold timing should be referenced to the edge of the signal that terminates the write.
13. High-Z and Low-Z parameters are characterized and are not 100% tested.
14. If invalid address signals shorter than min. $t_{RC}$ are continuously repeated for 80 μs, the device needs a normal read timing ($t_{RC}$) or needs to enter standby state at least once in every 80 μs.
15. Whenever $\overline{CE1}$ = HIGH or CE2 = LOW, $\overline{BHE}$ / $\overline{BLE}$ are taken inactive, they must remain inactive for a minimum of 5 ns.

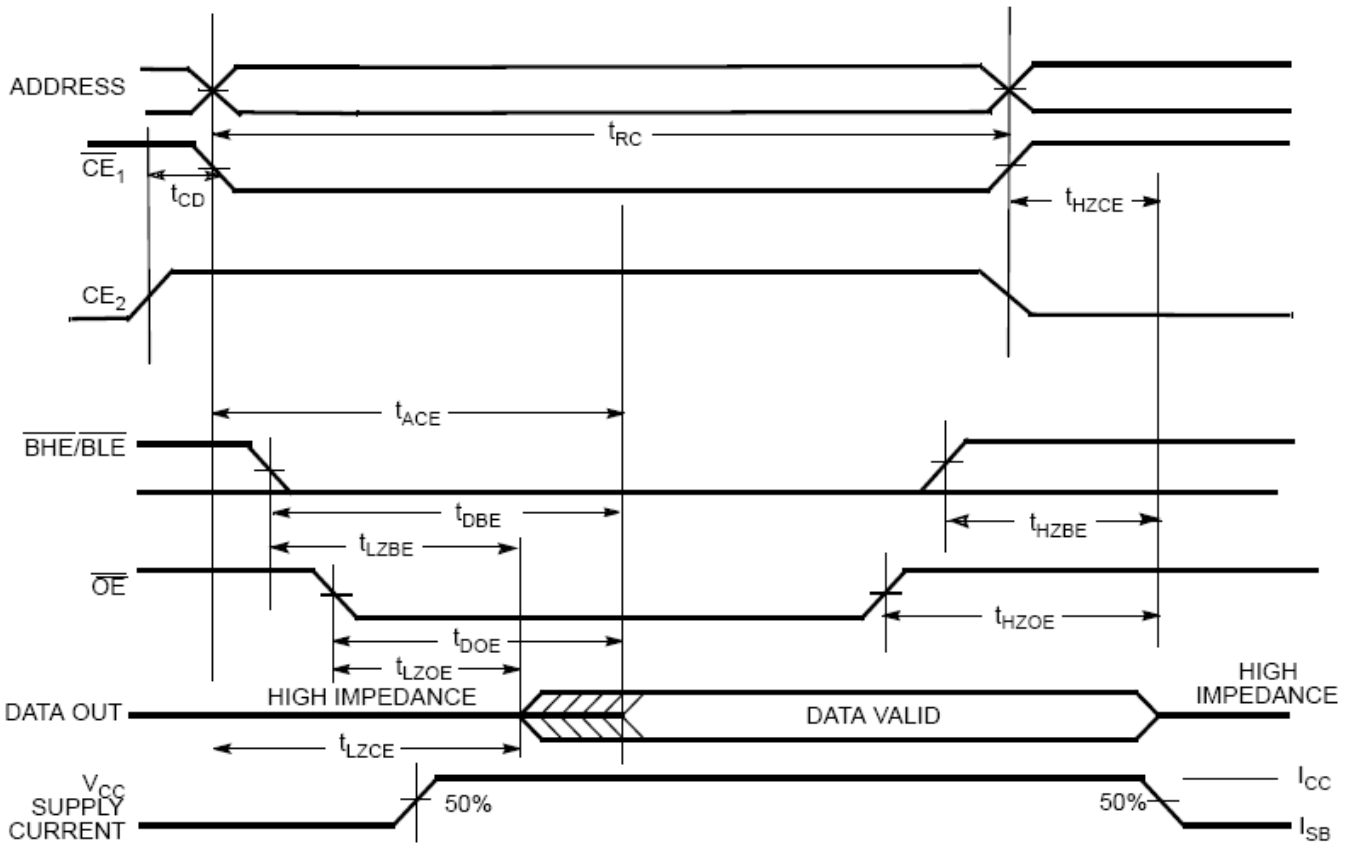
Switching Characteristics Over the Operating Range[9, 10, 11, 12] (continued)

| Parameter | Description | -55 | | -70 | | Unit |
|---|---|---|---|---|---|---|
| | | Min. | Max. | Min. | Max. | |
| Write Cycle [12] | | | | | | |
| $t_{WC}$ | Write Cycle Time | 50 | 80000 | 70 | 80000 | ns |
| $t_{SCE}$ | $\overline{CE1}$ LOW and CE2 HIGH to Write End | 50 | | 60 | | ns |
| $t_{AW}$ | Address Set-Up to Write End | 50 | | 60 | | ns |
| $t_{CD}$[15] | Chip Deselect Time $\overline{CE1}$ = HIGH or CE2 = LOW, $\overline{BLE}$ / $\overline{BHE}$ High Pulse Time | 5 | | 5 | | ns |
| $t_{HA}$ | Address Hold from Write End | 0 | | 0 | | ns |
| $t_{SA}$ | Address Set-Up to Write Start | 0 | | 0 | | ns |
| $t_{PWE}$ | $\overline{WE}$ Pulse Width | 45 | | 50 | | ns |
| $t_{BW}$ | $\overline{BLE}$ / $\overline{BHE}$ LOW to Write End | 50 | | 60 | | ns |
| $t_{SD}$ | Data Set-Up to Write End | 25 | | 25 | | ns |
| $t_{HD}$ | Data Hold from Write End | 0 | | 0 | | ns |
| $t_{HZWE}$ | $\overline{WE}$ LOW to High-Z[10, 11, 13] | | 20 | | 25 | ns |
| $t_{LZWE}$ | $\overline{WE}$ HIGH to Low-Z[10, 11, 13] | 10 | | 10 | | ns |

**Switching Waveforms**
**Read Cycle 1 (Address Transition Controlled)[16, 17]**



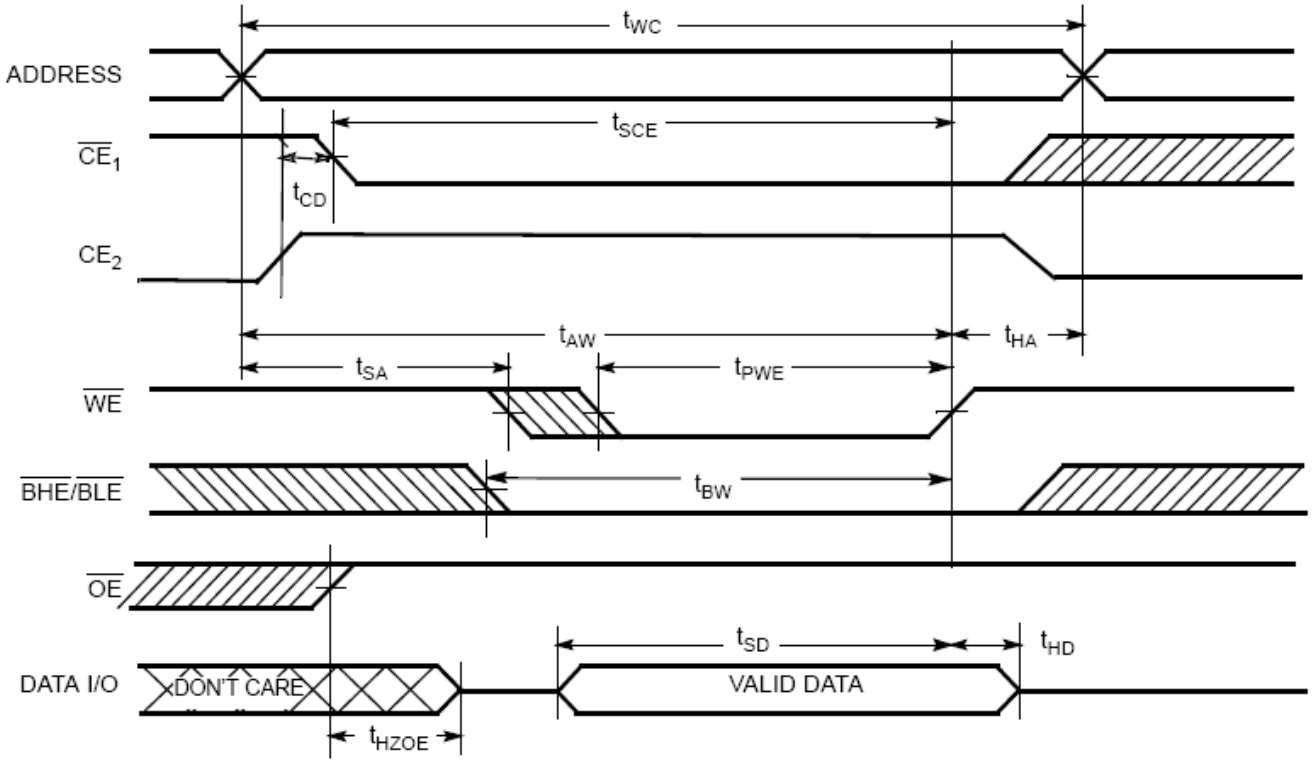

**Read Cycle 2 ($\overline{OE}$ Controlled)[15, 17]**




Notes:
15. Device is continuously selected. $\overline{OE}$ , $\overline{CE}1$ = $V_{IL}$ and CE2 = $V_{IH}$.
16. $\overline{WE}$ is HIGH for Read Cycle.

**Switching Waveforms (continued)**

**Write Cycle 1 ($\overline{WE}$ Controlled)[12, 13, 15, 18, 19]**



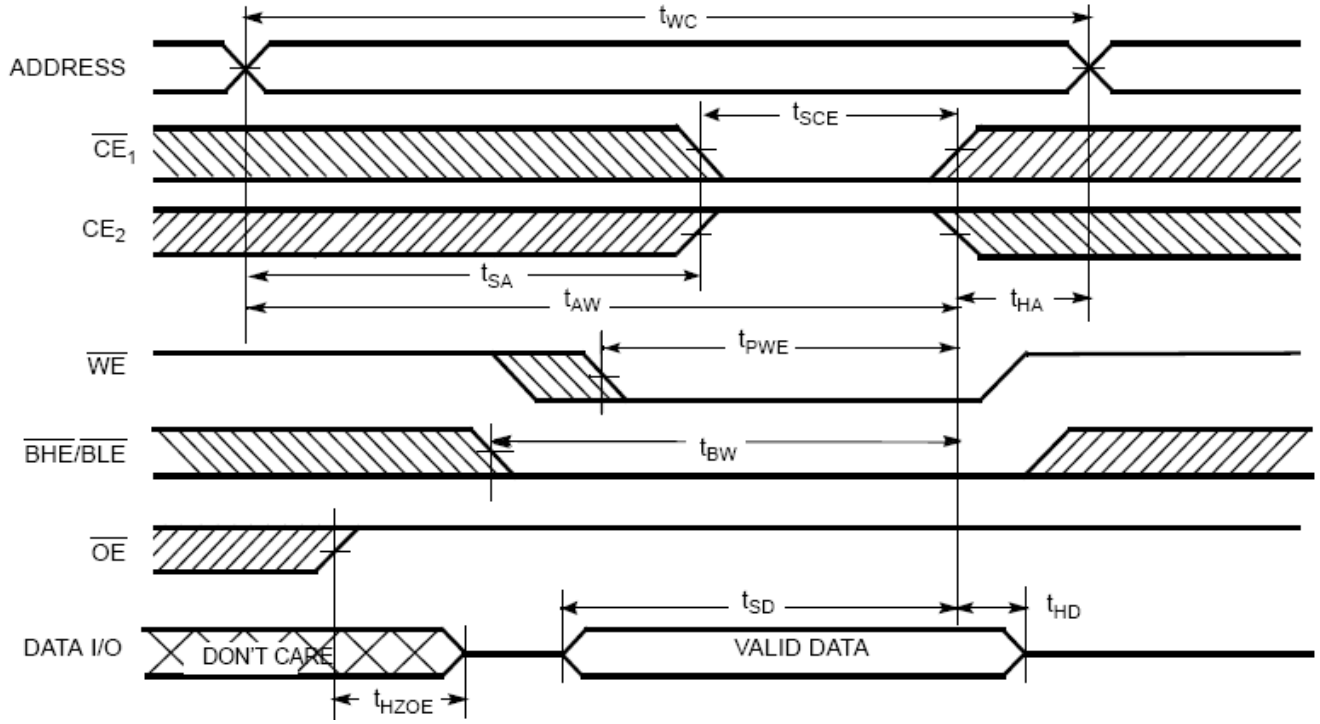

Notes:

18.Data I/O is high impedance if $\overline{OE}$ ≥ $V_{IH}$.

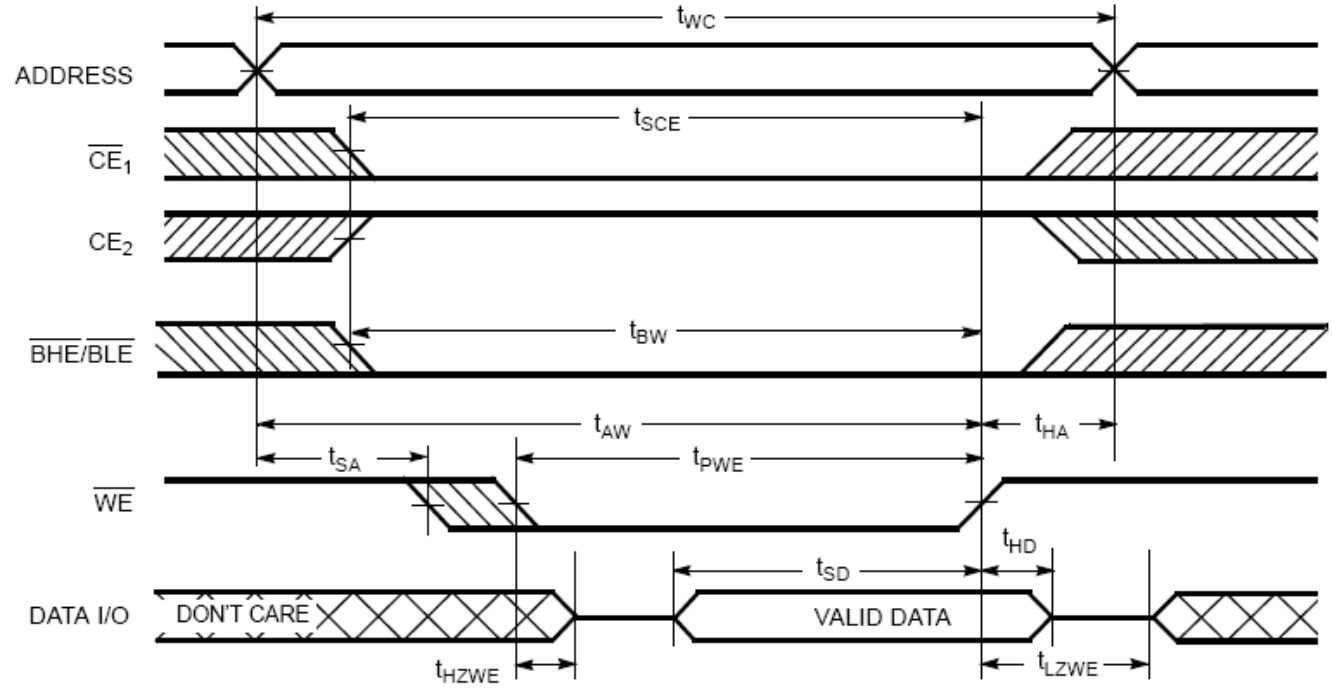
19.During the DON'T CARE period in the DATA I/O waveform, the I/Os are in output state and input signals should not be applied.

**Switching Waveforms (continued)**

**Write Cycle 2 ($\overline{CE}$1 or CE2 Controlled) [12, 13, 15, 18, 19]**

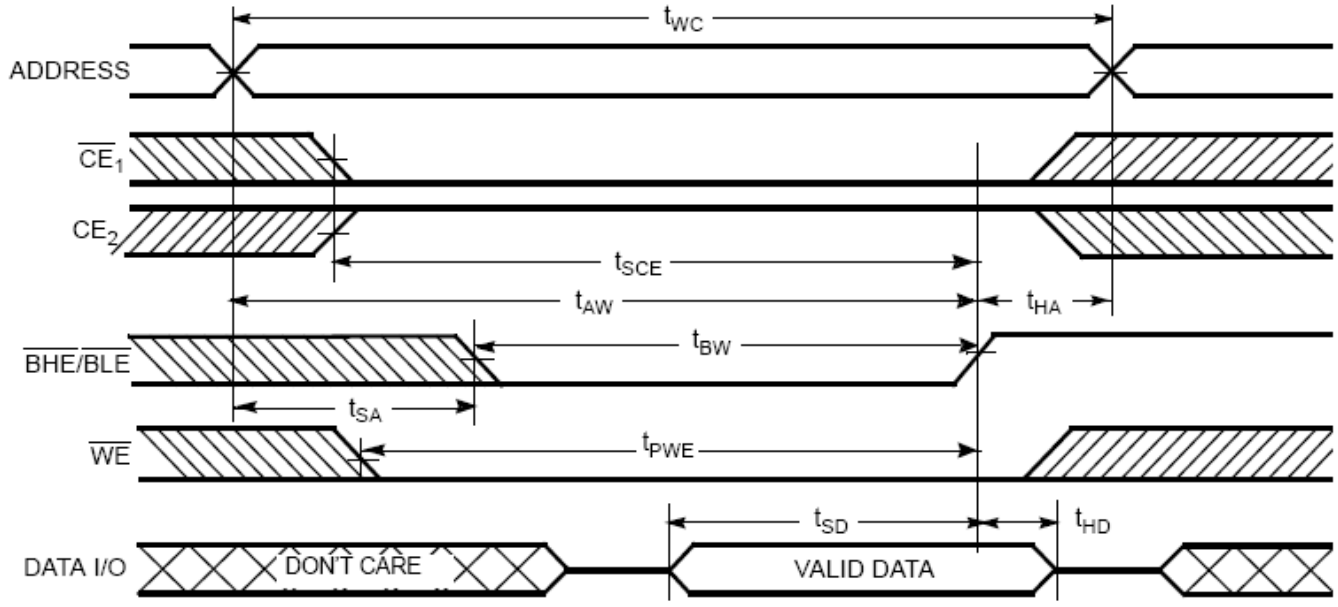



**Write Cycle 3 ($\overline{WE}$ Controlled, $\overline{OE}$ LOW)[15, 19]**



**Switching Waveforms (continued)**

**Write Cycle 4 ($\overline{BHE}$/$\overline{BLE}$ Controlled, $\overline{OE}$ LOW) [12, 15, 18, 19]**




Truth Table[20]

| $\overline{CE1}$ | CE2 | $\overline{WE}$ | $\overline{OE}$ | $\overline{BHE}$ | $\overline{BLE}$ | Inputs/Outputs | Mode | Power |
|---|---|---|---|---|---|---|---|---|
| H | X | X | X | X | X | High Z | Deselect/Power-Down | Standby ($I_{SB}$) |
| X | L | X | X | X | X | High Z | Deselect/Power-Down | Standby ($I_{SB}$) |
| X | X | X | X | H | H | High Z | Deselect/Power-Down | Standby ($I_{SB}$) |
| L | H | H | L | L | L | Data Out ($I/O_0$–$I/O_{15}$) | Read | Active ($I_{CC}$) |
| L | H | H | L | H | L | Data Out ($I/O_0$–$I/O_7$); ($I/O_8$–$I/O_{15}$) in High Z | Read | Active ($I_{CC}$) |
| L | H | H | L | L | H | Data Out ($I/O_8$–$I/O_{15}$); ($I/O_0$–$I/O_7$) in High Z | Read | Active ($I_{CC}$) |
| L | H | H | H | L | L | High Z | Output Disabled | Active ($I_{CC}$) |
| L | H | H | H | H | L | High Z | Output Disabled | Active ($I_{CC}$) |
| L | H | H | H | L | H | High Z | Output Disabled | Active ($I_{CC}$) |
| L | H | L | X | L | L | Data In ($I/O_0$–$I/O_{15}$) | Write (Upper Byte and Lower Byte) | Active ($I_{CC}$) |
| L | H | L | X | H | L | Data In ($I/O_0$–$I/O_7$); ($I/O_8$–$I/O_{15}$) in High Z | Write (Lower Byte Only) | Active ($I_{CC}$) |
| L | H | L | X | L | H | Data Out ($I/O_8$–$I/O_{15}$); ($I/O_0$–$I/O_7$) in High Z | Write (Upper Byte Only) | Active ($I_{CC}$) |

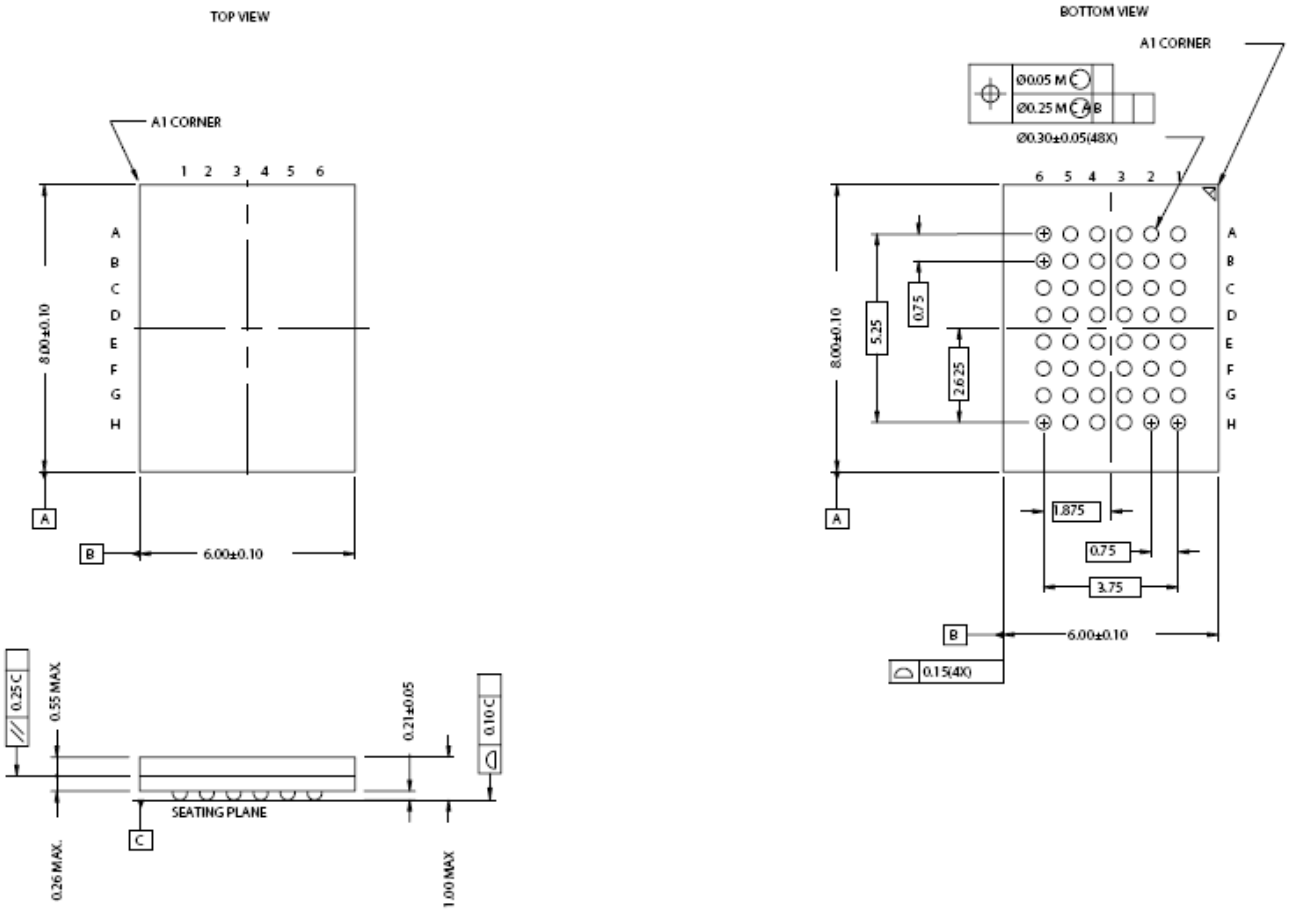
Note:
20.H = Logic HIGH, L = Logic LOW, X = Don't Care.

## Ordering Information

| Speed (ns) | Ordering Code | Package Type | Operating Range |
|---|---|---|---|
| 55 | M24D816128DA-55BIG | 48-ball Very Fine Pitch BGA (6.0 x 8.0 x 1.0 mm) (Pb-Free) | Industrial |
| 70 | M24D816128DA-70BIG | 48-ball Very Fine Pitch BGA (6.0 x 8.0 x 1.0 mm) (Pb-Free) | Industrial |

Package Diagrams

48-Lead VFBGA (6 x 8 x 1 mm)



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