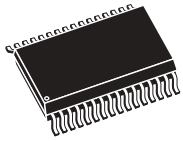
# M68AF127B

## 1Mbit (128K x8), 5V Asynchronous SRAM

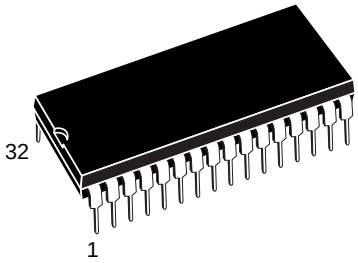
### FEATURES SUMMARY

- SUPPLY VOLTAGE: 4.5 to 5.5V
- 128K x 8 bits SRAM with OUTPUT ENABLE
- EQUAL CYCLE and ACCESS TIMES: 55ns
- LOW STANDBY CURRENT
- LOW $V_{CC}$ DATA RETENTION: 2V
- TRI-STATE COMMON I/O
- LOW ACTIVE and STANDBY POWER

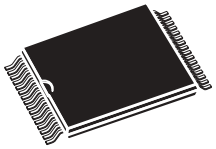
**Figure 1. Packages**



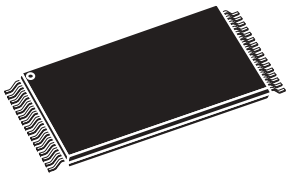
SO32 (MC)




PDIP32 (B)



TSOP32 (NK)
8 x 13.4mm



TSOP32 (N)
8 x 20mm

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## SUMMARY DESCRIPTION

The M68AF127B is a 1Mbit (1,048,576 bit) CMOS SRAM, organized as 131,072 words by 8 bits. The device features fully static operation requiring no external clocks or timing strobes, with equal address access and cycle times. It requires a single 4.5 to 5.5V supply.

This device has an automatic power-down feature, reducing the power consumption by over 99% when deselected.

The M68AF127B is available in SO32, PDIP32, TSOP32 (8x13.4mm) and TSOP32 (8x20mm) packages.

**Figure 2. Logic Diagram**

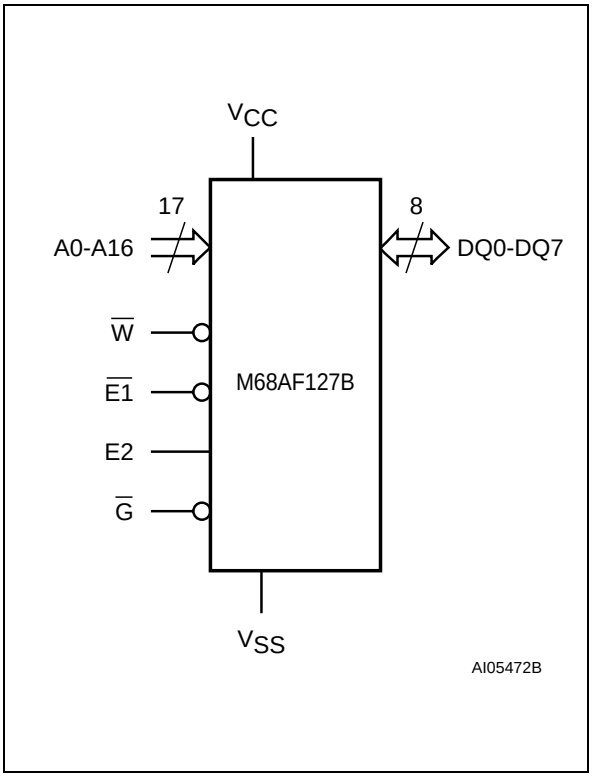



**Table 1. Signal Names**

| | |
|---|---|
| A0-A16 | Address Inputs |
| DQ0-DQ7 | Data Input/Output |
| $\overline{E1}$ | Chip Enable |
| E2 | Chip Enable |
| $\overline{G}$ | Output Enable |
| $\overline{W}$ | Write Enable |
| $V_{CC}$ | Supply Voltage |
| $V_{SS}$ | Ground |

**Figure 3. SO Connections**

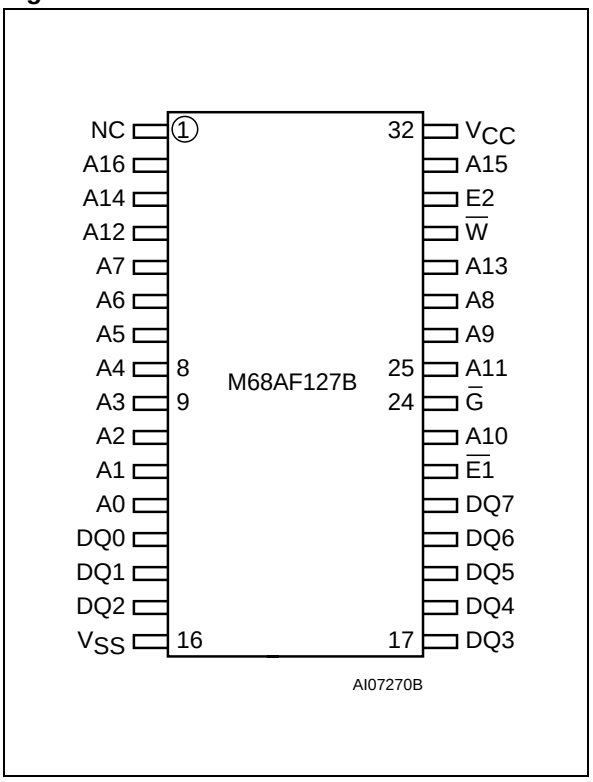



**Figure 5. TSOP Connections**

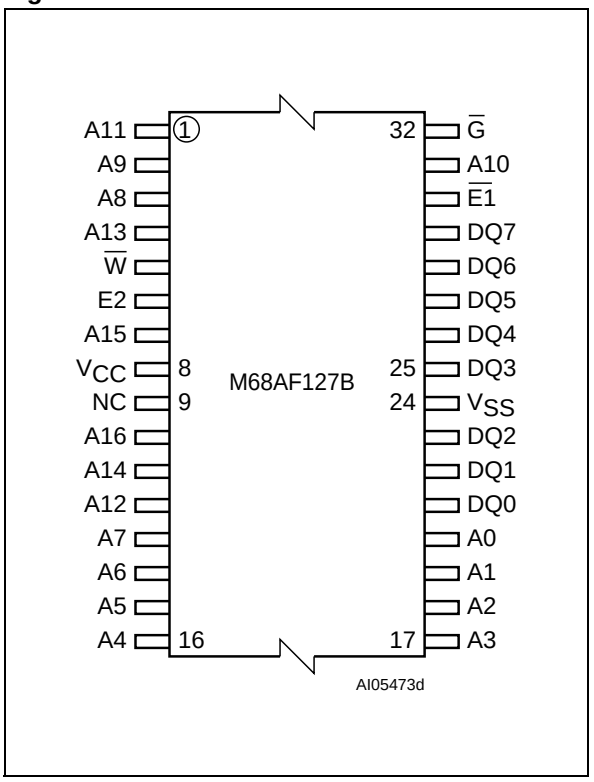



**Figure 4. DIP Connections**

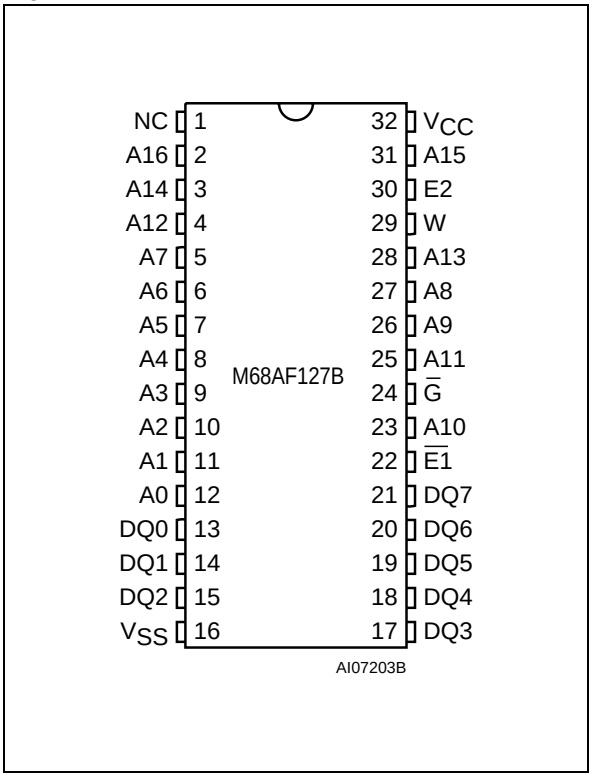
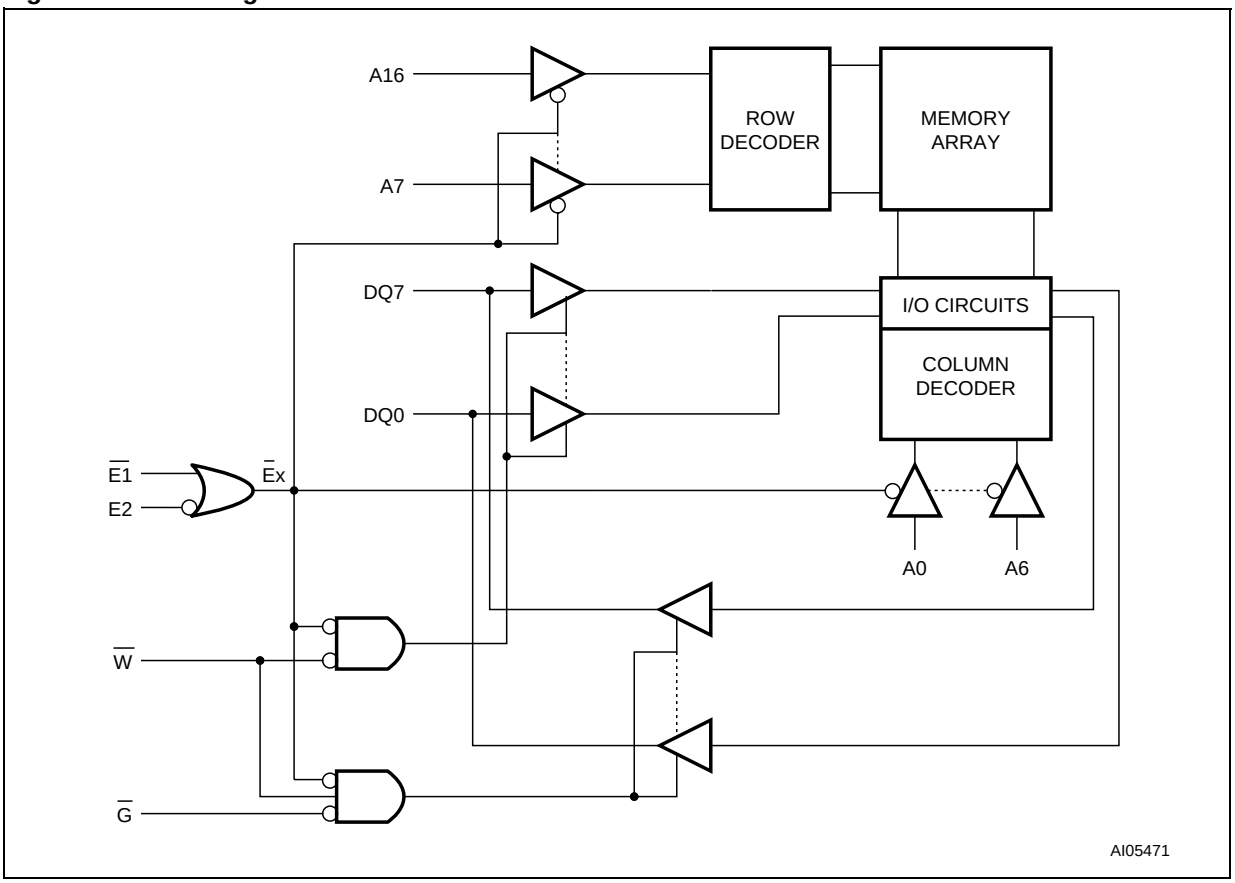


**Figure 6. Block Diagram**



## OPERATION

The M68AF127B has a Chip Enable power down feature which invokes an automatic standby mode whenever Chip Enable is de-asserted ($\overline{E1}$ = High), or Chip Select is asserted (E2 = Low). An Output Enable ($\overline{G}$) signal provides a high-speed, tri-state control, allowing fast read/write cycles to be achieved with the common I/O data bus. Operational modes are determined by device control inputs $\overline{W}$ and $\overline{E1}$ as summarized in the Operating Modes table (Table 2).

### Read Mode

The M68AF127B is in the Read mode whenever Write Enable ($\overline{W}$) is High with Output Enable ($\overline{G}$) Low, Chip Enable ($\overline{E1}$) is asserted and Chip Select (E2) is de-asserted. This provides access to data from eight of the 1,048,576 locations in the static memory array, specified by the 17 address inputs. Valid data will be available at the eight output pins within $t_{AVQV}$ after the last stable address, providing $\overline{G}$ is Low and $\overline{E1}$ is Low. If Chip Enable or Output Enable access times are not met, data access will be measured from the limiting parameter ($t_{ELQV}$ or $t_{GLQV}$) rather than the address. Data out may be indeterminate at $t_{ELQX}$ and $t_{GLQX}$, but data lines will always be valid at $t_{AVQV}$.

### Write Mode

The M68AF127B is in the Write mode whenever the $\overline{W}$ and $\overline{E1}$ pins are Low and the E2 pin is High. Either the Chip Enable input ($\overline{E1}$) or the Write Enable input ($\overline{W}$) must be de-asserted during Address transitions for subsequent write cycles. Write begins with the concurrence of $\overline{E1}$ being active with $\overline{W}$ low. Therefore, address setup time is referenced to Write Enable and Chip Enable as $t_{AVWL}$ and $t_{AVEH}$, respectively, and is determined by the latter occurring edge.

The Write cycle can be terminated by the earlier rising edge of $\overline{E1}$, or $\overline{W}$.

If the Output is enabled ($\overline{E1}$ = Low, E2 = High and $\overline{G}$ = Low), then $\overline{W}$ will return the outputs to high impedance within $t_{WLQZ}$ of its falling edge. Care must be taken to avoid bus contention in this type of operation. Data input must be valid for $t_{DVWH}$ before the rising edge of Write Enable, or for $t_{DVEH}$ before the rising edge of $\overline{E1}$, whichever occurs first, and remain valid for $t_{WHDX}$ or $t_{EHDX}$.

**Table 2. Operating Modes**

| Operation | $\overline{E1}$ | E2 | $\overline{W}$ | $\overline{G}$ | DQ0-DQ7 | Power |
|---|---|---|---|---|---|---|
| Read | $V_{IL}$ | $V_{IH}$ | $V_{IH}$ | $V_{IH}$ | Hi-Z | Active ($I_{CC}$) |
| Read | $V_{IL}$ | $V_{IH}$ | $V_{IH}$ | $V_{IL}$ | Data Output | Active ($I_{CC}$) |
| Write | $V_{IL}$ | $V_{IH}$ | $V_{IL}$ | X | Data Input | Active ($I_{CC}$) |
| Deselect | $V_{IH}$ | X | X | X | Hi-Z | Standby ($I_{SB}$) |
| Deselect | X | $V_{IL}$ | X | X | Hi-Z | Standby ($I_{SB}$) |

Note: X = $V_{IH}$ or $V_{IL}$.

## MAXIMUM RATING

Stressing the device above the rating listed in the "Absolute Maximum Ratings" table may cause permanent damage to the device. These are stress ratings only and operation of the device at these or any other conditions above those indicated in the Operating sections of this specification is not implied. Exposure to Absolute Maximum Rating conditions for extended periods may affect device reliability. Refer also to the STMicroelectronics SURE Program and other relevant quality documents.

**Table 3. Absolute Maximum Ratings**

| Symbol | Parameter | Value | Unit |
|---|---|---|---|
| $I_O$ (1) | Output Current | 20 | mA |
| $T_A$ | Ambient Operating Temperature | –55 to 125 | °C |
| $T_{STG}$ | Storage Temperature | –65 to 150 | °C |
| $V_{CC}$ | Supply Voltage | –0.5 to 6.5 | V |
| $V_{IO}$ (2) | Input or Output Voltage | –0.5 to $V_{CC}$ +0.5 | V |
| $P_D$ | Power Dissipation | 1 | W |

Note: 1. One output at a time, not to exceed 1 second duration.
2. Up to a maximum operating $V_{CC}$ of 6.0V only.

## DC AND AC PARAMETERS

This section summarizes the operating and measurement conditions, as well as the DC and AC characteristics of the device. The parameters in the following DC and AC Characteristic tables are derived from tests performed under the Measurement Conditions listed in the relevant tables. Designers should check that the operating conditions in their projects match the measurement conditions when using the quoted parameters.

**Table 4. Operating and AC Measurement Conditions**

| Parameter | | M68AF127B |
|---|---|---|
| $V_{CC}$ Supply Voltage | | 4.5 to 5.5V |
| Ambient Operating Temperature | Range 1 | 0 to 70°C |
| | Range 6 | –40 to 85°C |
| Load Capacitance ($C_L$) | | 100pF |
| Output Circuit Protection Resistance ($R_1$) | | 3.0kΩ |
| Load Resistance ($R_2$) | | 3.1kΩ |
| Input Rise and Fall Times | | 1ns/V |
| Input Pulse Voltages | | 0 to $V_{CC}$ |
| Input and Output Timing Ref. Voltages | | $V_{CC}/2$ |
| Output Transition Timing Ref. Voltages | | $V_{RL} = 0.3V_{CC}$; $V_{RH} = 0.7V_{CC}$ |

**Figure 7. AC Measurement I/O Waveform**

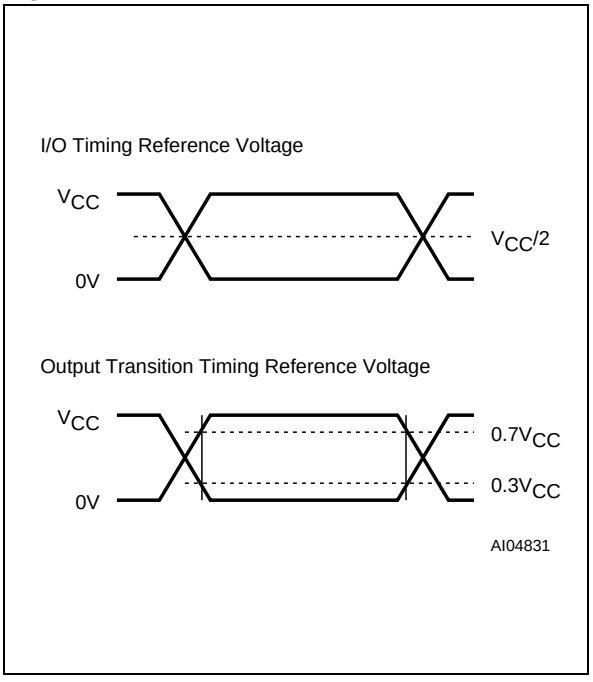
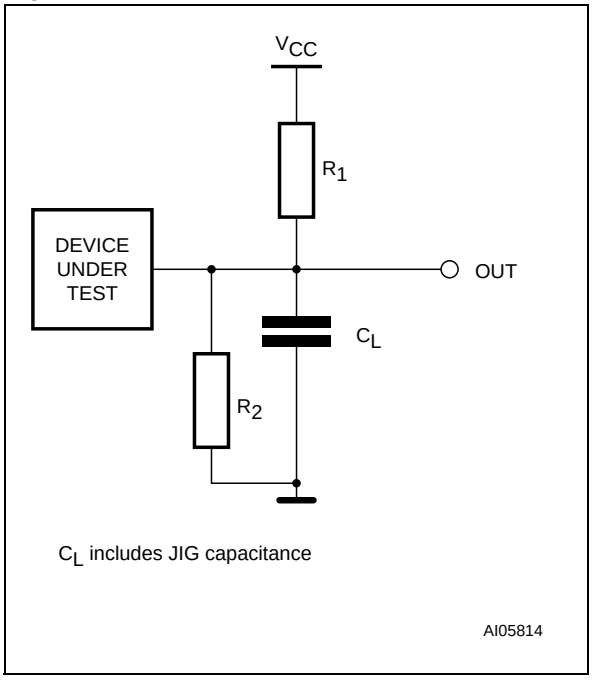



**Figure 8. AC Measurement Load Circuit**



### Table 5. Capacitance

| Symbol | Parameter (1,2) | Test Condition | Min | Max | Unit |
|---|---|---|---|---|---|
| $C_{IN}$ | Input Capacitance on all pins (except DQ) | $V_{IN}$ = 0V | | 6 | pF |
| $C_{OUT}$ | Output Capacitance | $V_{OUT}$ = 0V | | 8 | pF |

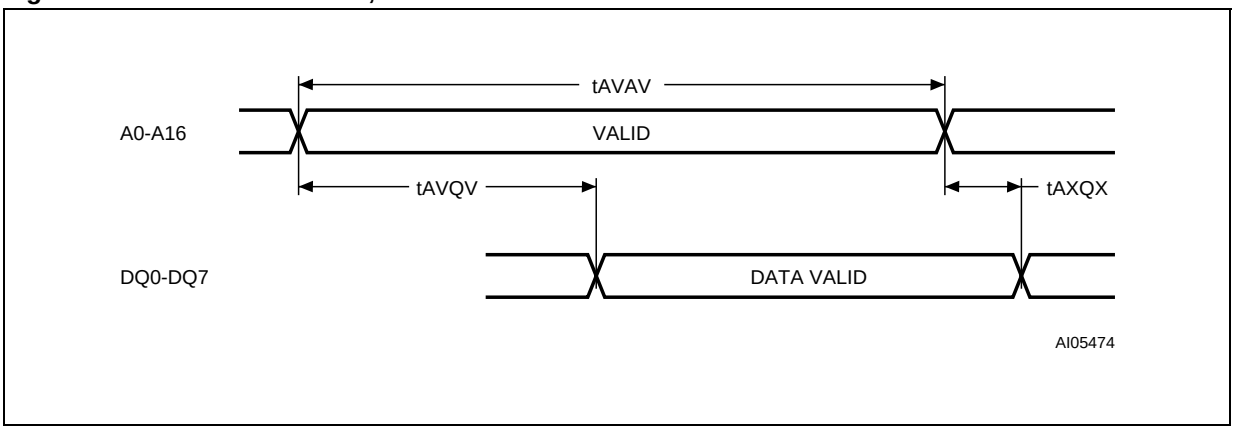
Note: 1. Sampled only, not 100% tested.
2. At $T_A$ = 25°C, f = 1MHz, $V_{CC}$ = 3.0V.

### Table 6. DC Characteristics

| Symbol | Parameter | Test Condition | | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|---|
| $I_{CC1}$ (1,2) | Supply Current | $V_{CC}$ = 5.5V, f = $1/t_{AVAV}$, $I_{OUT}$ = 0mA | 55 | | 7.5 | 20 | mA |
| | | | 70 | | 6.0 | 15 | mA |
| $I_{CC2}$ (3) | Operating Supply Current | $V_{CC}$ = 5.5V, f = 1MHz, $I_{OUT}$ = 0mA | | | | 2 | mA |
| $I_{LI}$ | Input Leakage Current | 0V ≤$V_{IN}$ ≤$V_{CC}$ | | –1 | | 1 | µA |
| $I_{LO}$ (4) | Output Leakage Current | 0V ≤$V_{OUT}$ ≤$V_{CC}$ | | –1 | | 1 | µA |
| $I_{SB}$ | Standby Supply Current CMOS | $V_{CC}$ = 5.5V, $\overline{E1}$ ≥ $V_{CC}$ – 0.2V, E2 ≤0.2V, f = 0 | | | 2.5 | 15 | µA |
| $V_{IH}$ | Input High Voltage | | | 2.2 | | $V_{CC}$ + 0.3 | V |
| $V_{IL}$ | Input Low Voltage | | | –0.3 | | 0.8 | V |
| $V_{OH}$ | Output High Voltage | $I_{OH}$ = –1mA | | 2.4 | | | V |
| $V_{OL}$ | Output Low Voltage | $I_{OL}$ = 2.1mA | | | | 0.4 | V |

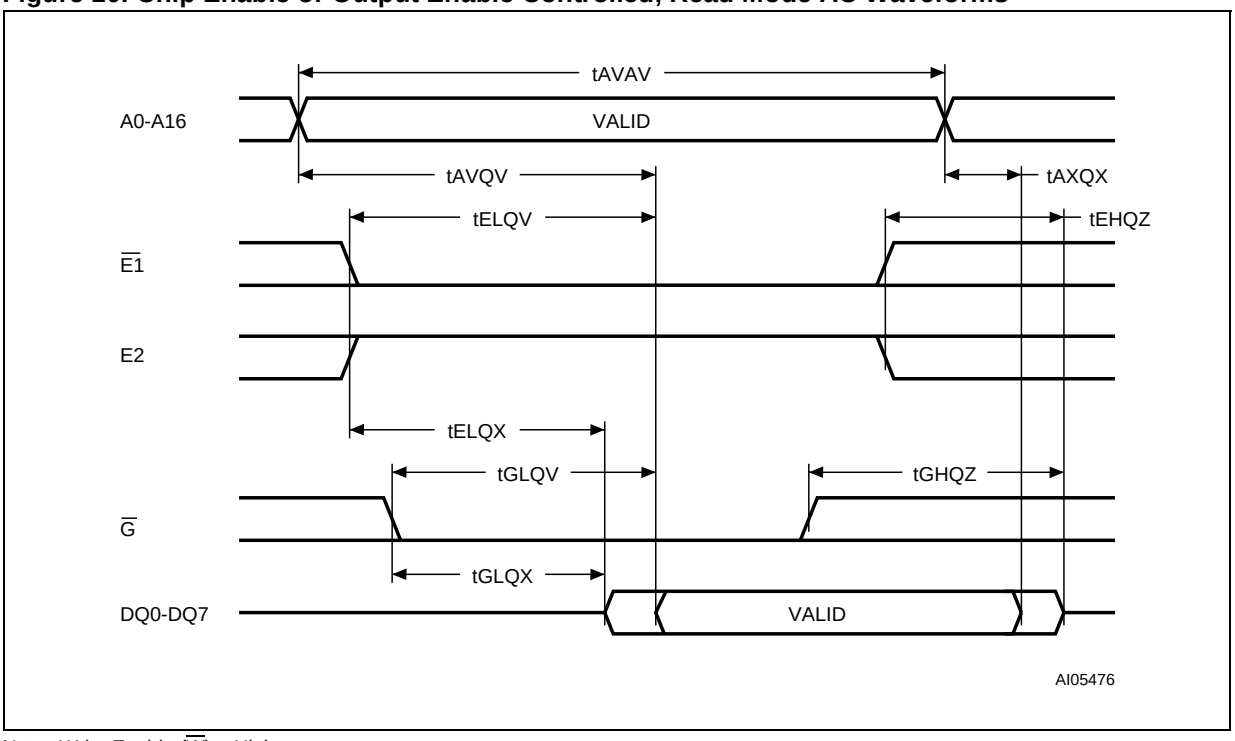
Note: 1. Average AC current, cycling at $t_{AVAV}$ minimum.
2. $\overline{E1}$ = $V_{IL}$, E2 = $V_{IH}$, $V_{IN}$ = $V_{IH}$ or $V_{IL}$.
3. $\overline{E1}$ ≤0.2V or E2 ≥ $V_{CC}$ –0.2V, $V_{IN}$ ≤0.2V or $V_{IN}$ ≥ $V_{CC}$ –0.2V.
4. Output disabled.

**Figure 9. Address Controlled, Read Mode AC Waveforms**




Note: $\overline{E1}$ = Low, E2 = High, $\overline{G}$ = Low, $\overline{W}$ = High.

**Figure 10. Chip Enable or Output Enable Controlled, Read Mode AC Waveforms**




Note: Write Enable ($\overline{W}$) = High.

**Figure 11. Chip Enable Controlled, Standby Mode AC Waveforms**

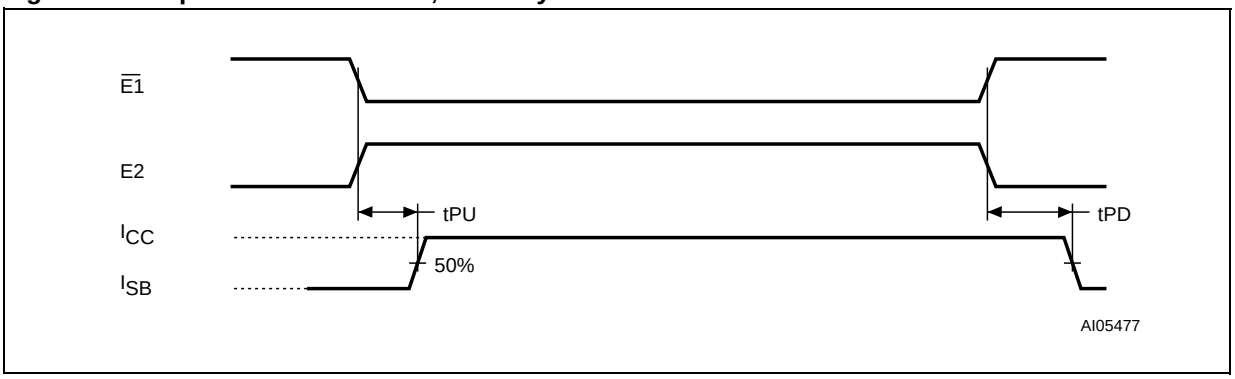


**Table 7. Read and Standby Mode AC Characteristics**

| Symbol | Parameter | | M68AF127B | | Unit |
|---|---|---|---|---|---|
| | | | 55 | 70 | |
| $t_{AVAV}$ | Read Cycle Time | Min | 55 | 70 | ns |
| $t_{AVQV}$ | Address Valid to Output Valid | Max | 55 | 70 | ns |
| $t_{AXQX}$ (1) | Data hold from address change | Min | 5 | 5 | ns |
| $t_{EHQZ}$ (2,3) | Chip Enable High to Output Hi-Z | Max | 20 | 25 | ns |
| $t_{ELQV}$ | Chip Enable Low to Output Valid | Max | 55 | 70 | ns |
| $t_{ELQX}$ (1) | Chip Enable Low to Output Transition | Min | 5 | 5 | ns |
| $t_{GHQZ}$ (2,3) | Output Enable High to Output Hi-Z | Max | 20 | 25 | ns |
| $t_{GLQV}$ | Output Enable Low to Output Valid | Max | 25 | 35 | ns |
| $t_{GLQX}$ (2) | Output Enable Low to Output Transition | Min | 5 | 5 | ns |
| $t_{PD}$ | Chip Enable or $\overline{UB}$/$\overline{LB}$ High to Power Down | Max | 55 | 70 | ns |
| $t_{PU}$ | Chip Enable or $\overline{UB}$/$\overline{LB}$ Low to Power Up | Min | 0 | 0 | ns |

Note: 1. Test conditions assume transition timing reference level = $0.3V_{CC}$ or $0.7V_{CC}$.
2. At any given temperature and voltage condition, $t_{GHQZ}$ is less than $t_{GLQX}$ and $t_{EHQZ}$ is less than $t_{ELQX}$ for any given device.
3. These parameters are defined as the time at which the outputs achieve the open circuit conditions and are not referenced to output voltage levels.

**Figure 12. Write Enable Controlled, Write AC Waveforms**

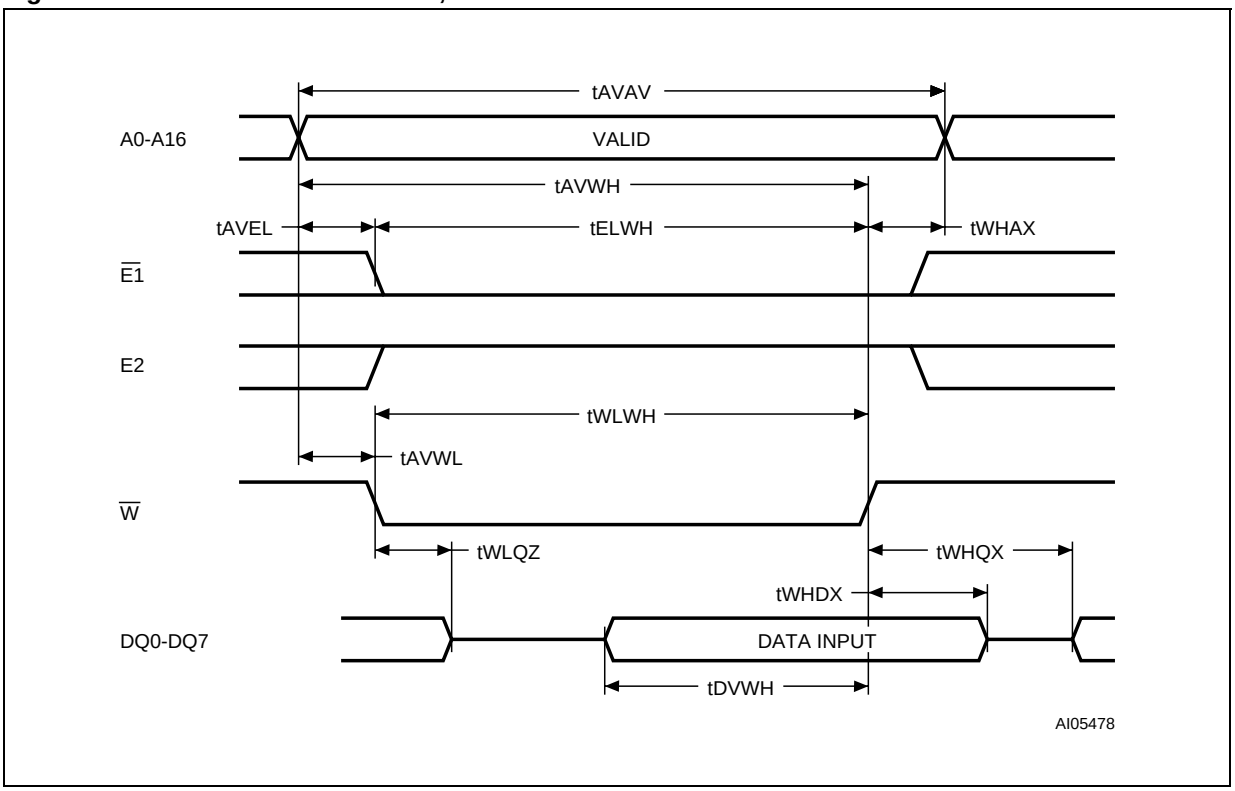



**Figure 13. Chip Enable Controlled, Write AC Waveforms**

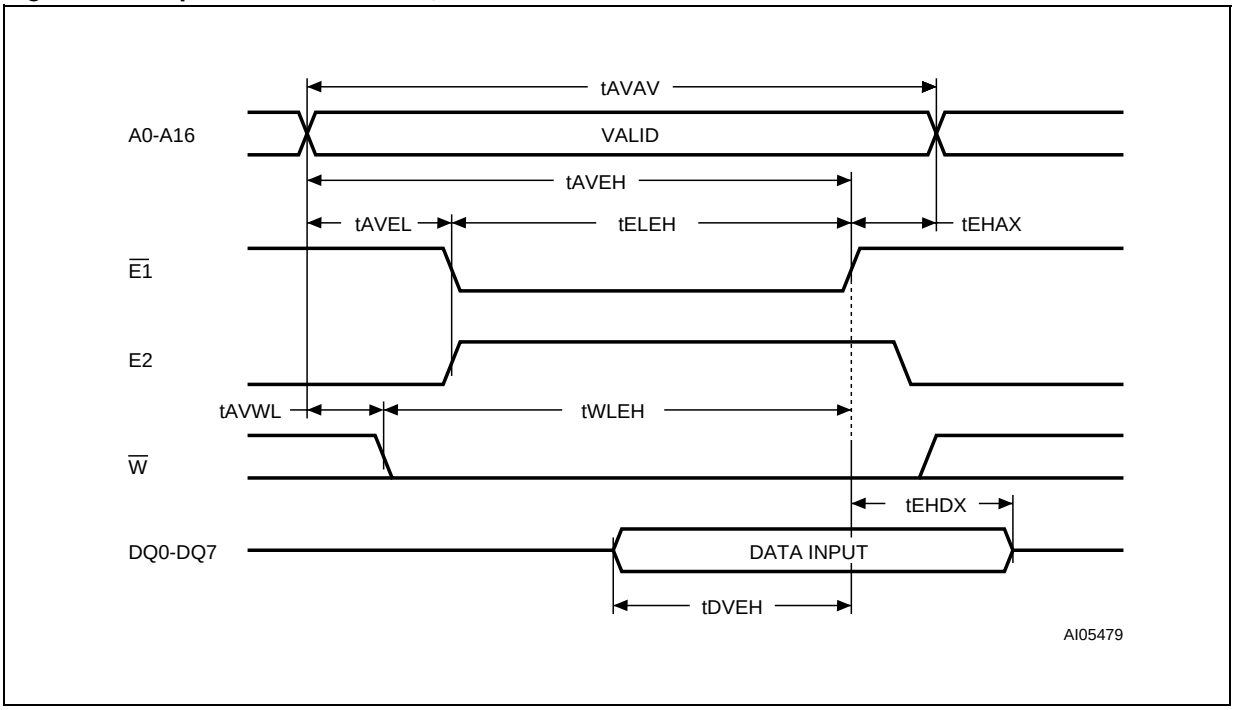


**Table 8. Write Mode AC Characteristics**

| Symbol | Parameter | | M68AF127B | | Unit |
|---|---|---|---|---|---|
| | | | 55 | 70 | |
| $t_{AVAV}$ | Write Cycle Time | Min | 55 | 70 | ns |
| $t_{AVEH}$ | Address Valid to Chip Enable High | Min | 45 | 60 | ns |
| $t_{AVEL}$ | Address valid to Chip Enable Low | Min | 0 | 0 | ns |
| $t_{AVWH}$ | Address Valid to Write Enable High | Min | 45 | 60 | ns |
| $t_{AVWL}$ | Address Valid to Write Enable Low | Min | 0 | 0 | ns |
| $t_{DVEH}$ | Input Valid to Chip Enable High | Min | 25 | 30 | ns |
| $t_{DVWH}$ | Input Valid to Write Enable High | Min | 25 | 30 | ns |
| $t_{EHAX}$ | Chip Enable High to Address Transition | Min | 0 | 0 | ns |
| $t_{EHDX}$ | Chip enable High to Input Transition | Min | 0 | 0 | ns |
| $t_{ELEH}$ | Chip Enable Low to Chip Enable High | Min | 45 | 60 | ns |
| $t_{ELWH}$ | Chip Enable Low to Write Enable High | Min | 45 | 60 | ns |
| $t_{WHAX}$ | Write Enable High to Address Transition | Min | 0 | 0 | ns |
| $t_{WHDX}$ | Write Enable High to Input Transition | Min | 0 | 0 | ns |
| $t_{WHQX}$ (1) | Write Enable High to Output Transition | Min | 5 | 5 | ns |
| $t_{WLEH}$ | Write Enable Low to Chip Enable High | Min | 45 | 60 | ns |
| $t_{WLQZ}$ (1,2) | Write Enable Low to Output Hi-Z | Max | 20 | 20 | ns |
| $t_{WLWH}$ | Write Enable Low to Write Enable High | Min | 45 | 60 | ns |

Note: 1. At any given temperature and voltage condition, $t_{WLQZ}$ is less than $t_{WHQX}$ for any given device.
2. These parameters are defined as the time at which the outputs achieve the open circuit conditions and are not referenced to output voltage levels.

**Figure 14. $\overline{E1}$ Controlled, Low $V_{CC}$ Data Retention AC Waveforms**

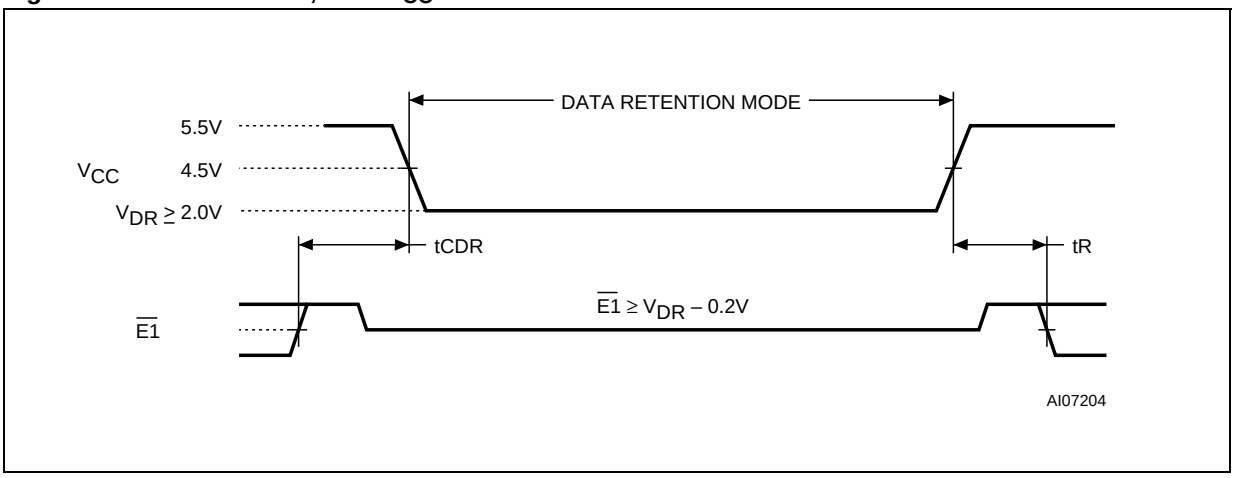



**Figure 15. E2 Controlled, Low $V_{CC}$ Data Retention AC Waveforms**

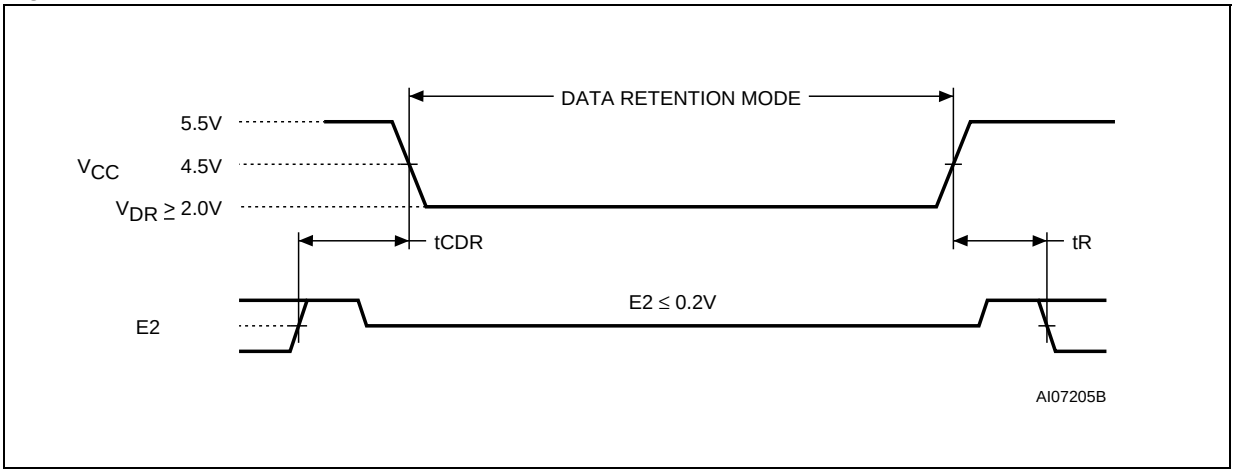


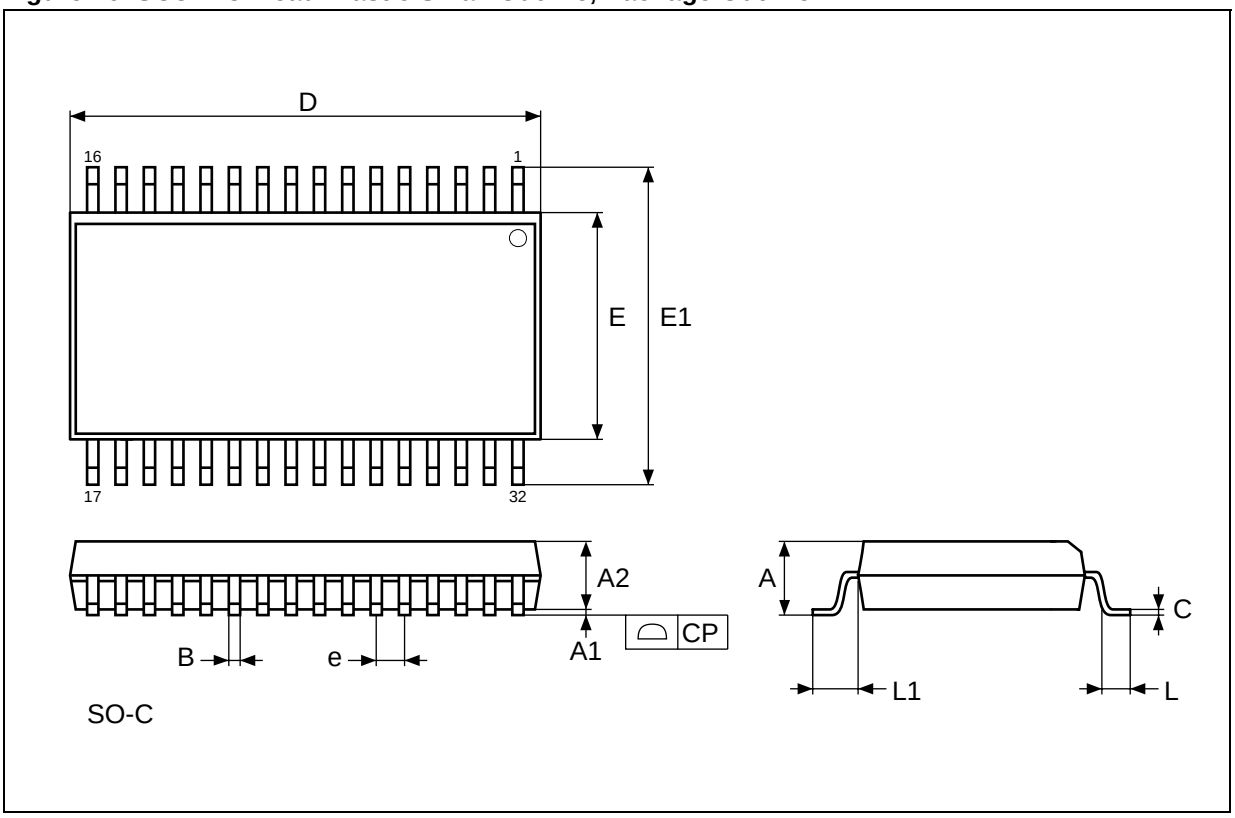

**Table 9. Low $V_{CC}$ Data Retention Characteristics**

| Symbol | Parameter | Test Condition | Min | Max | Unit |
|---|---|---|---|---|---|
| $I_{CCDR}$ (1) | Supply Current (Data Retention) | $V_{CC}$ = 2.0V, $\overline{E1} \geq V_{CC}$ –0.2V or E2 ≤0.2V, f = 0 | | 4.5 | µA |
| $t_{CDR}$ (1,2) | Chip Deselected to Data Retention Time | | 0 | | ns |
| $t_R$ (2) | Operation Recovery Time | | $t_{AVAV}$ | | ns |
| $V_{DR}$ (1) | Supply Voltage (Data Retention) | $\overline{E1} \geq V_{CC}$ –0.2V or E2 ≤0.2V, f = 0 | 2.0 | | V |

Note: 1. All other Inputs at $V_{IH} \geq V_{CC}$ –0.2V or $V_{IL} \leq$0.2V.
2. Tested initially and after any design or process that may affect these parameters. $t_{AVAV}$ is Read cycle time.
3. No input may exceed $V_{CC}$ +0.2V.

## PACKAGE MECHANICAL

**Figure 16. SO32 - 32 lead Plastic Small Outline, Package Outline**

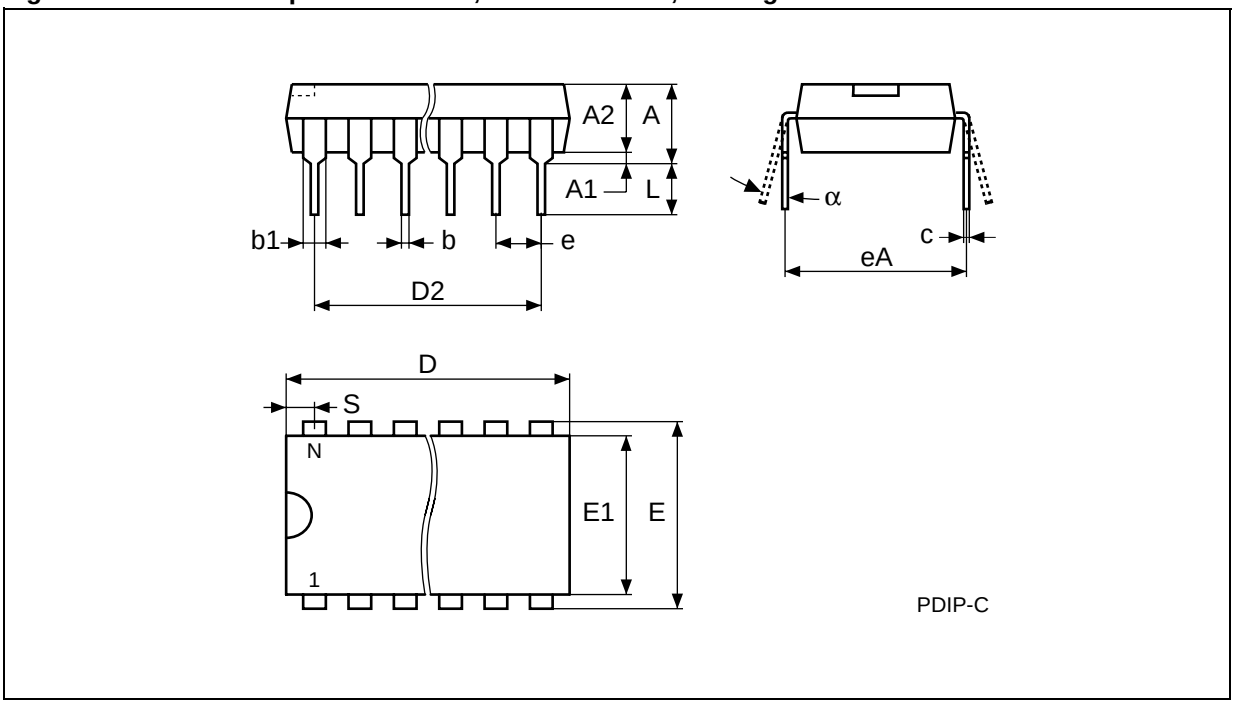



Note: Drawing is not to scale.

**Table 10. SO32 - 32 lead Plastic Small Outline, Package Mechanical Data**

| Symbol | millimeters | | | inches | | |
|---|---|---|---|---|---|---|
| | Typ | Min | Max | Typ | Min | Max |
| B | | 0.36 | 0.51 | | 0.014 | 0.020 |
| A | | | 3.00 | | | 0.118 |
| A1 | | 0.10 | | | 0.004 | |
| A2 | | 2.57 | 2.82 | | 0.101 | 0.111 |
| C | | 0.15 | 0.30 | | 0.006 | 0.012 |
| CP | | | 0.10 | | | 0.004 |
| D | | 20.14 | 20.75 | | 0.793 | 0.817 |
| E | | 11.18 | 11.43 | | 0.440 | 0.450 |
| E1 | | 13.87 | 14.38 | | 0.546 | 0.566 |
| e | 1.27 | – | – | 0.050 | – | – |
| L | | 0.58 | 0.99 | | 0.023 | 0.039 |
| L1 | | 1.19 | 1.60 | | 0.047 | 0.063 |
| N | 32 | | | 32 | | |

**Figure 17. PDIP32 - 32 pin Plastic DIP, 600 mils width, Package Outline**

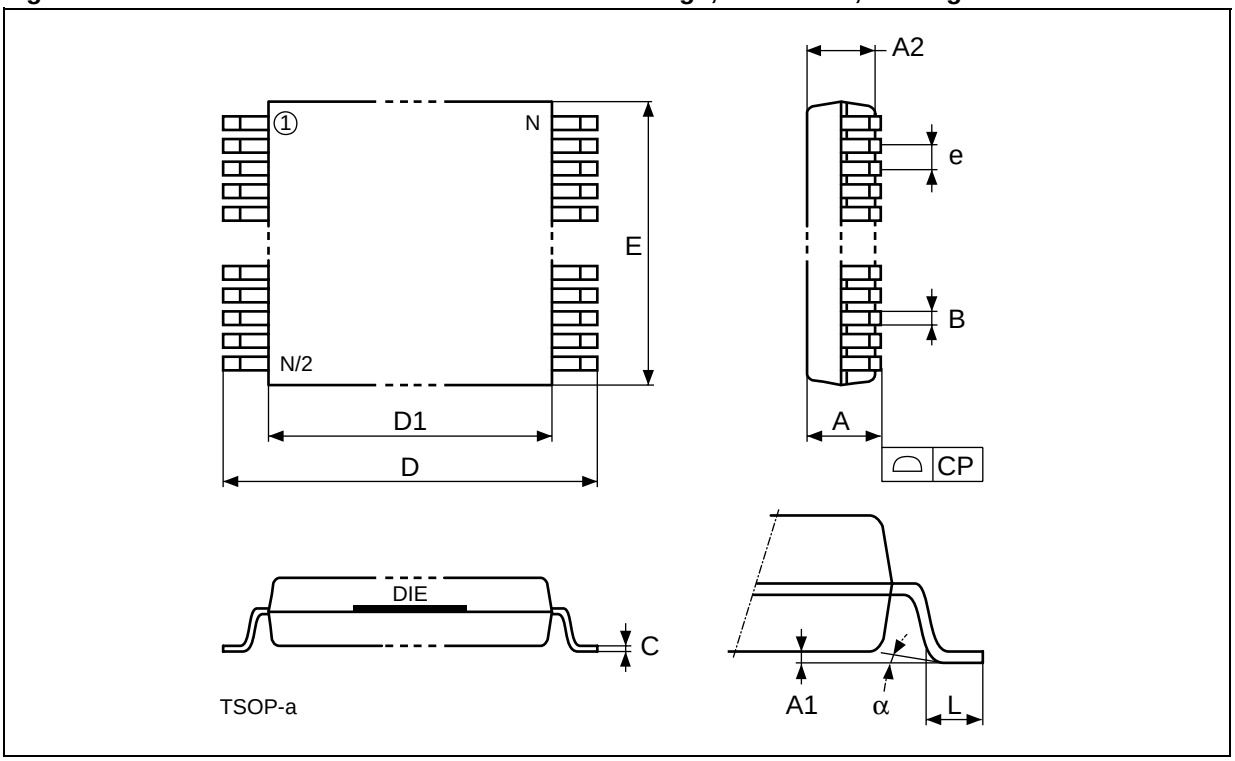



Note: Drawing is not to scale.

**Table 11. PDIP32 - 32 pin Plastic DIP, 600 mils width, Package Mechanical Data**

| Symbol | millimeters | | | inches | | |
|---|---|---|---|---|---|---|
| | Typ | Min | Max | Typ | Min | Max |
| A | | | 4.83 | | | 0.190 |
| A1 | | 0.38 | | | 0.015 | |
| A2 | 3.81 | | | 0.150 | | |
| b | | 0.41 | 0.53 | | 0.016 | 0.021 |
| b1 | | 1.14 | 1.65 | | 0.045 | 0.065 |
| c | | 0.23 | 0.38 | | 0.009 | 0.015 |
| D | | 41.78 | 42.29 | | 1.645 | 1.665 |
| eA | 15.24 | – | – | 0.600 | – | – |
| e | 2.54 | – | – | 0.100 | – | – |
| E | | 15.24 | 15.88 | | 0.600 | 0.625 |
| E1 | | 13.46 | 13.97 | | 0.530 | 0.550 |
| L | | 3.05 | 3.56 | | 0.120 | 0.140 |
| S | | 1.65 | 2.21 | | 0.065 | 0.087 |
| α | | 0° | 15° | | 0° | 15° |
| N | 32 | | | 32 | | |

**Figure 18. TSOP32 - 32-lead Thin Small Outline Package, 8x13.4mm, Package Outline**

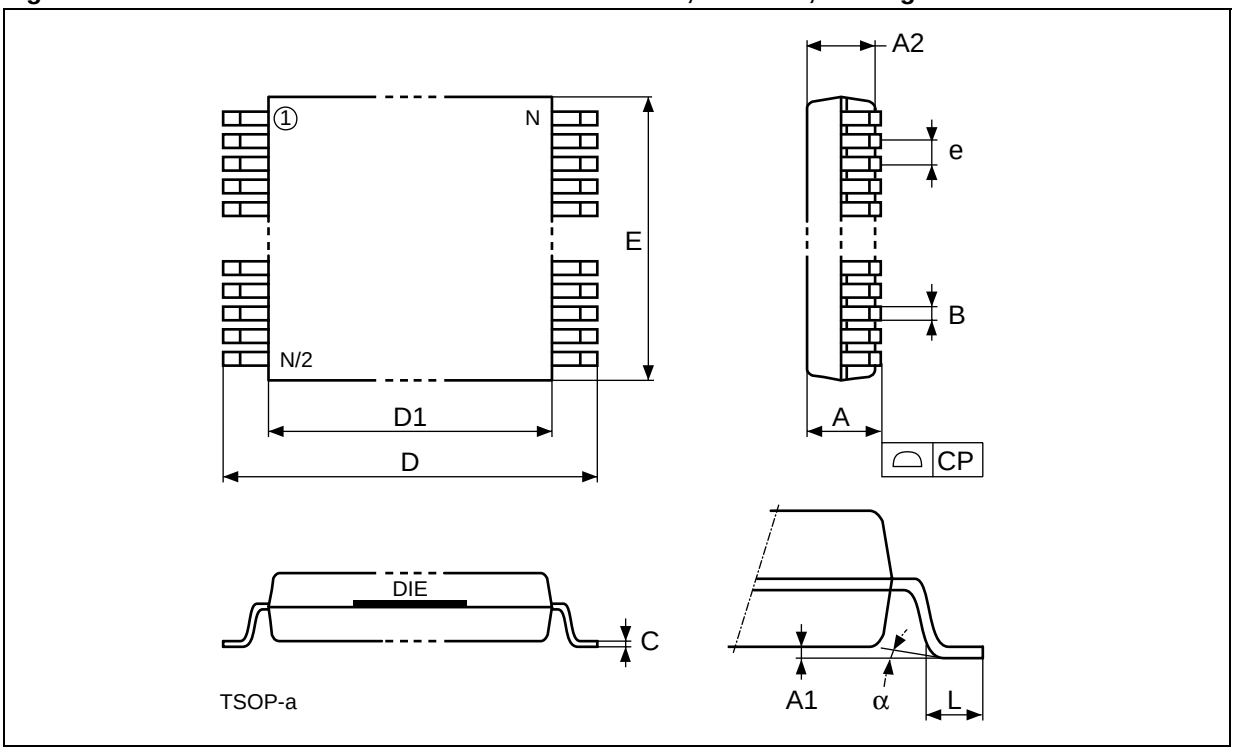



Note: Drawing is not to scale.

**Table 12. TSOP32 - 32-lead Thin Small Outline Package, 8x13.4mm, Package Mechanical Data**

| Symbol | millimeters | | | inches | | |
|---|---|---|---|---|---|---|
| | Typ | Min | Max | Typ | Min | Max |
| A | | | 1.20 | | | 0.0472 |
| A1 | | 0.05 | 0.15 | | 0.0020 | 0.0059 |
| A2 | | 0.91 | 1.05 | | 0.0358 | 0.0413 |
| B | 0.22 | | | 0.0087 | | |
| C | | 0.10 | 0.21 | | 0.0039 | 0.0083 |
| CP | | | 0.10 | | | 0.0039 |
| D | 13.40 | – | – | 0.5276 | – | – |
| D1 | 11.80 | – | – | 0.4646 | – | – |
| E | 8.00 | – | – | 0.3150 | – | – |
| e | 0.50 | – | – | 0.0197 | – | – |
| L | | 0.40 | 0.60 | | 0.0157 | 0.0236 |
| α | | 0° | 5° | | 0° | 5° |
| N | 32 | | | 32 | | |

**Figure 19. TSOP32 - 32 lead Plastic Thin Small Outline, 8x20mm, Package Outline**




Note: Drawing is not to scale.

**Table 13. TSOP32 - 32 lead Plastic Thin Small Outline, 8x20mm, Package Mechanical Data**

| | | millimeters | | | inches | |
|---|---|---|---|---|---|---|
| **Symbol** | **Typ** | **Min** | **Max** | **Typ** | **Min** | **Max** |
| A | | | 1.200 | | | 0.0472 |
| A1 | | 0.050 | 0.150 | | 0.0020 | 0.0059 |
| A2 | | 0.950 | 1.050 | | 0.0374 | 0.0413 |
| B | | 0.170 | 0.250 | | 0.0067 | 0.0098 |
| C | | 0.100 | 0.210 | | 0.0039 | 0.0083 |
| CP | | | 0.100 | | | 0.0039 |
| D | | 19.800 | 20.200 | | 0.7795 | 0.7953 |
| D1 | | 18.300 | 18.500 | | 0.7205 | 0.7283 |
| e | 0.500 | – | – | 0.0197 | – | – |
| E | | 7.900 | 8.100 | | 0.3110 | 0.3189 |
| L | | 0.500 | 0.700 | | 0.0197 | 0.0276 |
| α | | 0° | 5° | | 0° | 5° |
| N | 32 | | | 32 | | |

## PART NUMBERING

**Table 14. Ordering Information Scheme**

Example: M68AF127 B L 55 MC 6 T

**Device Type**
M68

**Mode**
A = Asynchronous

**Operating Voltage**
F = 4.5 to 5.5V

**Array Organization**
127 = 1Mbit (128K x8)

**Option 1**
B = 2 Chip Enable

**Option 2**
L = L-Die
M = M-Die

**Speed Class**
55 = 55ns
70 = 70ns

**Package**
MC = SO32
B = PDIP32
NK = TSOP32 8x13.4mm
N = TSOP32 8x20mm

**Operative Temperature**
1 = 0 to 70°C
6 = –40 to 85°C

**Shipping**
T = Tape & Reel Packing

For a list of available options (e.g., Speed, Package) or for further information on any aspect of this device, please contact the STMicroelectronics Sales Office nearest to you.

# REVISION HISTORY

**Table 15. Document Revision History**

| Date | Version | Revision Details |
|---|---|---|
| August 2001 | 1.0 | First Issue. |
| 18-Oct-2001 | 2.0 | SO32 Package Mechanical and Data added (Figure 1, 3 and 16, Table 10). |
| 29-Nov-2001 | 3.0 | Note removed from Ordering Information Scheme. |
| 06-Mar-2002 | 4.0 | Document status changed to Data Sheet. |
| 17-May-2002 | 5.0 | Document globally revised. |
| 31-May-2002 | 6.0 | PDIP32 Package added (Figure 1, 4 and 17, Table 11).<br>Chip Enable Low $V_{CC}$ Data Retention clarified (Figure 14 and 15, Table 9). |
| 09-Sep-2002 | 6.1 | TSOP32 8x13.4mm and TSOP32 8x20mm packages added (Figure 1, 5, 18 and 19, Table 12, 13 and 14).<br>Commercial code clarified. |
| 02-Oct-2002 | 6.2 | Title and header layout modified. |
| 09-Oct-2002 | 6.3 | Datasheet number simplified. |
| 16-Apr-2003 | 6.4 | Label corrected on “E2 Controlled, Low $V_{CC}$ Data Retention AC Waveforms” figure. |
| 08-Aug-2003 | 6.5 | TSOP Package connections modified (Figure 5).<br>Test conditions for ICCDR modified in Table 9, Low $V_{CC}$ Data Retention Characteristics. |
| 21-Aug-2003 | 6.6 | TSOP Package connections modified (Figure 5). |
| 24-Sep-2004 | 7 | Document structure modified:<br>– Chapter OPERATION moved before chapter MAXIMUM RATING.<br>– AC Characteristics Tables and waveforms moved to the DC/AC PARAMETERS section.<br>$t_{PU}$ ad $t_{PD}$ updated in Table 7. |

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