SONY

ILX503A

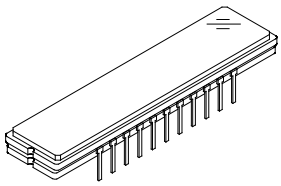
2048-pixel CCD Linear Image Sensor (B/W)

For the availability of this product, please contact the sales office.

Description

The ILX503A is a reduction type CCD linear sensor designed for facsimile, image scanner and OCR use. This sensor reads B4 size documents at a density of 200 DPI (Dot Per Inch). A built-in timing generator and clock-drivers ensure direct drive at 5V logic for easy use.

22 pin DIP (Plastic)



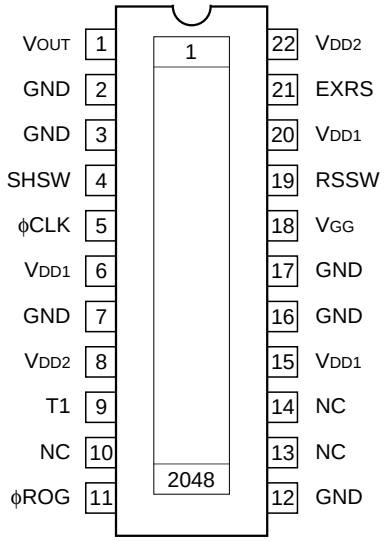
Features

- Number of effective pixels: 2048 pixels
- Pixel size: 14µm × 14µm (14µm pitch)
- Built-in timing generator and clock-drivers
- Ultra low lag
- Maximum clock frequency: 5MHz

Absolute Maximum Ratings

• Supply voltage	V_{DD1}	11	V
	V_{DD2}	6	V
• Operating temperature		–10 to +55	°C
• Storage temperature		–30 to +80	°C

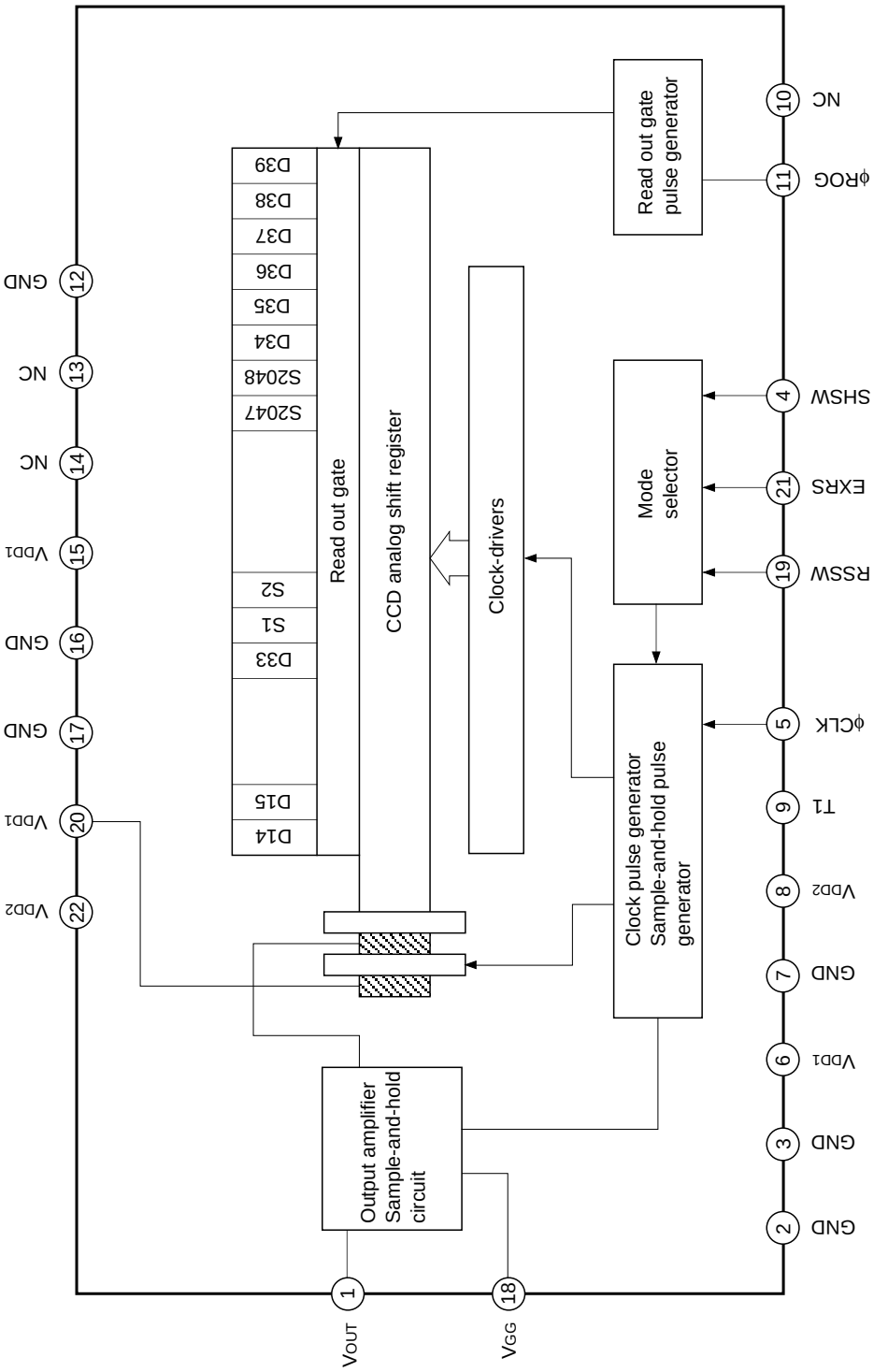
Pin Configuration (Top View)



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E92Y21E78-PS

Block Diagram



Pin Description

Pin No.	Symbol	Description
1	V_{OUT}	Signal output
2	GND	GND
3	GND	GND
4	SHSW	Switch { with S/H → GND / without S/H → V_{DD2}
5	ϕCLK	Clock pulse
6	V_{DD1}	9V power supply
7	GND	GND
8	V_{DD2}	5V power supply
9	T1	Test pin (V_{DD2})
10	NC	
11	ϕROG	Clock pulse
12	GND	GND
13	NC	
14	NC	
15	V_{DD1}	9V power supply
16	GND	GND
17	GND	GND
18	V_{GG}	Output circuit gate bias
19	RSSW	RS pulse external, internal selection (External RS → V_{DD2}, Internal RS → GND)
20	V_{DD1}	9V power supply
21	EXRS	RS input pin during external RS pulse usage
22	V_{DD2}	5V power supply

Recommended Voltage

Item	Min.	Typ.	Max.	Unit
V_{DD1}	8.5	9.0	9.5	V
V_{DD2}	4.75	5.0	5.25	V

Note) Rules for raising and lowering power supply voltage
To raise power supply voltage, first raise V_{DD1}(9V) and then V_{DD2} (5V).
To lower voltage, first lower V_{DD2} (5V) and then V_{DD1} (9V).

Mode Description

Mode Description		Pin condition		
RS	S/H	4 pin SHSW	19 pin RSSW	21 pin EXRS
Internal	Yes	GND	GND	V_{DD2}
	No	V_{DD2}	GND	V_{DD2}
Externel	No	V_{DD2}	V_{DD2}	ϕRS

Input Capacity of Pins

Item	Symbol	Min.	Typ.	Max.	Unit
Input capacity of ϕCLK pin	$C_{\phi CLK}$	—	10	—	pF
Input capacity of ϕROG pin	$C_{\phi ROG}$	—	10	—	pF
Input capacity of EXRS pin	C_{EXRS}	—	10	—	pF

Recommended Input Pulse Voltage

Parameter	Min.	Typ.	Max.	Unit
Input clock high level	4.5	5.0	5.5	V
Input clock low level	0.0	—	0.5	V

Electro-optical Characteristics

(Ta = 25°C, V_{DD1} = 9V, V_{DD2} = 5V, Clock frequency: 1MHz,
Light source = 3200K, IR cut filter: CM-500S (t = 1.0mm)),
When Internal RS (Pin 19 = GND, Pin 21 = V_{DD2})

Item	Symbol	Min.	Typ.	Max.	Unit	Remarks
Sensitivity 1	R1	22.5	30	37.5	V/(lx · s)	Note 1
Sensitivity 2	R2	—	95	—	V/(lx · s)	Note 2
Sensitivity 3	R3	—	20	—	V/(lx · s)	Note 3
Sensitivity 4	R4	—	500	—	V/(lx · s)	Note 4
Sensitivity nonuniformity	PRNU	—	2.0	8.0	%	Note 5
Saturation output voltage	V_{SAT}	1.5	1.8	—	V	—
Dark voltage average	V_{DRK}	—	0.3	2.0	mV	Note 6
Dark signal nonuniformity	DSNU	—	0.5	3.0	mV	Note 6
Image lag	IL	—	0.02	—	%	Note 7
Dynamic range	DR	750	6000	—	—	Note 8
Saturation exposure	SE	0.040	0.060	—	lx · s	Note 9
9V supply current	I_{VDD1}	—	8.0	14.0	mA	—
5V supply current	I_{VDD2}	—	3.0	6.0	mA	—
Total transfer efficiency	TTE	92.0	97.0	—	%	—
Output impedance	Z_O	—	600	—	Ω	—
Offset level	V_{OS}	—	4.5	—	V	Note 10

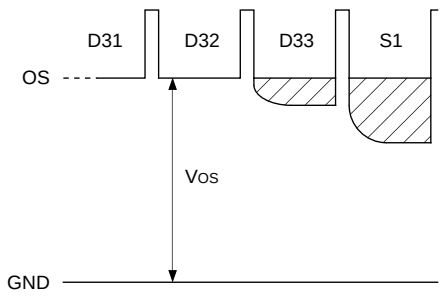
Notes)

1) For the sensitivity test light is applied with a uniform intensity of illumination.
2) W lamp (2854K)
3) Light source: LED λ = 570nm
4) Light source: LED λ = 660nm
5) PRNU is defined as indicated below. Ray incidence conditions are the same as for Note 1.

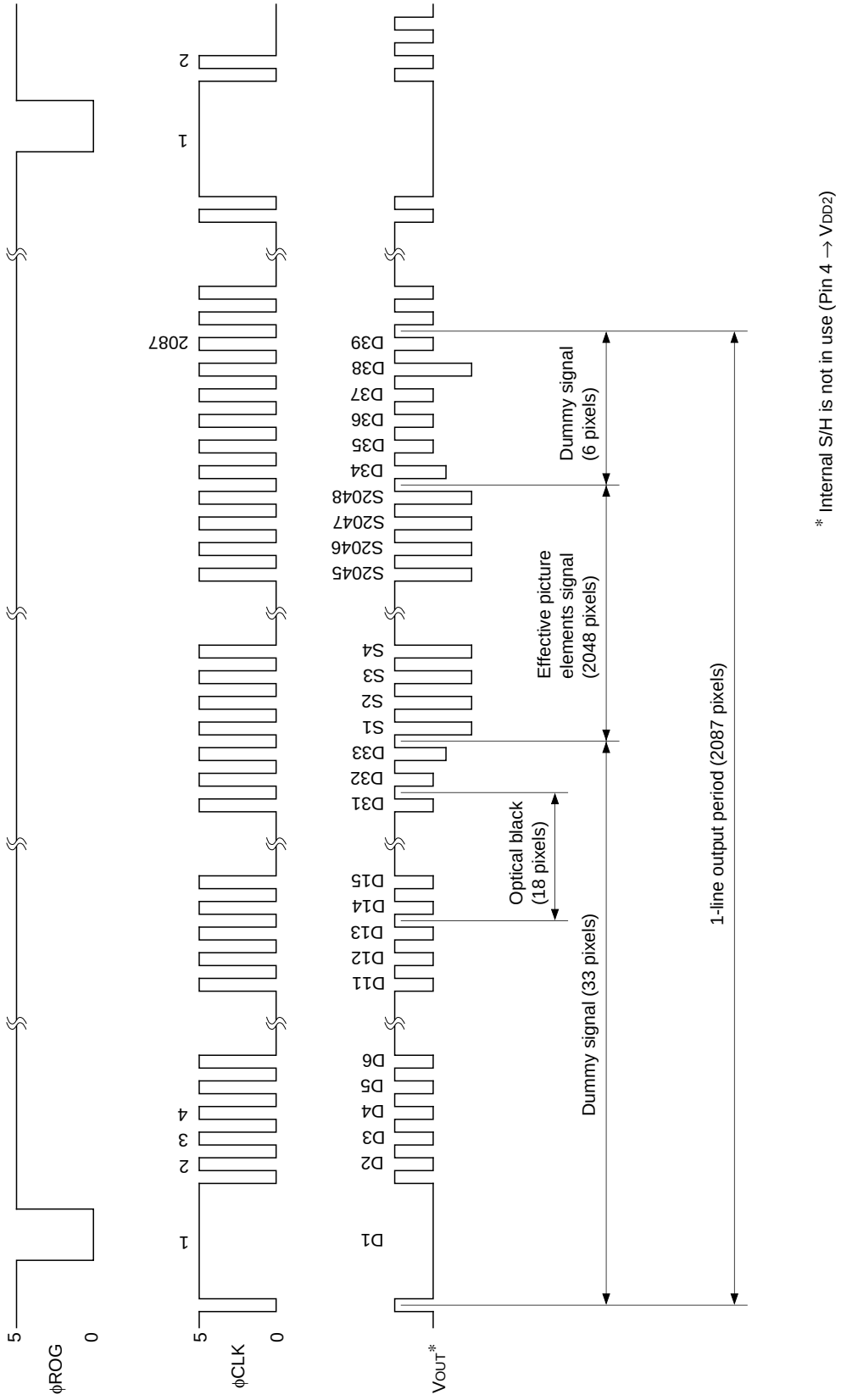
$$PRNU = \frac{(V_{MAX} - V_{MIN})/2}{V_{AVE}} \times 100\ [\%]$$

The maximum output is set to V_{MAX}, the minimum output to V_{MIN} and the average output to V_{AVE}.

6) Integration time is 10ms.
7) V_{OUT} = 500mV
8) DR = V_{SAT}/V_{DRK}
When optical accumulated time is shorter, the dynamic range gets wider because dark voltage is in propagation to optical accumulated time.
9) SE = $V_{SAT}/R1$
10) V_{OS} is defined as indicated below.

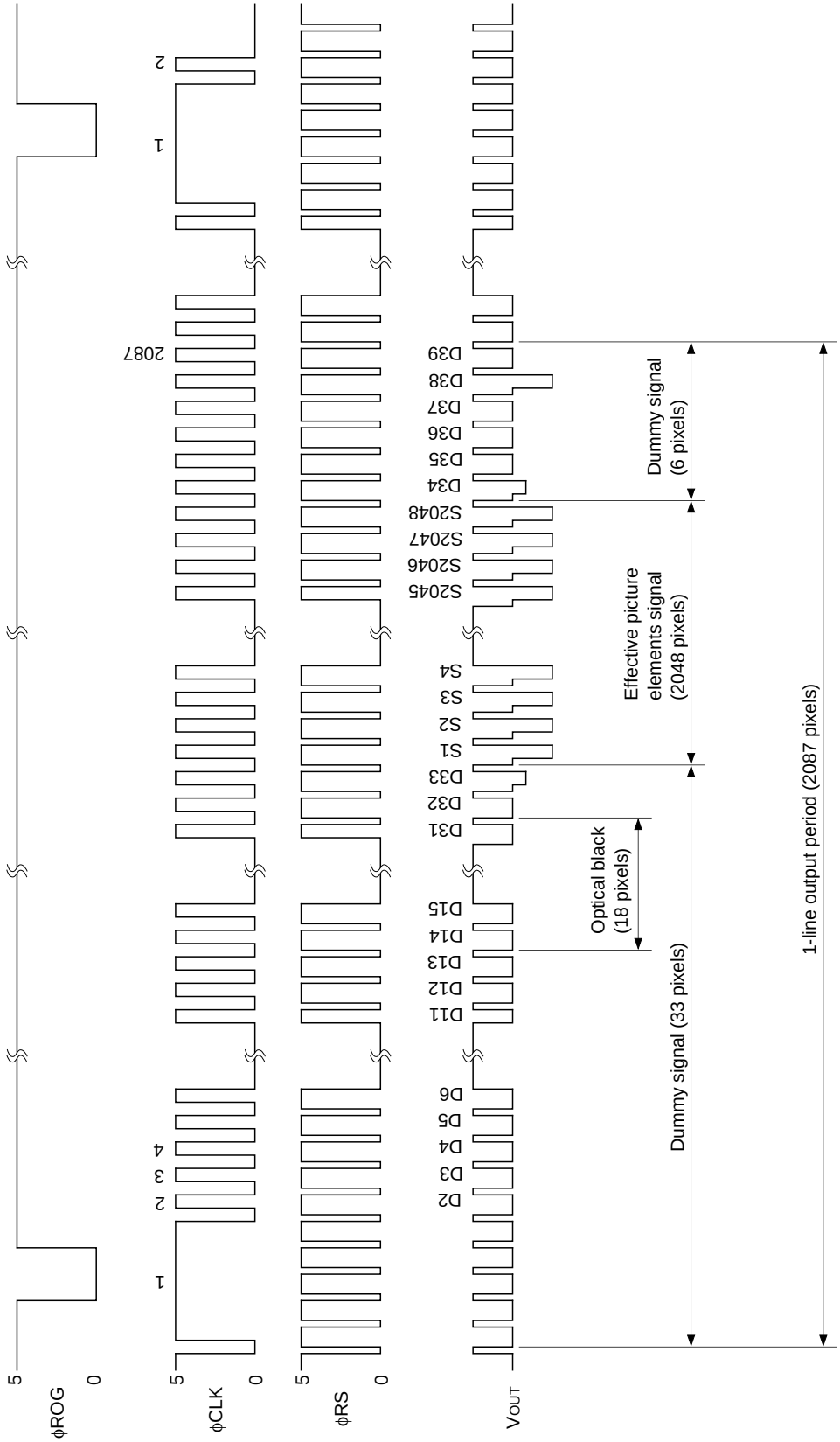


Clock Timing Diagram (For internal RS mode)

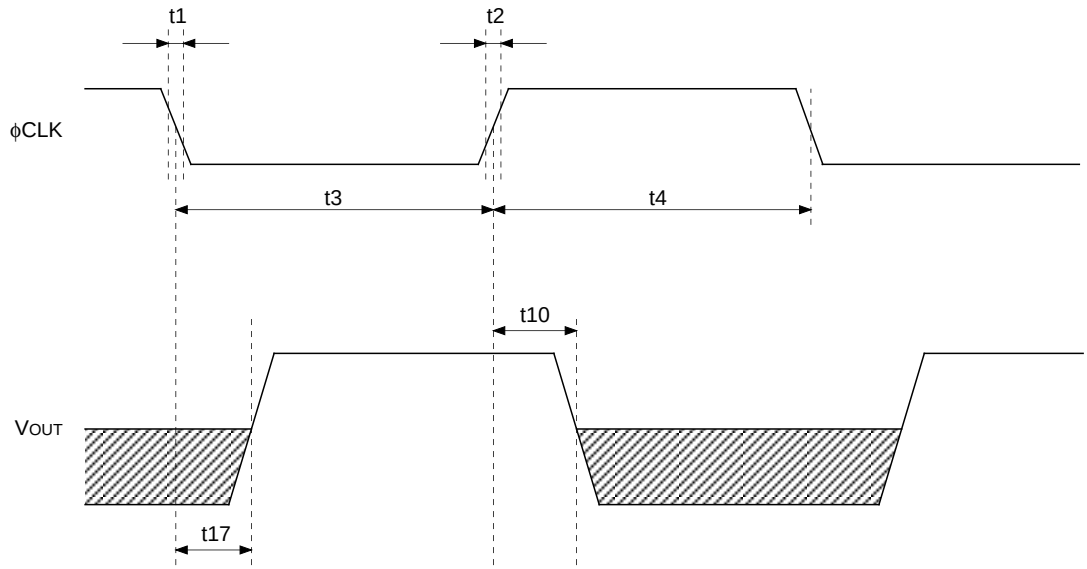


* Internal S/H is not in use (Pin 4 → V_{DD2})

Clock Timing Diagram (For external RS mode)



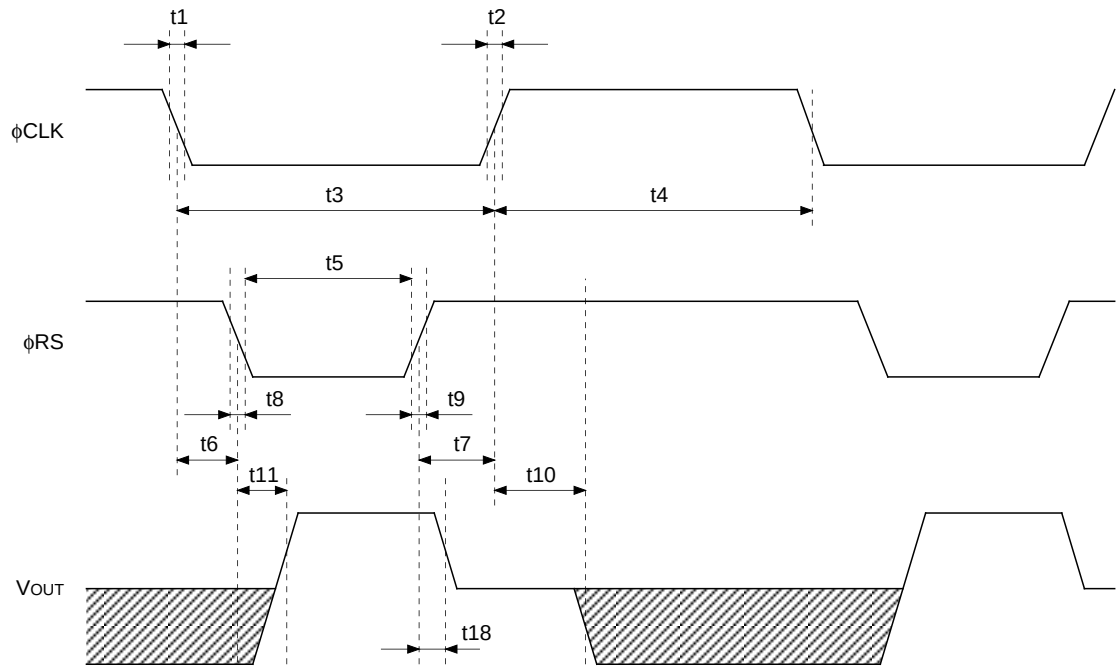
φCLK, VOUT Timing (For internal RS mode)



Item	Symbol	Min.	Typ.	Max.	Unit
φCLK pulse rise/fall time	t1, t2	0	10	—	ns
φCLK pulse duty*1	—	40	50	60	%
φCLK – VOUT 1	t10	50	80	110	ns
φCLK – VOUT 2	t17	30	75	120	ns

*1 $100 \times t3/(t3 + t4)$

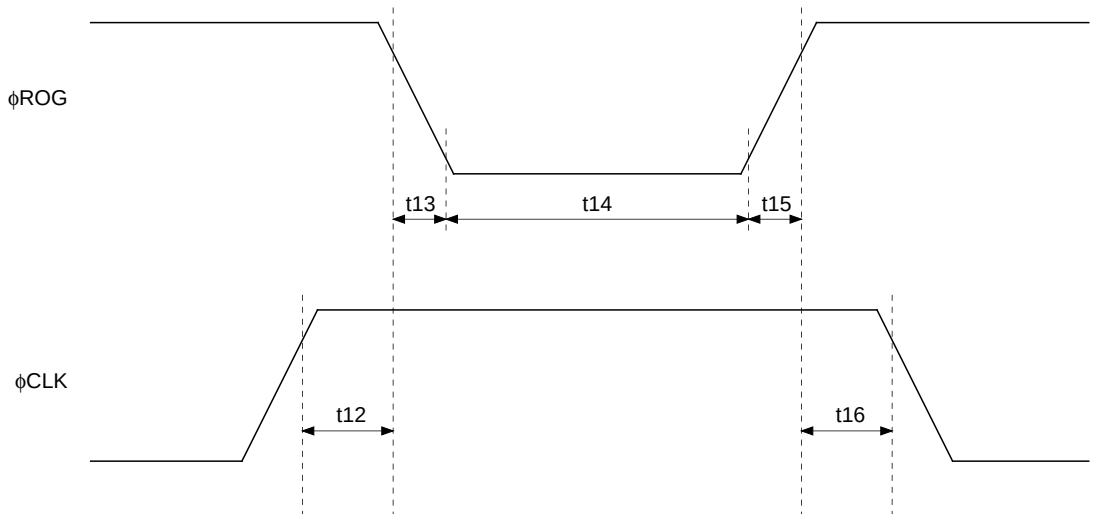
φCLK, φRS, VOUT Timing (For external RS mode)



Item	Symbol	Min.	Typ.	Max.	Unit
φCLK, φRS pulse rise/fall time	t1, t2, t8, t9	—	10	50	ns
φCLK pulse duty*1	—	40	50	60	%
φCLK – φRS pulse timing	t6	0	100	—	ns
φCLK – φRS pulse timing	t7	50	100	—	ns
φRS pulse period	t5	50	100	—	ns
φCLK – VOUT	t10	50	80	110	ns
φRS – VOUT	t11, t18	30	50	70	ns

*1 $100 \times t3/(t3 + t4)$

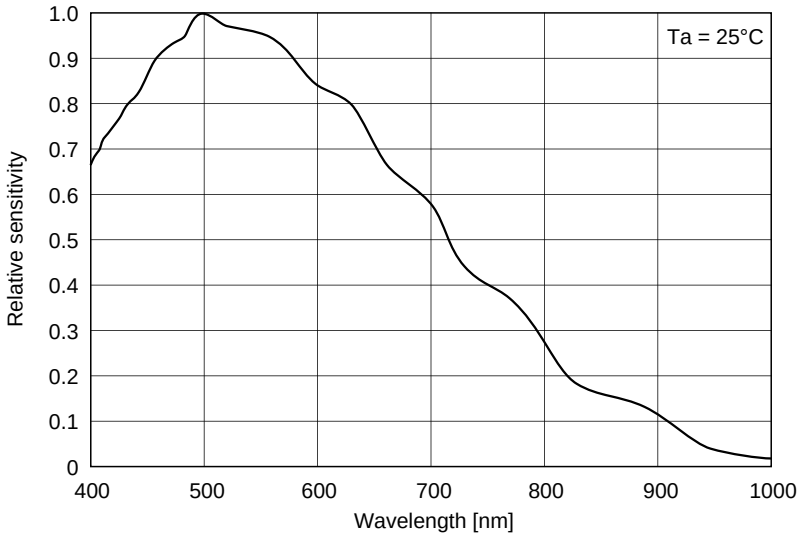
ϕROG, ϕCLK Timing



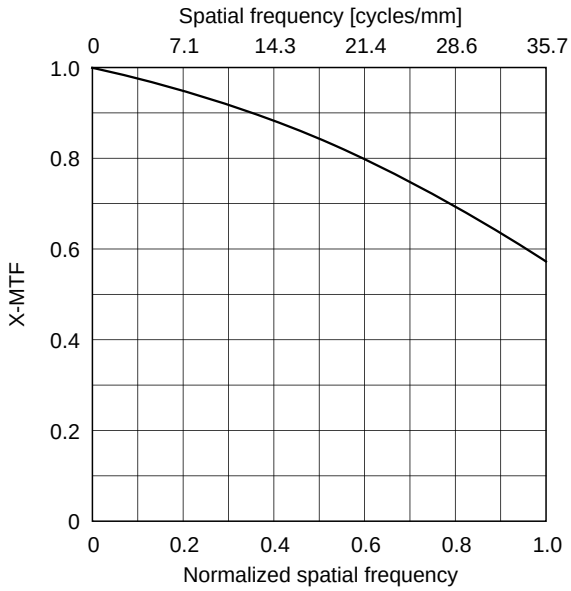
Item	Symbol	Min.	Typ.	Max.	Unit
ϕROG, ϕCLK pulse timing	t12, t16	500	1000	—	ns
ϕROG pulse rise/fall time	t13, t15	0	10	—	ns
ϕROG pulse period	t14	500	1000	—	ns

Example of Representative Characteristics

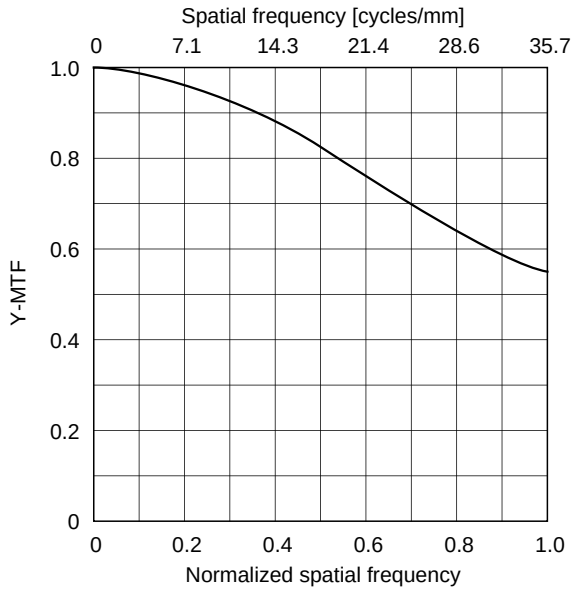
Spectral sensitivity characteristics
(Standard characteristics)



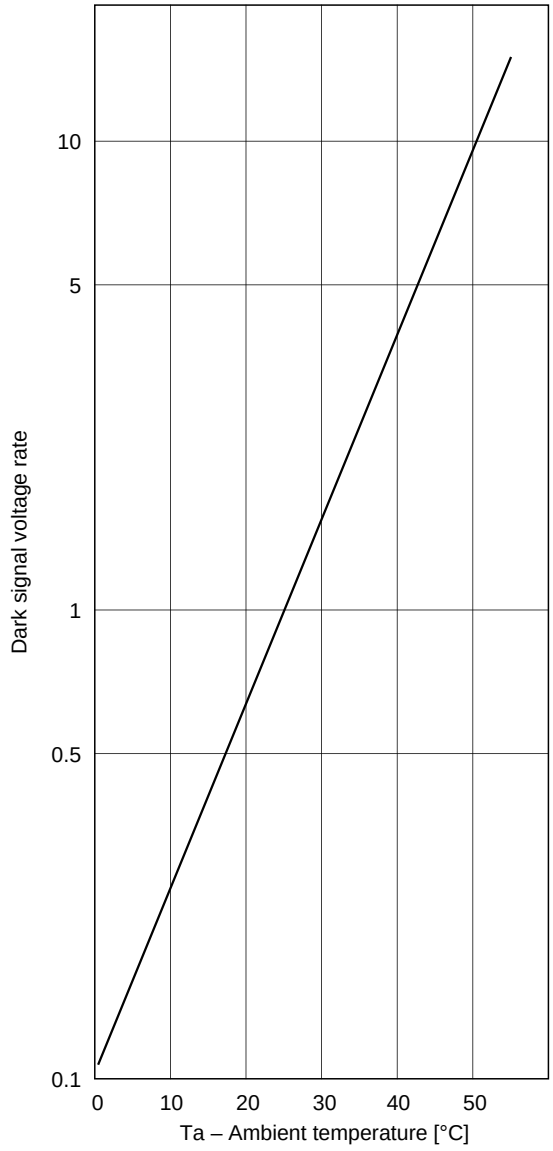
MTF of main scanning direction
(Standard characteristics)



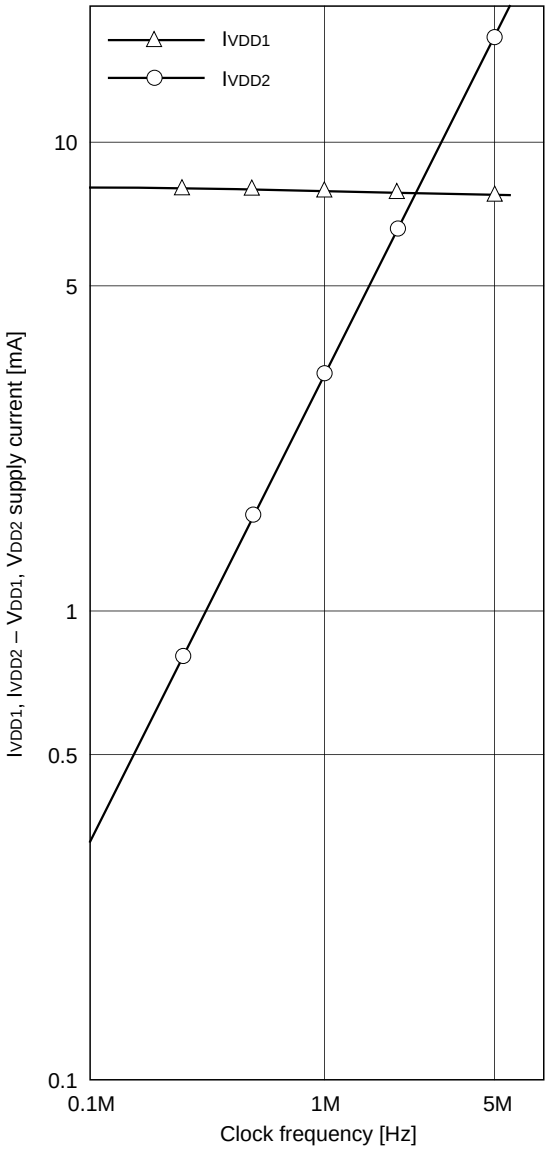
MTF of sub scanning direction
(Standard characteristics)



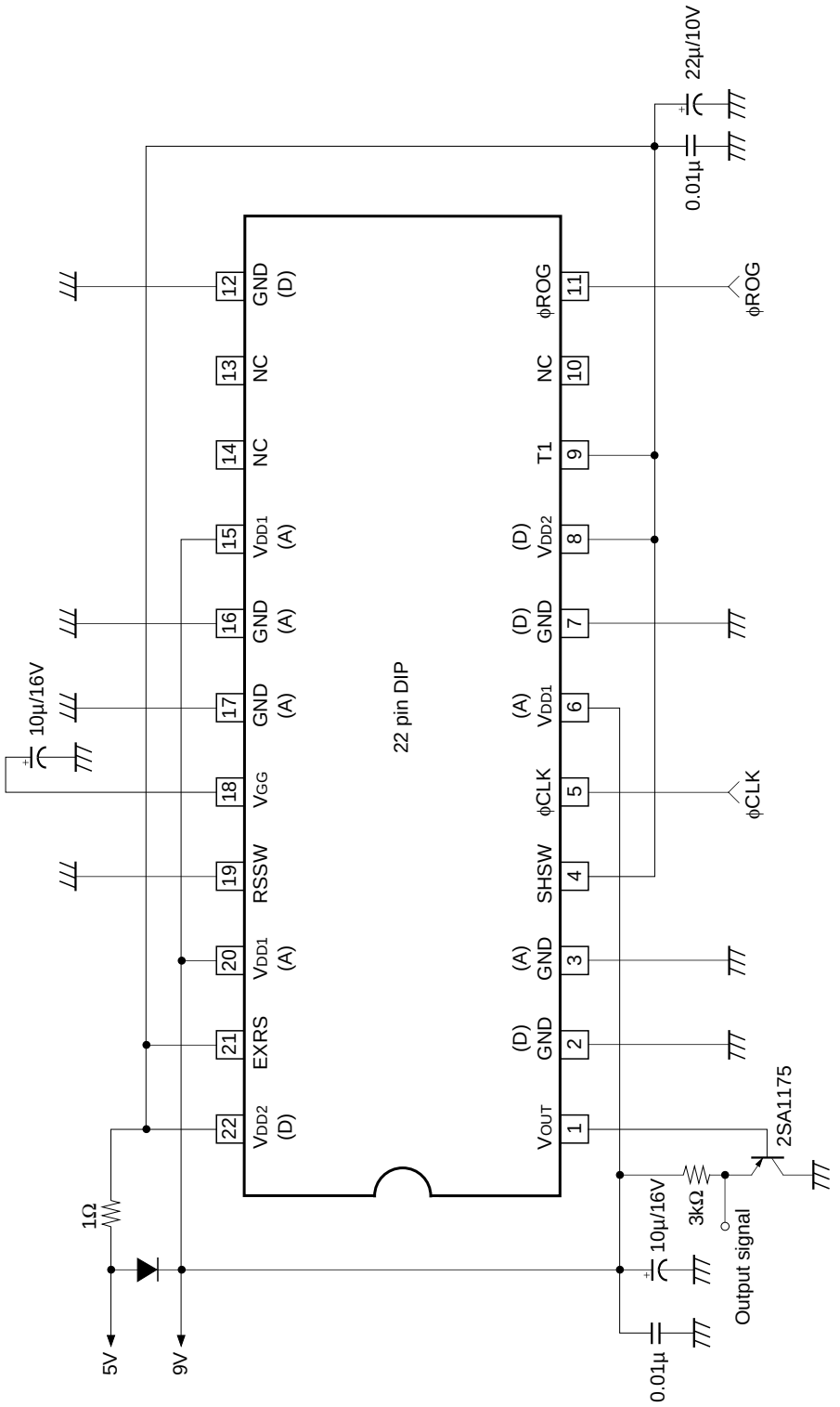
Dark signal voltage rate vs. Ambient temperature (Standard characteristics)



$V_{DD}1$, $V_{DD}2$ supply current vs. Clock frequency (Standard characteristics)



Application Circuit (When internal RS)



Application circuits shown are typical examples illustrating the operation of the devices. Sony cannot assume responsibility for any problems arising out of the use of these circuits or for any infringement of third party patent and other right due to same.

Notes on Handling

1) Static charge prevention
   CCD image sensors are easily damaged by static discharge. Before handling be sure to take the following protective measures.
   a) Either handle bare handed or use non chargeable gloves, clothes or material. Also use conductive shoes.
   b) When handling directly use an earth band.
   c) Install a conductive mat on the floor or working table to prevent the generation of static electricity.
   d) Ionized air is recommended for discharge when handling CCD image sensor.
   e) For the shipment of mounted substrates, use boxes treated for the prevention of static charges.

2) Regulation for raising and lowering the power supply voltage
   When raising the supply voltage, first raise V_{DD1} (9V) and then V_{DD2} (5V). Similarly, lower V_{DD2} (5V) first and then V_{DD1} (9V).

3) Soldering
   a) Make sure the package temperature does not exceed 80°C.
   b) Solder dipping in a mounting furnace causes damage to the glass and other defects. Use a grounded 30W soldering iron and solder each pin in less than 2 seconds. For repairs and remount, cool sufficiently.
   c) To dismount an image sensor, do not use a solder suction equipment. When using an electric desoldering tool, ground the controller. For the control system, use a zero cross type.

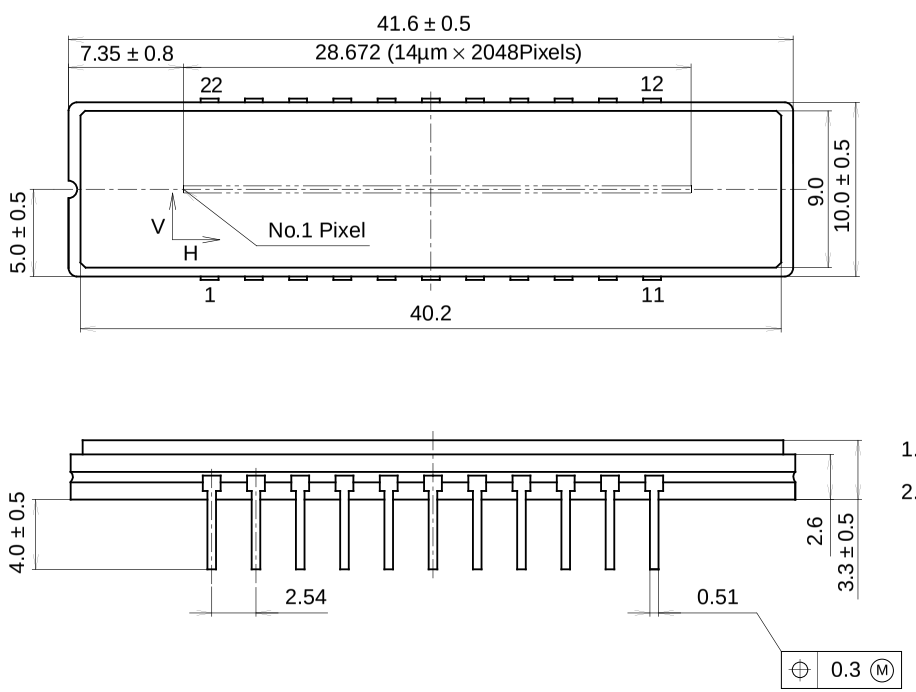
4) Dust and dirt protection
   a) Operate in clean environments.
   b) Do not either touch glass plates by hand or have any object come in contact with glass surfaces. Should dirt stick to a glass surface, blow it off with an air blower. (For dirt stuck through static electricity ionized air is recommended.)
   c) Clean with a cotton bud and ethyl alcohol if the grease stained. Be careful not to scratch the glass.
   d) Keep in a case to protect from dust and dirt. To prevent dew condensation, preheat or precool when moving to a room with great temperature differences.

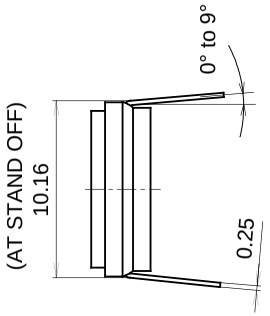
5) Exposure to high temperatures or humidity will affect the characteristics. Accordingly avoid storage or usage in such conditions.

6) CCD image sensors are precise optical equipment that should not be subject to mechanical shocks.

Package Outline Unit: mm

22pin DIP (400mil)





1. The height from the bottom to the sensor surface is 1.61 ± 0.3mm.
2. The thickness of the cover glass is 0.7mm, and the refractive index is 1.5 .

PACKAGE STRUCTURE

PACKAGE MATERIAL	Cer-DIP
LEAD TREATMENT	TIN PLATING
LEAD MATERIAL	42 ALLOY
PACKAGE WEIGHT	3.9g