LT1054 Switched-Capacitor Voltage Converters With Regulators

1 Features

- Output Current, 100 mA
- Low Loss, 1.1 V at 100 mA
- Operating Range, 3.5 V to 15 V
- Reference and Error Amplifier for Regulation
- External Shutdown
- External Oscillator Synchronization
- Devices Can Be Paralleled
- Pin-to-Pin Compatible With the LTC1044/7660

2 Applications

- Industrial Communications (RS232)
- Data Acquisition Supply
- Voltage Inverters
- Voltage Regulators
- Negative Voltage Doublers
- Positive Voltage Doublers

3 Description

The LT1054 device is a bipolar, switched-capacitor voltage converter with regulator. It provides higher output current and significantly lower voltage losses than previously available converters. An adaptive-switch drive scheme optimizes efficiency over a wide range of output currents.

Total voltage drop at 100-mA output current typically is 1.1 V. This applies to the full supply-voltage range of 3.5 V to 15 V. Quiescent current typically is 2.5 mA.

The LT1054 also provides regulation, a feature previously not available in switched-capacitor voltage converters. By adding an external resistive divider, a regulated output can be obtained. This output is regulated against changes in both input voltage and output current. The LT1054 can also shut down by grounding the feedback terminal. Supply current in shutdown typically is 100 µA.

The internal oscillator of the LT1054 runs at a nominal frequency of 25 kHz. The oscillator terminal can be used to adjust the switching frequency or to externally synchronize the LT1054.

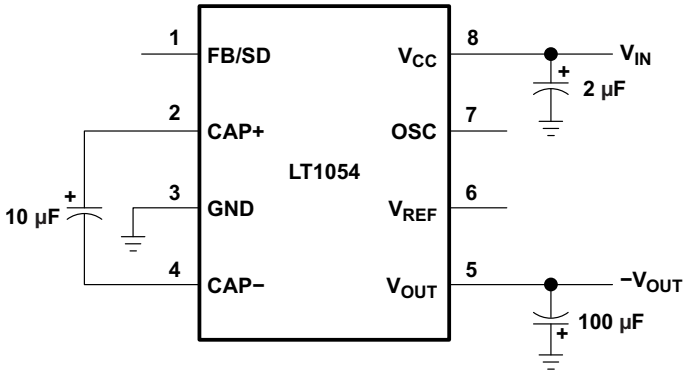
The LT1054C is characterized for operation over a free-air temperature range of 0°C to 70°C. The LT1054I is characterized for operation over a free-air temperature range of −40°C to 85°C.

Device Information(1)

PART NUMBER	PACKAGE	BODY SIZE (NOM)
LT1054	PDIP (8)	9.50 mm × 6.35 mm
	SOIC (16)	10.30 mm × 10.30 mm

(1) For all available packages, see the orderable addendum at the end of the data sheet.

Basic Voltage Inverter



An IMPORTANT NOTICE at the end of this data sheet addresses availability, warranty, changes, use in safety-critical applications, intellectual property matters and other important disclaimers. PRODUCTION DATA.

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4 Revision History

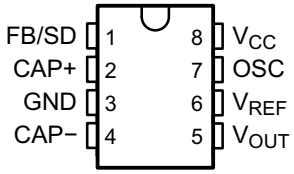
NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Revision F (November 2004) to Revision G	Page
• Added *ESD Ratings* table, *Feature Description* section, *Device Functional Modes*, *Application and Implementation* section, *Power Supply Recommendations* section, *Layout* section, *Device and Documentation Support* section, and *Mechanical, Packaging, and Orderable Information* section.	1

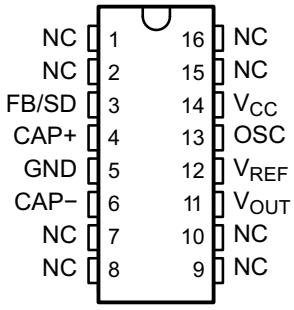
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5 Pin Configuration and Functions

P Package
8-Pin PDIP
Top View



DW Package
16-Pin SOIC
Top View



NC − No internal connection

Pin Functions

PIN			I/O	DESCRIPTION
NAME	PDIP	SOIC		
FB/SD	1	3	Input	Shutdown for low Iq operation or error amp input for regulation
CAP+	2	4	Input	Positive side of CIN
GND	3	5	—	Ground
CAP-	4	6	Input	Negative side of CIN
V_{OUT}	5	11	Output	Regulated output voltage
V_{REF}	6	12	Output	Internal Reference Voltage
OSC	7	13	Input	Oscillator control pin
V_{CC}	8	14	—	Supply pin
NC	—	1, 2, 7, 8, 9, 10, 15, 16	—	No connect (no internal connection)

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6 Specifications

6.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)(1)

			MIN	MAX	UNIT
V_{CC}	Supply voltage(2)			16	V
V_I	Input voltage	FB/SD	0	V_{CC}	V
		OSC	0	V_{ref}	V
T_J	Junction temperature(3)	LT1054C		125	°C
		LT1054I		135	°C
T_{stg}	Storage temperature		–55	150	°C

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) The absolute maximum supply-voltage rating of 16 V is for unregulated circuits. For regulation-mode circuits with $V_{OUT} \leq 15$ V, this rating may be increased to 20 V.
(3) The devices are functional up to the absolute maximum junction temperature.

6.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human body model (HBM), per ANSI/ESDA/JEDEC JS-001(1)	±500	V
		Charged-device model (CDM), per JEDEC specification JESD22-C101(2)	±3500	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

6.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

			MIN	MAX	UNIT
V_{CC}	Supply voltage		3.5	15	V
T_A	Operating free-air temperature range	LT1054C	0	70	°C
		LT1054I	–40	85	

6.4 Thermal Information

THERMAL METRIC(1)		LT1054		UNIT
		P (PDIP)	DW (SOIC)	
		8 PINS	16 PINS	
$R_{\theta JA}$	Junction-to-ambient thermal resistance	85	57	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report, SPRA953.

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6.5 Electrical Characteristics

over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS		T_A (1)	LT1054C, LT1054I			UNIT
					MIN	TYP (2)	MAX	
V_O	Regulated output voltage	V_{CC} = 7 V, T_J = 25°C, R_L = 500 Ω (3)		25°C	−4.7	−5	−5.2	V
	Input regulation	V_{CC} = 7 V to 12 V, R_L = 500 Ω (3)		Full range		5	25	mV
	Output regulation	V_{CC} = 7 V, R_L = 100 Ω to 500 Ω (3)		Full range		10	50	mV
	Voltage loss, $V_{CC} - \lvert V_O \rvert$ (4)	$C_I = C_O$ = 100-µF tantalum	I_O = 10 mA	Full range		0.35	0.55	V
			I_O = 100 mA			1.1	1.6	
	Output resistance	ΔI_O = 10 mA to 100 mA	See (5)	Full range		10	15	Ω
	Oscillator frequency	V_{CC} = 3.5 V to 15 V		Full range	15	25	35	kHz
V_{ref}	Reference voltage	$I_{(REF)}$ = 60 µA		25°C	2.35	2.5	2.65	V
				Full range	2.25		2.75	
	Maximum switch current			25°C		300	4	mA
I_{CC}	Supply current	I_O = 0	V_{CC} = 3.5 V	Full range		2.5	5	mA
			V_{CC} = 15 V			3	200	
	Supply current in shutdown	$V_{(FB/SD)}$ = 0 V		Full range		100		µA

(1) Full range is 0°C to 70°C for the LT1054C and −40°C to 85°C for the LT1054I.
(2) All typical values are at T_A = 25°C.
(3) All regulation specifications are for a device connected as a positive-to-negative converter/regulator with R1 = 20 kΩ, R2 = 102.5 kΩ, external capacitor C_{IN} = 10 µF (tantalum), external capacitor C_{OUT} = 100 µF (tantalum) and C1 = 0.002 µF (see).
(4) For voltage-loss tests, the device is connected as a voltage inverter, with terminals 1, 6, and 7 unconnected. The voltage losses may be higher in other configurations. C_{IN} and C_{OUT} are external capacitors.
(5) Output resistance is defined as the slope of the curve (ΔV_O versus ΔI_O) for output currents of 10 mA to 100 mA. This represents the linear portion of the curve. The incremental slope of the curve is higher at currents less than 10 mA due to the characteristics of the switch transistors.

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6.6 Typical Characteristics

Data at high and low temperatures are applicable only within the recommended operating free-air temperature range.

Table 1. Table of Graphs

		FIGURE
Shutdown threshold voltage	vs Free-air temperature	Figure 1
Supply current	vs Input voltage	Figure 2
Oscillator frequency	vs Free-air temperature	Figure 3
Supply current in shutdown	vs Input voltage	Figure 4
Average supply current	vs Output current	Figure 5
Output voltage loss	vs Input capacitance	Figure 6
Output voltage loss	vs Oscillator frequency (10 µF)	Figure 7
Output voltage loss	vs Oscillator frequency (100 µF)	Figure 8
Regulated output voltage	vs Free-air temperature	Figure 9
Reference voltage change	vs Free-air temperature	Figure 10
Voltage loss	vs Output current	Figure 17

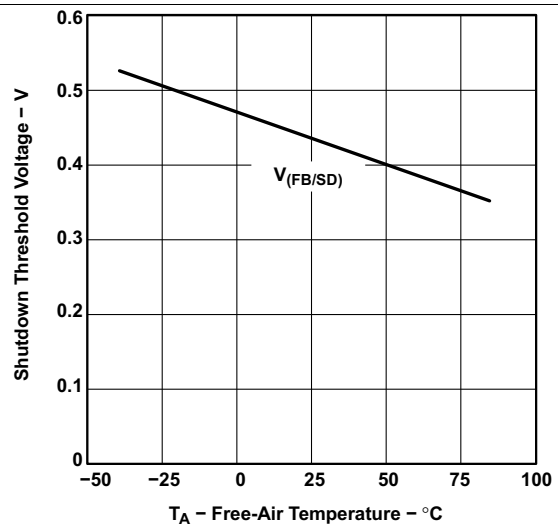


Figure 1. Shutdown Threshold Voltage vs Free-Air Temperature

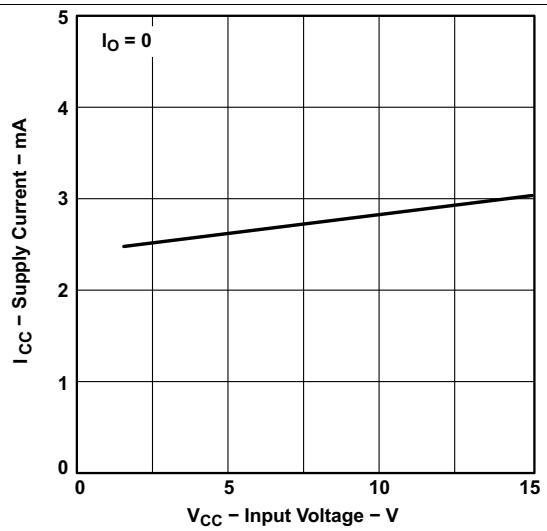


Figure 2. Supply Current vs Input Voltage

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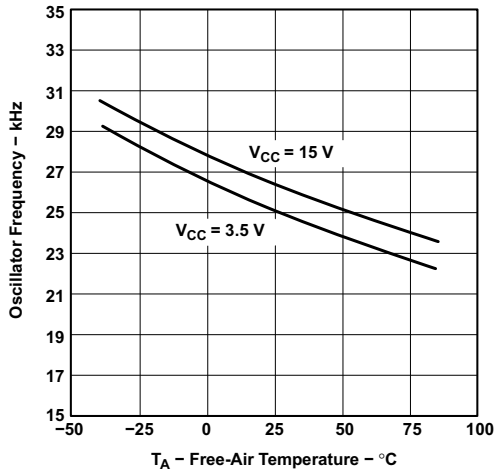


Figure 3. Oscillator Frequency vs Free-air Temperature

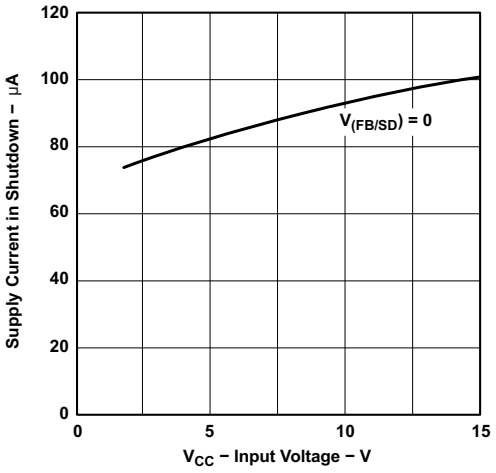


Figure 4. Supply Current in Shutdown vs Input Voltage

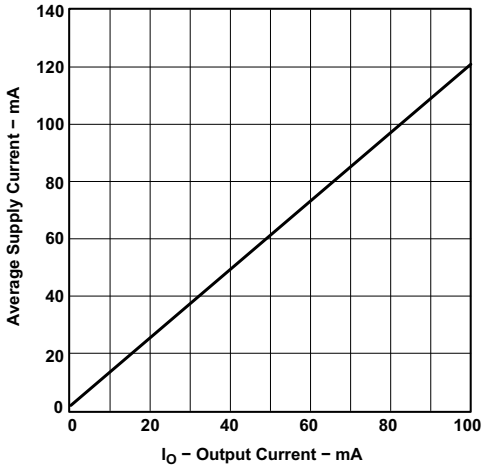


Figure 5. Average Supply Current vs Output Current

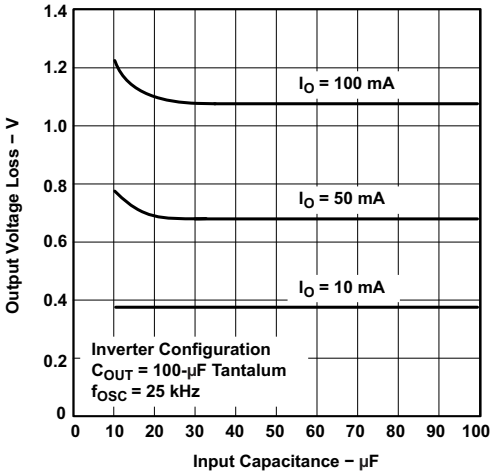


Figure 6. Output Voltage Loss vs Input Capacitance

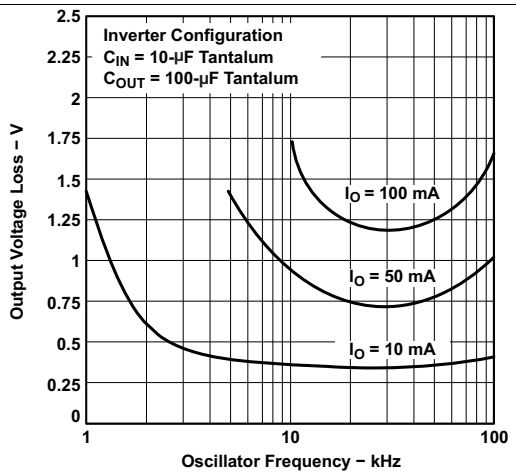


Figure 7. Output Voltage Loss vs Oscillator Frequency

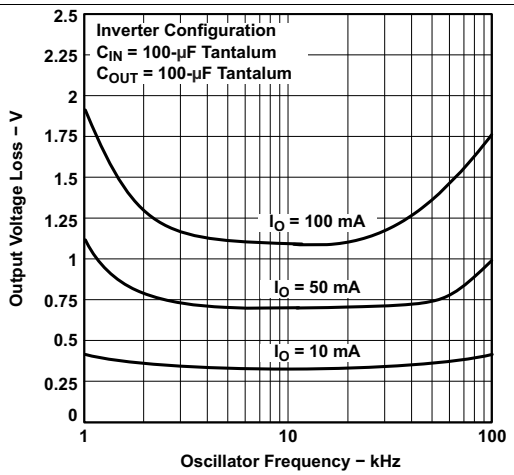


Figure 8. Output Voltage Loss vs Oscillator Frequency

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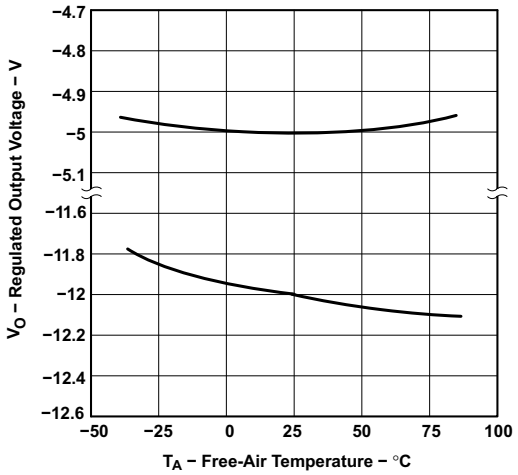


Figure 9. Regulated Output Voltage vs Free-air Temperature

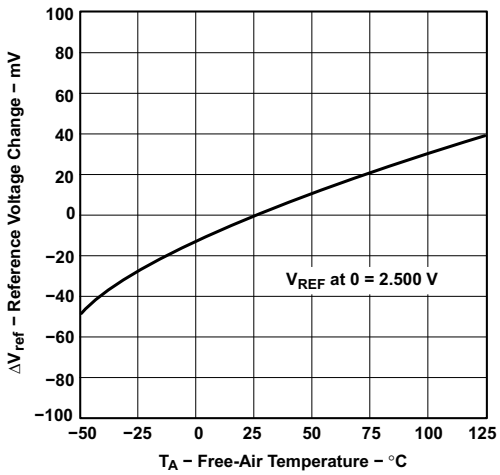


Figure 10. Reference Voltage Change vs Free-air Temperature

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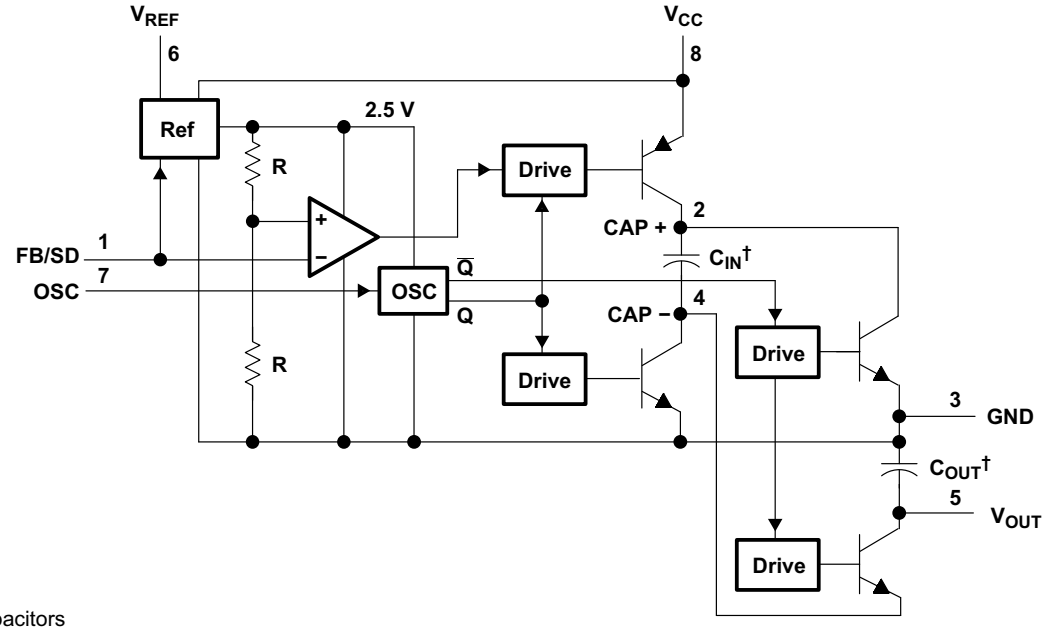
7 Detailed Description

7.1 Overview

LT1054 is a "negative voltage generator" or "negative charge pump" that will output a negative voltage that is proportional to the input voltage (or V_{CC}). With proper supply voltage, V_{OUT} will regulate to an unregulated V_{OUT} that is approximately $-V_{CC}$ (reduced by a small voltage loss). If a lower absolute voltage is desired, V_{OUT} can be regulated to that value when proper feedback resistors are applied.

LT1054 regulates up to 100mA with minimal loss and has a shutdown mode that makes this part optimal across a wide range of applications.

7.2 Functional Block Diagram



† External capacitors

Pin numbers shown are for the P package.

7.3 Feature Description

7.3.1 Reference and Error Amplifier for Regulation

The feedback/shutdown (FB/SD) terminal has two functions. Pulling FB/SD below the shutdown threshold (≈ 0.45 V) puts the device into shutdown. In shutdown, the reference/regulator is turned off and switching stops. The switches are set such that both C_{IN} and C_{OUT} are discharged through the output load. Quiescent current in shutdown drops to approximately 100 µA. Any open-collector gate can be used to put the LT1054 into shutdown. For normal (unregulated) operation, the device will restart when the external gate is shut off. In LT1054 circuits that use the regulation feature, the external resistor divider can provide enough pulldown to keep the device in shutdown until the output capacitor (C_{OUT}) has fully discharged. For most applications, where the LT1054 is run intermittently, this does not present a problem because the discharge time of the output capacitor is short compared to the off time of the device. In applications where the device has to start up before the output capacitor (C_{OUT}) has fully discharged, a restart pulse must be applied to FB/SD of the LT1054. Using the circuit shown in Figure 11, the restart signal can be either a pulse (t_p > 100 µs) or a logic high. Diode coupling the restart signal into FB/SD allows the output voltage to rise and regulate without overshoot. The resistor divider R3/R4 shown in Figure 11 should be chosen to provide a signal level at FB/SD of 0.7−1.1 V.

FB/SD also is the inverting input of the LT1054 error amplifier and, as such, can be used to obtain a regulated output voltage.

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Feature Description (continued)

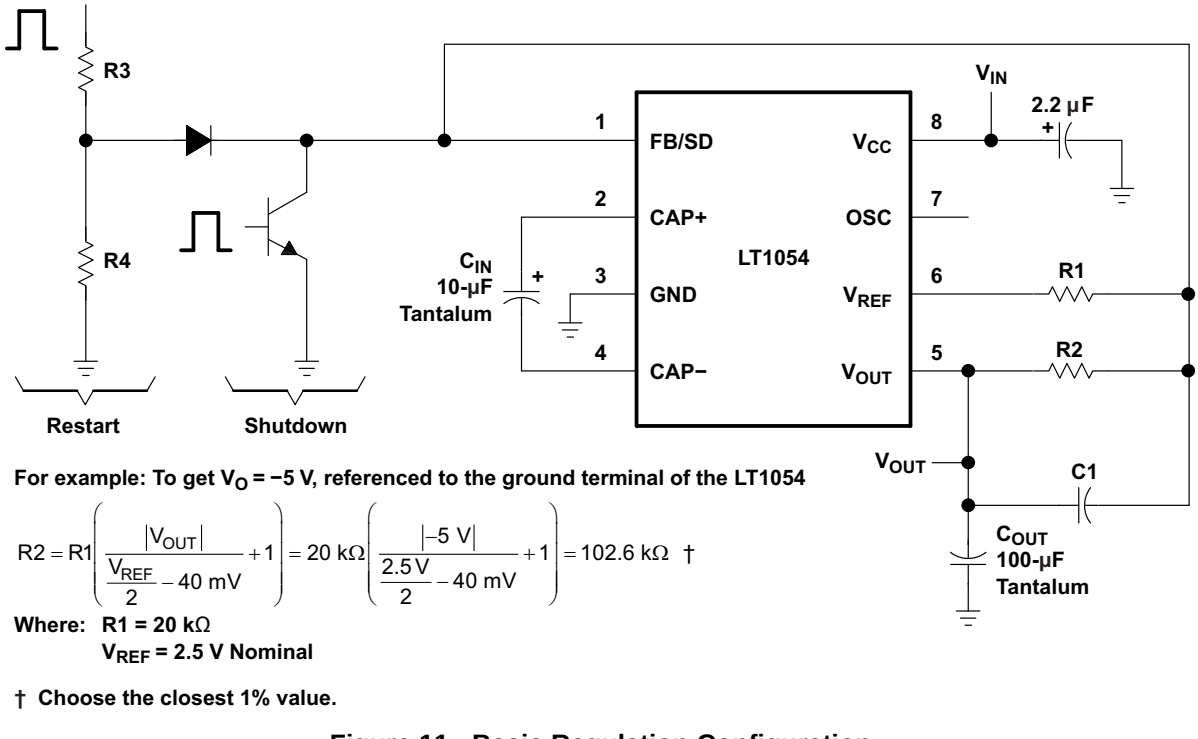


Figure 11. Basic Regulation Configuration

7.3.2 External Oscillator Synchronization

This pin can be used to raise or lower the oscillator frequency or to synchronize the device to an external clock. Internally Pin 7 is connected to the oscillator timing capacitor (Ct ≈ 150pF) which is alternately charged and discharged by current sources of ±7µA so that the duty cycle is ≈50%. The LT1054 oscillator is designed to run in the frequency band where switching losses are minimized. However the frequency can be raised, lowered, or synchronized to an external system clock if necessary.

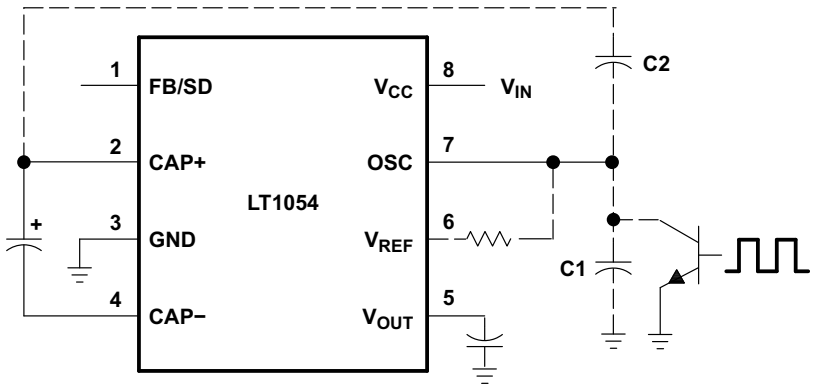


Figure 12. External-Clock System

The frequency can be lowered by adding an external capacitor (C1, Figure 12) from Pin 7 to ground. This will increase the charge and discharge times which lowers the oscillator frequency. The frequency can be increased by adding an external capacitor (C2, Figure 12, in the range of 5pF to 20pF) from Pin 2 to Pin 7. This capacitor will couple charge into CT at the switch transitions, which will shorten the charge and discharge time, raising the oscillator frequency. Synchronization can be accomplished by adding an external resistive pull-up from Pin 7 to

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Feature Description (continued)

the reference pin (Pin 6). A 20k pull-up is recommended. An open collector gate or an NPN transistor can then be used to drive the oscillator pin at the external clock frequency as shown in Figure 12. Pulling up Pin 7 to an external voltage is not recommended. For circuits that require both frequency synchronization and regulation, an external reference can be used as the reference point for the top of the R1/R2 divider allowing Pin 6 to be used as a pullup point for Pin 7.

7.3.3 Output Current and Voltage Loss

The functional block diagram shows that the maximum regulated output voltage is limited by the supply voltage. For the basic configuration, $|V_{OUT}|$ referenced to the ground terminal of the LT1054 must be less than the total of the supply voltage minus the voltage loss due to the switches. The voltage loss versus output current due to the switches can be found in the typical performance curves. Other configurations, such as the negative doubler, can provide higher voltages at reduced output currents.

7.3.4 Reference Voltage

Reference Output. This pin provides a 2.5V reference point for use in LT1054-based regulator circuits. The temperature coefficient of the reference voltage has been adjusted so that the temperature coefficient of the regulated output voltage is close to zero. This requires the reference output to have a positive temperature coefficient as can be seen in the typical performance curves. This nonzero drift is necessary to offset a drift term inherent in the internal reference divider and comparator network tied to the feedback pin. The overall result of these drift terms is a regulated output which has a slight positive temperature coefficient at output voltages below 5V and a slight negative TC at output voltages above 5V. Reference output current should be limited, for regulator feedback networks, to approximately 60µA. The reference pin will draw ≈100µA when shorted to ground and will not affect the internal reference/regulator, so that this pin can also be used as a pull-up for LT1054 circuits that require synchronization.

7.4 Device Functional Modes

7.4.1 Main Operation

A review of a basic switched-capacitor building block is helpful in understanding the operation of the LT1054. When the switch shown in Figure 13 is in the left position, capacitor C1 charges to the voltage at V1. The total charge on C1 is q1 = C1*V1. When the switch is moved to the right, C1 is discharged to the voltage at V2. After this discharge time, the charge on C1 is q2 = C1*V2. The charge has been transferred from the source V1 to the output V2. The amount of charge transferred is shown in Equation 1.

$$\Delta q = q1 - q2 = C1(V1 - V2) \quad (1)$$

If the switch is cycled f times per second, the charge transfer per unit time (that is, current) is as shown in Equation 2.

$$I = f \times L\backslash q = f \times C1(1 - V2) \quad (2)$$

To obtain an equivalent resistance for a switched-capacitor network, this equation can be rewritten in terms of voltage and impedance equivalence as shown in Equation 3.

$$I = \frac{V1 - V2}{(1/fC1)} = \frac{V1 - V2}{R_{EQUIV}} \quad (3)$$

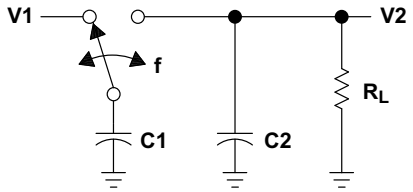


Figure 13. Switched-Capacitor Building Block

Device Functional Modes (continued)

A new variable, R_{EQUIV}, is defined as $R_{EQUIV} = 1 / (f \times C1)$. The equivalent circuit for the switched-capacitor network is shown in Figure 14. The LT1054 has the same switching action as the basic switched-capacitor building block. Even though this simplification does not include finite switch-on resistance and output-voltage ripple, it provides an insight into how the device operates.

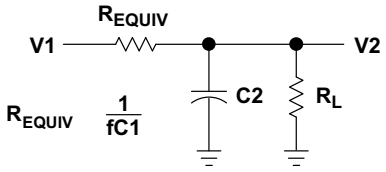


Figure 14. Switched-Capacitor Equivalent Circuit

These simplified circuits explain voltage loss as a function of oscillator frequency (see Figure 7). As oscillator frequency is decreased, the output impedance eventually is dominated by the 1 / (f × C1) term, and voltage losses rise.

Voltage losses also rise as oscillator frequency increases. This is caused by internal switching losses that occur due to some finite charge being lost on each switching cycle. This charge loss per-unit-cycle, when multiplied by the switching frequency, becomes a current loss. At high frequency, this loss becomes significant and voltage losses again rise.

The oscillator of the LT1054 is designed to operate in the frequency band where voltage losses are at a minimum.

7.4.2 Shutdown

LT1054 can be put into a low quiescent current state by grounding the FB/SD pin. Once FB/SD is pulled low, current being drawn from the supply will be approximately 100 µA.

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8 Application and Implementation

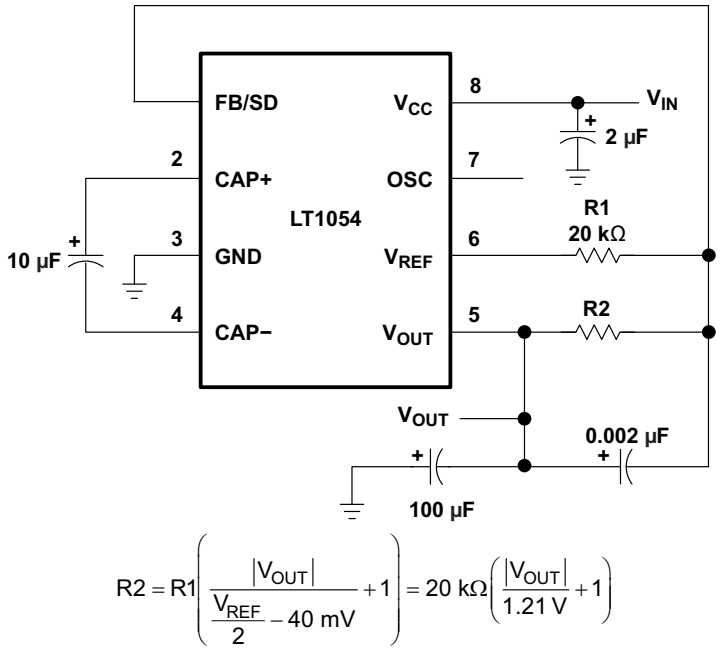
NOTE

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

8.1 Application Information

The negative voltage converting and regulating ability of the LT1054 make this device optimal across a wide range of applications. As it is a regulator, there are many general design considerations that must be taken into account. Below will describe what to consider for using this device as a basic voltage inverter/regulator. This is the most common application for the LT1054 and the fundamental building block for the applications shown in *System Examples*.

8.2 Typical Application



Pin numbers shown are for the P package.

Figure 15. Basic Voltage Inverter/Regulator

8.2.1 Design Requirements

For this design example, use the parameters listed in Table 2 as the input parameters.

Table 2. Design Parameters

Design Parameter	Example Value
Input Voltage Range	3.5V to 15V
V_{OUT}	-5V
I_{OUT}	100mA

8.2.2 Detailed Design Procedure

When using LT1054 as a basic voltage inverter, determine the following:

- Input Voltage
- Desired output Voltage
- Desired Ripple
- Power Dissipation

8.2.2.1 Output Voltage Programming

The error amplifier of the LT1054 drives the PNP switch to control the voltage across the input capacitor (C_{IN}), which determines the output voltage. When the reference and error amplifier of the LT1054 are used, an external resistive divider is all that is needed to set the regulated output voltage. shows the basic regulator configuration and the formula for calculating the appropriate resistor values. R1 should be 20 kΩ or greater because the reference current is limited to ±100 µA. R2 should be in the range of 100 kΩ to 300 kΩ.

8.2.2.2 Capacitor Selection

While the exact values of C_{IN} and C_{OUT} are noncritical, good-quality low-ESR capacitors, such as solid tantalum, are necessary to minimize voltage losses at high currents. For C_{IN}, the effect of the ESR of the capacitor is multiplied by four, because switch currents are approximately two times higher than output current. Losses occur on both the charge and discharge cycle, which means that a capacitor with 1 Ω of ESR for C_{IN} has the same effect as increasing the output impedance of the LT1054 by 4 Ω. This represents a significant increase in the voltage losses. C_{OUT} alternately is charged and discharged at a current approximately equal to the output current. The ESR of the capacitor causes a step function to occur in the output ripple at the switch transitions. This step function degrades the output regulation for changes in output load current and should be avoided. A technique used to gain both low ESR and reasonable cost is to parallel a smaller tantalum capacitor with a large aluminum electrolytic capacitor.

Frequency compensation is accomplished by adjusting the ratio of C_{IN} to C_{OUT}.

For best results, this ratio should be approximately 1:10. Capacitor C1, required for good load regulation, should be 0.002 µF for all output voltages.

8.2.2.3 Output Ripple

The peak-to-peak output ripple is determined by the output capacitor and the output current values. Peak-to-peak output ripple is approximated as:

$$\Delta V = \frac{I_{OUT}}{2fC_{OUT}} \quad (4)$$

where

- ΔV = peak-to-peak ripple
- f_{OSC} = oscillator frequency

For output capacitors with significant ESR, a second term must be added to account for the voltage step at the switch transitions. This step is approximately equal to:

$$(2I_{OUT})(\text{ESR of } C_{OUT}) \quad (5)$$

8.2.2.4 Power Dissipation

The power dissipation of any LT1054 circuit must be limited so that the junction temperature of the device does not exceed the maximum junction-temperature ratings. The total power dissipation is calculated from two components–the power loss due to voltage drops in the switches, and the power loss due to drive-current losses. The total power dissipated by the LT1054 is calculated as:

$$P = (V_{CC} - V_{OUT})\, I_{OUT} + (V_{CC})(I_{OUT})(0.2) \quad (6)$$

where

- both V_{CC} and V_{OUT} are referenced to ground

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The power dissipation is equivalent to that of a linear regulator. Limited power-handling capability of the LT1054 packages causes limited output-current requirements, or steps can be taken to dissipate power external to the LT1054 for large input or output differentials. This is accomplished by placing a resistor in series with C_{IN} as shown in Figure 16. A portion of the input voltage is dropped across this resistor without affecting the output regulation. Since switch current is approximately 2.2 times the output current and the resistor causes a voltage drop when C_{IN} is both charging and discharging, the resistor chosen is as shown:

$$R_x = \frac{V_x}{4.4\ I_{OUT}}$$

where

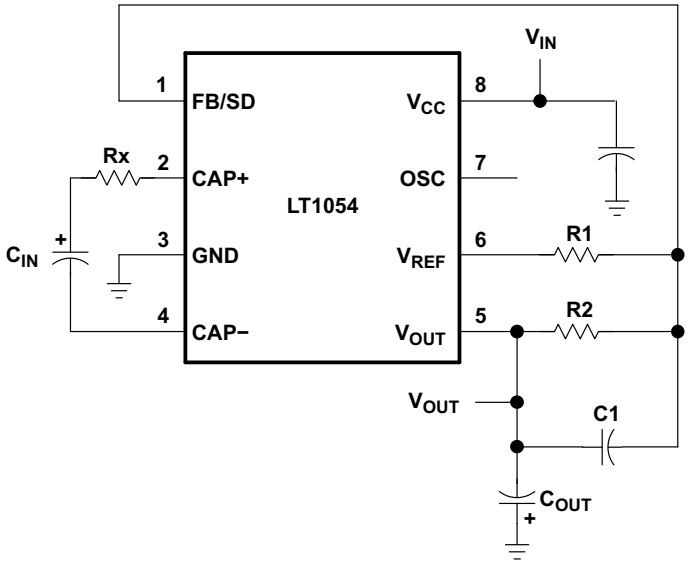
- $V_X \approx V_{CC}$ − [(LT1054 voltage loss)(1.3) + $|V_{OUT}|$]
- I_{OUT} = maximum required output current (7)

The factor of 1.3 allows some operating margin for the LT1054.

When using a 12-V to −5-V converter at 100-mA output current, calculate the power dissipation without an external resistor.

$$P = (12\ V - |-5\ V|)(100\ mA) + (12\ V)(100\ mA)(0.2)$$

$$P = 700\ mW + 240\ mW = 940\ mW \quad (8)$$



Pin numbers shown are for the P package.

Figure 16. Power-Dissipation-Limiting Resistor in Series With CIN

At $R_{\theta JA}$ of 130°C/W for a commercial plastic device, a junction temperature rise of 122°C occurs. The device exceeds the maximum junction temperature at an ambient temperature of 25°C. To calculate the power dissipation with an external resistor (R_X), determine how much voltage can be dropped across RX. The maximum voltage loss of the LT1054 in the standard regulator configuration at 100 mA output current is 1.6 V.

$$V_X = 12\ V - [(1.6\ V)(1.3) + |-5\ V|] = 4.9\ V \quad (9)$$

and

$$R_x = \frac{4.9\ V}{(4.4)(100\ mA)} = 11\ \Omega \quad (10)$$

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The resistor reduces the power dissipated by the LT1054 by (4.9 V)(100 mA) = 490 mW. The total power dissipated by the LT1054 is equal to (940 mW − 490 mW) = 450 mW. The junction-temperature rise is 58°C. Although commercial devices are functional up to a junction temperature of 125°C, the specifications are tested to a junction temperature of 100°C. In this example, this means limiting the ambient temperature to 42°C. To allow higher ambient temperatures, the thermal resistance numbers for the LT1054 packages represent worst-case numbers, with no heat sinking and still air. Small clip-on heat sinks can be used to lower the thermal resistance of the LT1054 package. Airflow in some systems helps to lower the thermal resistance. Wide printed circuit board traces from the LT1054 leads help remove heat from the device. This is especially true for plastic packages.

8.2.3 Application Curve

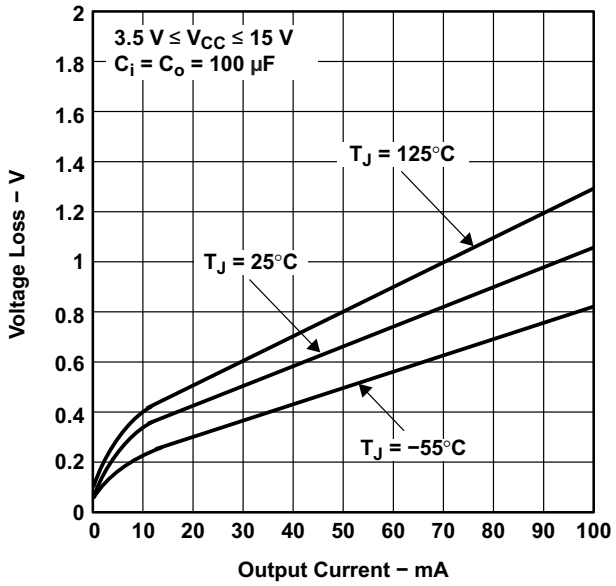
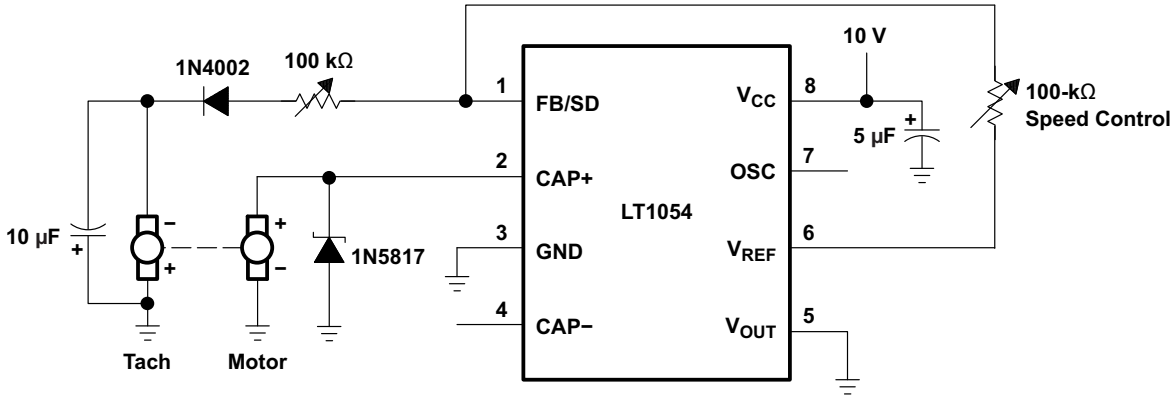


Figure 17. Voltage Loss vs Output Current

8.3 System Examples

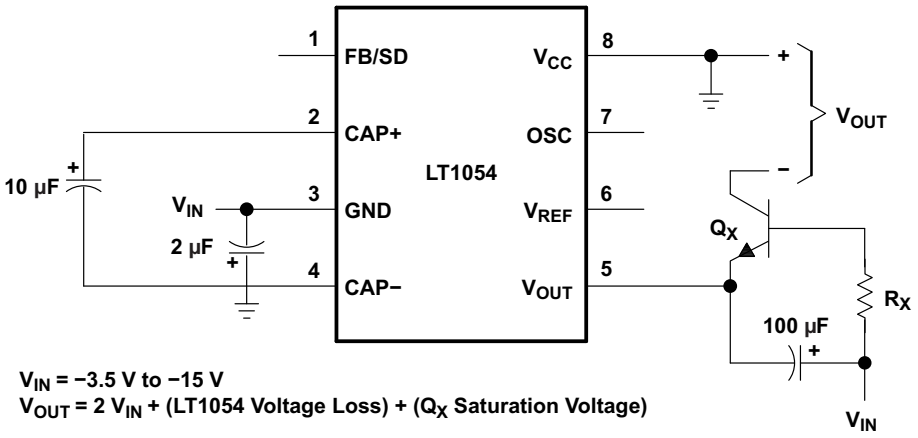


NOTE: Motor-Tach is Canon CKT26-T5-3SAE.
Pin numbers shown are for the P package.

Figure 18. Motor-Speed Servo

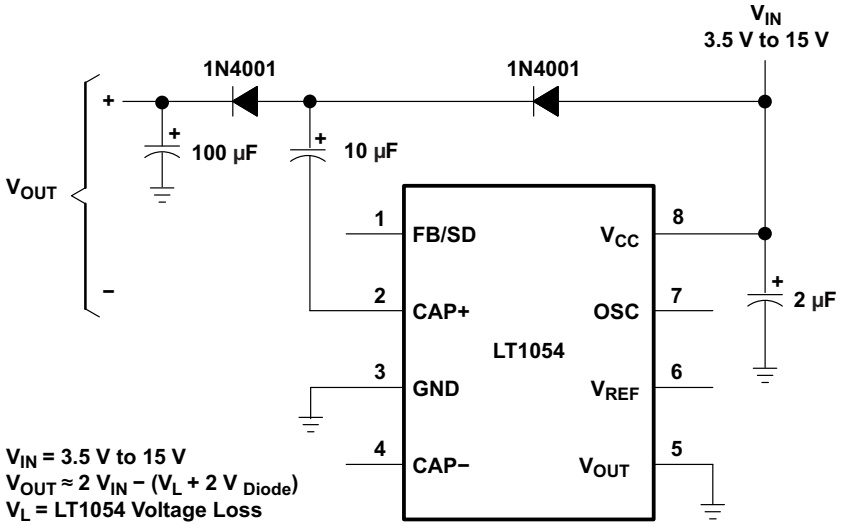
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System Examples (continued)



Pin numbers shown are for the P package.

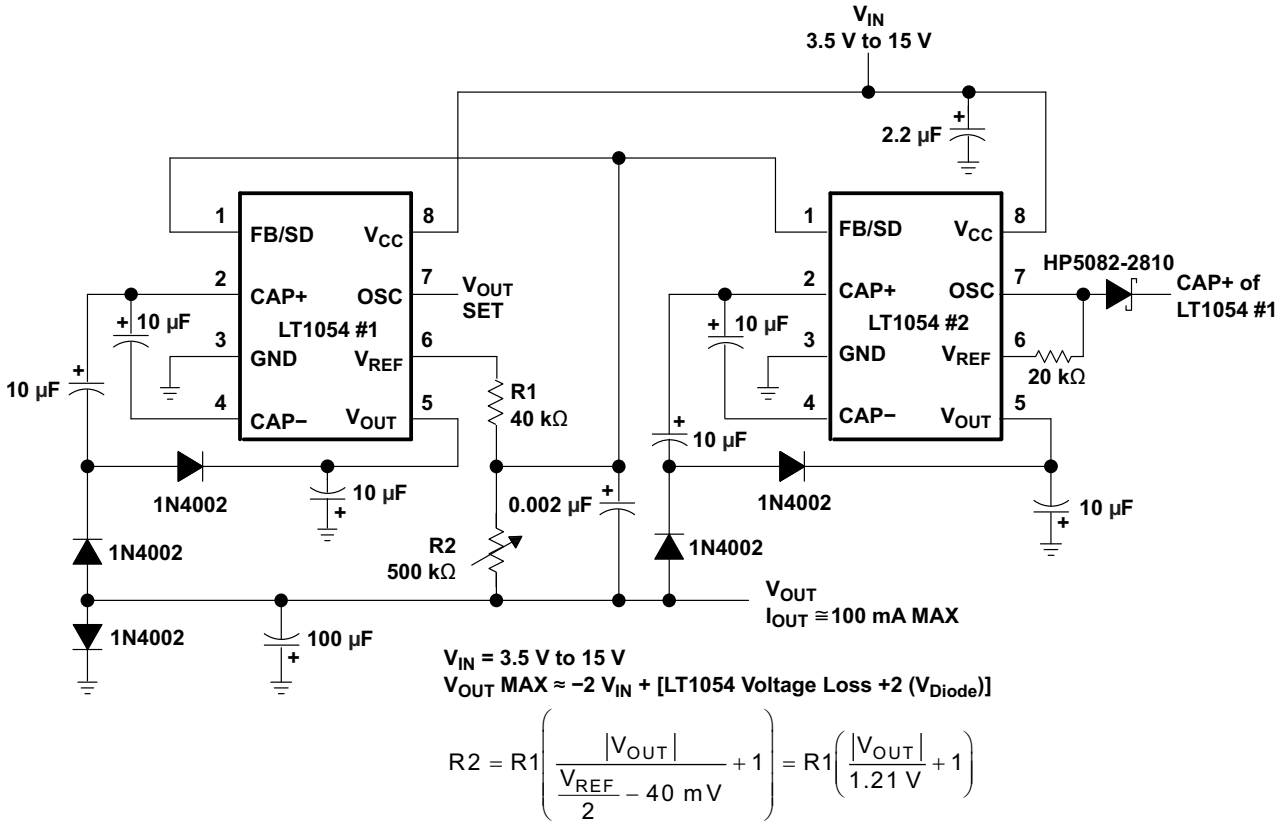
Figure 19. Negative-Voltage Doubler



Pin numbers shown are for the P package.

Figure 20. Positive-Voltage Doubler

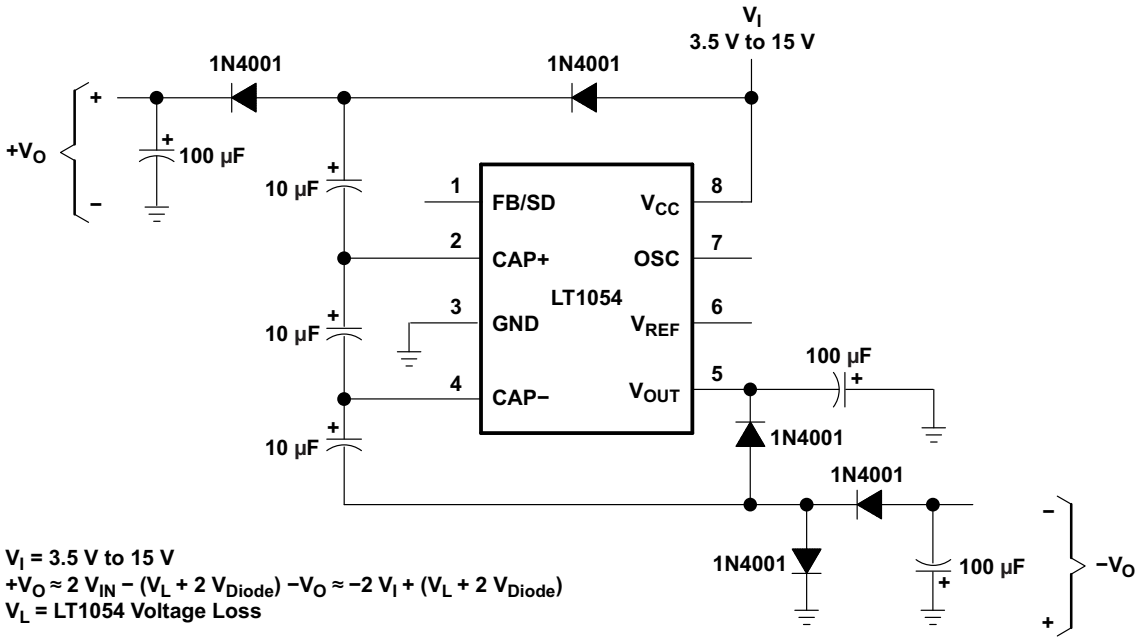
System Examples (continued)



$$R2 = R1\left(\frac{|V_{OUT}|}{\frac{V_{REF}}{2} - 40\ mV} + 1\right) = R1\left(\frac{|V_{OUT}|}{1.21\ V} + 1\right)$$

Pin numbers shown are for the P package.

Figure 21. 100-mA Regulating Negative Doubler

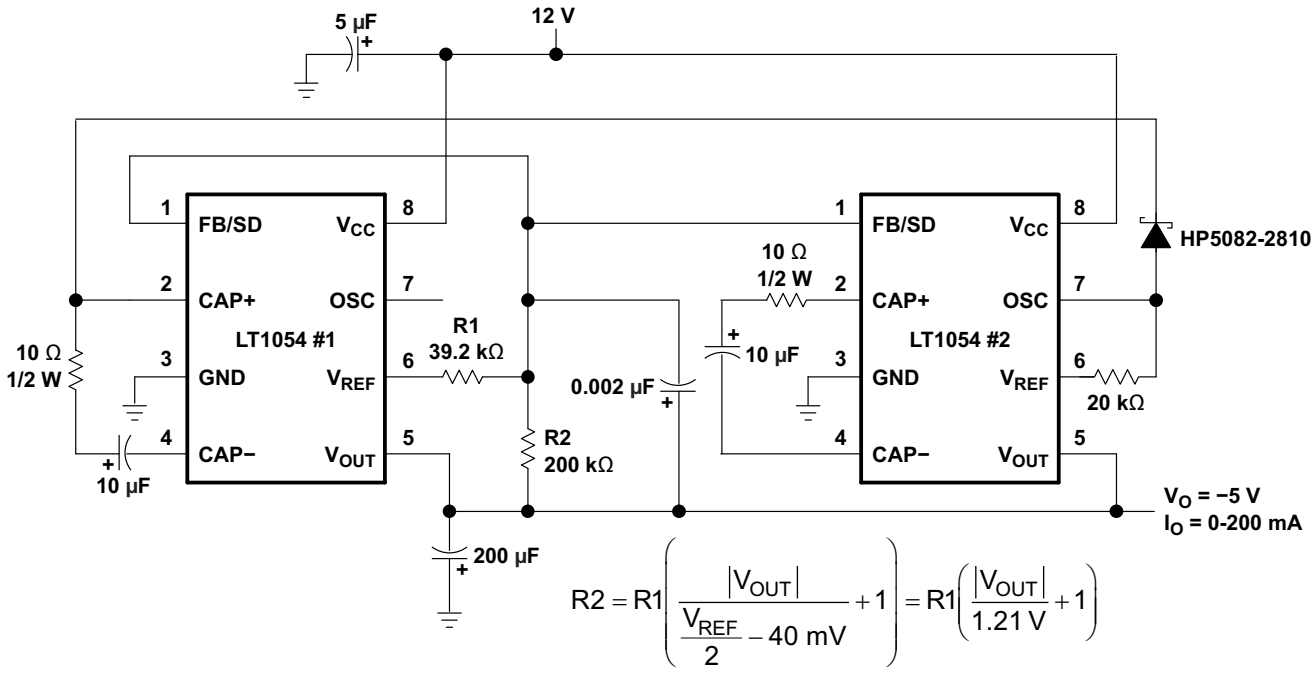


Pin numbers shown are for the P package.

Figure 22. Dual-Output Voltage Doubler

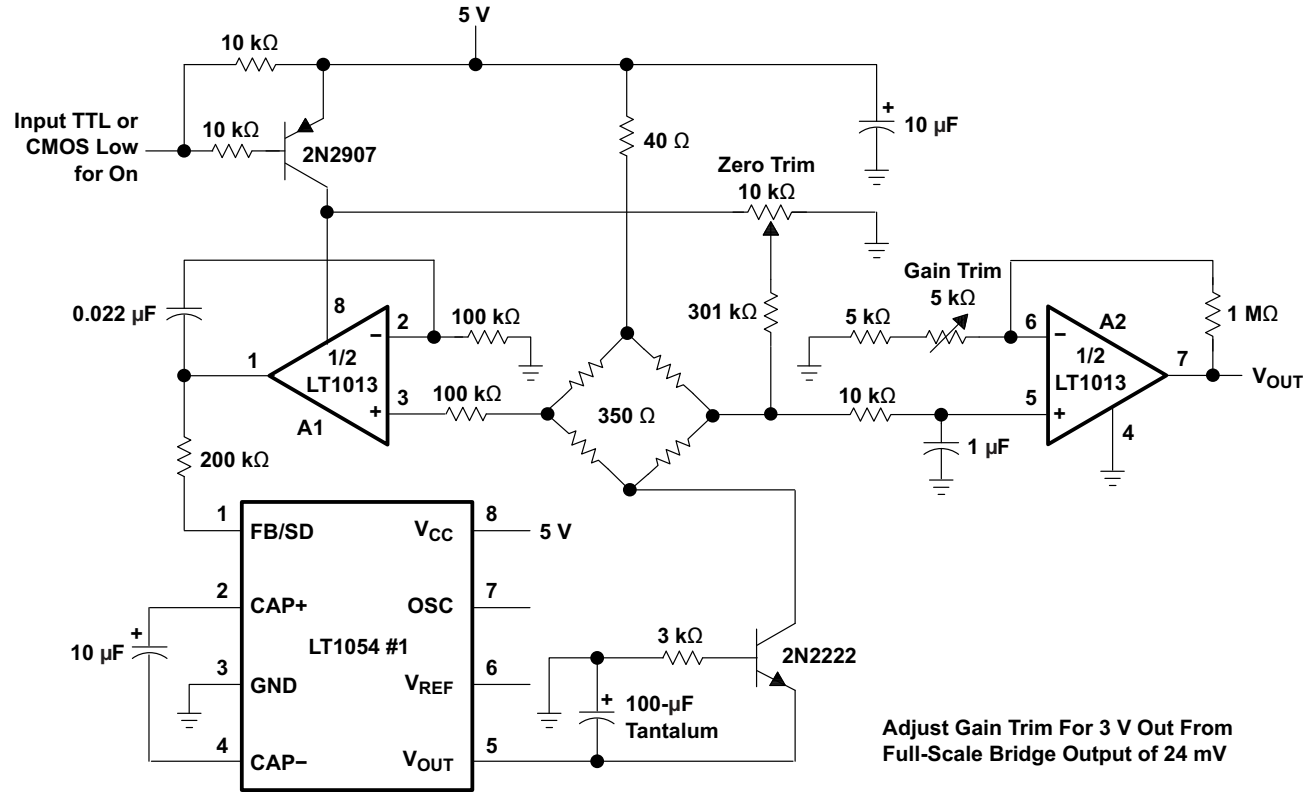
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System Examples (continued)



Pin numbers shown are for the P package.

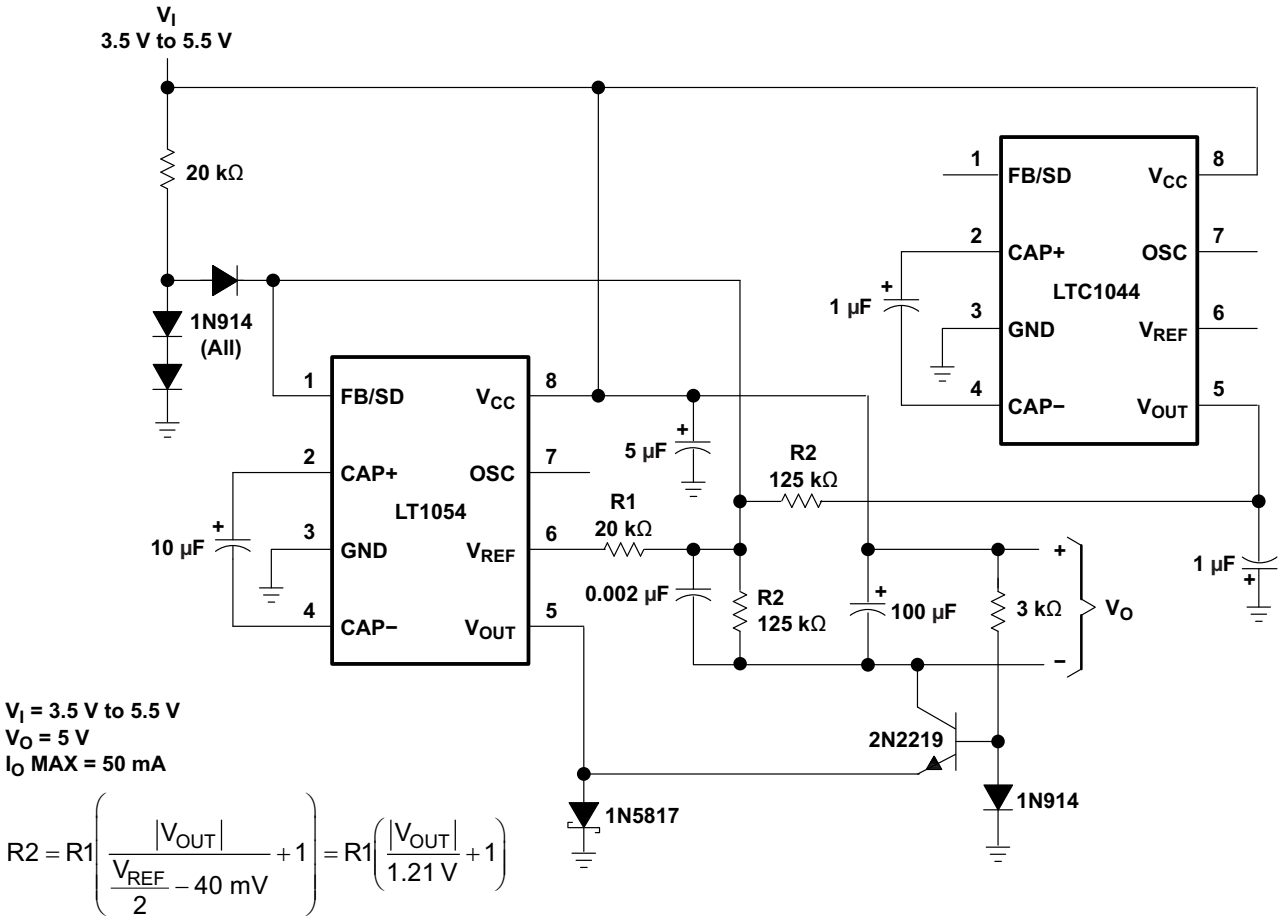
Figure 23. 5-V to ±12-V Converter



Pin numbers shown are for the P package.

Figure 24. Strain-Gage Bridge Signal Conditioner

System Examples (continued)



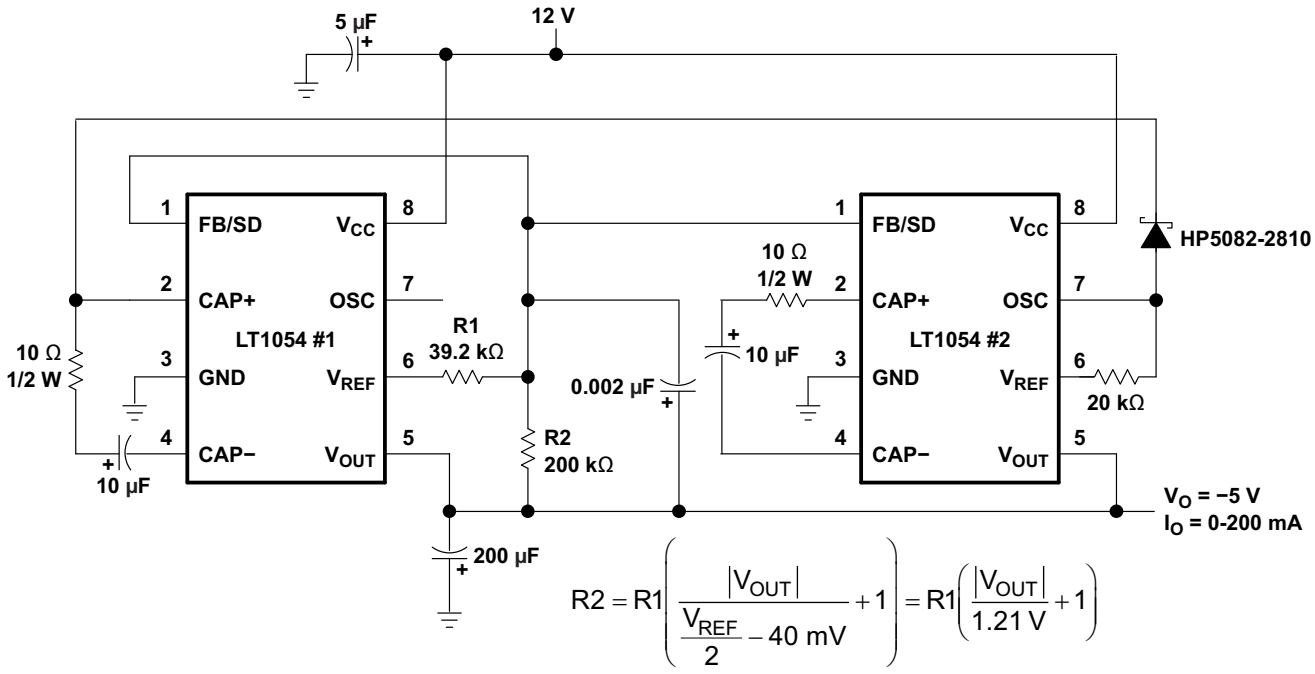
$$R2 = R1\left(\frac{|V_{OUT}|}{\frac{V_{REF}}{2} - 40\ mV} + 1\right) = R1\left(\frac{|V_{OUT}|}{1.21\ V} + 1\right)$$

Pin numbers shown are for the P package.

Figure 25. 3.5-V to 5-V Regulator

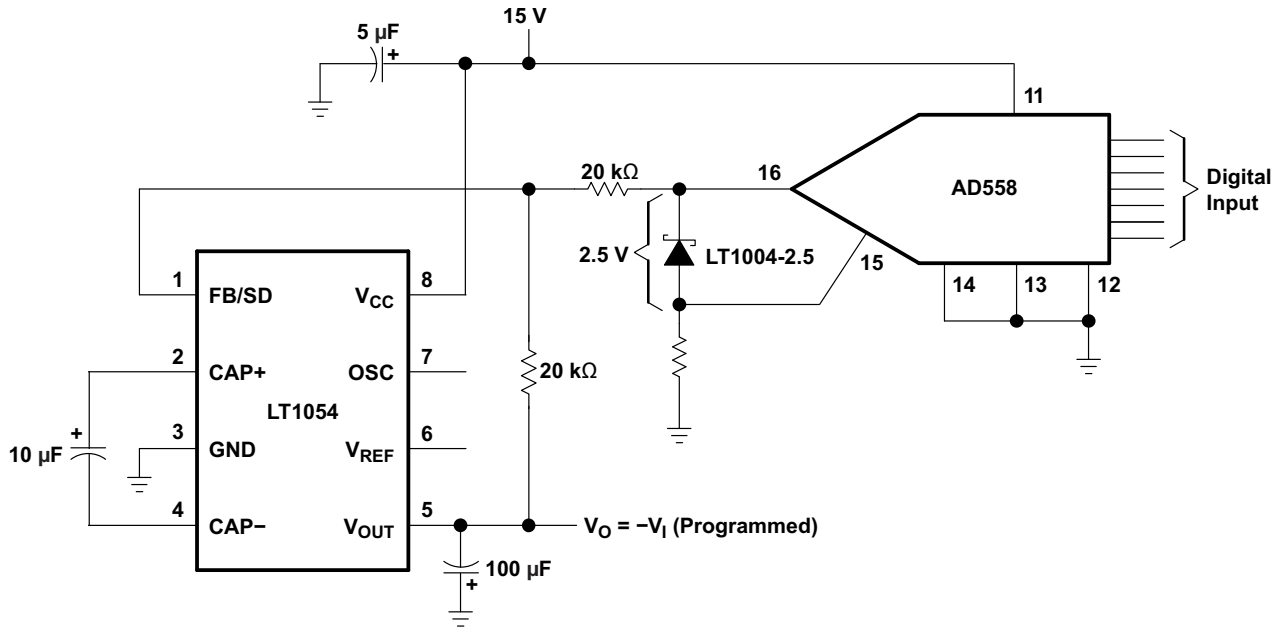
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System Examples (continued)



Pin numbers shown are for the P package.

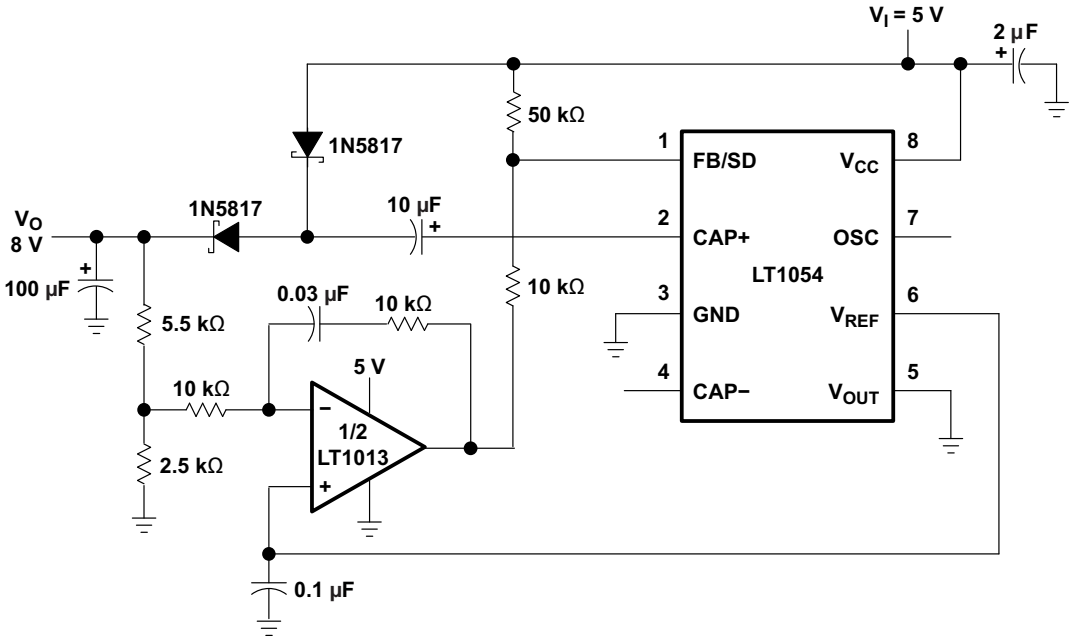
Figure 26. Regulating 200-mA +12-V to −5-V Converter



Pin numbers shown are for the P package.

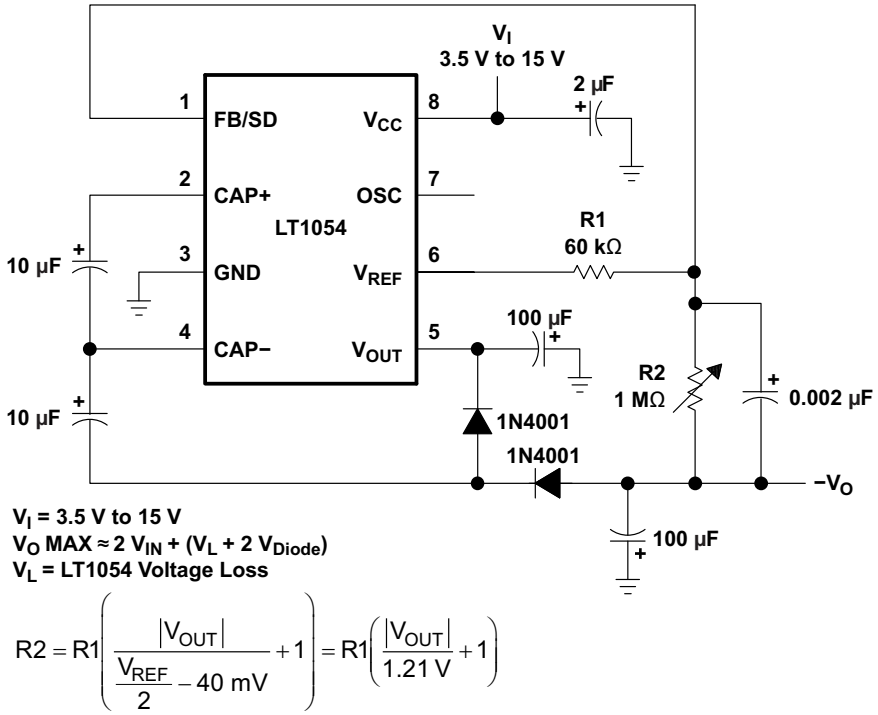
Figure 27. Digitally Programmable Negative Supply

System Examples (continued)



Pin numbers shown are for the P package.

Figure 28. Positive Doubler With Regulation (5-V to 8-V Converter)



$$R2 = R1\left(\frac{|V_{OUT}|}{\frac{V_{REF}}{2} - 40\ mV} + 1\right) = R1\left(\frac{|V_{OUT}|}{1.21\ V} + 1\right)$$

Pin numbers shown are for the P package.

Figure 29. Negative Doubler With Regulator

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9 Power Supply Recommendations

The LT1054 alternately charges C_{IN} to the input voltage when C_{IN} is switched in parallel with the input supply and then transfers charge to C_{OUT} when C_{IN} is switched in parallel with C_{OUT}. Switching occurs at the oscillator frequency. During the time that C_{IN} is charging, the peak supply current will be approximately equal to 2.2 times the output current. During the time that C_{IN} is delivering charge to C_{OUT} the supply current drops to approximately 0.2 times the output current. An input supply bypass capacitor will supply part of the peak input current drawn by the LT1054 and average out the current drawn from the supply. A minimum input supply bypass capacitor of 2µF, preferably tantalum or some other low ESR type is recommended. A larger capacitor may be desirable in some cases, for example, when the actual input supply is connected to the LT1054 through long leads, or when the pulse current drawn by the LT1054 might affect other circuitry through supply coupling.

In addition to being the output terminal, V_{OUT} is tied to the substrate of the device. Special care must be taken in LT1054 circuits to avoid making V_{OUT} positive with respect to any of the other terminals. For circuits with the output load connected from V_{CC} to V_{OUT} or from some external positive supply voltage to V_{OUT}, an external transistor must be added (see Figure 30). This transistor prevents V_{OUT} from being pulled above GND during startup. Any small general-purpose transistor such as a 2N2222 or a 2N2219 device can be used. Resistor R1 should be chosen to provide enough base drive to the external transistor so that it is saturated under nominal output voltage and maximum output current conditions.

$$R1 \leq \frac{(|V_{OUT}|)\beta}{I_{OUT}} \tag{11}$$

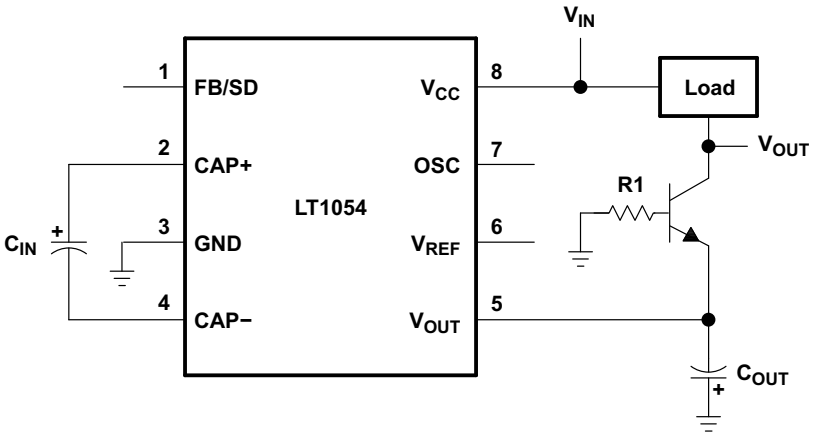


Figure 30. Circuit With Load Connected from V_{CC} to V_{OUT}

10 Layout

10.1 Layout Guidelines

- Try to run the feedback trace as far from the noisy power or clocking traces as possible. In the case that the OSC pin is not being used, as in Figure 31, the FB trace can be ran on a lower layer under the OSC pin. When OSC is being utilized by a noisy clocking signal, it is recommended to run the FB trace on a lower layer through the Vref pin.
  - Keep the FB trace to be as direct as possible and somewhat thick. These two sometimes involve a trade-off, but keeping it away from EMI and other noise sources is the more critical of the two.
- Keep the external capacitor traces short, specifically on the CAP+ and CAP- nodes that have the fastest rise and fall times.
- Make all of the power (high current) traces as short, direct, and thick as possible. It is good practice on a standard PCB board to make the traces an absolute minimum of 15 mils (0.381 mm) per Ampere.

10.2 Layout Example

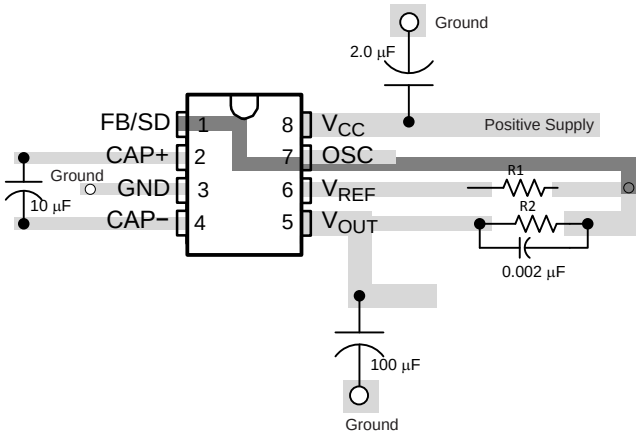


Figure 31. Basic Inverter/Regulator Layout

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11 Device and Documentation Support

11.1 Community Resources

The following links connect to TI community resources. Linked contents are provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

TI E2E™ Online Community ***TI's Engineer-to-Engineer (E2E) Community.*** Created to foster collaboration among engineers. At e2e.ti.com, you can ask questions, share knowledge, explore ideas and help solve problems with fellow engineers.

Design Support ***TI's Design Support*** Quickly find helpful E2E forums along with design support tools and contact information for technical support.

11.2 Trademarks

E2E is a trademark of Texas Instruments.
All other trademarks are the property of their respective owners.

11.3 Electrostatic Discharge Caution



These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

11.4 Glossary

SLYZ022 — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

12 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

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PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
LT1054CDW	ACTIVE	SOIC	DW	16	40	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	0 to 70	LT1054C	Samples
LT1054CDWG4	ACTIVE	SOIC	DW	16	40	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	0 to 70	LT1054C	Samples
LT1054CDWR	ACTIVE	SOIC	DW	16	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	0 to 70	LT1054C	Samples
LT1054CDWRE4	ACTIVE	SOIC	DW	16	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	0 to 70	LT1054C	Samples
LT1054CDWRG4	ACTIVE	SOIC	DW	16	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	0 to 70	LT1054C	Samples
LT1054CP	ACTIVE	PDIP	P	8	50	Pb-Free (RoHS)	CU NIPDAU	N / A for Pkg Type	0 to 70	LT1054CP	Samples
LT1054CPE4	ACTIVE	PDIP	P	8	50	Pb-Free (RoHS)	CU NIPDAU	N / A for Pkg Type	0 to 70	LT1054CP	Samples
LT1054IDW	ACTIVE	SOIC	DW	16	40	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	LT1054I	Samples
LT1054IDWG4	ACTIVE	SOIC	DW	16	40	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	LT1054I	Samples
LT1054IDWR	ACTIVE	SOIC	DW	16	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	LT1054I	Samples
LT1054IDWRG4	ACTIVE	SOIC	DW	16	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	LT1054I	Samples
LT1054IP	ACTIVE	PDIP	P	8	50	Pb-Free (RoHS)	CU NIPDAU	N / A for Pkg Type	-40 to 85	LT1054IP	Samples
LT1054IPE4	ACTIVE	PDIP	P	8	50	Pb-Free (RoHS)	CU NIPDAU	N / A for Pkg Type	-40 to 85	LT1054IP	Samples
LT1054Y	OBSOLETE	DIESALE	Y	0		TBD	Call TI	Call TI			

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

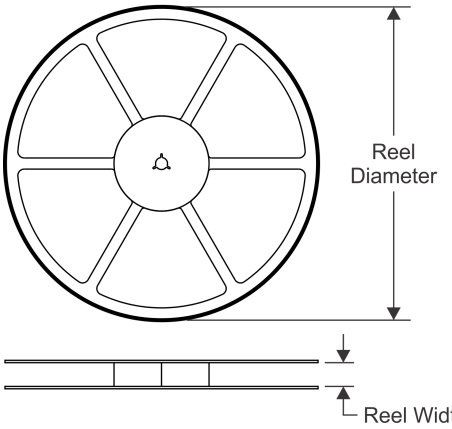
(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

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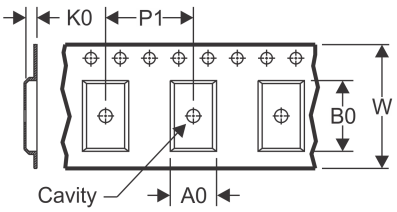
In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

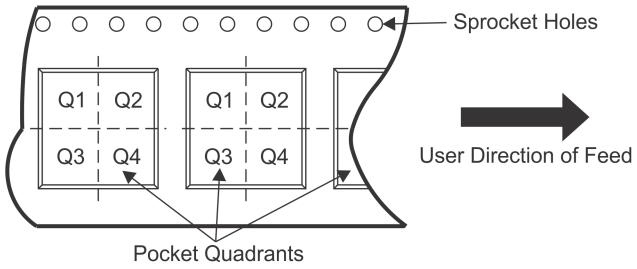


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

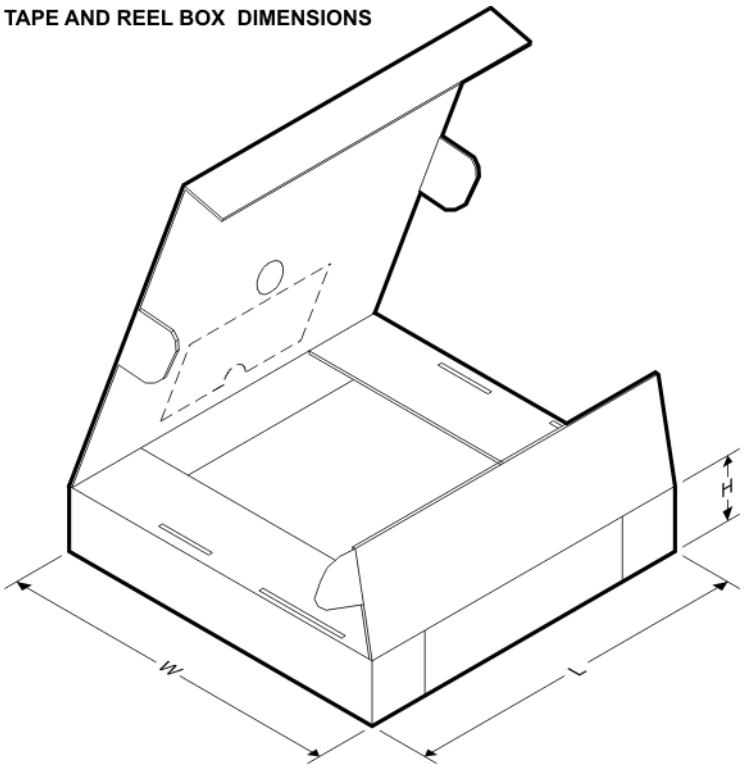
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
LT1054CDWR	SOIC	DW	16	2000	330.0	16.4	10.75	10.7	2.7	12.0	16.0	Q1
LT1054IDWR	SOIC	DW	16	2000	330.0	16.4	10.75	10.7	2.7	12.0	16.0	Q1

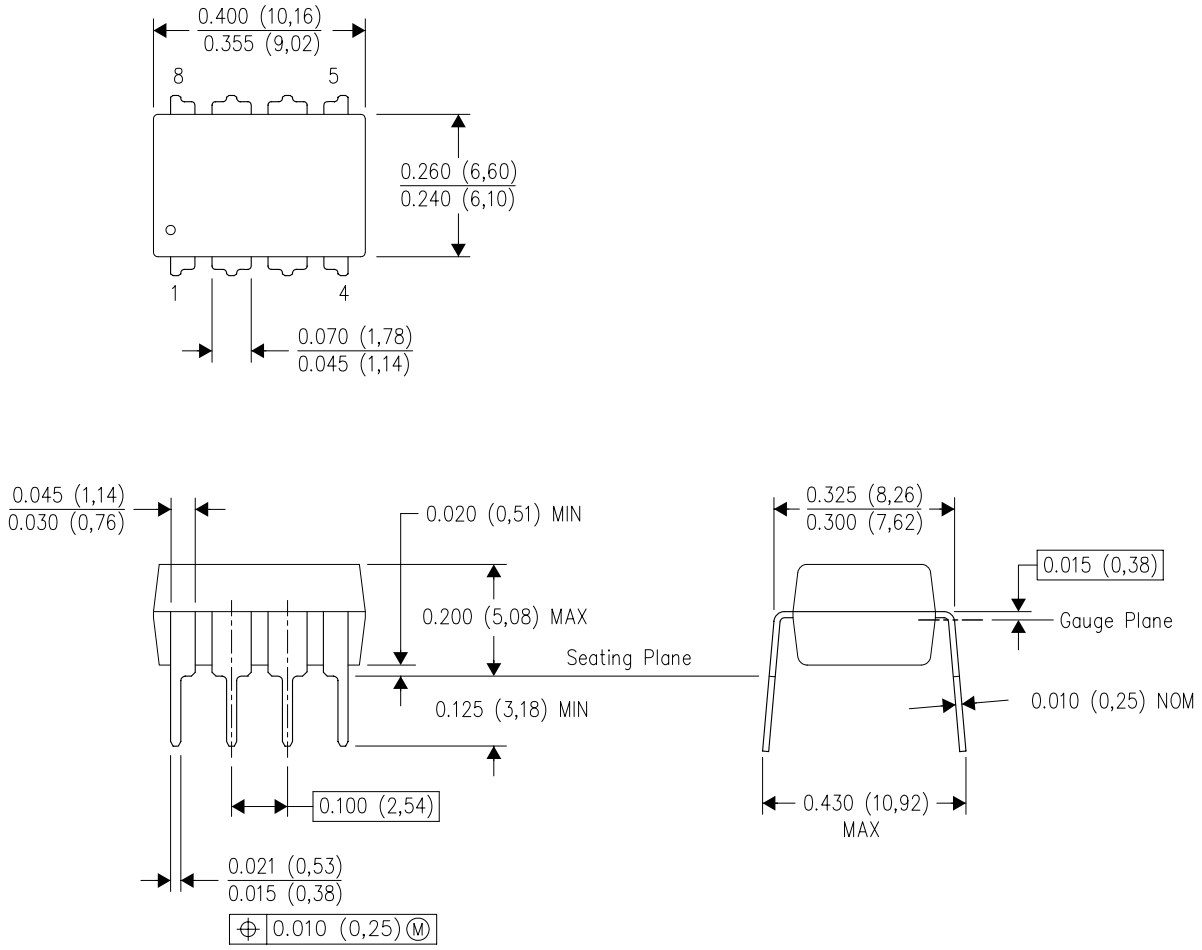
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

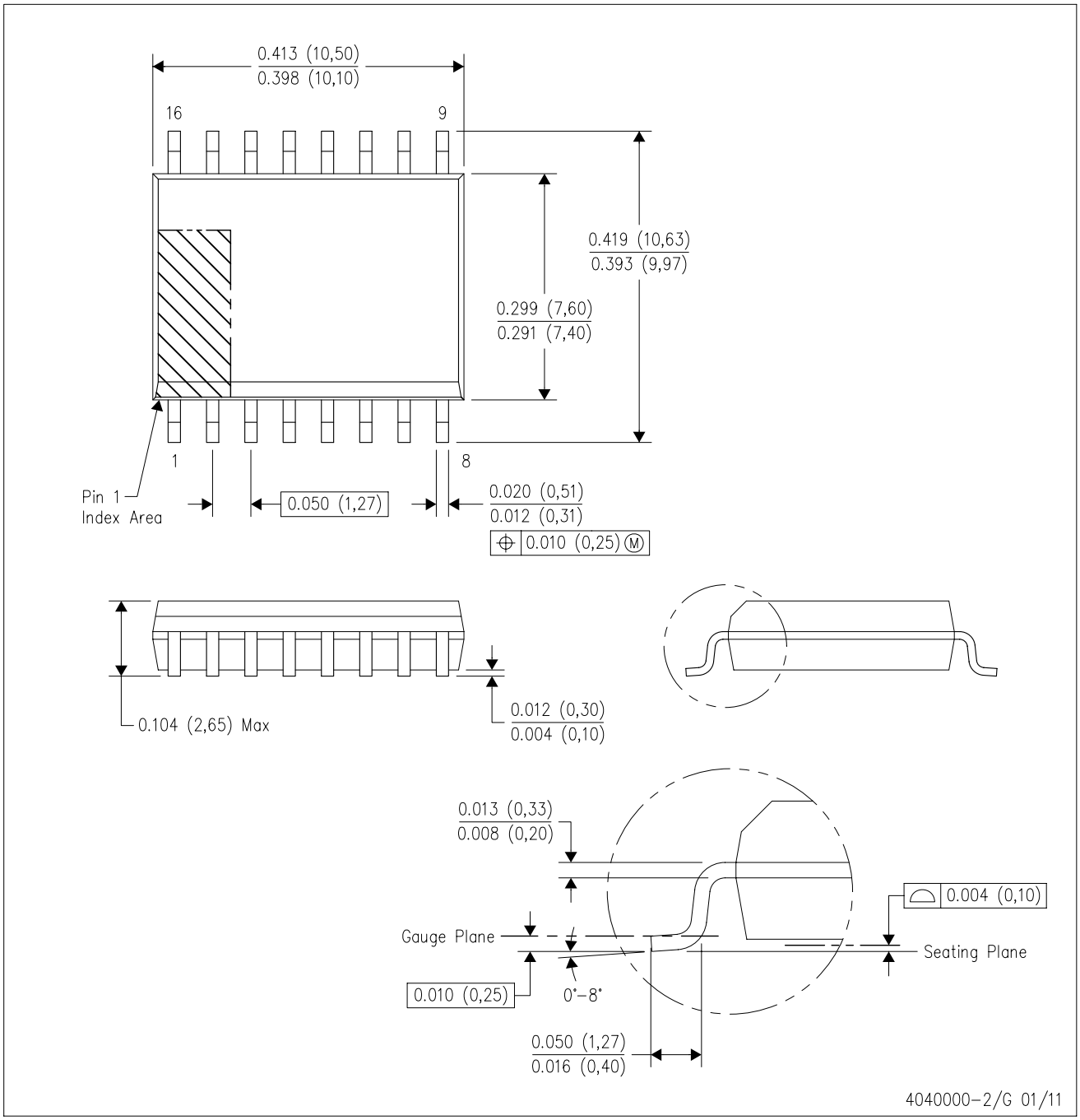
Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
LT1054CDWR	SOIC	DW	16	2000	367.0	367.0	38.0
LT1054IDWR	SOIC	DW	16	2000	367.0	367.0	38.0

P (R–PDIP–T8) PLASTIC DUAL–IN–LINE PACKAGE



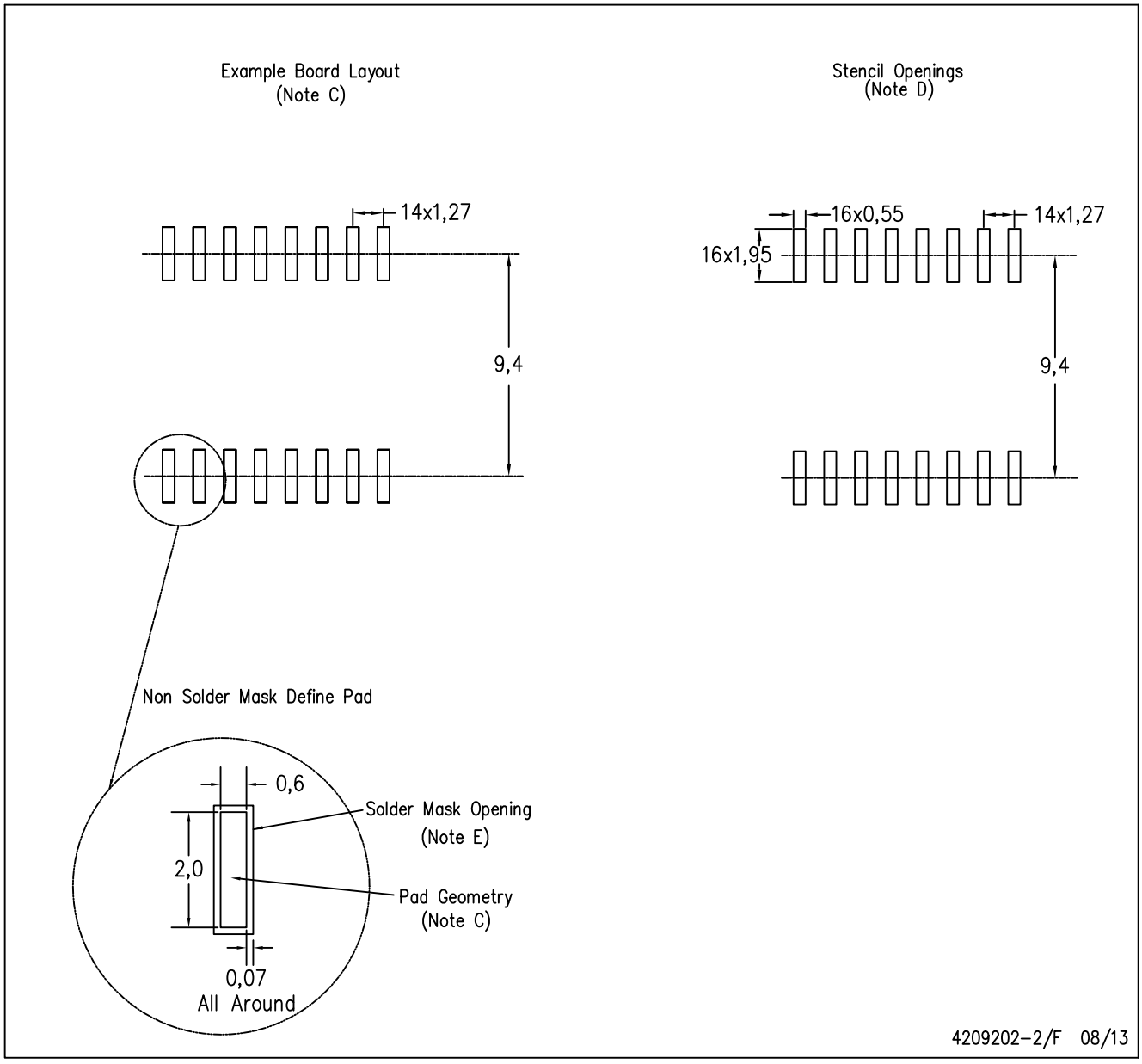
NOTES:
A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Falls within JEDEC MS–001 variation BA.

DW (R–PDSO–G16) PLASTIC SMALL OUTLINE



NOTES:
A. All linear dimensions are in inches (millimeters). Dimensioning and tolerancing per ASME Y14.5M–1994.
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusion not to exceed 0.006 (0,15).
D. Falls within JEDEC MS–013 variation AA.

DW (R–PDSO–G16) PLASTIC SMALL OUTLINE



NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Refer to IPC7351 for alternate board design.
D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC–7525
E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

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