FAIRCHILD SEMICONDUCTOR®

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FAN3278
30V PMOS-NMOS Bridge Driver

Features

- 8V to 27V Optimum Operating Range
- Drives High-Side PMOS and Low-Side NMOS in Motor Control or Buck Step-Down Applications
- Output Drive-Voltage Magnitude Limited: < 13V for V_{DD} up to 30V
- Biases Each Load Device OFF with a 100kΩ Resistor when V_{DD} Below Operating Level
- Low-Voltage TTL Input Thresholds
- Peak Gate Drives at 12V: +1.5A Sink, -1.0A Source
- Internal Resistors Hold Driver Off When No Inputs Present
- 8-Lead SOIC Package
- Rated from –40°C to +125°C Ambient

Applications

- Motor Control with PMOS / NMOS Half-Bridge Configuration
- Buck Converters with High-Side PMOS Device; 100% Duty Cycle Operation Possible
- Logic-Controlled Load Circuits with High-Side PMOS Switch

Description

The FAN3278 dual 1.5A gate driver is optimized to drive a high-side P-channel MOSFET and a low-side N-channel MOSFET in motor control applications operating from a voltage rail up to 27V. Internal circuitry limits the voltage applied to the gates of the external MOSFETs to 13V maximum. The driver has TTL input thresholds and provides buffer and level translation from logic inputs. Internal circuitry prevents the output switching devices from operating if the V_{DD} supply voltage is below the IC operation level. Internal 100kΩ resistors bias the non-inverting output LOW and the inverting output to V_{DD} to keep the external MOSFETs off during startup intervals when logic control signals may not be present.

The FAN3278 driver incorporates MOSFET devices for the final output stage, providing high current throughout the MOSFET turn-on / turn-off transition to minimize switching loss. The internal gate-drive regulators provide optimum gate-drive voltage when operating from a rail of 8V to 27V. The FAN3278 can be driven from a voltage rail of less than 8V; however, its gate drive current is reduced.

The FAN3278 has two independent ENABLE pins that default to ON if not connected. If the ENABLE pin for non-inverting channel A is pulled LOW, OUTA is forced LOW. If the ENABLE pin for inverting channel B is pulled LOW, OUTB is forced HIGH. If an input is left unconnected, internal resistors bias the inputs such that the external MOSFETs are OFF.

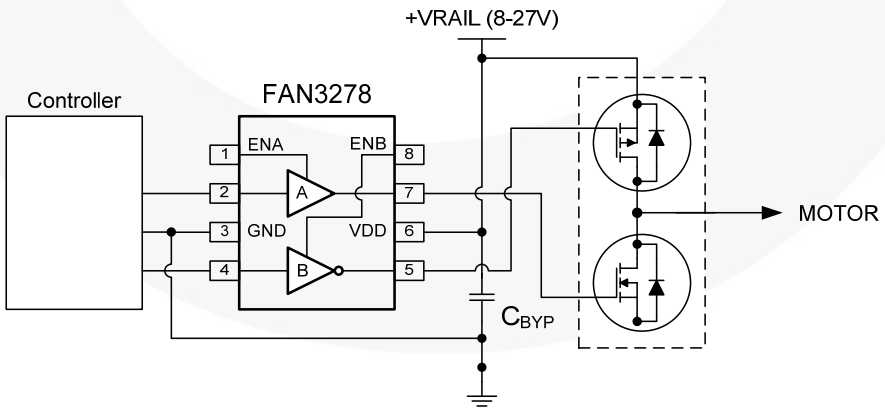


Figure 1. Typical Application

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Ordering Information

Part Number	Logic	Input Threshold	Packing Method
FAN3278TMX	Non-Inverting Channel and Inverting Channel with Dual Enable	TTL	2,500 Units on Tape & Reel

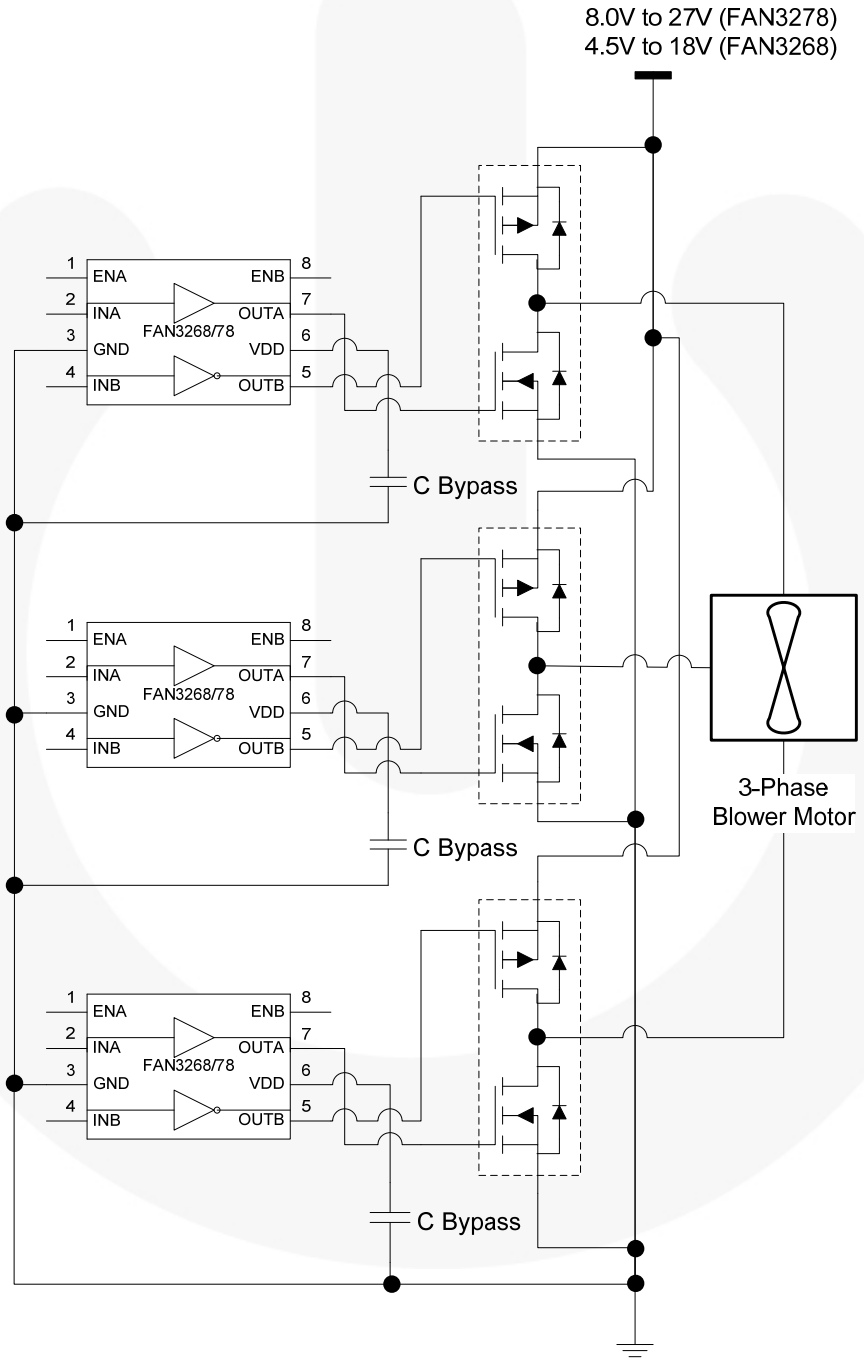


Figure 2. Typical 3-Phase Blower Motor Drive Application

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Pin Configuration

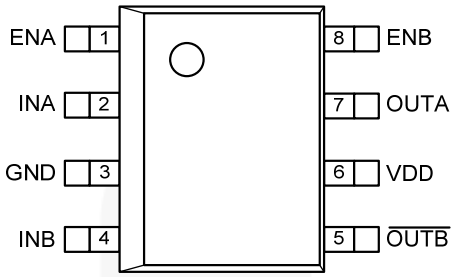


Figure 3. Pin Configuration (Top View)

Thermal Characteristics[1]

Package	Θ_{JL}[2]	Θ_{JT}[3]	Θ_{JA}[4]	Ψ_{JB}[5]	Ψ_{JT}[6]	Unit
8-Pin Small-Outline Integrated Circuit (SOIC)	40	31	89	43	3	°C/W

Notes:

1. Estimates derived from thermal simulation; actual values depend on the application.
2. Theta_JL (Θ_{JL}): Thermal resistance between the semiconductor junction and the bottom surface of all the leads (including any thermal pad) that are typically soldered to a PCB.
3. Theta_JT (Θ_{JT}): Thermal resistance between the semiconductor junction and the top surface of the package, assuming it is held at a uniform temperature by a top-side heatsink.
4. Theta_JA (Θ_{JA}): Thermal resistance between junction and ambient, dependent on the PCB design, heat sinking, and airflow. The value given is for natural convection with no heatsink using a 2S2P board, as specified in JEDEC standards JESD51-2, JESD51-5, and JESD51-7, as appropriate.
5. Psi_JB (Ψ_{JB}): Thermal characterization parameter providing correlation between semiconductor junction temperature and an application circuit board reference point for the thermal environment defined in Note 4. For the SOIC-8 package, the board reference is defined as the PCB copper adjacent to pin 6.
6. Psi_JT (Ψ_{JT}): Thermal characterization parameter providing correlation between the semiconductor junction temperature and the center of the top of the package for the thermal environment defined in Note 4.

Pin Definitions

Pin#	Name	Description
1	ENA	**Enable Input for Channel A**. Pull pin LOW to inhibit driver A. ENA has TTL thresholds.
8	ENB	**Enable Input for Channel B**. Pull pin LOW to inhibit driver B. ENB has TTL thresholds.
3	GND	**Ground**. Common ground reference for input and output circuits.
2	INA	**Input to Channel A**.
4	INB	**Input to Channel B**.
7	OUTA	**Gate Drive Output A**: Held LOW unless required input is present and V_{DD} is above the internal voltage threshold where the IC is functional.
5	$\overline{\text{OUTB}}$	**Gate Drive Output B** (inverted from the input). Held HIGH unless the required input is present and V_{DD} is above the internal voltage threshold where the IC is functional.
6	VDD	**Supply Voltage**. Provides power to the IC.

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Output Logic

FAN3278 (Channel A)		
ENA	INA	OUTA
0	0[7]	0
0	1	0
1[7]	0[7]	0
1[7]	1	1

FAN3278 (Channel B)		
ENB	INB	$\overline{\text{OUTB}}$
0	0[7]	1
0	1	1
1[7]	0[7]	1
1[7]	1	0

Note:
7. Default input signal if no external connection is made.

Block Diagram

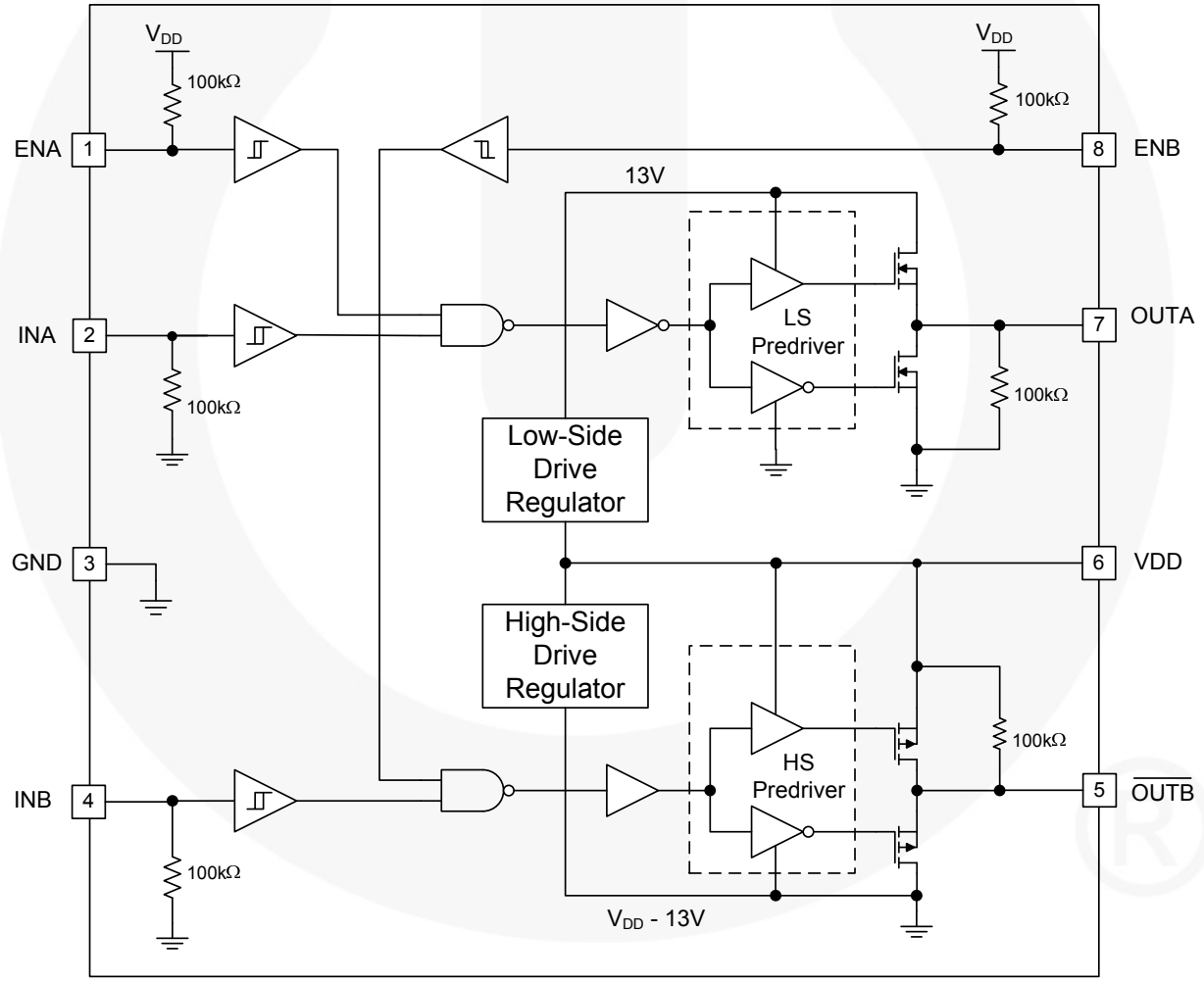


Figure 4. Block Diagram

Absolute Maximum Ratings

Stresses exceeding the absolute maximum ratings may damage the device. The device may not function or be operable above the recommended operating conditions and stressing the parts to these levels is not recommended. In addition, extended exposure to stresses above the recommended operating conditions may affect device reliability. The absolute maximum ratings are stress ratings only.

Symbol	Parameter		Min.	Max.	Unit
V_{DD}	VDD to PGND		-0.3	30.0	V
V_{EN}	ENA, ENB to GND		GND - 0.3	V_{DD} + 0.3	V
V_{IN}	INA, INB to GND		GND - 0.3	V_{DD} + 0.3	V
V_{OUT}	OUTA, OUTB to GND		GND - 0.3	V_{DD} + 0.3	V
T_L	Lead Soldering Temperature (10 Seconds)			+260	ºC
T_J	Junction Temperature		-55	+150	ºC
T_{STG}	Storage Temperature		-65	+150	ºC
ESD	Electrostatic Discharge Protection Level	Human Body Model, JEDEC JESD22-A114	2		kV
		Charged Device Model, JEDEC JESD22-C101	2		

Recommended Operating Conditions

The Recommended Operating Conditions table defines the conditions for actual device operation. Recommended operating conditions are specified to ensure optimal performance to the datasheet specifications. Fairchild does not recommend exceeding them or designing to Absolute Maximum Ratings.

Symbol	Parameter	Min.	Max.	Unit
V_{DD}	Supply Voltage Range	8	27	V
V_{EN}	Enable Voltage (ENA, ENB)	0	V_{DD}	V
V_{IN}	Input Voltage (INA, INB)	0	V_{DD}	V
T_A	Operating Ambient Temperature	-40	+125	°C

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Electrical Characteristics

Unless otherwise noted, V_{DD}=12V and T_J=-40°C to +125°C. Currents are defined as positive into the device (I_{sink}) and negative out of the device (I_{source}).

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
Supply						
V_{DD}	Optimum Operating Range[8]		8		27	V
I_{DD}	Supply Current Inputs / EN Not Connected			1.3	2.0	mA
V_{ON}	Turn-On Voltage[9]	INA=ENA=V_{DD}, INB=ENB=0V		3.8		V
V_{HYS}	Turn-On / Turn-Off Hysteresis [9]	INA=ENA=V_{DD}, INB=ENB=0V		10		mV
Input[9]						
V_{IL}	INx Logic Low Threshold		0.8	1.1		V
V_{IH}	INx Logic High Threshold			1.80	2.25	V
V_{HYS}	Logic Hysteresis Voltage		0.4	0.7	1.0	V
Enable						
V_{ENL}	Enable Logic Low Threshold	EN from 5V to 0V	0.8	1.2		V
V_{ENH}	Enable Logic High Threshold	EN from 0V to 5V		1.60	2.25	V
V_{HYS}	Logic Hysteresis Voltage[10]			0.7		V
R_{PU}	Enable Pull-Up Resistance			100		kΩ
t_{D1}	Propagation A Delay, EN Rising[11]	0 - 5V_{IN}, 1V/ns Slew Rate		44	70	ns
t_{D2}	Propagation A Delay, EN Falling[11]	0 – 5V_{IN}, 1V/ns Slew Rate		33	60	ns
t_{D2}	Propagation B Delay, EN Rising[11]	0 - 5V_{IN}, 1V/ns Slew Rate		39	70	ns
t_{D1}	Propagation B Delay, EN Falling[11]	0 – 5V_{IN}, 1V/ns Slew Rate		29	60	ns

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Timing Diagrams

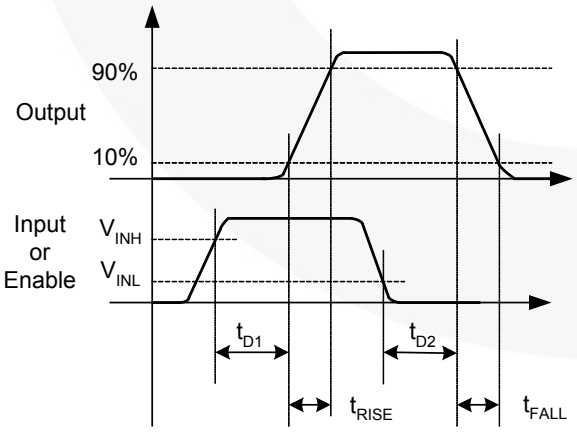


Figure 5. Non-Inverting

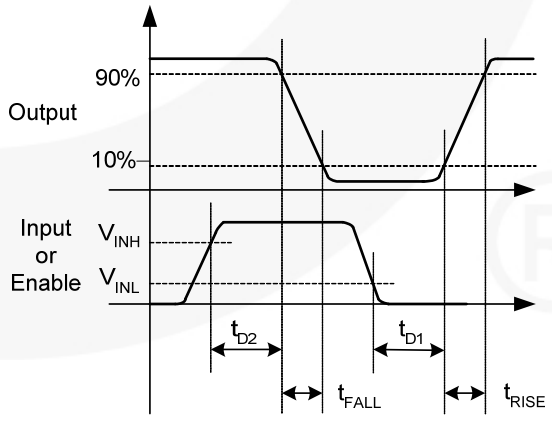


Figure 6. Inverting

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Electrical Characteristics (Continued)

Unless otherwise noted, V_{DD}=12V and T_J=-40°C to +125°C. Currents are defined as positive into the device (I_{sink}) and negative out of the device (I_{source}).

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
Output						
I_{PK_OFF}	OUT Current, Peak, Turn-Off(10)	C_{LOAD}=0.1µF, f=1kHz		1.5		A
I_{PK_ON}	OUT Current, Peak, Turn-On(10)	C_{LOAD}=0.1µF, f=1kHz		-1.0		A
I_{OFF}	OUT Current, Mid-Voltage, Turn-Off(10	OUT at V_{DD}, C_{LOAD}=0.1µF, f=1kHz		1.0		A
I_{ON}	OUT Current, Mid-Voltage, Turn-On(10)	OUT at V_{DD}/2, C_{LOAD}=0.1µF, f=1kHz		-0.5		A
V_{OUTA}	OUTA Drive Voltage	V_{DD}=27V, INA="HI"		11	13	V
V_{OUTB}	OUTB Drive Voltage, $V_{DD} - V_{OUTB}$	V_{DD}=27V, INA="HI"		11	13	V
V_{OUTA}	OUTA Drive Voltage	V_{DD}=10V, INB="HI"	6.5	7.0		V
V_{OUTB}	OUTB Drive Voltage, $V_{DD} - V_{OUTB}$	V_{DD}=10V, INB="HI"	6.5	7.0		V
$R_{O_A_SINK}$	OUTA Sink Impedance (Turn-Off)(10)	V_{DD}=6V, C_{LOAD}=0.1µF		4.2		Ω
$R_{O_A_SRC}$	OUTA Source Impedance (Turn-On)(10)	V_{DD}=6V, C_{LOAD}=0.1µF		10.3		Ω
$R_{O_B_SINK}$	OUTB Sink Impedance (Turn-On)(10)	V_{DD}=6V, C_{LOAD}=0.1µF		6.8		Ω
$R_{O_B_SRC}$	OUTB Source Impedance (Turn-Off)(10)	V_{DD}=6V, C_{LOAD}=0.1µF		13.7		Ω
$t_{ON,N}$	Output A Rise Time(11)	C_{LOAD}=1000pF to GND		17	30	ns
$t_{OFF,N}$	Output A Fall Time(11)	C_{LOAD}=1000pF to GND		8	15	ns
$t_{ON,P}$	Output B Fall Time(11)	C_{LOAD}=1000pF to V_{DD}		21	30	ns
$t_{OFF,P}$	Output B Rise Time(11)	C_{LOAD}=1000pF to V_{DD}		8	15	ns
t_{D1}	Output Propagation Delay On(11)	0 - 5V_{IN}, 1V/ns Slew Rate		45	70	ns
t_{D2}	Output Propagation Delay Off(11)	0 - 5V_{IN}, 1V/ns Slew Rate		35	60	ns
I_{RVS}	Output Reverse Current Withstand(10)			500		mA

Notes:

8. The internal gate-drive regulators provide optimum gate-drive voltage when operating from a rail of 8V to 27V. The FAN3278 can be driven from a voltage rail of less than 8V; however, with reduced gate drive current.
9. EN inputs have near-TTL thresholds *(refer to the ENABLE section)*.
10. Not tested in production.
11. *See the Timing Diagrams of Figure 5 and Figure 6.*

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Typical Performance Characteristics

Typical characteristics are provided at T_A=25°C and V_{DD}=12V unless otherwise noted.

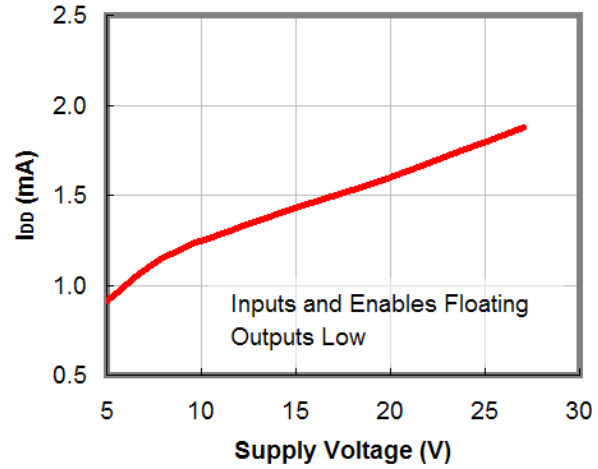


Figure 7. I_{DD} (Static) vs. Supply Voltage(12)

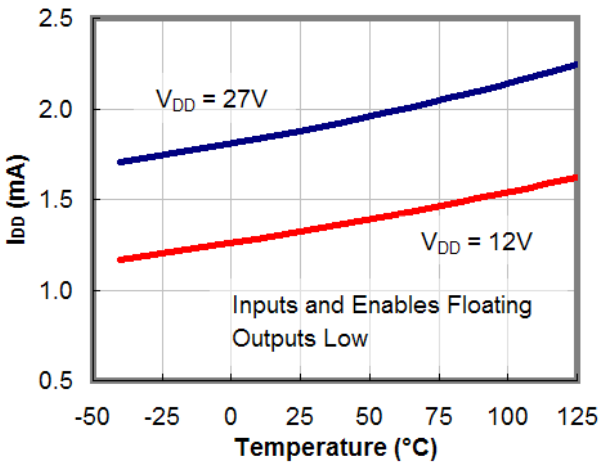


Figure 8. I_{DD} (Static) vs. Temperature(12)

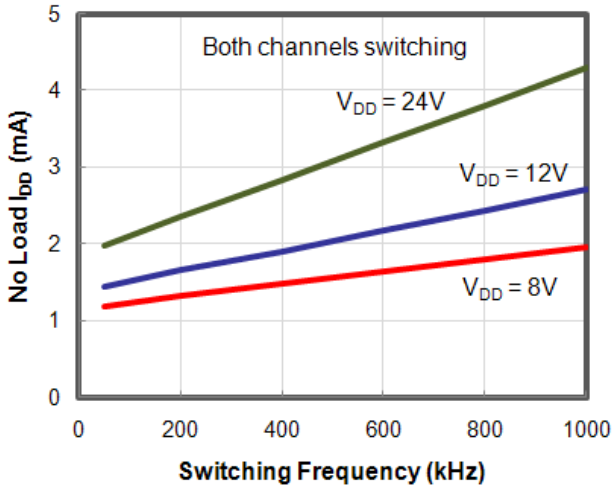


Figure 9. I_{DD} (No Load) vs. Frequency

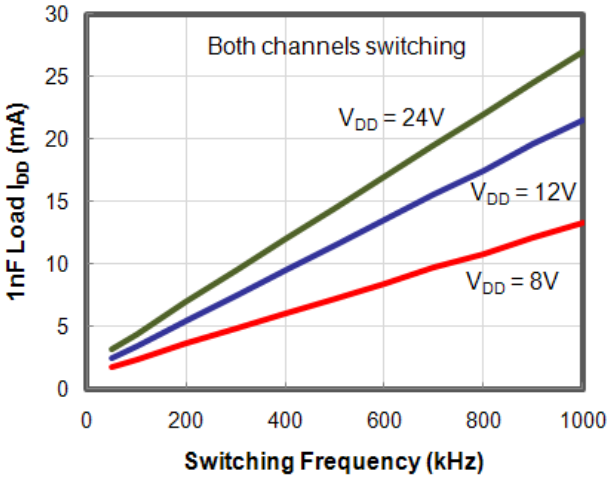


Figure 10. I_{DD} (1nF Load) vs. Frequency

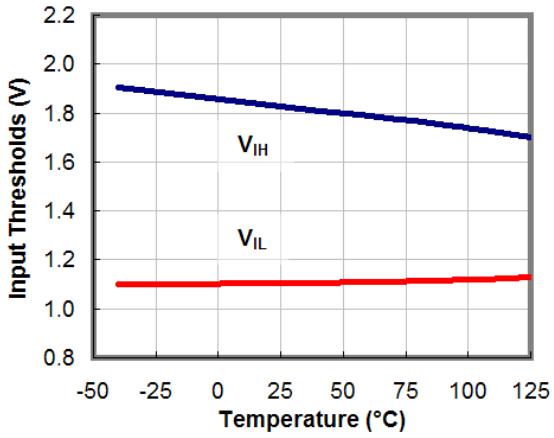


Figure 11. Input Thresholds vs. Temperature

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Typical Performance Characteristics

Typical characteristics are provided at T_A=25°C and V_{DD}=12V unless otherwise noted.

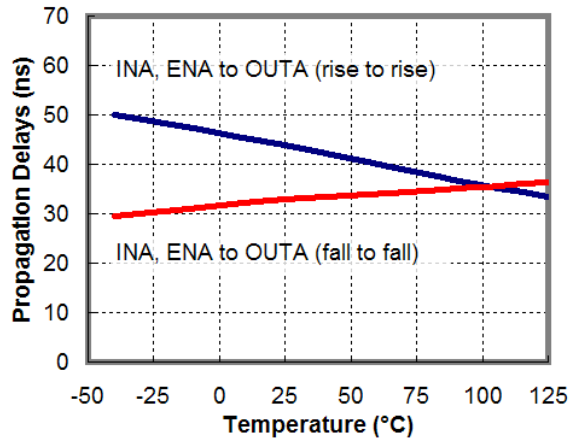


Figure 12. Propagation Delays vs. Temperature

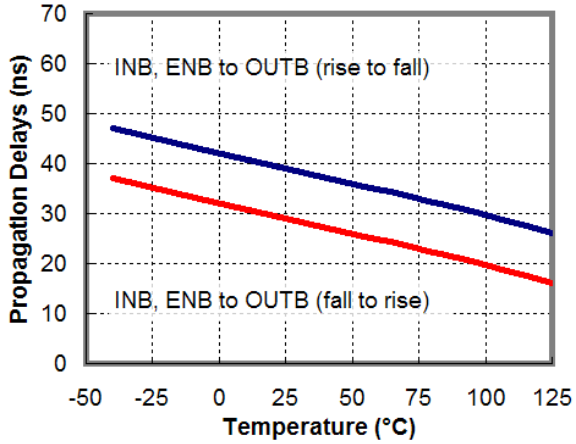


Figure 13. Propagation Delays vs. Temperature

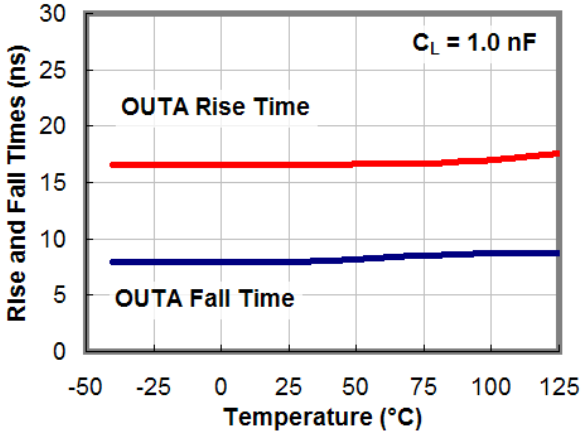


Figure 14. Rise and Fall Times vs. Temperature

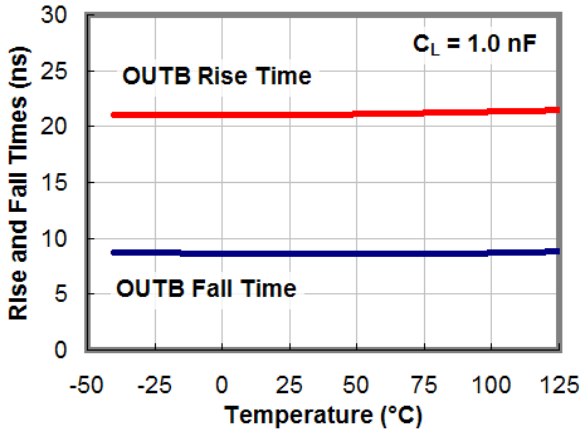


Figure 15. Rise and Fall Times vs. Temperature

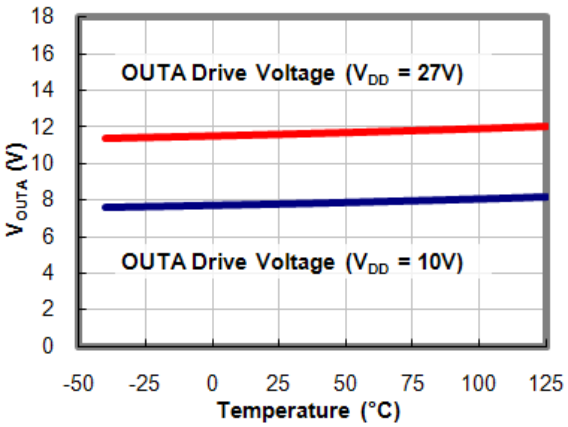


Figure 16. Gate Drive Voltage vs. Temperature

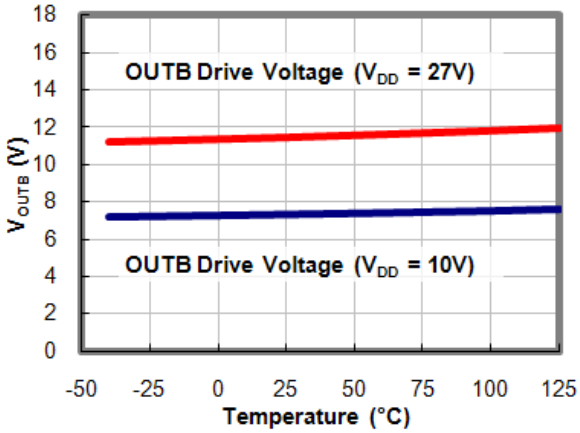


Figure 17. Gate Drive Voltage vs. Temperature

Note:

12. For any inverting inputs pulled LOW, non-inverting inputs pulled HIGH, or outputs driven HIGH; static I_{DD} increases by the current flowing through the corresponding pull-up/down resistor, shown in Figure 4.

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Applications Information

Input Thresholds

The FAN3278 driver has TTL input thresholds and provides buffer and level translation functions from logic inputs. The input thresholds meet industry-standard TTL-logic thresholds, independent of the V_{DD} voltage, and there is a hysteresis voltage of approximately 0.4V. These levels permit the inputs to be driven from a range of input logic signal levels for which a voltage over 2V is considered logic HIGH. The driving signal for the TTL inputs should have fast rising and falling edges with a slew rate of 6V/µs or faster, so a rise time from 0 to 3.3V should be 550ns or less. With reduced slew rate, circuit noise could cause the driver input voltage to exceed the hysteresis voltage and retrigger the driver input inadvertently.

Static Supply Current

In the I_{DD} (static) typical performance characteristics *(see Figure 7 and Figure 8)*, the curve is produced with all inputs / enables floating (OUTA is LOW, OUTB is HIGH) and indicates the lowest static I_{DD} current for the tested configuration. For other states, additional current flows through the 100kΩ resistors on the inputs and outputs, shown in the block diagram *(see Figure 4)*. In these cases, the static I_{DD} current is the value obtained from the curves plus this additional current.

Gate Drive Regulator

FAN3278 incorporates internal regulators to regulate the gate drive voltage. The output pin slew rate is determined by this gate drive voltage and the load on the output. It is not user adjustable, but a series resistor can be added if a slower rise or fall time is needed at the MOSFET gate.

Startup Operation

The FAN3278 startup logic is optimized to drive a ground-referenced N-channel MOSFET with channel A and a V_{DD}-referenced P-channel MOSFET with channel B.

The optimum operating voltage of the FAN3278 is 8V to 27V. It has an internal “watchdog” circuit that provides a loose UVLO turn-on voltage (V_{ON}) of approximately 3.8V with a small hysteresis of about 10mV. However, it is recommended that V_{DD} is greater than 4.75V in all application circuits.

When the V_{DD} supply voltage is below the level needed to operate the internal circuitry, the outputs are biased to hold the external MOSFETs in OFF state. Internal 100kΩ resistors bias the non-inverting output LOW and the inverting output to V_{DD} to keep the external MOSFETs off during startup intervals when input control signals may not be present.

Figure 18 shows startup waveforms for non-inverting channel A. At power-up, the driver output for channel A remains LOW until V_{DD} reaches the voltage where the device starts operating, then OUTA operates in-phase with INA.

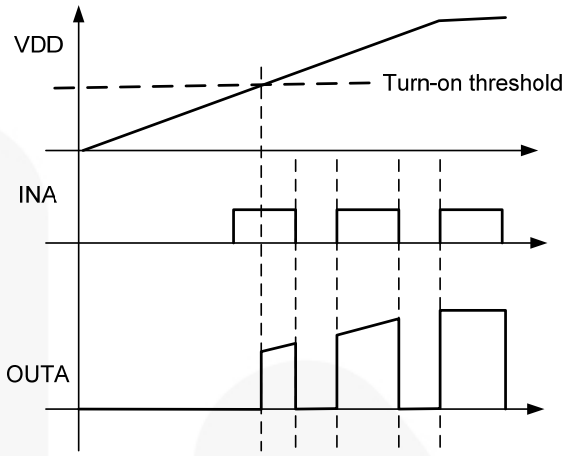


Figure 18. Non-Inverting Startup Waveforms

Figure 19 illustrates startup waveforms for inverting channel B. At power-up, the driver output for channel B is tied to V_{DD} through an internal 100kΩ resistor until V_{DD} reaches the voltage where the device starts operating, then OUTB operates out of phase with INB.

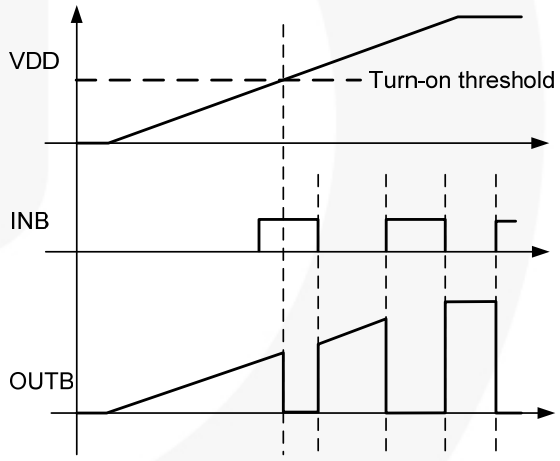


Figure 19. Inverting Startup Waveforms

It is possible, during startup, before V_{DD} has reached approximately 4.5V, that the output pulse width may take a few switching cycles to reach the full duty-cycle of the input pulse. This is due to internal propagation delays affecting the operation with higher switching frequency (e.g. >100kHz) and slow V_{DD} ramp-up (e.g. <20V/ms). For this reason, it is recommended that V_{DD} should be greater than 4.75V before any INA or INB signals are present.

For high-frequency applications (several hundred kHz up to 1MHz), where the above recommendation of V_{DD} > 4.75V is not possible, the use of ENABLES to actively hold the outputs LOW until V_{DD} > 4.75V assures the driver output pulse width follows the input from 4.75V up to 28V.

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V_{DD} Bypass Capacitor Guidelines

To enable this IC to turn a device on quickly, a local high-frequency bypass capacitor, C_{BYP}, with low ESR and ESL should be connected between the VDD and GND pins with minimal trace length. This capacitor is in addition to bulk electrolytic capacitance of 10µF to 47µF commonly found on driver and controller bias circuits.

A typical criterion for choosing the value of C_{BYP} is to keep the ripple voltage on the V_{DD} supply to ≤5%. This is often achieved with a value ≥20 times the equivalent load capacitance C_{EQV}, defined as Q_{GATE}/V_{DD}. Ceramic capacitors of 0.1µF to 1µF or larger are common choices, as are dielectrics, such as X5R and X7R, with stable temperature characteristics and high pulse current capability.

If circuit noise affects normal operation, the value of C_{BYP} may be increased to 50-100 times the C_{EQV} or C_{BYP} may be split into two capacitors. One should be a larger value, based on equivalent load capacitance, and the other a smaller value, such as 1-10nF, mounted closest to the VDD and GND pins to carry the higher-frequency components of the current pulses. The bypass capacitor must provide the pulsed current from both of the driver channels and, if the drivers are switching simultaneously, the combined peak current sourced from the C_{BYP} can be twice as large as when a single channel is switching.

Layout and Connection Guidelines

The FAN3278 gate driver incorporates fast-reacting input circuits, short propagation delays, and powerful output stages capable of delivering current peaks over 1.5A to facilitate fast voltage transition times. The following layout and connection guidelines are strongly recommended:

- Keep high-current output and power ground paths separate from logic and enable input signals and signal ground paths. This is especially critical when dealing with TTL-level logic thresholds at driver inputs and enable pins.
- Keep the driver as close to the load as possible to minimize the length of high-current traces. This reduces the series inductance to improve high-speed switching, while minimizing the loop area that can couple EMI to the driver inputs and surrounding circuitry.
- If the inputs to a channel are not externally connected, the internal 100kΩ resistors indicated on block diagrams command a low output on channel A and a high output on channel B. In noisy environments, it may be necessary to tie inputs of an unused channel to VDD or GND using short traces to prevent noise from causing spurious output switching.
- Many high-speed power circuits can be susceptible to noise injected from their own output or other external sources, possibly causing output mis-triggering. These effects can be obvious if the circuit is tested in breadboard or non-optimal circuit layouts with long input, enable, or output leads. For best results, make connections to all pins as short and direct as possible.
- The turn-on and turn-off current paths should be minimized, as discussed above.

Thermal Guidelines

Gate drivers used to switch MOSFETs and IGBTs at high frequencies can dissipate significant amounts of power. It is important to determine the driver power dissipation and the resulting junction temperature in the application to ensure the part is operating within acceptable temperature limits.

The total power dissipation in a gate driver is the sum of two components, P_{GATE} and $P_{DYNAMIC}$:

$$P_{TOTAL}=P_{GATE} + P_{DYNAMIC} \quad (1)$$

Gate Driving Loss: The most significant power loss results from supplying gate current (charge per unit time) to switch the load MOSFET on and off at the switching frequency. The power dissipation that results from driving a MOSFET with a specified gate-source voltage, V_{GS}, with gate charge, Q_G, at switching frequency, f_{SW}, is determined by:

$$P_{GATE}=Q_G \bullet V_{GS} \bullet f_{SW} \quad (2)$$

This needs to be calculated for each P-channel and N-channel MOSFET where the Q_G is likely to be different.

Dynamic Pre-drive / Shoot-through Current: Power loss resulting from internal current consumption under dynamic operating conditions, including pin pull-up / pull-down resistors, can be obtained using the "I_{DD} (No-Load) vs. Frequency" graphs in Figure 9 to determine the current $I_{DYNAMIC}$ drawn from V_{DD} under actual operating conditions.

$$P_{DYNAMIC}=I_{DYNAMIC} \bullet V_{DD} \quad (3)$$

Once the power dissipated in the driver is determined, the driver junction rise with respect to circuit board can be evaluated using the following thermal equation, assuming ψ_{JB} was determined for a similar thermal design (heat sinking and air flow):

$$T_J = P_{TOTAL} \bullet \psi_{JB} + T_B \quad (4)$$

where:

T_J =driver junction temperature

ψ_{JB} =(psi) thermal characterization parameter relating temperature rise to total power dissipation

T_B =board temperature in location defined in Note 1 under Thermal Resistance table.

As an example of a power dissipation calculation, consider an application driving two MOSFETs (one P-channel and one N-channel, both with a gate charge of 60nC each) with $V_{GS}=V_{DD}=12V$. At a switching frequency of 200kHz, the total power dissipation is:

$$P_{GATE}=60nC \bullet 12V \bullet 200kHz \bullet 2=0.288W \quad (5)$$

$$P_{DYNAMIC}=1.65mA \bullet 12V =0.020W \quad (6)$$

$$P_{TOTAL}=0.308W \quad (7)$$

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The SOIC-8 package has a junction-to-board thermal characterization parameter of Ψ_{JB}=43°C/W. In a system application, the localized temperature around the device is a function of the layout and construction of the PCB along with airflow across the surfaces. To ensure reliable operation, the maximum junction temperature of the device must not exceed the absolute maximum rating of 150°C; with 80% derating, T_J would be limited to 120°C. Rearranging Equation 4 determines the board temperature required to maintain the junction temperature below 120°C:

$$T_B = T_J - P_{TOTAL} \bullet \Psi_{JB} \quad (8)$$

$$T_B = 120°C - 0.308W \bullet 43°C/W = 107°C \quad (9)$$

Test Circuit

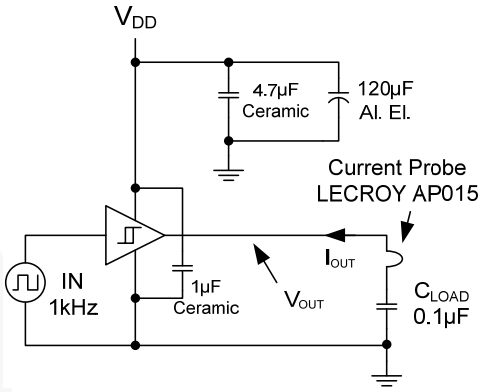


Figure 20. Quasi-Static I_{OUT} / V_{OUT} Test Circuit

Differences between FAN3278 and FAN3268

FAN3278 and FAN3268 are pin-compatible to each other and are designed to drive one P-Channel and one N-channel MOSFET in applications such as battery-powered compact fan / pump DC motor drives. However, there are key differences, highlighted in Table 1.

Table 1. Differences between FAN3278 and FAN3268

	FAN3278	FAN3268
Supply Voltage	27V Operating Maximum 30V Absolute Maximum	18V Operating Maximum 20V Absolute Maximum
Gate Drive Regulator	Yes, since the maximum operating V_{DD} can be as high as 27V, the gate voltage to the external MOSFETs is limited to about 13V.	No gate drive regulator is needed. The gate drive voltage is V_{DD} and the FAN3268 switches rail-to-rail.
Minimum Operating Voltage	The optimum operating range is 8V to 27V. After the IC turns on at about 3.8V, the output tracks V_{DD} up to the regulated voltage rail of about 11~13V. Below 8V of V_{DD}, the FAN3278 operates, but (a) slower and (b) with limited gate drive voltage until it reaches around 8V.	4.1V is the UVLO turn-off voltage which is the minimum operating voltage.
Startup	The IC starts operating approximately at 3.8V which acts as a loose UVLO threshold. It incorporates a “smart startup” feature where the outputs are held OFF before the IC starts operating.	Has the tight UVLO threshold of 4.5V on / 4.1V off. Incorporates “smart startup” (outputs held OFF before IC is fully operational at the UVLO threshold).
Output Gate Drive Architecture	Standard MOS-based output structure with gate drive clamp.	Compound MillerDrive™ architecture in the final output stage to provide a more efficient gate drive current during the Miller plateau stage of the turn-on/turn-off switching transition.
OUTB Gate Drive Current Strength	Optimized for P-channel: The turn-OFF (1.5 A) is stronger than turn-ON (1.0A).	P-channel turn-ON (2.4A) is stronger than turn-OFF (1.6A).

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Table 2. Related Products

Part Number	Type	Gate Drive[13] (Sink / Src)	Input Threshold	Logic	Package
FAN3111C	Single 1A	+1.1A / -0.9A	CMOS	Single Channel of Dual-Input/Single-Output	SOT23-5, MLP6
FAN3111E	Single 1A	+1.1A / -0.9A	External[14]	Single Non-Inverting Channel with External Reference	SOT23-5, MLP6
FAN3100C	Single 2A	+2.5A / -1.8A	CMOS	Single Channel of Two-Input/One-Output	SOT23-5, MLP6
FAN3100T	Single 2A	+2.5A / -1.8A	TTL	Single Channel of Two-Input/One-Output	SOT23-5, MLP6
FAN3226C	Dual 2A	+2.4A / -1.6A	CMOS	Dual Inverting Channels + Dual Enable	SOIC8, MLP8
FAN3226T	Dual 2A	+2.4A / -1.6A	TTL	Dual Inverting Channels + Dual Enable	SOIC8, MLP8
FAN3227C	Dual 2A	+2.4A / -1.6A	CMOS	Dual Non-Inverting Channels + Dual Enable	SOIC8, MLP8
FAN3227T	Dual 2A	+2.4A / -1.6A	TTL	Dual Non-Inverting Channels + Dual Enable	SOIC8, MLP8
FAN3228C	Dual 2A	+2.4A / -1.6A	CMOS	Dual Channels of Two-Input/One-Output, Pin Config.1	SOIC8, MLP8
FAN3228T	Dual 2A	+2.4A / -1.6A	TTL	Dual Channels of Two-Input/One-Output, Pin Config.1	SOIC8, MLP8
FAN3229C	Dual 2A	+2.4A / -1.6A	CMOS	Dual Channels of Two-Input/One-Output, Pin Config.2	SOIC8, MLP8
FAN3229T	Dual 2A	+2.4A / -1.6A	TTL	Dual Channels of Two-Input/One-Output, Pin Config.2	SOIC8, MLP8
FAN3268T	Dual 2A	+2.4A / -1.6A	TTL	Non-Inverting Channel (NMOS) and Inverting Channel (PMOS) + Dual Enables	SOIC8
FAN3278T	**Dual 2A**	**+1.4A / -1.0A**	**TTL**	**30V Non-Inverting (NMOS) and Inverting (PMOS) + Dual Enable**	**SOIC8**
FAN3223C	Dual 4A	+4.3A / -2.8A	CMOS	Dual Inverting Channels + Dual Enable	SOIC8, MLP8
FAN3223T	Dual 4A	+4.3A / -2.8A	TTL	Dual Inverting Channels + Dual Enable	SOIC8, MLP8
FAN3224C	Dual 4A	+4.3A / -2.8A	CMOS	Dual Non-Inverting Channels + Dual Enable	SOIC8, MLP8
FAN3224T	Dual 4A	+4.3A / -2.8A	TTL	Dual Non-Inverting Channels + Dual Enable	SOIC8, MLP8
FAN3225C	Dual 4A	+4.3A / -2.8A	CMOS	Dual Channels of Two-Input/One-Output	SOIC8, MLP8
FAN3225T	Dual 4A	+4.3A / -2.8A	TTL	Dual Channels of Two-Input/One-Output	SOIC8, MLP8
FAN3121C	Single 9A	+9.7A / -7.1A	CMOS	Single Inverting Channel + Enable	SOIC8, MLP8
FAN3121T	Single 9A	+9.7A / -7.1A	TTL	Single Inverting Channel + Enable	SOIC8, MLP8
FAN3122T	Single 9A	+9.7A / -7.1A	CMOS	Single Non-Inverting Channel + Enable	SOIC8, MLP8
FAN3122C	Single 9A	+9.7A / -7.1A	TTL	Single Non-Inverting Channel + Enable	SOIC8, MLP8

Notes:

13. Typical currents with OUT at 6V and V_{DD}=12V.
14. Thresholds proportional to an externally supplied reference voltage.

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Physical Dimensions

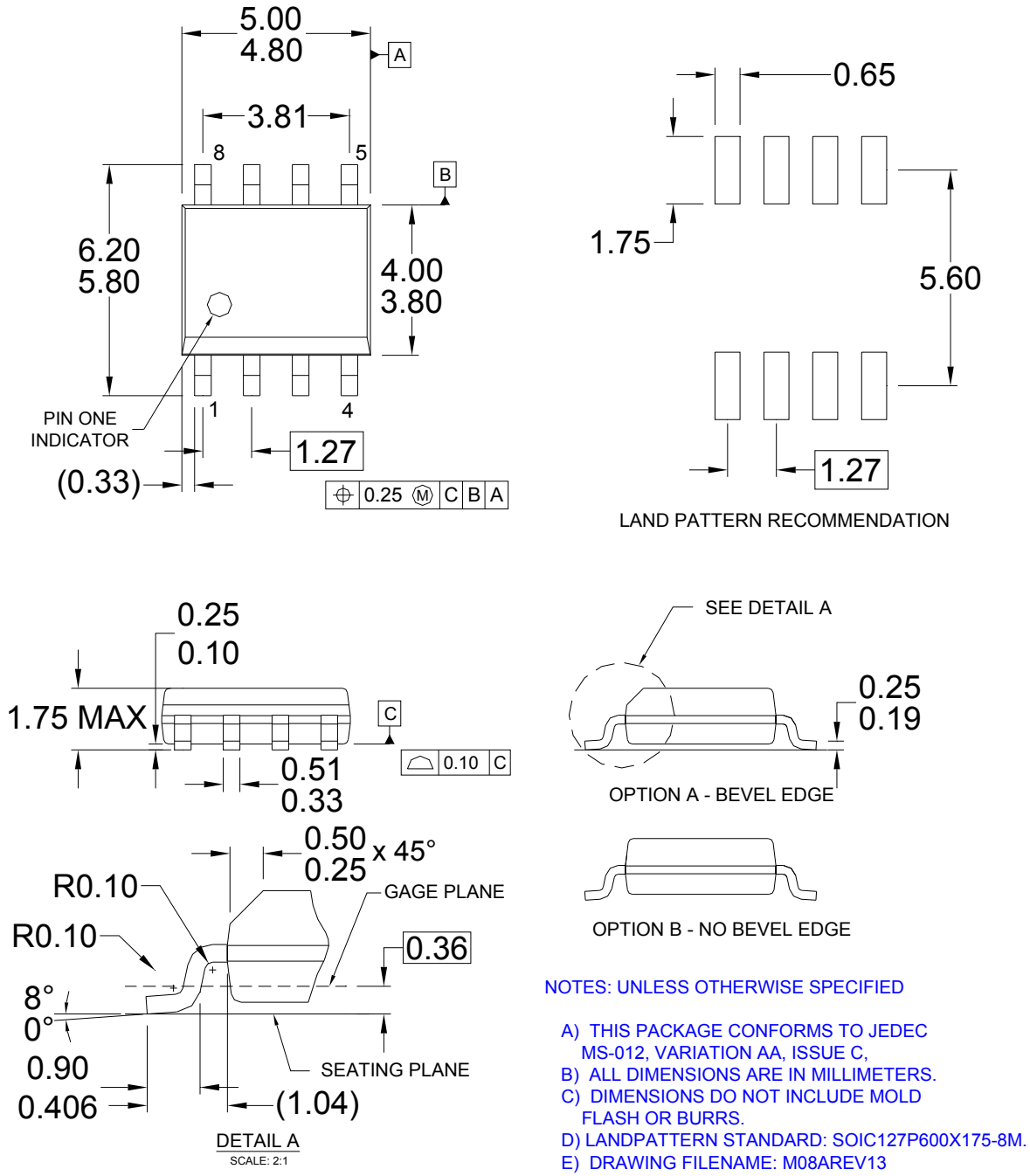


Figure 21. 8-Lead, Small-Outline Integrated Circuit (SOIC)

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