WM8750JL

Stereo CODEC for Portable Audio Applications

DESCRIPTION

The WM8750JL is a low power, high quality stereo CODEC designed for portable digital audio applications.

The device integrates complete interfaces to stereo or mono microphones and a stereo headphone. External component requirements are drastically reduced as no separate microphone or headphone amplifiers are required. Advanced on-chip digital signal processing performs graphic equaliser, 3-D sound enhancement and automatic level control for the microphone or line input.

The WM8750JL can operate as a master or a slave, with various master clock frequencies including 12 or 24MHz for USB devices, or standard 256f_s rates like 12.288MHz and 24.576MHz. Different audio sample rates such as 96kHz, 48kHz, 44.1kHz are generated directly from the master clock without the need for an external PLL.

The WM8750JL operates at supply voltages down to 1.8V, although the digital core can operate at voltages down to 1.42V to save power, and the maximum for all supplies is 3.6 Volts. Different sections of the chip can also be powered down under software control.

The WM8750JL is supplied in a very small and thin 5x5mm QFN package, ideal for use in hand-held and portable systems.

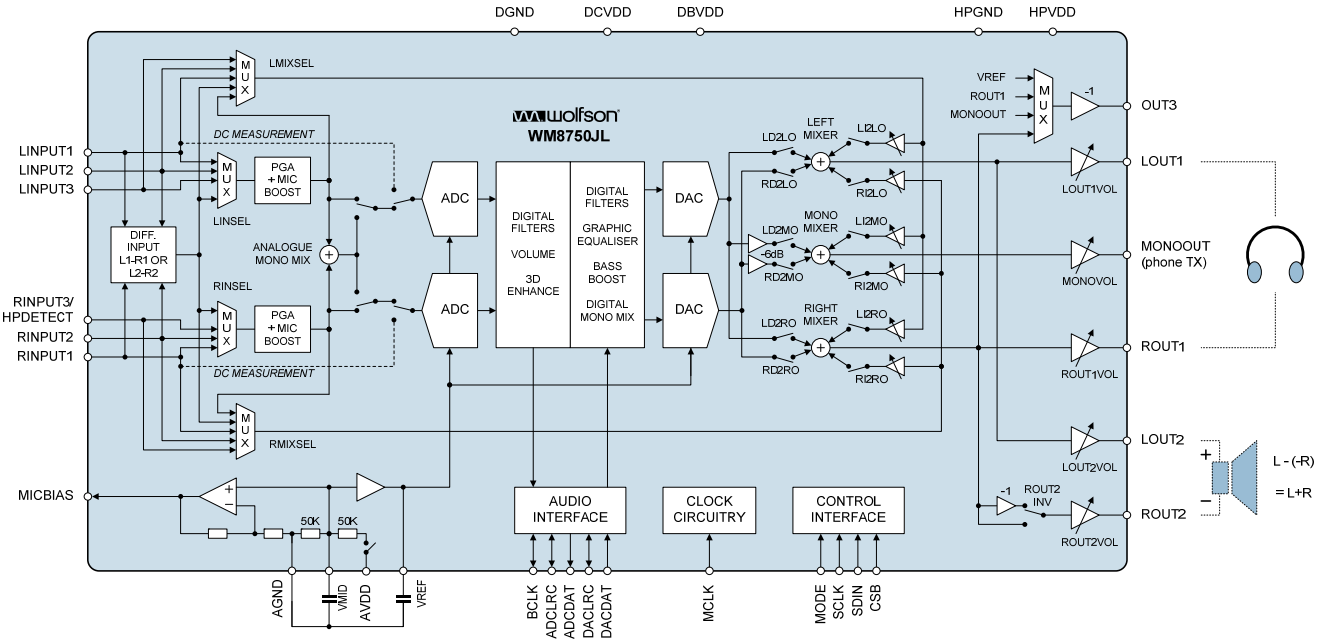
FEATURES

- DAC SNR 97dB ('A' weighted), THD -85dB at 48kHz, 3.3V
- ADC SNR 88dB ('A' weighted), THD -80dB at 48kHz, 3.3V
- Complete Stereo / Mono Microphone Interface
  - Programmable ALC (timed out) / Noise Gate
- On-chip 400mW BTL Speaker Driver (mono)
- On-chip Headphone Driver
  - >40mW output power on 16Ω / 3.3V
  - THD –73dB at 5mW, SNR 98dB with 16Ω load
  - No DC blocking capacitors required (capless mode)
- Separately mixed mono output
- Digital Graphic Equaliser
- Low Power
  - 6 mW stereo playback (1.8V / 1.5V supplies)
  - 13 mW record & playback (1.8V / 1.5V supplies)
- Low Supply Voltages
  - Analogue 1.8V to 3.6V
  - Digital core: 1.42V to 3.6V
  - Digital I/O: 1.8V to 3.6V
- 256fs / 384fs or USB master clock rates: 12MHz, 24MHz
- Audio sample rates: 8, 11.025, 16, 22.05, 24, 32, 44.1, 48, 88.2, 96kHz generated internally from master clock
- 5x5x0.9mm QFN package

APPLICATIONS

- Portable Media Player
- Mobile phone handsets
- Mobile gaming

BLOCK DIAGRAM



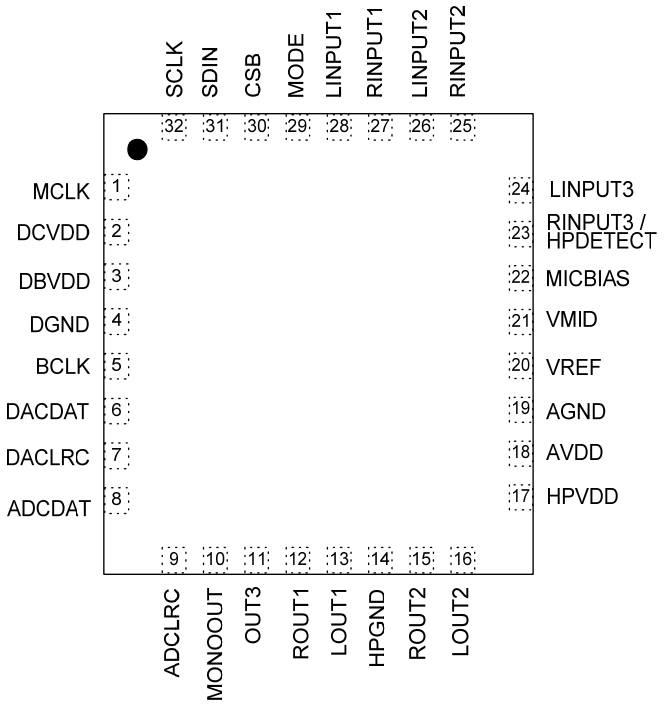
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PIN CONFIGURATION



ORDERING INFORMATION

ORDER CODE	TEMPERATURE RANGE	PACKAGE	MOISTURE SENSITIVITY LEVEL	PEAK SOLDERING TEMPERATURE
WM8750CJLGEFL	-25°C to +85°C	32-lead QFN (5x5x0.9mm) (Pb-free)	MSL1	260°C
WM8750CJLGEFL/R	-25°C to +85°C	32-lead QFN (5x5x0.9mm) (Pb-free, tape and reel)	MSL1	260°C

Note:
Reel quantity = 3500

PIN DESCRIPTION

PIN NO	NAME	TYPE	DESCRIPTION
1	MCLK	Digital Input	Master Clock
2	DCVDD	Supply	Digital Core Supply
3	DBVDD	Supply	Digital Buffer (I/O) Supply
4	DGND	Supply	Digital Ground (return path for both DCVDD and DBVDD)
5	BCLK	Digital Input / Output	Audio Interface Bit Clock
6	DACDAT	Digital Input	DAC Digital Audio Data
7	DACLRC	Digital Input / Output	Audio Interface Left / Right Clock/Clock Out
8	ADCDAT	Digital Output	ADC Digital Audio Data
9	ADCLRC	Digital Input / Output	Audio Interface Left / Right Clock
10	MONOOUT	Analogue Output	Mono Output
11	OUT3	Analogue Output	Analogue Output 3 (can be used as Headphone Pseudo Ground)
12	ROUT1	Analogue Output	Right Output 1 (Line or Headphone)
13	LOUT1	Analogue Output	Left Output 1 (Line or Headphone)
14	HPGND	Supply	Supply for Analogue Output Drivers (LOUT1/2, ROUT1/2)
15	ROUT2	Analogue Output	Right Output 1 (Line or Headphone or Speaker)
16	LOUT2	Analogue Output	Left Output 1 (Line or Headphone or Speaker)
17	HPVDD	Supply	Supply for Analogue Output Drivers (LOUT1/2, ROUT1/2, MONOUT)
18	AVDD	Supply	Analogue Supply
19	AGND	Supply	Analogue Ground (return path for AVDD)
20	VREF	Analogue Output	Reference Voltage Decoupling Capacitor
21	VMID	Analogue Output	Midrail Voltage Decoupling Capacitor
22	MICBIAS	Analogue Output	Microphone Bias
23	RINPUT3 / HPDETECT	Analogue Input	Right Channel Input 3 or Headphone Plug-in Detection
24	LINPUT3	Analogue Input	Left Channel Input 3
25	RINPUT2	Analogue Input	Right Channel Input 2
26	LINPUT2	Analogue Input	Left Channel Input 2
27	RINPUT1	Analogue Input	Right Channel Input 1
28	LINPUT1	Analogue Input	Left Channel Input 1
29	MODE	Digital Input	Control Interface Selection
30	CSB	Digital Input	Chip Select / Device Address Selection
31	SDIN	Digital Input/Output	Control Interface Data Input / 2-wire Acknowledge output
32	SCLK	Digital Input	Control Interface Clock Input

Note:

It is recommended that the QFN ground paddle should be connected to analogue ground on the application PCB.

ABSOLUTE MAXIMUM RATINGS

Absolute Maximum Ratings are stress ratings only. Permanent damage to the device may be caused by continuously operating at or beyond these limits. Device functional operating limits and guaranteed performance specifications are given under Electrical Characteristics at the test conditions specified.



ESD Sensitive Device. This device is manufactured on a CMOS process. It is therefore generically susceptible to damage from excessive static voltages. Proper ESD precautions must be taken during handling and storage of this device.

Wolfson tests its package types according to IPC/JEDEC J-STD-020B for Moisture Sensitivity to determine acceptable storage conditions prior to surface mount assembly. These levels are:

MSL1 = unlimited floor life at <30°C / 85% Relative Humidity. Not normally stored in moisture barrier bag.

MSL2 = out of bag storage for 1 year at <30°C / 60% Relative Humidity. Supplied in moisture barrier bag.

MSL3 = out of bag storage for 168 hours at <30°C / 60% Relative Humidity. Supplied in moisture barrier bag.

The Moisture Sensitivity Level for each package type is specified in Ordering Information.

CONDITION	MIN	MAX
Supply voltages	-0.3V	+3.63V
Voltage range digital inputs	DGND -0.3V	DBVDD +0.3V
Voltage range analogue inputs	AGND -0.3V	AVDD +0.3V
Operating temperature range, T_A	-25°C	+85°C
Storage temperature after soldering	-65°C	+150°C

Notes

1. Analogue and digital grounds must always be within 0.3V of each other.
2. All digital and analogue supplies are independent of each other.
3. DCVDD must be less than or equal to AVDD and DBVDD.

RECOMMENDED OPERATION CONDITIONS

PARAMETER	SYMBOL	MIN	TYP	MAX	UNIT
Digital supply range (Core)	DCVDD	1.42		3.6	V
Digital supply range (Buffer)	DBVDD	1.7		3.6	V
Analogue supplies range	AVDD, HPVDD	1.8		3.6	V
Ground	DGND,AGND, HPGND		0		V

ELECTRICAL CHARACTERISTICS

Test Conditions

DCVDD = 1.5V, DBVDD = 3.3V, AVDD = HPVDD = 3.3V, T_A = +25°C, 1kHz signal, fs = 48kHz, ADCOSR=1, DACOSR=1, PGA gain = 0dB, 24-bit audio data unless otherwise stated.

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Analogue Inputs (LINPUT1, RINPUT1, LINPUT2, RINPUT2, LINPUT3, RINPUT3) to ADC out						
Full Scale Input Signal Level (for ADC 0dB Input at 0dB Gain)	V_{INFS}			AVDD/3.3		V rms
Input Resistance Pins LINPUT1/2/3, RINPUT1/2/3		PGA gain=0dB into ADC		22		kΩ
		PGA gain=+30dB into ADC		1.5		
		DC Measurement from L/RINPUT1		16		
		input pin unused		17		
Input Capacitance				10		pF
Signal to Noise Ratio (A-weighted)	SNR	AVDD = 3.3V ADCOSR=1	80	88		dB
		AVDD = 3.3V ADCOSR=0		95		
		AVDD = 1.8V ADCOSR=1		85		
		AVDD = 1.8V ADCOSR=0		90		
Total Harmonic Distortion	THD	-1dBFs input, AVDD = 3.3V		-80 0.01		dB %
		-1dBFs input, AVDD = 1.8V		-74 0.02		
ADC Channel Separation		1kHz signal		85		dB
Channel Matching		1kHz signal	-0.5		0.5	dB
Analogue Outputs (LOUT1/2, ROUT1/2, MONOOUT)						
0dB Full scale output voltage				AVDD/3.3		Vrms
Mute attenuation		1kHz, full scale signal		90		dB
		MONOOUT pin		81		
Channel Separation		analogue in to analogue out		85		dB
DAC to Line-Out (L/ROUT2 with 10kΩ / 50pF load)						
Signal to Noise Ratio (A-weighted)	SNR	AVDD=3.3V	90	97		dB
		AVDD=1.8V		94		
Total Harmonic Distortion	THD	AVDD=3.3V		-85		dB
		AVDD=1.8V		-79		
Channel Separation		1kHz signal		100		dB
Headphone Output (LOUT1/ROUT1, using capacitors)						
Output Power per channel	P_O	Output power is very closely correlated with THD; see below.				
Total Harmonic Distortion plus Noise	THD+N	HPVDD=1.8V, R_L=32Ω P_O=5mW		0.02 -73		% dB
		HPVDD=1.8V, R_L=16Ω P_O=5mW		0.03 -70		
		HPVDD=3.3V, R_L=32Ω, P_O=5mW		0.015 -76		
		HPVDD=3.3V, R_L=16Ω, P_O=5mW		0.02 -73		
Signal to Noise Ratio (A-weighted)	SNR	HPVDD = 3.3V	90	98		dB
		HPVDD = 1.8V		93		

Test Conditions

DCVDD = 1.5V, DBVDD = 3.3V, AVDD = HPVDD = 3.3V, T_A = +25°C, 1kHz signal, fs = 48kHz, ADCOSR=1, DACOSR=1, PGA gain = 0dB, 24-bit audio data unless otherwise stated.

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Speaker Output (LOUT2/ROUT2 with 8Ω bridge tied load, ROUT2INV=1)						
Output Power at 1% THD	P_O	THD = 1%		330		mW (rms)
Maximum Achievable Output Power	$P_O$max	AVDD=HPVDD=3.3V, R_L=8Ω		400		mW (rms)
Total Harmonic Distortion	THD	Po=200mW, R_L=8Ω, HPVDD=3.3V		-60 0.1		dB %
Signal to Noise Ratio (A-weighted)	SNR	HPVDD=3.3V, R_L=8Ω		95		dB
Analogue Reference Levels						
Midrail Reference Voltage	VMID		–3%	AVDD/2	+3%	V
Buffered Reference Voltage	VREF		–3%	AVDD/2	+3%	V
Microphone Bias						
Bias Voltage	$V_{MICBIAS}$	3mA load current	–5%	0.9×AVDD	+ 5%	V
Bias Current Source	$I_{MICBIAS}$				3	mA
Output Noise Voltage	Vn	1K to 20kHz		15		nV/√Hz
Digital Input / Output						
Input HIGH Level	V_{IH}		0.7×DBVDD			V
Input LOW Level	V_{IL}				0.3×DBVDD	V
Output HIGH Level	V_{OH}	I_{OH} = +1mA	0.9×DBVDD			V
Output LOW Level	V_{OL}	I_{OL} = -1mA			0.1×DBVDD	V
HPDETECT (pin 23)						
Input HIGH Level	V_{IH}		0.7×AVDD			V
Input LOW Level	V_{IL}				0.3×AVDD	V

TYPICAL PERFORMANCE

POWER CONSUMPTION

The power consumption of the WM8750JL depends on the following factors.

- Supply voltages: Reducing the supply voltages also reduces supply currents, and therefore results in significant power savings, especially in the digital sections of the WM8750JL.
- Oversampling rate: Significant power savings can be achieved by running the DAC and ADC at the lower over-sampling rate of 64 (this is achieved by setting ADCOSR and DACOSR to '1' in R24). Note all figures quoted here assume ADCOSR=DACOSR=1.
- Operating mode: Disabling parts of the WM8750JL that are not currently in use (e.g. mic pre-amps, unused outputs, DAC, ADC, etc.) also saves power.

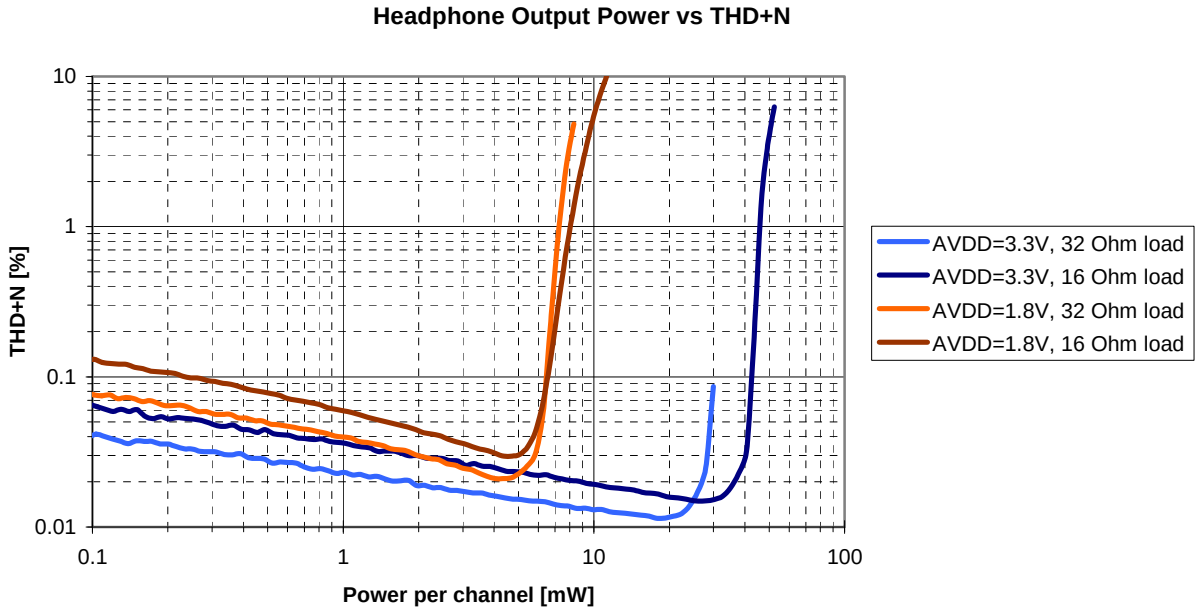
Control Register	R25 (19h)							R26 (1Ah)								R24		R23	Other settings	AVDD		DCVDD		DBVDD		HPVDD		Tot. Power
Bit	VMIDSEL	VREF	AINL	AINR	ADCL	ADCR	MICB	DACL	DACR	LOUT1	ROUT1	LOUT2	ROUT2	MONO	OUT3	ADCOSR	DACOSR	VSEL		V	I (mA)	V	I (mA)	V	I (mA)	V	I (mA)	mW
OFF	00	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	11	Clocks stopped	3.3	0.000	3.3	0.010	3.3	0.000	3.3	0.000	0.0330
																		01		2.5	0.000	2.5	0.008	2.5	0.000	2.5	0.000	0.0200
																		00		1.8	0.000	1.5	0.007	1.8	0.000	1.8	0.000	0.0105
Standby	10	1	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	11	Interface Stopped	3.3	0.360	3.3	0.011	3.3	0.000	3.3	0.000	1.2243
(500 KOhm VMID string)																		01		2.5	0.268	2.5	0.009	2.5	0.000	2.5	0.000	0.6925
																		00		1.8	0.183	1.5	0.007	1.8	0.000	1.8	0.000	0.3399
Playback to Line-out	01	1	0	0	0	0	0	1	1	1	1	0	0	0	0	1	1	11		3.3	2.457	3.3	4.687	3.3	0.250	3.3	0.683	26.6541
																		01		2.5	1.814	2.5	2.779	2.5	0.178	2.5	0.670	13.6025
																		00		1.8	1.606	1.5	1.483	1.8	0.122	1.8	0.406	6.0657
Playback to 32 Ohm Headphone	01	1	0	0	0	0	0	1	1	1	1	0	0	0	0	1	1	11		3.3	2.456	3.3	4.649	3.3	0.250	3.3	0.709	26.6112
																		01		2.5	1.814	2.5	2.758	2.5	0.178	2.5	0.682	13.5800
																		00		1.8	1.606	1.5	1.483	1.8	0.122	1.8	0.410	6.0729
Playback to 32 Ohm Headphone	01	1	0	0	0	0	0	1	1	1	1	0	0	0	0	1	1	11		3.3	2.456	3.3	5.454	3.3	0.250	3.3	1.929	33.2937
0.1mW / channel into load																		01		2.5	1.814	2.5	3.354	2.5	0.178	2.5	1.927	18.1825
(JEITA CP-2905B)																		00		1.8	1.607	1.5	1.831	1.8	0.122	1.8	1.793	9.0861
Playback to 32 Ohm Headphone	01	1	0	0	0	0	0	1	1	1	1	0	0	0	0	1	1	11		3.3	2.470	3.3	5.469	3.3	0.250	3.3	11.248	64.1421
5mW / channel into load																		01		2.5	1.833	2.5	3.408	2.5	0.178	2.5	11.283	41.7550
																		00		1.8	1.635	1.5	1.862	1.8	0.122	1.8	10.974	25.7088
Playback to 32 Ohm Headphone	01	1	0	0	0	0	0	1	1	1	1	0	0	0	1	1	1	11	R24, OUT3SW=00	3.3	2.426	3.3	3.969	3.3	0.251	3.3	1.010	25.2648
(capless mode using OUT3)																		01		2.5	1.788	2.5	2.705	2.5	0.179	2.5	0.980	14.1300
																		00		1.8	1.244	1.5	1.481	1.8	0.122	1.8	0.670	5.8863
Playback to 8 Ohm BTL Speaker	01	1	0	0	0	0	0	1	1	0	0	1	1	0	0	1	1	11	R24, ROUT2INV=1	3.3	2.652	3.3	4.655	3.3	0.250	3.3	1.256	29.0829
																		01		2.5	1.950	2.5	2.761	2.5	0.178	2.5	1.095	14.9600
																		00		1.8	1.694	1.5	1.482	1.8	0.122	1.8	0.773	6.8832
Headphone Amp	01	1	0	0	0	0	0	0	0	1	1	0	0	0	0	1	1	11	Clocks Stopped	3.3	1.107	3.3	0.624	3.3	0.000	3.3	0.685	7.9728
(line-in to 32 Ohm headphone)																		01		2.5	0.812	2.5	0.090	2.5	0.000	2.5	0.672	3.9350
																		00		1.8	0.559	1.5	0.007	1.8	0.000	1.8	0.407	1.7493
Speaker Amp	01	1	0	0	0	0	0	0	0	0	0	1	1	0	0	1	1	11	Clocks Stopped	3.3	1.305	3.3	0.565	3.3	0.000	3.3	0.691	8.4513
(line-in to 8 Ohm speaker)																		01	R24, ROUT2INV=1	2.5	0.948	2.5	0.092	2.5	0.000	2.5	0.679	4.2975
																		00		1.8	0.649	1.5	0.007	1.8	0.000	1.8	0.455	1.9977
Record from Line-in	01	1	1	1	1	1	0	0	0	0	0	0	0	0	0	1	1	11		3.3	4.631	3.3	5.010	3.3	0.273	3.3	0.000	32.7162
																		01		2.5	3.892	2.5	3.237	2.5	0.196	2.5	0.000	18.3125
																		00		1.8	3.239	1.5	1.649	1.8	0.135	1.8	0.000	8.5467
Record from mono microphone	01	1	1	0	1	0	1	0	0	0	0	0	0	0	0	1	1	11	R32, LMICBOOST=11	3.3	2.829	3.3	4.996	3.3	0.273	3.3	0.000	26.7234
																		01	R23, DATSEL=01	2.5	2.330	2.5	3.208	2.5	0.194	2.5	0.000	14.3300
																		00		1.8	1.892	1.5	1.632	1.8	0.134	1.8	0.000	6.0948
Record from mono microphone	01	1	1	0	1	0	1	0	0	0	0	0	0	0	0	1	1	11	R32, LMICBOOST=11	3.3	3.197	3.3	4.993	3.3	0.273	3.3	0.000	27.9279
(differential)																		01	R23, DATSEL=01;	2.5	2.593	2.5	3.208	2.5	0.194	2.5	0.000	14.9875
																		00	R32, LINSEL=11	1.8	2.067	1.5	1.636	1.8	0.134	1.8	0.000	6.4158
Stereo Record & Playback	01	1	1	1	1	1	1	1	1	0	0	1	1	0	0	1	1	11		3.3	6.670	3.3	8.014	3.3	0.272	3.3	0.805	52.0113
																		01		2.5	5.389	2.5	5.326	2.5	0.196	2.5	0.613	28.8100
																		00		1.8	4.281	1.5	2.851	1.8	0.135	1.8	0.329	12.8175

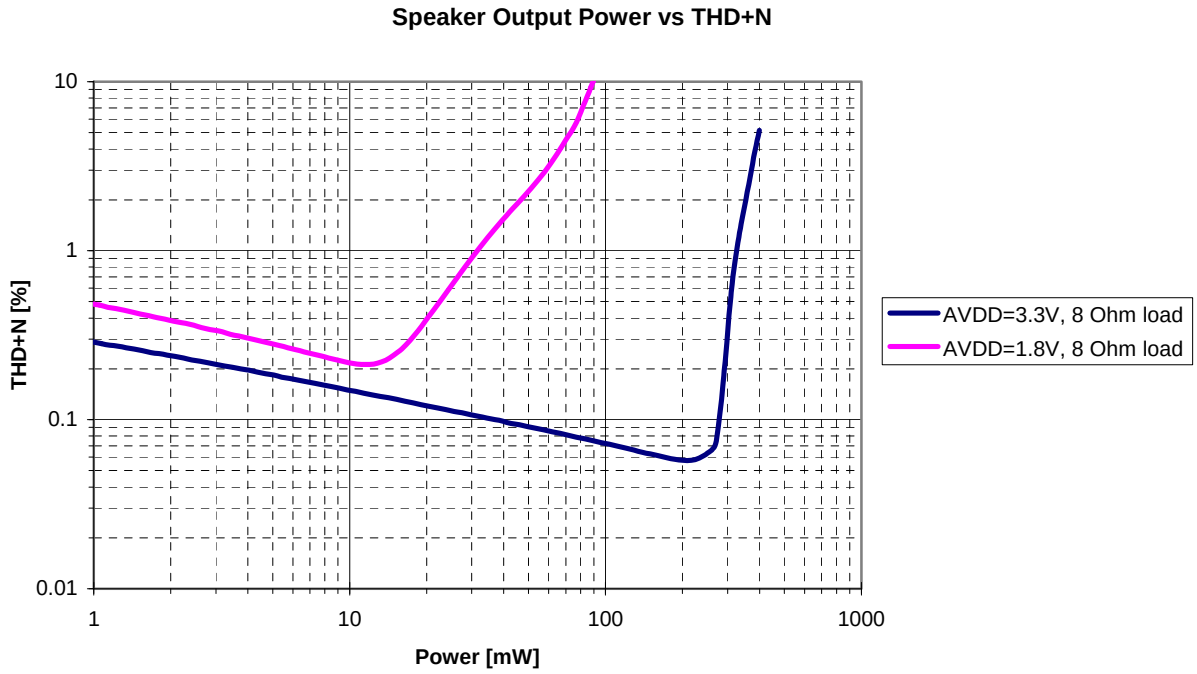
Table 1 Supply Current Consumption

Notes:

1. All figures are at T_A = +25°C, Slave Mode, fs = 48kHz, MCLK = 12.288 MHz (256fs), ADCOSR=DACOSR=1.
2. Unless otherwise noted, these measurements are quiescent (i.e. signal amplitude is zero).

OUTPUT DRIVERS

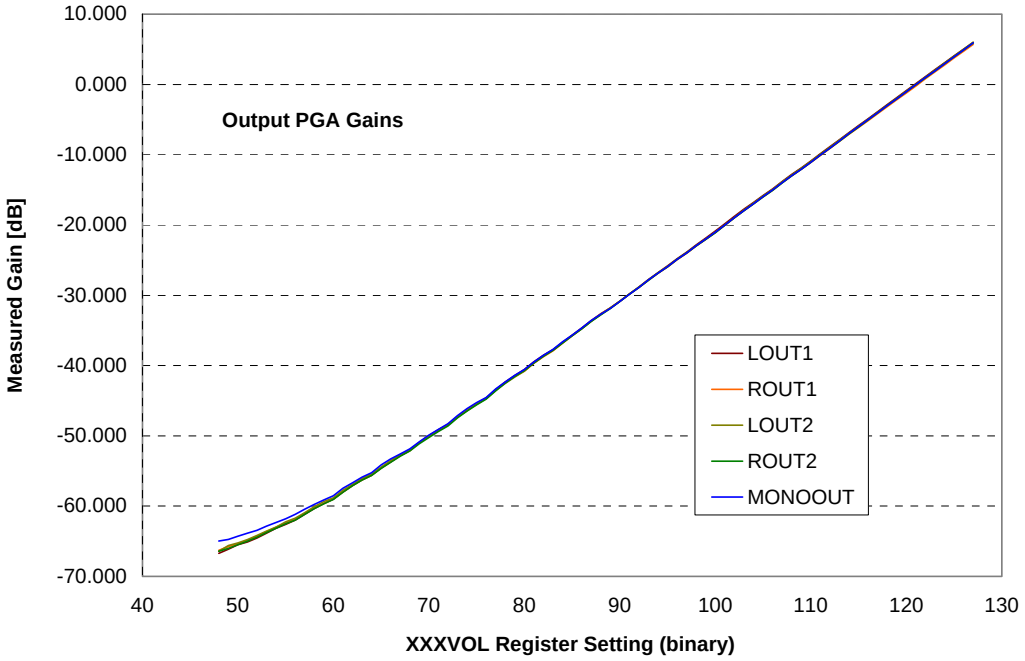


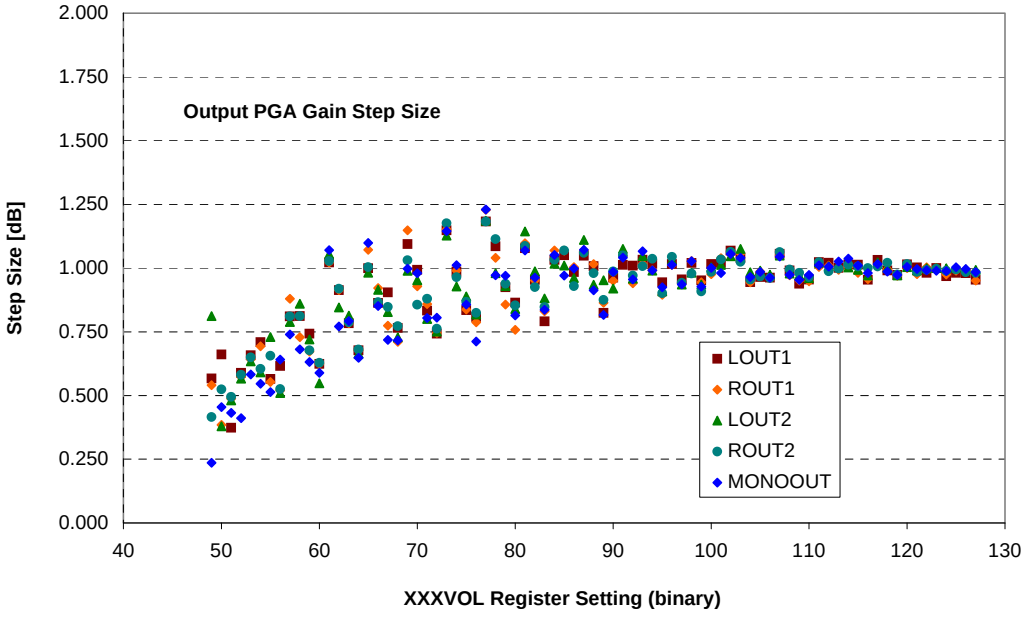


Notes:

1. These graphs show THD+N relative to the signal amplitude at each point (not relative to full scale).
2. Signal frequency = 1kHz

OUTPUT PGA'S LINEARITY





SIGNAL TIMING REQUIREMENTS

SYSTEM CLOCK TIMING

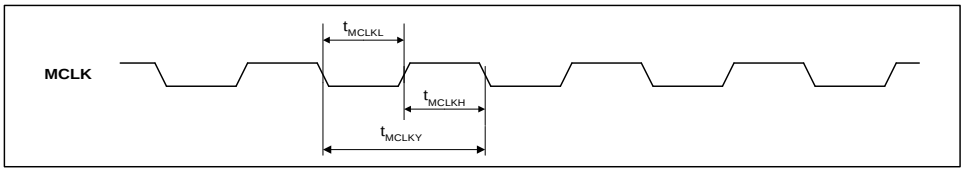


Figure 1 System Clock Timing Requirements

Test Conditions

CLKDIV2=0, DCVDD = 1.42V, DBVDD = 3.3V, DGND = 0V, T_A = +25°C, Slave Mode fs = 48kHz, MCLK = 384fs, 24-bit data, unless otherwise stated.

PARAMETER	SYMBOL	MIN	TYP	MAX	UNIT
System Clock Timing Information					
MCLK System clock pulse width high	T_{MCLKL}	21			ns
MCLK System clock pulse width low	T_{MCLKH}	21			ns
MCLK System clock cycle time	T_{MCLKY}	54			ns
MCLK duty cycle	T_{MCLKDS}	60:40		40:60	

Test Conditions

CLKDIV2=1, DCVDD = 1.42V, DBVDD = 3.3V, DGND = 0V, T_A = +25°C, Slave Mode fs = 48kHz, MCLK = 384fs, 24-bit data, unless otherwise stated.

PARAMETER	SYMBOL	MIN	TYP	MAX	UNIT
System Clock Timing Information					
MCLK System clock pulse width high	T_{MCLKL}	10			ns
MCLK System clock pulse width low	T_{MCLKH}	10			ns
MCLK System clock cycle time	T_{MCLKY}	27			ns

AUDIO INTERFACE TIMING – MASTER MODE

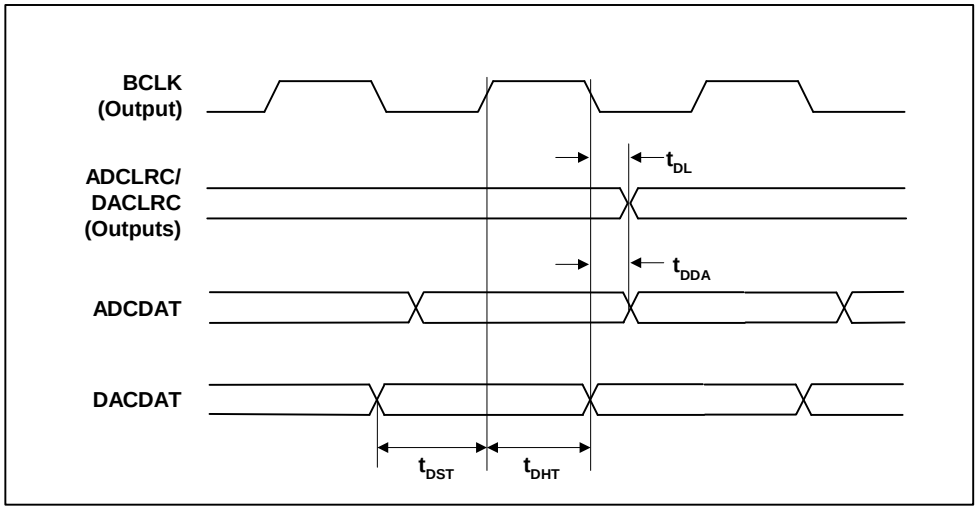


Figure 2 Digital Audio Data Timing – Master Mode (see Control Interface)

Test Conditions

DCVDD = 1.42V, DBVDD = 3.3V, DGND = 0V, T_A = +25°C, Master Mode, fs = 48kHz, MCLK = 256fs, 24-bit data, unless otherwise stated.

PARAMETER	SYMBOL	MIN	TYP	MAX	UNIT
Bit Clock Timing Information					
BCLK rise time (10pF load)	t_{BCLKR}			3	ns
BCLK fall time (10pF load)	t_{BCLKF}			3	ns
BCLK duty cycle (normal mode, BCLK = MCLK/n)	t_{BCLKDS}		50:50		
BCLK duty cycle (USB mode, BCLK = MCLK)	t_{BCLKDS}		T_{MCLKDS}		
Audio Data Input Timing Information					
ADCLRC/DACLRC propagation delay from BCLK falling edge	t_{DL}			10	ns
ADCDAT propagation delay from BCLK falling edge	t_{DDA}			40	ns
DACDAT setup time to BCLK rising edge	t_{DST}	10			ns
DACDAT hold time from BCLK rising edge	t_{DHT}	10			ns

AUDIO INTERFACE TIMING – SLAVE MODE

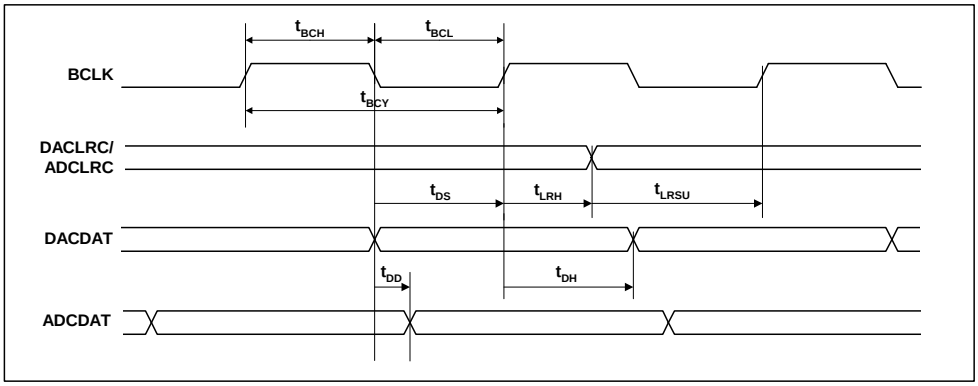


Figure 3 Digital Audio Data Timing – Slave Mode

Test Conditions

DCVDD = 1.42V, DBVDD = 3.3V, DGND = 0V, T_A = +25°C, Slave Mode, fs = 48kHz, MCLK = 256fs, 24-bit data, unless otherwise stated.

PARAMETER	SYMBOL	MIN	TYP	MAX	UNIT
Audio Data Input Timing Information					
BCLK cycle time	t_{BCY}	50			ns
BCLK pulse width high	t_{BCH}	20			ns
BCLK pulse width low	t_{BCL}	20			ns
ADCLRC/DACLRC set-up time to BCLK rising edge	t_{LRSU}	10			ns
ADCLRC/DACLRC hold time from BCLK rising edge	t_{LRH}	10			ns
DACDAT hold time from BCLK rising edge	t_{DH}	10			ns
ADCDAT propagation delay from BCLK falling edge	t_{DD}			10	ns

Note:

BCLK period should always be greater than or equal to MCLK period.

CONTROL INTERFACE TIMING – 3-WIRE MODE

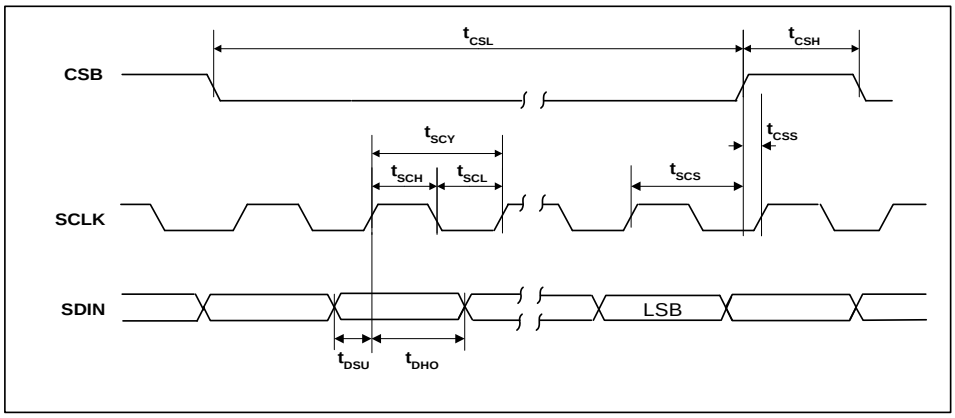


Figure 4 Control Interface Timing – 3-Wire Serial Control Mode

Test Conditions

DCVDD = 1.42V, DBVDD = 3.3V, DGND = 0V, T_A = +25°C, Slave Mode, fs = 48kHz, MCLK = 256fs, 24-bit data, unless otherwise stated.

PARAMETER	SYMBOL	MIN	TYP	MAX	UNIT
Program Register Input Information					
SCLK rising edge to CSB rising edge	t_{SCS}	80			ns
SCLK pulse cycle time	t_{SCY}	200			ns
SCLK pulse width low	t_{SCL}	80			ns
SCLK pulse width high	t_{SCH}	80			ns
SDIN to SCLK set-up time	t_{DSU}	40			ns
SCLK to SDIN hold time	t_{DHO}	40			ns
CSB pulse width low	t_{CSL}	40			ns
CSB pulse width high	t_{CSH}	40			ns
CSB rising to SCLK rising	t_{CSS}	40			ns
Pulse width of spikes that will be suppressed	t_{ps}	0		5	ns

CONTROL INTERFACE TIMING – 2-WIRE MODE

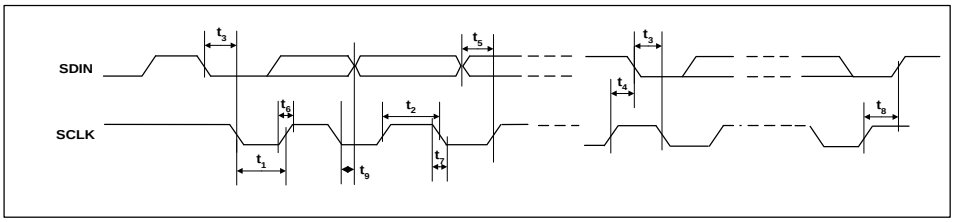


Figure 5 Control Interface Timing – 2-Wire Serial Control Mode

Test Conditions

DCVDD = 1.42V, DBVDD = 3.3V, DGND = 0V, T_A = +25°C, Slave Mode, fs = 48kHz, MCLK = 256fs, 24-bit data, unless otherwise stated.

PARAMETER	SYMBOL	MIN	TYP	MAX	UNIT
Program Register Input Information					
SCLK Frequency		0		526	kHz
SCLK Low Pulse-Width	t_1	1.3			us
SCLK High Pulse-Width	t_2	600			ns
Hold Time (Start Condition)	t_3	600			ns
Setup Time (Start Condition)	t_4	600			ns
Data Setup Time	t_5	100			ns
SDIN, SCLK Rise Time	t_6			300	ns
SDIN, SCLK Fall Time	t_7			300	ns
Setup Time (Stop Condition)	t_8	600			ns
Data Hold Time	t_9			900	ns
Pulse width of spikes that will be suppressed	t_{ps}	0		5	ns

INTERNAL POWER ON RESET CIRCUIT

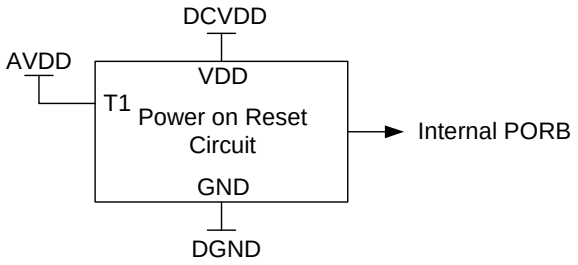


Figure 6 Internal Power on Reset Circuit Schematic

The WM8750JL includes an internal Power-On-Reset Circuit, as shown in Figure 6, which is used to reset the digital logic into a default state after power up. The power on reset circuit is powered from DCVDD and monitors DCVDD and AVDD. It asserts PORB low if DCVDD or AVDD are below a minimum threshold.

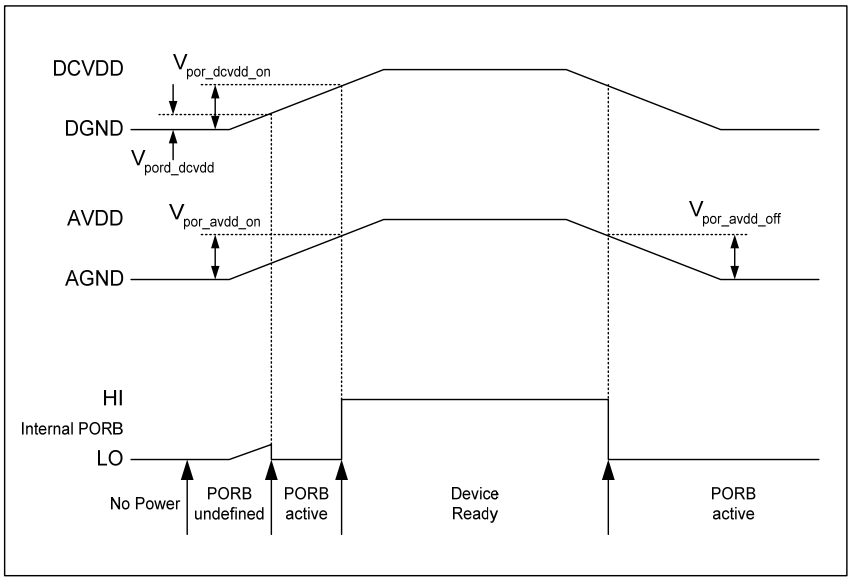


Figure 7 Typical Power-Up Sequence

Figure 7 shows a typical power-up sequence. When DCVDD and AVDD rise above the minimum thresholds, Vpord_dcvdd and Vpord_avdd, there is enough voltage for the circuit to guarantee the Power on Reset is asserted low and the chip is held in reset. In this condition, all writes to the control interface are ignored. When DCVDD rises to Vpor_dcvdd_on and AVDD rises to Vpor_avdd_on, PORB is released high and all registers are in their default state and writes to the control interface may take place. If DCVDD and AVDD rise at different rates then PORB will only be released when DCVDD and AVDD have both exceeded the Vpor_dcvdd_on and Vpor_avdd_on thresholds.

On power down, PORB is asserted low whenever DCVDD drops below the minimum threshold Vpor_dcvdd_off or AVDD drops below the minimum threshold Vpor_avdd_off.

SYMBOL	MIN	TYP	MAX	UNIT
V_{pord_dcvdd}	0.4	0.6	0.8	V
$V_{por_dcvdd_on}$	0.9	1.26	1.6	V
$V_{por_avdd_on}$	0.5	0.7	0.9	V
$V_{por_avdd_off}$	0.4	0.6	0.8	V

Table 2 Typical POR Operation (typical values, not tested)

DEVICE DESCRIPTION

INTRODUCTION

The WM8750JL is a low power audio codec offering a combination of high quality audio, advanced features, low power and small size. These characteristics make it ideal for portable digital audio applications such as MP3 and minidisk player / recorders. Stereo 24-bit multi-bit delta sigma ADCs and DACs are used with oversampling digital interpolation and decimation filters.

The device includes three stereo analogue inputs that can be switched internally. Each can be used as either a line level input or microphone input and LINPUT1/RINPUT1 and LINPUT2/RINPUT2 can be configured as mono differential inputs. A programmable gain amplifier with automatic level control (ALC) keeps the recording volume constant. The on-chip stereo ADC and DAC are of a high quality using a multi-bit, low-order oversampling architecture to deliver optimum performance with low power consumption.

The DAC output signal first enters an analogue mixer where an analogue input and/or the post-ALC signal can be added to it. This mix is available on line and headphone outputs.

The WM8750JL has a configurable digital audio interface where ADC data can be read and digital audio playback data fed to the DAC. It supports a number of audio data formats including I^2S, DSP Mode (a burst mode in which frame sync plus 2 data packed words are transmitted), and MSB-First, left justified, and can operate in master or slave modes.

The WM8750JL uses a unique clocking scheme that can generate many commonly used audio sample rates from either a 12.00MHz USB clock or an industry standard 256/384 f_s clock. This feature eliminates the common requirement for an external phase-locked loop (PLL) in applications where the master clock is not an integer multiple of the sample rate. Sample rates of 8kHz, 11.025kHz, 12kHz, 16kHz, 22.05kHz, 24kHz, 32kHz, 44.1kHz, 48kHz, 88.2kHz and 96kHz can be generated. The digital filters used for recording and playback are optimised for each sampling rate used.

To allow full software control over all its features, the WM8750JL offers a choice of 2 or 3 wire MPU control interface. It is fully compatible and an ideal partner for a wide range of industry standard microprocessors, controllers and DSPs.

The design of the WM8750JL has given much attention to power consumption without compromising performance. It operates at very low voltages, and includes the ability to power off parts of the circuitry under software control, including standby and power off modes.

INPUT SIGNAL PATH

The input signal path for each channel consists of a switch to select between three analogue inputs, followed by a PGA (programmable gain amplifier) and an optional microphone gain boost. A differential input of either (LINPUT1 – RINPUT1) or (LINPUT2 – RINPUT2) may also be selected. The gain of the PGA can be controlled either by the user or by the on-chip ALC function (see Automatic Level Control).

The signal then enters an ADC where it is digitised. Alternatively, the two channels can also be mixed in the analogue domain and digitised in one ADC while the other ADC is switched off. The mono-mix signal appears on both digital output channels.

SIGNAL INPUTS

The WM8750JL has three sets of high impedance, low capacitance AC coupled analogue inputs, LINPUT1/RINPUT1, LINPUT2/RINPUT2 and LINPUT3/RINPUT3. Inputs can be configured as microphone or line level by enabling or disabling the microphone gain boost.

LINSEL and RINSEL control bits (see Table 3) are used to select independently between external inputs and internally generated differential products (LINPUT1-RINPUT1 or LINPUT2-RINPUT2). The choice of differential signal, LINPUT1-RINPUT1 or LINPUT2-RINPUT2 is made using DS (refer to Table 5).

As an example, the WM8750JL can be set up to convert one differential and one single ended mono signal by applying the differential signal to LINPUT1/RINPUT1 and the single ended signal to RINPUT2. By setting LINSEL to L-R Differential (see Table 3), DS to LINPUT1 – RINPUT1 (see Table 5) and RINSEL to RINPUT2, each mono signal can then be routed to a separate ADC or Bypass path.

The signal inputs are biased internally to the reference voltage VREF. Whenever the line inputs are muted or the device placed into standby mode, the inputs are kept biased to VREF using special anti-thump circuitry. This reduces any audible clicks that may otherwise be heard when changing inputs.

DC MEASUREMENT

For DC measurements (for example, battery voltage monitoring), the input signal at the LINPUT1 and/or RINPUT1 pins can be taken directly into the respective ADC, bypassing both PGA and microphone boost. The ADC output then becomes unsigned relative to AVDD, instead of being a signed (two's complement) number relative to VREF. Setting L/RDCM will override L/RINSEL. The input range for dc measurement is AGND to AVDD.

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION
R32 (20h) ADC Signal Path Control (Left)	7:6	LINSEL	00	Left Channel Input Select 00 = LINPUT1 01 = LINPUT2 10 = LINPUT3 11 = L-R Differential (either LINPUT1-RINPUT1 or LINPUT2-RINPUT2, selected by DS)
	5:4	LMICBOOST	00	Left Channel Microphone Gain Boost 00 = Boost off (bypassed) 01 = 13dB boost 10 = 20dB boost 11 = 29dB boost
R33 (21h) ADC Signal Path Control (Right)	7:6	RINSEL	00	Right Channel Input Select 00 = RINPUT1 01 = RINPUT2 10 = RINPUT3 11 = L-R Differential (either LINPUT1-RINPUT1 or LINPUT2-RINPUT2, selected by DS)
	5:4	RMICBOOST	00	Right Channel Microphone Gain Boost 00 = Boost off (bypassed) 01 = 13dB boost 10 = 20dB boost 11 = 29dB boost

Table 3 Input Software Control

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION
R31 (1Fh) ADC input Mode	5	RDCM	0	Right Channel DC Measurement 0 = Normal Operation, PGA Enabled 1 = Measure DC level on RINPUT1
	4	LDCM	0	Left Channel DC Measurement 0 = Normal Operation, PGA Enabled 1 = Measure DC level on LINPUT1

Table 4 DC Measurement Select

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION
R31 (1Fh) ADC Input Mode	8	DS	0	Differential input select 0: LINPUT1 – RINPUT1 1: LINPUT2 – RINPUT2

Table 5 Differential Input Select

MONO MIXING

The stereo ADC can operate as a stereo or mono device, or the two channels can be mixed to mono in the analogue domain (i.e. before the ADC). MONOMIX selects the mode of operation; either the left or right channel ADC can be used, allowing the unused ADC to be powered off or used for a DC measurement conversion. The user also has the flexibility to select the data output from the audio interface using DATSEL. The default is for left and right channel ADC data to be output, but the interface may also be configured so that e.g. left channel ADC data is output as both left and right data for when mono mixing is selected.

Note:

If DC measurement is selected this overrides the MONOMIX selection.

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION
R31 (1Fh) ADC input Mode	7:6	MONOMIX [1:0]	00	00: Stereo 01: Analogue Mono Mix (using left ADC) 10: Analogue Mono Mix (using right ADC) 11: Reserved

Table 6 Mono Mixing

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION
R23 (17h) Additional Control (1)	3:2	DATSEL [1:0]	00	00: left data=left ADC; right data =right ADC 01: left data =left ADC; right data = left ADC 10: left data = right ADC; right data =right ADC 11: left data = right ADC; right data = left ADC

Table 7 ADC Data Output Configuration

The MICBIAS output provides a low noise reference voltage suitable for biasing electret type microphones and the associated external resistor biasing network. Refer to the Applications Information section for recommended external components. The output can be enabled or disables using the MICB control bit (see also the “Power Management” section).

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION
R25 (19h) Power Management (1)	1	MICB	0	Microphone Bias Enable 0 = OFF (high impedance output) 1 = ON

Table 8 Microphone Bias Control

The internal MICBIAS circuitry is shown below. Note that the is a maximum source current capability for MICBIAS is 3mA. The external biasing resistors therefore must be large enough to limit the MICBIAS current to 3mA.

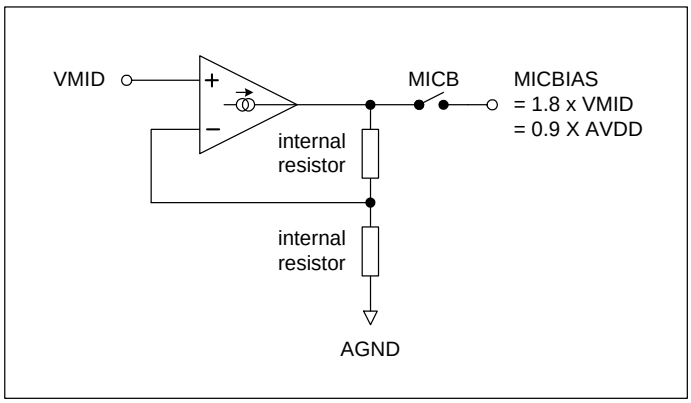


Figure 8 Microphone Bias Schematic

PGA CONTROL

The PGA matches the input signal level to the ADC input range. The PGA gain is logarithmically adjustable from +30dB to –17.25dB in 0.75dB steps. Each PGA can be controlled either by the user or by the ALC function (see Automatic Level Control). When ALC is enabled for one or both channels, then writing to the corresponding PGA control register has no effect.

The gain is independently adjustable on both Right and Left Line Inputs. Additionally, by controlling the register bits LIVU and RIVU, the left and right gain settings can be simultaneously updated. Setting the LZCEN and RZCEN bits enables a zero-cross detector which ensures that PGA gain changes only occur when the signal is at zero, eliminating any zipper noise. If zero cross is enabled a timeout is also available to update the gain if a zero cross does not occur. This function may be enabled by setting TOEN in register R23 (17h).

The inputs can also be muted in the analogue domain under software control. The software control registers are shown in Table 9. If zero crossing is enabled, it is necessary to enable zero cross timeout to un-mute the input PGAs. This is because their outputs will not cross zero when muted. Alternatively, zero cross can be disabled before sending the un-mute command.

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION
R0 (00h) Left Channel PGA	8	LIVU	0	Left Volume Update 0 = Store LINVOL in intermediate latch (no gain change) 1 = Update left and right channel gains (left = LINVOL, right = intermediate latch)
	7	LINMUTE	1	Left Channel Input Analogue Mute 1 = Enable Mute 0 = Disable Mute Note: LIVU must be set to un-mute.
	6	LZCEN	0	Left Channel Zero Cross Detector 1 = Change gain on zero cross only 0 = Change gain immediately
	5:0	LINVOL [5:0]	010111 (0dB)	Left Channel Input Volume Control 111111 = +30dB 111110 = +29.25dB . . 0.75dB steps down to 000000 = -17.25dB
R1 (01h) Right Channel PGA	8	RIVU	0	Right Volume Update 0 = Store RINVOL in intermediate latch (no gain change) 1 = Update left and right channel gains (right = RINVOL, left = intermediate latch)
	7	RINMUTE	1	Right Channel Input Analogue Mute 1 = Enable Mute 0 = Disable Mute Note: RIVU must be set to un-mute.
	6	RZCEN	0	Right Channel Zero Cross Detector 1 = Change gain on zero cross only 0 = Change gain immediately
	5:0	RINVOL [5:0]	010111 (0dB)	Right Channel Input Volume Control 111111 = +30dB 111110 = +29.25dB . . 0.75dB steps down to 000000 = -17.25dB
R23 (17h) Additional Control (1)	0	TOEN	0	Timeout Enable 0 : Timeout Disabled 1 : Timeout Enabled

Table 9 Input PGA Software Control

ANALOGUE TO DIGITAL CONVERTER (ADC)

The WM8750JL uses a multi-bit, oversampled sigma-delta ADC for each channel. The use of multi-bit feedback and high oversampling rates reduces the effects of jitter and high frequency noise. The ADC Full Scale input level is proportional to AVDD. With a 3.3V supply voltage, the full scale level is 1.0 Volts r.m.s. Any voltage greater than full scale may overload the ADC and cause distortion.

ADC DIGITAL FILTER

The ADC filters perform true 24 bit signal processing to convert the raw multi-bit oversampled data from the ADC to the correct sampling frequency to be output on the digital audio interface. The digital filter path is illustrated in Figure 9.

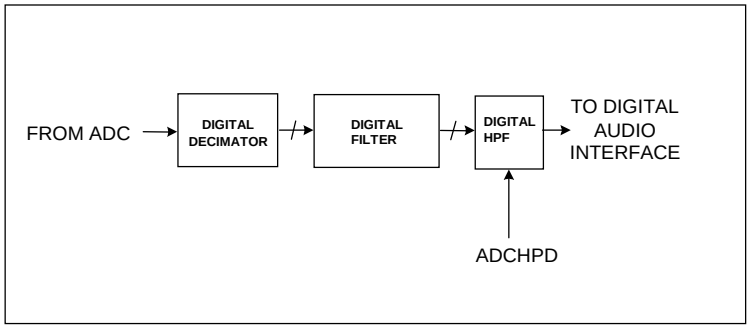


Figure 9 ADC Digital Filter

The ADC digital filters contain a digital high pass filter, selectable via software control. The high-pass filter response is detailed in the Digital Filter Characteristics section. When the high-pass filter is enabled the dc offset is continuously calculated and subtracted from the input signal. By setting HPOR, the last calculated dc offset value is stored when the high-pass filter is disabled and will continue to be subtracted from the input signal. If the DC offset is changed, the stored and subtracted value will not change unless the high-pass filter is enabled. This feature can be used for calibration purposes. In addition the highpass filter may be enabled separately on the left and right channels (see Table 11).

The output data format can be programmed by the user to accommodate stereo or monophonic recording on both inputs. The polarity of the output signal can also be changed under software control. The software control is shown in Table 10.

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION
R5 (05h) ADC and DAC Control	6:5	ADCPOL [1:0]	00	00 = Polarity not inverted 01 = L polarity invert 10 = R polarity invert 11 = L and R polarity invert
	4	HPOR	0	Store dc offset when high-pass filter disabled 1 = store offset 0 = clear offset
	0	ADCHPD	0	ADC high-pass filter enable (Digital) HPFLREN = 0 1 = Disable high-pass filter on left and right channels 0 = Enable high-pass filter on left and right channels
				HPFLREN = 1 0 = High-pass enabled on left, disabled on right 1 = High-pass enabled on right, disabled on left
R27 (1Bh)	5	HPFLREN	0	ADC high-pass filter left or right enable 0 = High-pass filter enable/disable on left and right channels controlled by ADCHPD 1 = High-pass filter enabled on left or right channel, as selected by ADCHPD

Table 10 ADC Signal Path Control

HPFLREN	ADCHPD	HIGH PASS MODE
0	0	High-pass filter enabled on left and right channels
0	1	High-pass filter disabled on left and right channels
1	0	High-pass filter enabled on left channel, disabled on right channel
1	1	High-pass filter disabled on left channel, enabled on right channel

Table 11 ADC High Pass Filter Enable Modes

DIGITAL ADC VOLUME CONTROL

The output of the ADCs can be digitally amplified or attenuated over a range from –97dB to +30dB in 0.5dB steps. The volume of each channel can be controlled separately. The gain for a given eight-bit code X is given by:

$0.5 \times (X-195)$ dB for $1 \leq X \leq 255$; MUTE for $X = 0$

The LAVU and RAVU control bits control the loading of digital volume control data. When LAVU or RAVU are set to 0, the LADCVOL or RADCVOL control data will be loaded into the respective control register, but will not actually change the digital gain setting. Both left and right gain settings are updated when either LAVU or RAVU are set to 1. This makes it possible to update the gain of both channels simultaneously.

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION
R21 (15h) Left ADC Digital Volume	7:0	LADCVOL [7:0]	11000011 (0dB)	Left ADC Digital Volume Control 0000 0000 = Digital Mute 0000 0001 = -97dB 0000 0010 = -96.5dB ... 0.5dB steps up to 1111 1111 = +30dB
	8	LAVU	0	Left ADC Volume Update 0 = Store LADCVOL in intermediate latch (no gain change) 1 = Update left and right channel gains (left = LADCVOL, right = intermediate latch)
R22 (16h) Right ADC Digital Volume	7:0	RADCVOL [7:0]	11000011 (0dB)	Right ADC Digital Volume Control 0000 0000 = Digital Mute 0000 0001 = -97dB 0000 0010 = -96.5dB ... 0.5dB steps up to 1111 1111 = +30dB
	8	RAVU	0	Right ADC Volume Update 0 = Store RADCVOL in intermediate latch (no gain change) 1 = Update left and right channel gains (left = intermediate latch, right = RADCVOL)

Table 12 ADC Digital Volume Control

AUTOMATIC LEVEL CONTROL (ALC)

The WM8750JL has an automatic level control that aims to keep a constant recording volume irrespective of the input signal level. This is achieved by continuously adjusting the PGA gain so that the signal level at the ADC input remains constant. A digital peak detector monitors the ADC output and changes the PGA gain if necessary. Note that when the ALC function is enabled, the settings of registers 0 and 1 (LINVOL, LIVU, LIZC, LINMUTE, RINVOL, RIVU, RIZC and RINMUTE) are ignored. A selectable Zero-Cross function ensures that the ALC volume updates will be timed to coincide with a zero-crossing of the audio signal.

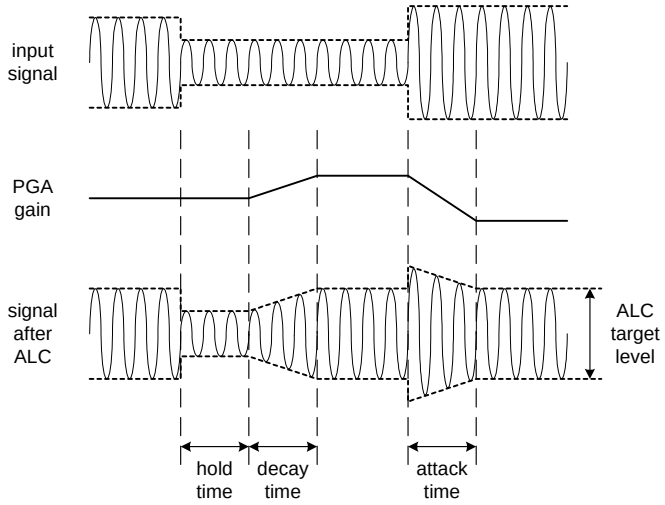


Figure 10 ALC Operation

The ALC function is enabled using the ALCSEL control bits. When enabled, the recording volume can be programmed between –6dB and –28.5dB (relative to ADC full scale) using the ALCL register bits. An upper limit for the PGA gain can be imposed by setting the MAXGAIN control bits.

HLD, DCY and ATK control the hold, decay and attack times, respectively:

Hold time is the time delay between the peak level detected being below target and the PGA gain beginning to ramp up. It can be programmed in power-of-two (2^n) steps, e.g. 2.67ms, 5.33ms, 10.67ms etc. up to 43.7s. Alternatively, the hold time can also be set to zero. The hold time only applies to gain ramp-up, there is no delay before ramping the gain down when the signal level is above target.

Decay (Gain Ramp-Up) Time is the time that it takes for the PGA gain to ramp up across 90% of its range (e.g. from –15B up to 27.75dB). The time it takes for the recording level to return to its target value therefore depends on both the decay time and on the gain adjustment required. If the gain adjustment is small, it will be shorter than the decay time. The decay time can be programmed in power-of-two (2^n) steps, from 24ms, 48ms, 96ms, etc. to 24.58s.

Attack (Gain Ramp-Down) Time is the time that it takes for the PGA gain to ramp down across 90% of its range (e.g. from 27.75dB down to -15B gain). The time it takes for the recording level to return to its target value therefore depends on both the attack time and on the gain adjustment required. If the gain adjustment is small, it will be shorter than the attack time. The attack time can be programmed in power-of-two (2^n) steps, from 6ms, 12ms, 24ms, etc. to 6.14s.

When operating in stereo, the peak detector takes the maximum of left and right channel peak values, and any new gain setting is applied to both left and right PGAs, so that the stereo image is preserved. However, the ALC function can also be enabled on one channel only. In this case, only one PGA is controlled by the ALC mechanism, while the other channel runs independently with its PGA gain set through the control register.

When one ADC channel is unused or used for DC measurement, the peak detector disregards that channel. The ALC function can also operate when the two ADC outputs are mixed to mono in the digital domain, but not if they are mixed to mono in the analogue domain, before entering the ADCs.

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION
R17 (11h) ALC Control 1	8:7	ALCSEL [1:0]	00 (OFF)	ALC function select 00 = ALC off (PGA gain set by register) 01 = Right channel only 10 = Left channel only 11 = Stereo (PGA registers unused) Note: ensure that LINVOL and RINVOL settings (reg. 0 and 1) are the same before entering this mode.
	6:4	MAXGAIN [2:0]	111 (+30dB)	Set Maximum Gain of PGA 111 : +30dB 110 : +24dB ….(-6dB steps) 001 : -6dB 000 : -12dB
	3:0	ALCL [3:0]	1011 (-12dB)	ALC target – sets signal level at ADC input 0000 = -28.5dB FS 0001 = -27.0dB FS … (1.5dB steps) 1110 = -7.5dB FS 1111 = -6dB FS
R18 (12h) ALC Control 2	7	ALCZC	0 (zero cross off)	ALC Zero Cross detect 0 = Change gain immediately 1 = Change gain on zero cross only
	3:0	HLD [3:0]	0000 (0ms)	ALC hold time before gain is increased. 0000 = 0ms 0001 = 2.67ms 0010 = 5.33ms … (time doubles with every step) 1111 = 43.691s
R19 (13h) ALC Control 3	7:4	DCY [3:0]	0011 (192ms)	ALC decay (gain ramp-up) time 0000 = 24ms 0001 = 48ms 0010 = 96ms … (time doubles with every step) 1010 or higher = 24.58s
	3:0	ATK [3:0]	0010 (24ms)	ALC attack (gain ramp-down) time 0000 = 6ms 0001 = 12ms 0010 = 24ms … (time doubles with every step) 1010 or higher = 6.14s

Table 13 ALC Control

Note: For correct ALC operation in differential input mode it is recommended that the ALC is not used with a combined signal gain (mic boost and PGA) greater than 30dB.

ALC ZERO CROSS

The ALC Zero Cross function can be used to ensure that the ALC volume updates will be timed to coincide with a suitable zero-crossing of the audio signal. This avoids audible 'zipper noise' effects of instantaneous volume changes. The ALC Zero Cross function includes a timeout to ensure that the gain is updated even if a zero cross does not occur. If the signal level is small, it is possible that a zero cross does not occur, due to DC offset within the signal path. In this case, the timeout will ensure that the ALC volume change is still executed.

Note that the PGA Control Zero Cross function described earlier (see "Input Signal Path") also has a timeout function. Because the ALC function applies volume changes via a series of small changes, the ALC Zero Cross timeout needs to be many times faster than the normal, register-controlled PGA volume control. This improves the ALC response, in particular when handling small signals, where the zero-cross function may be less effective.

The ALC zero-cross timeout is duration is fixed in relation to MCLK. The maximum ALC zero-cross timeout period is given by the equation below. In the case of a 12.288MHz MCLK, the maximum timeout duration is approximately 21ms.

$$\text{Maximum Timeout (s)} = \frac{2 \times 2^{17}}{\text{MCLK (Hz)}}$$

PEAK LIMITER

To prevent clipping when a large signal occurs just after a period of quiet, the ALC circuit includes a limiter function. If the ADC input signal exceeds 87.5% of full scale (–1.16dB), the PGA gain is ramped down at the maximum attack rate (as when ATK = 0000), until the signal level falls below 87.5% of full scale. This function is automatically enabled whenever the ALC is enabled.

Note:

If ATK = 0000, then the limiter makes no difference to the operation of the ALC. It is designed to prevent clipping when long attack times are used.

NOISE GATE

When the signal is very quiet and consists mainly of noise, the ALC function may cause "noise pumping", i.e. loud hissing noise during silence periods. The WM8750JL has a noise gate function that prevents noise pumping by comparing the signal level at the LINPUT1/2/3 and/or RINPUT1/2/3 pins against a noise gate threshold, NGTH. The noise gate cuts in when:

- Signal level at ADC [dB] < NGTH [dB] + PGA gain [dB] + Mic Boost gain [dB]

This is equivalent to:

- Signal level at input pin [dB] < NGTH [dB]

The ADC output can then either be muted or alternatively, the PGA gain can be held constant (preventing it from ramping up as it normally would when the signal is quiet).

The table below summarises the noise gate control register. The NGTH control bits set the noise gate threshold with respect to the ADC full-scale range. The threshold is adjusted in 1.5dB steps. Levels at the extremes of the range may cause inappropriate operation, so care should be taken with set–up of the function. Note that the noise gate only works in conjunction with the ALC function, and always operates on the same channel(s) as the ALC (left, right, both, or none).

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION
R20 (14h) Noise Gate Control	7:3	NGTH [4:0]	00000	Noise gate threshold 17 -76.5dBfs 17 -75dBfs … 1.5 dB steps 11110 -31.5dBfs 11111 -30dBfs
	2:1	NGG [1:0]	00	Noise gate type X0 = PGA gain held constant 01 = mute ADC output 11 = reserved (do not use this setting)
	0	NGAT	0	Noise gate function enable 1 = enable 0 = disable

Table 14 Noise Gate Control

Note:

The performance of the ADC may degrade at high input signal levels if the monitor bypass mux is selected with MIC boost and ALC enabled.

3D STEREO ENHANCEMENT

The WM8750JL has a digital 3D enhancement option to artificially increase the separation between the left and right channels. This effect can be used for recording or playback, but not for both simultaneously. Selection of 3D for record or playback is controlled by register bit MODE3D.

Important:

Switching the 3D filter from record to playback or from playback to record may only be done when ADC and DAC are disabled. The WM8750JL control interface will only allow MODE3D to be changed when ADC and DAC are disabled (i.e. bits ADCL, ADCR, DACL and DACR in reg. 26 / 1Ah are all zero).

The 3D enhancement function is activated by the 3DEN bit, and has two programmable parameters. The 3DDEPTH setting controls the degree of stereo expansion. Additionally, one of four filter characteristics can be selected for the 3D processing, using the 3DVC and 3DLC control bits.

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION
R16 (10h) 3D enhance	7	MODE3D	0	Playback/Record 3D select 0 = 3D selected for Record 1 = 3D selected for Playback
	6	3DUC	0	Upper Cut-off frequency 0 = High (2.2kHz at 48kHz sampling) 1 = Low (1.5kHz at 48kHz sampling)
	5	3DLC	0	Lower Cut-off frequency 0 = Low (200Hz at 48kHz sampling) 1 = High (500Hz at 48kHz sampling)
	4:1	3DDEPTH [3:0]	0000	Stereo depth 0000: 0% (minimum 3D effect) 0001: 6.67% .... 1110: 93.3% 1111: 100% (maximum 3D effect)
	0	3DEN	0	3D function enable 1: enabled 0: disabled

Table 15 3D Stereo Enhancement Function

When 3D enhancement is enabled (and/or the graphic equaliser for playback) it may be necessary to attenuate the signal by 6dB to avoid limiting. This is a user selectable function, enabled by setting ADCDIV2 for the record path and DACDIV2 for the playback path.

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION
R5 (05h) ADC and DAC control	8	ADCDIV2	0	ADC 6dB attenuate enable 0 = disabled (0dB) 1 = -6dB enabled
	7	DACDIV2	0	DAC 6dB attenuate enable 0 = disabled (0dB) 1 = -6dB enabled

Table 16 ADC and DAC 6dB Attenuation Select

OUTPUT SIGNAL PATH

The WM8750JL output signal paths consist of digital filters, DACs, analogue mixers and output drivers. The digital filters and DACs are enabled when the WM8750JL is in 'playback only' or 'record and playback' mode. The mixers and output drivers can be separately enabled by individual control bits (see Analogue Outputs). Thus it is possible to utilise the analogue mixing and amplification provided by the WM8750JL, irrespective of whether the DACs are running or not.

The WM8750JL receives digital input data on the DACDAT pin. The digital filter block processes the data to provide the following functions:

- Digital volume control
- Graphic equaliser and Dynamic Bass Boost
- Sigma-Delta Modulation

Two high performance sigma-delta audio DACs convert the digital data into two analogue signals (left and right). These can then be mixed with analogue signals from the LINPUT1/2/3 and RINPUT1/2/3 pins, and the mix is fed to the output drivers, LOUT1/ROUT1, LOUT2/ROUT2, OUT3 and MONOOUT.

- LOUT1/ROUT1/OUT3: can drive a 16Ω or 32Ω stereo headphone or stereo line output.
- LOUT2/ROUT2: can drive a 16Ω or 32Ω stereo headphone or stereo line output, or an 8Ω mono speaker.
- MONOOUT: can drive a mono line output or other load down to 10kΩ

DIGITAL DAC VOLUME CONTROL

The signal volume from each DAC can be controlled digitally, in the same way as the ADC volume (see Digital ADC Volume Control). The gain and attenuation range is –127dB to 0dB in 0.5dB steps. The level of attenuation for an eight-bit code X is given by:

$0.5 \times (X-255)$ dB for $1 \leq X \leq 255$; MUTE for $X = 0$

The LDVU and RDVU control bits control the loading of digital volume control data. When LDVU or RDVU are set to 0, the LDACVOL or RDACVOL control data is loaded into an intermediate register, but the actual gain does not change. Both left and right gain settings are updated simultaneously when either LDVU or RDVU are set to 1.

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION
R10 (0Ah) Left Channel Digital Volume	8	LDVU	0	Left DAC Volume Update 0 = Store LDACVOL in intermediate latch (no gain change) 1 = Update left and right channel gains (left = LDACVOL, right = intermediate latch)
	7:0	LDACVOL [7:0]	11111111 (0dB)	Left DAC Digital Volume Control 0000 0000 = Digital Mute 0000 0001 = -127dB 0000 0010 = -126.5dB ... 0.5dB steps up to 1111 1111 = 0dB
R11 (0Bh) Right Channel Digital Volume	8	RDVU	0	Right DAC Volume Update 0 = Store RDACVOL in intermediate latch (no gain change) 1 = Update left and right channel gains (left = intermediate latch, right = RDACVOL)
	7:0	RDACVOL [7:0]	11111111 (0dB)	Right DAC Digital Volume Control similar to LDACVOL

Table 17 Digital Volume Control

GRAPHIC EQUALISER

The WM8750JL has a digital graphic equaliser and adaptive bass boost function. This function operates on digital audio data before it is passed to the audio DACs. Bass enhancement can take two different forms:

- Linear bass control: bass signals are amplified or attenuated by a user programmable gain. This is independent of signal volume, and very high bass gains on loud signals may lead to signal clipping.
- Adaptive bass boost: The bass volume is amplified by a variable gain. When the bass volume is low, it is boosted more than when the bass volume is high. This method is recommended because it prevents clipping, and usually sounds more pleasant to the human ear.

Treble control applies a user programmable gain, without any adaptive boost function. Bass and treble control are completely independent with separately programmable gains and filter characteristics.

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION		
R12 (0Ch) Bass Control	7	BB	0	Bass Boost 0 = Linear bass control 1 = Adaptive bass boost		
	6	BC	0	Bass Filter Characteristic 0 = Low Cutoff (130Hz at 48kHz sampling) 1 = High Cutoff (200Hz at 48kHz sampling)		
	3:0	BASS [3:0]	1111 (Disabled)	Bass Intensity		
				Code	BB=0	BB=1
				0000	+9dB	15 (max)
				0001	+9dB	14
				0010	+7.5dB	13
				0011	+6dB	12
				0100	+4.5dB	11
				0101	+3dB	10
				0110	+1.5dB	9
				0111	0dB	8
				1000	-1.5dB	7
				1001	-3dB	6
				1010	-4.5dB	5
				1011	-6dB	4
				1100	-6dB	3
				1101	-6dB	2
				1110	-6dB	1
				1111	Bypass (OFF)	
R13 (0Dh) Treble Control	6	TC	0	Treble Filter Characteristic 0 = High Cutoff (8kHz at 48kHz sampling) 1 = Low Cutoff (4kHz at 48kHz sampling)		
	3:0	TRBL [3:0]	1111 (Disabled)	Treble Intensity 0000 or 0001 = +9dB 0010 = +7.5dB … (1.5dB steps) 1011 to 1110 = -6dB 1111 = Disable		

Table 18 Graphic Equaliser

DIGITAL TO ANALOGUE CONVERTER (DAC)

After passing through the graphic equaliser filters, digital 'de-emphasis' can be applied to the audio data if necessary (e.g. when the data comes from a CD with pre-emphasis used in the recording). De-emphasis filtering is available for sample rates of 48kHz, 44.1kHz and 32kHz.

The WM8750JL also has a Soft Mute function, which gradually attenuates the volume of the digital signal to zero. When removed, the gain will return to the original setting. This function is enabled by default. To play back an audio signal, it must first be disabled by setting the DACMU bit to zero.

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION
R5 (05h) ADC and DAC Control	2:1	DEEMP [1:0]	00	De-emphasis Control 11 = 48kHz sample rate 10 = 44.1kHz sample rate 01 = 32kHz sample rate 00 = No De-emphasis
	3	DACMU	1	Digital Soft Mute 1 = mute 0 = no mute (signal active)

Table 19 DAC Control

The digital audio data is converted to oversampled bit streams in the on-chip, true 24-bit digital interpolation filters. The bitstream data enters two multi-bit, sigma-delta DACs, which convert them to high quality analogue audio signals. The multi-bit DAC architecture reduces high frequency noise and sensitivity to clock jitter. It also uses a Dynamic Element Matching technique for high linearity and low distortion.

In normal operation, the left and right channel digital audio data is converted to analogue in two separate DACs. However, it is also possible to disable one channel, so that the same signal (left or right) appears on both analogue output channels. Additionally, there is a mono-mix mode where the two audio channels are mixed together digitally and then converted to analogue using only one DAC, while the other DAC is switched off. The mono-mix signal can be selected to appear on both analogue output channels.

The DAC output defaults to non-inverted. Setting DACINV will invert the DAC output phase on both left and right channels.

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION
R23 (17h) Additional Control (1)	5:4	DMONOMIX [1:0]	00	DAC mono mix 00: stereo 01: mono ((L+R)/2) into DACL, '0' into DACR 10: mono ((L+R)/2) into DACR, '0' into DACL 11: mono ((L+R)/2) into DACL and DACR
	1	DACINV	0	DAC phase invert 0 : non-inverted 1 : inverted

Table 20 DAC Mono Mix and Phase Invert Select

OUTPUT MIXERS

The WM8750JL provides the option to mix the DAC output signal with analogue line-in signals from the LINPUT1/2/3, RINPUT1/2/3 pins or a mono differential input (LINPUT1 – RINPUT1) or (LINPUT2 – RINPUT2), selected by DS (see Table 5) . The level of the mixed-in signals can be controlled with PGAs (Programmable Gain Amplifiers).

The mono mixer is designed to allow a number of signal combinations to be mixed, including the possibility of mixing both the right and left channels together to produce a mono output. To prevent overloading of the mixer when full-scale DAC left and right signals are input, the mixer inputs from the DAC outputs each have a fixed gain of -6dB. The bypass path inputs to the mono mixer have variable gain as determined by R38/R39 bits [6:4].

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION
R34 (22h) Left Mixer (1)	2:0	LMIXSEL	000	Left Input Selection for Output Mix 000 = LINPUT1 001 = LINPUT2 010 = LINPUT3 011 = Left ADC Input (after PGA / MICBOOST) 100 = Differential input
R36 (24h) Right Mixer (1)	2:0	RMIXSEL	000	Right Input Selection for Output Mix 000 = RINPUT1 001 = RINPUT2 010 = RINPUT3 011 = Right ADC Input (after PGA / MICBOOST) 100 = Differential input

Table 21 Output Mixer Signal Selection

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION
R34 (22h) Left Mixer Control (1)	8	LD2LO	0	Left DAC to Left Mixer 0 = Disable (Mute) 1 = Enable Path
	7	LI2LO	0	LMIXSEL Signal to Left Mixer 0 = Disable (Mute) 1 = Enable Path
	6:4	LI2LOVOL [2:0]	101 (-9dB)	LMIXSEL Signal to Left Mixer Volume 000 = +6dB … (3dB steps) 111 = -15dB
R35 (23h) Left Mixer Control (2)	8	RD2LO	0	Right DAC to Left Mixer 0 = Disable (Mute) 1 = Enable Path
	7	RI2LO	0	RMIXSEL Signal to Left Mixer 0 = Disable (Mute) 1 = Enable Path
	6:4	RI2LOVOL [2:0]	101 (-9dB)	RMIXSEL Signal to Left Mixer Volume 000 = +6dB … (3dB steps) 111 = -15dB

Table 22 Left Output Mixer Control

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION
R36 (24h) Right Mixer Control (1)	8	LD2RO	0	Left DAC to Right Mixer 0 = Disable (Mute) 1 = Enable Path
	7	LI2RO	0	LMIXSEL Signal to Right Mixer 0 = Disable (Mute) 1 = Enable Path
	6:4	LI2ROVOL [2:0]	101 (-9dB)	LMIXSEL Signal to Right Mixer Volume 000 = +6dB … (3dB steps) 111 = -15dB
R37 (25h) Right Mixer Control (2)	8	RD2RO	0	Right DAC to Right Mixer 0 = Disable (Mute) 1 = Enable Path
	7	RI2RO	0	RMIXSEL Signal to Right Mixer 0 = Disable (Mute) 1 = Enable Path
	6:4	RI2ROVOL [2:0]	101 (-9dB)	RMIXSEL Signal to Right Mixer Volume 000 = +6dB … (3dB steps) 111 = -15dB

Table 23 Right Output Mixer Control

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION
R38 (26h) Mono Mixer Control (1)	8	LD2MO	0	Left DAC to Mono Mixer 0 = Disable (Mute) 1 = Enable Path
	7	LI2MO	0	LMIXSEL Signal to Mono Mixer 0 = Disable (Mute) 1 = Enable Path
	6:4	LI2MOVOL [2:0]	101 (-9dB)	LMIXSEL Signal to Mono Mixer Volume 000 = +6dB … (3dB steps) 111 = -15dB
R39 (27h) Mono Mixer Control (2)	8	RD2MO	0	Right DAC to Mono Mixer 0 = Disable (Mute) 1 = Enable Path
	7	RI2MO	0	RMIXSEL Signal to Mono Mixer 0 = Disable (Mute) 1 = Enable Path
	6:4	RI2MOVOL [2:0]	101 (-9dB)	RMIXSEL Signal to Mono Mixer Volume 000 = +6dB … (3dB steps) 111 = -15dB

Table 24 Mono Output Mixer Control

ANALOGUE OUTPUTS

LOUT1/ROUT1 OUTPUTS

The LOUT1 and ROUT1 pins can drive a 16Ω or 32Ω headphone or a line output (see Headphone Output and Line Output sections, respectively). The signal volume on LOUT1 and ROUT1 can be independently adjusted under software control by writing to LOUT1VOL and ROUT1VOL, respectively. Note that gains over 0dB may cause clipping if the signal is large. Any gain setting below 0101111 (minimum) mutes the output driver. The corresponding output pin remains at the same DC level (the reference voltage on the VREF pin), so that no click noise is produced when muting or un-muting.

A zero cross detect on the analogue output may also be enabled when changing the gain setting to minimize audible clicks and zipper noise as the gain updates. If zero cross is enabled a timeout is also available to update the gain if a zero cross does not occur. This function may be enabled by setting TOEN in register R23 (17h).

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION
R2 (02h) LOUT1 Volume	8	LO1VU	0	Left Volume Update 0 = Store LOUT1VOL in intermediate latch (no gain change) 1 = Update left and right channel gains (left = LOUT1VOL, right = intermediate latch)
	7	LO1ZC	0	Left zero cross enable 1 = Change gain on zero cross only 0 = Change gain immediately
	6:0	LOUT1VOL [6:0]	1111001 (0dB)	LOUT1 Volume 1111111 = +6dB … (80 steps) 0110000 = -67dB 0101111 to 0000000 = Analogue MUTE
R3 (03h) ROUT1 Volume	8	RO1VU	0	Right Volume Update 0 = Store ROUT1VOL in intermediate latch (no gain change) 1 = Update left and right channel gains (left = intermediate latch, right = ROUT1VOL)
	7	RO1ZC	0	Right zero cross enable 1 = Change gain on zero cross only 0 = Change gain immediately
	6:0	ROUT1VOL [6:0]	1111001	ROUT1 Volume 1111111 = +6dB … (80 steps) 0110000 = -67dB 0101111 to 0000000 = Analogue MUTE

Table 25 LOUT1/ROUT1 Volume Control

LOUT2/ROUT2 OUTPUTS

The LOUT2 and ROUT2 output pins are essentially similar to LOUT1 and ROUT1, but they are independently controlled and can also drive an 8Ω mono speaker (see Speaker Output section). For speaker drive, the ROUT2 signal must be inverted (ROUT2INV = 1), so that the left and right channel are mixed to mono in the speaker [L–(-R) = L+R].

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION
R40 (28h) LOUT2 Volume	6:0	LOUT2VOL [6:0]	1111001 (0dB)	LOUT2 Volume 1111111 = +6dB … (80 steps) 0110000 = -67dB 0101111 to 0000000 = Analogue MUTE
	7	LO2ZC	0	Left zero cross enable 1 = Change gain on zero cross only 0 = Change gain immediately
	8	LO2VU	0	Left Volume Update 0 = Store LOUT2VOL in intermediate latch (no gain change) 1 = Update left and right channel gains (left = LOUT2VOL, right = intermediate latch)
R41 (29h) ROUT2 Volume	6:0	ROUT2VOL [6:0]	1111001 (0dB)	ROUT2 Volume 1111111 = +6dB … (80 steps) 0110000 = -67dB 0101111 to 0000000 = Analogue MUTE
	7	RO2ZC	0	Right zero cross enable 1 = Change gain on zero cross only 0 = Change gain immediately
	8	RO2VU	0	Right Volume Update 0 = Store ROUT1VOL in intermediate latch (no gain change) 1 = Update left and right channel gains (left = ROUT1VOL, right = intermediate latch)
R24 (18h) Additional Control (2)	4	ROUT2INV	0	ROUT2 Invert 0 = No Inversion (0° phase shift) 1 = Signal inverted (180° phase shift)

Table 26 LOUT2/ROUT2 Volume Control

MONO OUTPUT

The MONOOUT pin can drive a mono line output. The signal volume on MONOOUT can be adjusted under software control by writing to MONOOUTVOL.

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION
R42 (2Ah) MONOOUT Volume	6:0	MONOOUT VOL [6:0]	1111001 (0dB)	MONOOUT Volume 1111111 = +6dB … (80 steps) 0110000 = -67dB 0101111 to 0000000 = Analogue MUTE
	7	MOZC	0	MONOOUT zero cross enable 1 = Change gain on zero cross only 0 = Change gain immediately

Table 27 MONOOUT Volume Control

OUT3 OUTPUT

The OUT3 pin can drive a 16Ω or 32Ω headphone or a line output or be used as a DC reference for a headphone output (see Headphone Output section). It can be selected to either drive out an inverted ROUT1 or inverted MONOOUT for e.g. an earpiece drive between OUT3 and LOUT1 or differential output between OUT3 and MONOOUT. OUT3 can also drive an un-inverted ROUT1 signal, which originates at the right mixer output before the output PGA.

OUT3SW selects the mode of operation required.

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION
R24 (18h) Additional Control (2)	8:7	OUT3SW [1:0]	00	OUT3 select 00 : VREF 01 : ROUT1 signal (volume controlled by ROUT1VOL) 10 : MONOOUT 11 : right mixer output (no volume control through ROUT1VOL)

Table 28 OUT3 Select

ENABLING THE OUTPUTS

Each analogue output of the WM8750JL can be separately enabled or disabled. The analogue mixer associated with each output is powered on or off along with the output pin. All outputs are disabled by default. To save power, unused outputs should remain disabled.

Outputs can be enabled at any time, except when VREF is disabled (VR=0), as this may cause pop noise (see "Power Management" and "Applications Information" sections)

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION
R26 (1Ah) Power Management (2)	6	LOUT1	0	LOUT1 Enable
	5	ROUT1	0	ROUT1 Enable
	4	LOUT2	0	LOUT2 Enable
	3	ROUT2	0	ROUT2 Enable
	2	MONO	0	MONOOUT Enable
	1	OUT3	0	OUT3 Enable
Note: All "Enable" bits are 1 = ON, 0 = OFF				

Table 29 Analogue Output Control

Whenever an analogue output is disabled, it remains connected to VREF (pin 20) through a resistor. This helps to prevent pop noise when the output is re-enabled. The resistance between VREF and each output can be controlled using the VROI bit in register 27. The default is low (1.5kΩ), so that any capacitors on the outputs can charge up quickly at start-up. If a high impedance is desired for disabled outputs, VROI can then be set to 1, increasing the resistance to about 40kΩ.

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION
R27 (1Bh) Additional (1)	6	VROI	0	VREF to analogue output resistance 0: 1.5 kΩ 1: 40 kΩ

Table 30 Disabled Outputs to VREF Resistance

HEADPHONE SWITCH

The RINPUT3/HPDETECT pin can be used as a headphone switch control input to automatically disable the speaker output and enable the headphone output e.g. when a headphone is plugged into a jack socket. In this mode, enabled by setting HPSWEN, HPDETECT switches between headphone and speaker outputs (e.g. when the pin is connected to a mechanical switch in the headphone socket to detect plug-in). The HPSWPOL bit reverses the pin's polarity. Note that the LOUT1, ROUT1, LOUT2 and ROUT2 bits in register 26 must also be set for headphone and speaker output (see Table 31 and Table 32).

Note:

When RINPUT3/HPDETECT is used as the HPDETECT input, the thresholds become CMOS levels (0.3 AVDD / 0.7 AVDD).

HPSWEN	HPSWPOL	HPDETECT (PIN23)	L/ROUT1 (REG. 26)	L/ROUT2 (REG. 26)	HEADPHONE ENABLED	SPEAKER ENABLED
0	X	X	0	0	no	no
0	X	X	0	1	no	yes
0	X	X	1	0	yes	no
0	X	X	1	1	yes	yes
1	0	0	X	0	no	no
1	0	0	X	1	no	yes
1	0	1	0	X	no	no
1	0	1	1	X	yes	no
1	1	0	0	X	no	no
1	1	0	1	X	yes	no
1	1	1	X	0	no	no
1	1	1	X	1	no	yes

Table 31 Headphone Switch Operation

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION
R24 (18h) Additional Control (2)	6	HPSWEN	0	Headphone Switch Enable 0 : Headphone switch disabled 1 : Headphone switch enabled
	5	HPSWPOL	0	Headphone Switch Polarity 0 : HPDETECT high = headphone 1 : HPDETECT high = speaker

Table 32 Headphone Switch

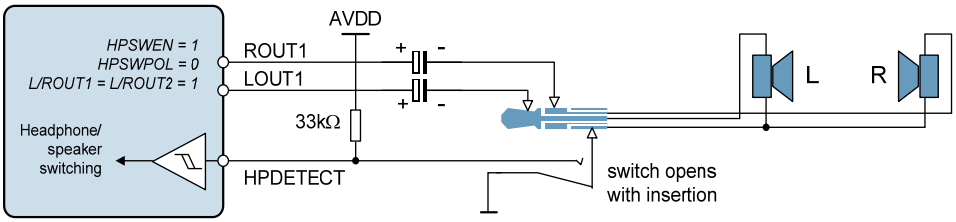


Figure 11 Example Headset Detection Circuit Using Normally-Open Switch

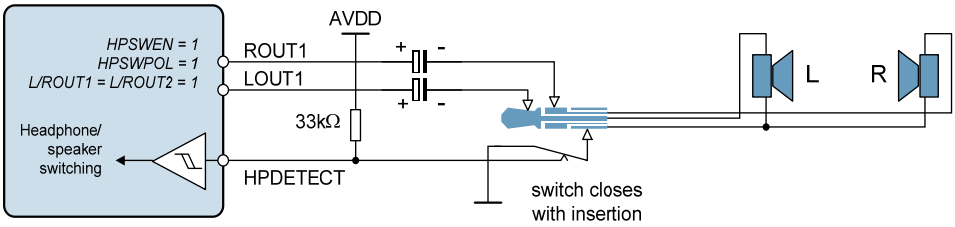


Figure 12 Example Headset Detection Circuit Using Normally-Closed Switch

THERMAL SHUTDOWN

The speaker and headphone outputs can drive very large currents. To protect the WM8750JL from overheating a thermal shutdown circuit is included. If the device temperature reaches approximately 150°C and the thermal shutdown circuit is enabled (TSDEN = 1) then the speaker and headphone amplifiers (outputs OUT1L/R, OUT2L/R and OUT3) will be disabled.

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION
R23 (17h) Additional Control (1)	8	TSDEN	0	Thermal Shutdown Enable 0 : thermal shutdown disabled 1 : thermal shutdown enabled

Table 33 Thermal Shutdown

HEADPHONE OUTPUT

Analogue outputs LOUT1/ROUT1, LOUT2/ROUT2, and OUT3, can drive a 16Ω or 32Ω headphone load, either through DC blocking capacitors, or DC coupled without any capacitor.

Headphone Output using DC blocking capacitors

DC Coupled Headphone Output (OUT3SW = 00)

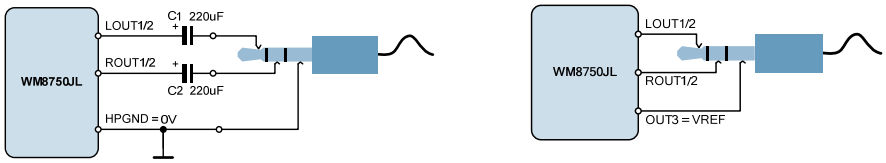


Figure 13 Recommended Headphone Output Configurations

When DC blocking capacitors are used, then their capacitance and the load resistance together determine the lower cut-off frequency, f_c. Increasing the capacitance lowers f_c, improving the bass response. Smaller capacitance values will diminish the bass response. Assuming a 16 Ohm load and C1, C2 = 220µF:

$f_c = 1 / 2\pi R_L C_1 = 1 / (2\pi \times 16\Omega \times 220\mu F) = 45$ Hz

In the DC coupled configuration, the headphone "ground" is connected to the OUT3 pin, which must be enabled by setting OUT3 = 1 and OUT3SW = 00. As the OUT3 pin produces a DC voltage of AVDD/2 (=VREF), there is no DC offset between LOUT1/ROUT1 and OUT3, and therefore no DC blocking capacitors are required. This saves space and material cost in portable applications.

It is recommended to connect the DC coupled headphone outputs only to headphones, and not to the line input of another device. Although the built-in thermal shutdown circuit will prevent any damage to the headphone outputs if overloaded, such a connection may be noisy, and may not function properly if the other device is grounded.

SPEAKER OUTPUT

LOUT2 and ROUT2 can differentially drive a mono 8Ω speaker as shown below.

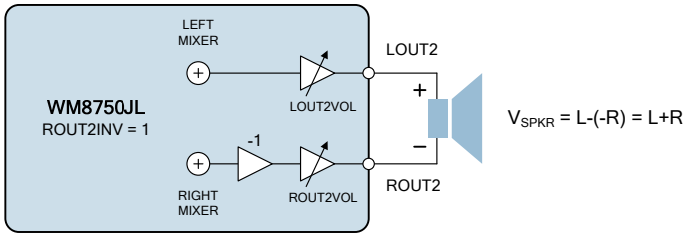


Figure 14 Speaker Output Connection

The right channel is inverted by setting the ROUT2INV bit, so that the signal across the loudspeaker is the sum of left and right channels.

LINE OUTPUT

The analogue outputs, LOUT1/ROUT1 and LOUT2/ROUT2, can be used as line outputs. Additionally, OUT3 and MONOOUT can be used as a stereo line-out by setting OUT3SW=11 (reg. 24) and ensuring the contents of registers 38 and 39 (mono-out mix) are the same as reg. 34 and 35 (left out mix). Recommended external components are shown below.

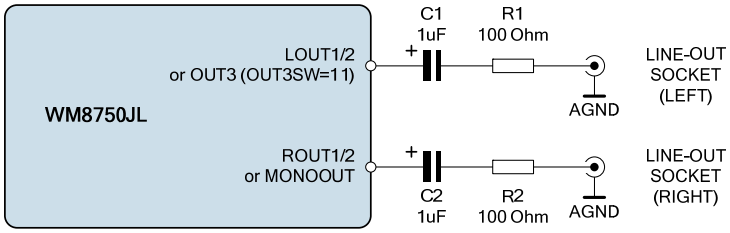


Figure 15 Recommended Circuit for Line Output

The DC blocking capacitors and the load resistance together determine the lower cut-off frequency, f_c. Assuming a 10 kOhm load and C1, C2 = 1μF:

$f_c = 1 / 2\pi (R_L+R_1) C_1 = 1 / (2\pi \times 10.1k\Omega \times 1\mu F) = 16$ Hz

Increasing the capacitance lowers f_c, improving the bass response. Smaller values of C1 and C2 will diminish the bass response. The function of R1 and R2 is to protect the line outputs from damage when used improperly.

DIGITAL AUDIO INTERFACE

The digital audio interface is used for inputting DAC data into the WM8750JL and outputting ADC data from it. It uses five pins:

- ADCDAT: ADC data output
- ADCLRC: ADC data alignment clock
- DACDAT: DAC data input
- DACLRC: DAC data alignment clock
- BCLK: Bit clock, for synchronisation

The clock signals BCLK, ADCLRC and DACLRC can be outputs when the WM8750JL operates as a master, or inputs when it is a slave (see Master and Slave Mode Operation, below).

Four different audio data formats are supported:

- Left justified
- I^2S
- DSP mode

All four of these modes are MSB first. They are described in Audio Data Formats, below. Refer to the Electrical Characteristic section for timing information.

MASTER AND SLAVE MODE OPERATION

The WM8750JL can be configured as either a master or slave mode device. As a master device the WM8750JL generates BCLK, ADCLRC and DACLRC and thus controls sequencing of the data transfer on ADCDAT and DACDAT. In slave mode, the WM8750JL responds with data to clocks it receives over the digital audio interface. The mode can be selected by writing to the MS bit (see Table 23). Master and slave modes are illustrated below.

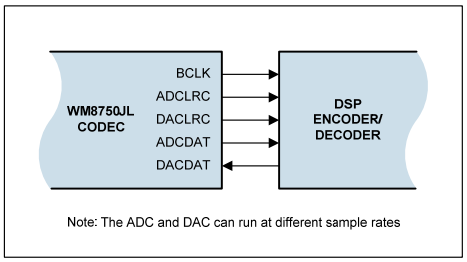


Figure 16 Master Mode

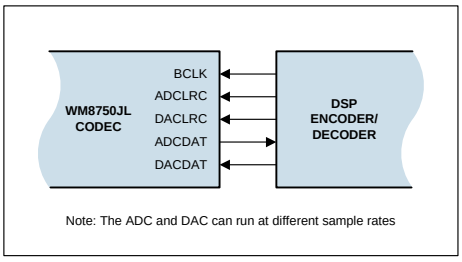


Figure 17 Slave Mode

Note: For optimum ADC audio performance in slave mode, the BCLK input signal should be configured to transition at the same time as the falling edge of MCLK.

The ADCDAT digital data output is buffered inside the CODEC using a digital logic buffering block. However, the ADCDAT buffering block is not reset by the power-on reset circuit and hence the ADCDAT pin stage (logic high or logic low) is undefined at power up until data is clocked out from the ADC. Implementation of either of these workarounds will ensure correct operation:

- Ensure that any external connection to the ADCDAT pin is made with the understanding that ADCDAT pin may be driven high or low by the CODEC until ADC data is clocked out.
- Tri-state the ADCDACDAT output pin by setting the TRI bit in R24 (Additional Control 2 register). Setting this bit will also configure ADCLRC, DACLRC and BCLK as inputs and (as the CODEC has no internal pull-up/down resistors) the input voltage level must be set on these pins by an external source (either the device connected to the digital audio interface or pull-up/down resistors) to prevent excess current consumption.

AUDIO DATA FORMATS

In I^2S mode, the MSB is available on the second rising edge of BCLK following a LRCLK transition. The other bits up to the LSB are then transmitted in order. Depending on word length, BCLK frequency and sample rate, there may be unused BCLK cycles between the LSB of one sample and the MSB of the next.

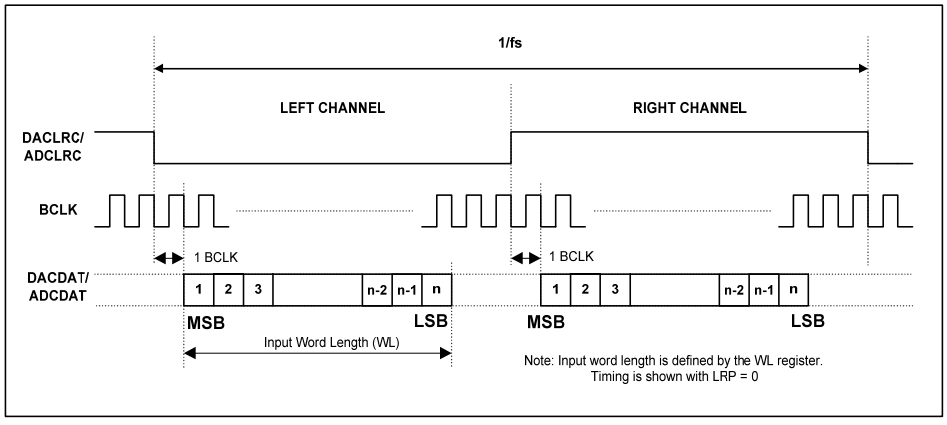


Figure 18 I^2S Audio Interface Format (assuming n-bit word length)

In Left Justified mode, the MSB is available on the first rising edge of BCLK following a LRCLK transition. The other bits up to the LSB are then transmitted in order. Depending on word length, BCLK frequency and sample rate, there may be unused BCLK cycles before each LRCLK transition.

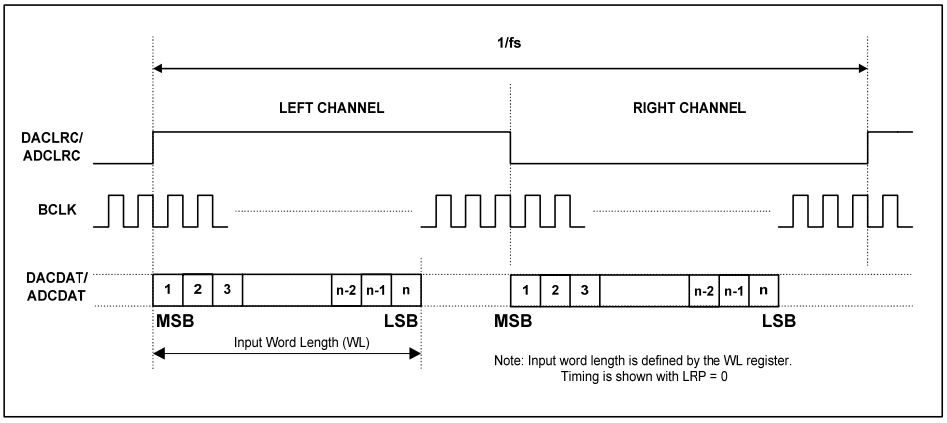


Figure 19 Left Justified Audio Interface (assuming n-bit word length)

In DSP/PCM mode, the left channel MSB is available on either the 1st (mode B) or 2nd (mode A) rising edge of BCLK (selectable by LRP) following a rising edge of LRC. Right channel data immediately follows left channel data. Depending on word length, BCLK frequency and sample rate, there may be unused BCLK cycles between the LSB of the right channel data and the next sample.

In device master mode, the LRC output will resemble the frame pulse shown in Figure 20 and Figure 21. In device slave mode, Figure 22 and Figure 23, it is possible to use any length of frame pulse less than 1/fs, providing the falling edge of the frame pulse occurs greater than one BCLK period before the rising edge of the next frame pulse.

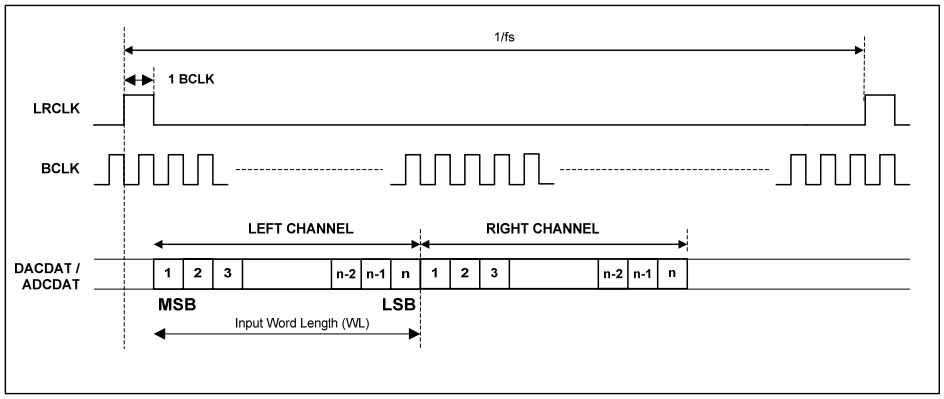


Figure 20 DSP/PCM Mode Audio Interface (mode A, LRP=0, Master)

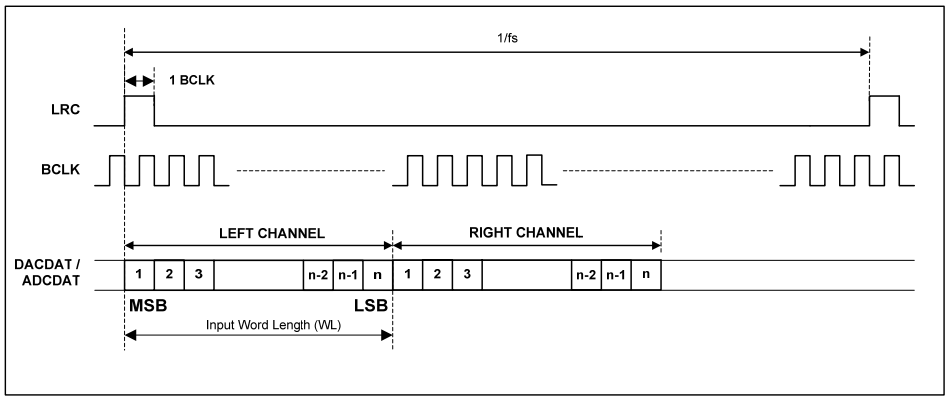


Figure 21 DSP/PCM Mode Audio Interface (mode B, LRP=1, Master)

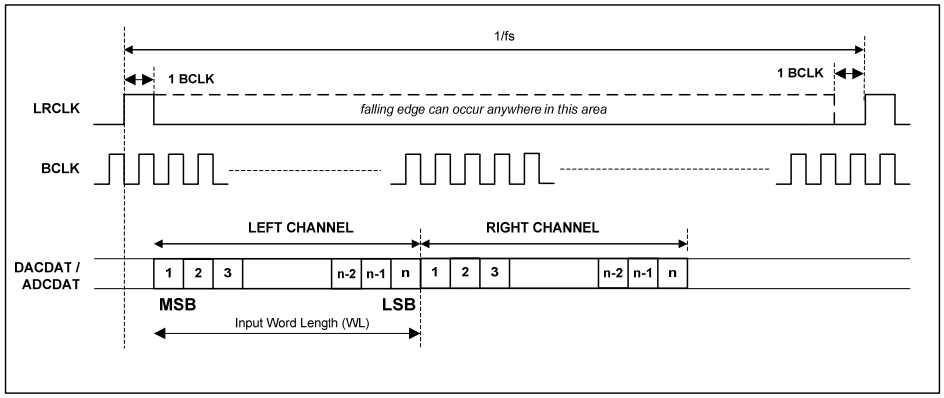


Figure 22 DSP/PCM Mode Audio Interface (mode A, LRP=0, Slave)

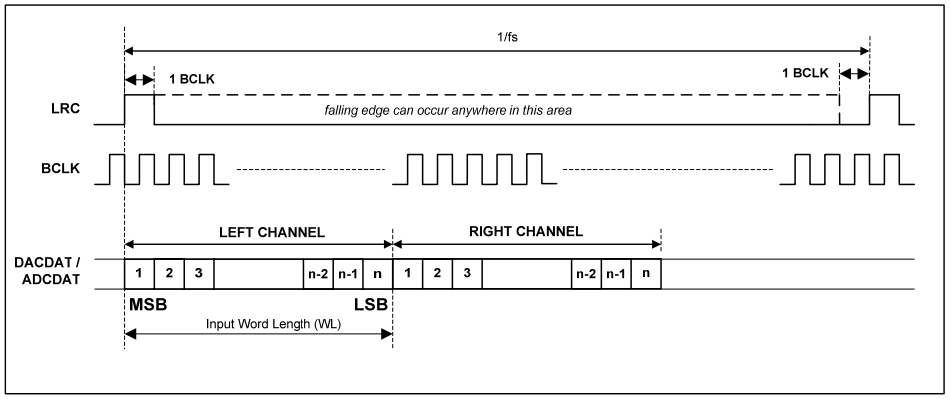


Figure 23 DSP/PCM Mode Audio Interface (mode B, LRP=0, Slave)

AUDIO INTERFACE CONTROL

The register bits controlling audio format, word length and master / slave mode are summarised in Table 34. MS selects audio interface operation in master or slave mode. In Master mode BCLK, ADCLRC and DACLRC are outputs. The frequency of ADCLRC and DACLRC is set by the sample rate control bits SR[4:0] and USB. In Slave mode BCLK, ADCLRC and DACLRC are inputs.

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION
R7 (07h) Digital Audio Interface Format	7	BCLKINV	0	BCLK invert bit (for master and slave modes) 0 = BCLK not inverted 1 = BCLK inverted
	6	MS	0	Master / Slave Mode Control 1 = Enable Master Mode 0 = Enable Slave Mode
	5	LRSWAP	0	Left/Right channel swap 1 = swap left and right DAC data in audio interface 0 = output left and right data as normal
	4	LRP	0	right, left and i2s modes – LRCLK polarity 1 = invert LRCLK polarity 0 = normal LRCLK polarity
				DSP Mode – mode A/B select 1 = MSB is available on 1st BCLK rising edge after LRC rising edge (mode B) 0 = MSB is available on 2nd BCLK rising edge after LRC rising edge (mode A)
	3:2	WL[1:0]	10	Audio Data Word Length 11 = 32 bits (see Note) 10 = 24 bits 01 = 20 bits 00 = 16 bits
	1:0	FORMAT[1:0]	10	Audio Data Format Select 11 = DSP Mode 10 = I^2S Format 01 = Left justified 00 = Reserved

Table 34 Audio Data Format Control

AUDIO INTERFACE OUTPUT TRISTATE

Register bit TRI, register 24(18h) bit[3] can be used to tristate the ADCDAT pin and switch ADCLRC, DACLRC and BCLK to inputs. In Slave mode (MASTER=0) ADCLRC, DACLRC and BCLK are by default configured as inputs and only ADCDAT will be tri-stated, (see Table 35).

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION
R24(18h) Additional Control (2)	3	TRI	0	Tristates ADCDAT and switches ADCLRC, DACLRC and BCLK to inputs. 0 = ADCDAT is an output, ADCLRC, DACLRC and BCLK are inputs (slave mode) or outputs (master mode) 1 = ADCDAT is tristated, ADCLRC, DACLRC and BCLK are inputs

Table 35 Tri-stating the Audio Interface

MASTER MODE ADCLRC AND DACLRC ENABLE

In Master mode, by default ADCLRC is disabled when the ADC is disabled and DACLRC is disabled when the DAC is disabled. Register bit LRCM, register 24(18h) bit[2] changes the control so that the ADCLRC and DACLRC are disabled only when ADC and DAC are disabled. This enables the user to use e.g. ADCLRC for both ADC and DAC LRCLK and disable the ADC when DAC only operation is required, (see Table 36).

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION
R24(18h) Additional Control (2)	2	LRCM	0	Selects disable mode for ADCLRC and DACLRC 0 = ADCLRC disabled when ADC (Left and Right) disabled, DACLRC disabled when DAC (Left and Right) disabled. 1 = ADCLRC and DACLRC disabled only when ADC (Left and Right) and DAC (Left and Right) are disabled.

Table 36 ADCLRC/DACLRC Enable

BIT CLOCK MODE

The default master mode bit clock generator produces a bit clock frequency based on the sample rate and input MCLK frequency as shown in Table 40. When enabled by setting the appropriate BCM[1:0] bits, the bit clock mode (BCM) function overrides the default master mode bit clock generator to produce the bit clock frequency shown in the table below:

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION
R8 (08h) Clocking and Sample Rate Control	8:7	BCM[1:0]	00	BCLK Frequency 00 = BCM function disabled 01 = MCLK/4 10 = MCLK/8 11 = MCLK/16

Table 37 Master Mode BCLK Frequency Control

The BCM mode bit clock generator produces 16 or 24 bit clock cycles per sample. The number of bit clock cycles per sample in this mode is determined by the word length bits (WL[1:0]) in the Digital Audio Interface Format register (R7). When these bits are set to 00, there will be 16 bit clock cycles per sample. When these bits are set to 01, 10 or 11, there will be 24 bit clock cycles per sample. Please refer to Figure 24.

The BCM generator uses the ADCLRC signal, hence the ADCLRC signal must be enabled when using bit clock mode. To enable the ADCLRC signal, either the ADC must be powered up or, if the ADC is not in use, the LRCM bit must be set to enable both the ADCLRC and DACLRC signals when either the ADC or the DAC is enabled.

When the BCM function is enabled, the following restrictions apply:

1. The bit clock invert (BCLKINV) function is not available.

2. The DAC and ADC must be operated at the same sample rate.

3. DSP late digital audio interface mode is not available and must not be enabled.

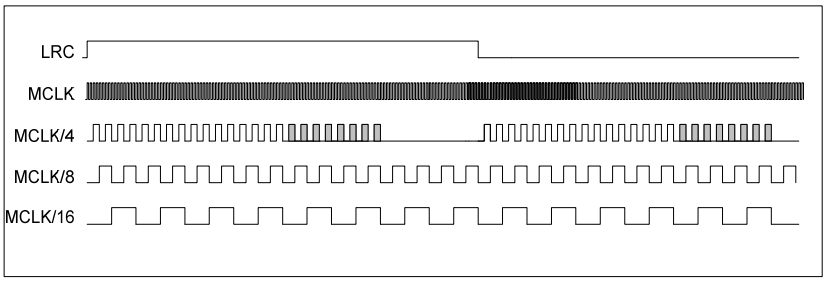


Figure 24 Bit Clock Mode

Note: The shaded bit clock cycles are present only when 24-bit mode is selected. Please refer to the "Bit Clock Mode" description for details.

CLOCK OUTPUT

By default ADCLRC (pin 9) is the ADC word clock input/output. Under the control of ADCLRM[1:0], register 27(1Bh) bits [8:7] the ADCLRC pin may be configured as a clock output. If ADCLRM is 01, 10 or 11 then ADCLRC pin is always an output even in slave mode or when TRI = '1', (see Table 38). The ADC then uses the DACLRC pin as its LRCLK in both master and slave modes.

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION
R27(1Bh) Additional Control (3)	[8:7]	ADCLRM [1:0]	00	Configures ADCLRC pin 00 = ADCLRC is ADC word clock input (slave mode) or ADCLRC output (master mode) 01 = ADCLRC pin is MCLK output 10 = ADCLRC pin is MCLK / 5.5 output 11 = ADCLRC pin is MCLK / 6 output

Table 38 ADCLRC Clock Output

CLOCKING AND SAMPLE RATES

The WM8750JL supports a wide range of master clock frequencies on the MCLK pin, and can generate many commonly used audio sample rates directly from the master clock. The ADC and DAC do not need to run at the same sample rate; several different combinations are possible.

There are two clocking modes:

- 'Normal' mode supports master clocks of $128f_s$, $192f_s$, $256f_s$, $384f_s$, and their multiples (Note: f_s refers to the ADC or DAC sample rate, whichever is faster)
- USB mode supports 12MHz or 24MHz master clocks. This mode is intended for use in systems with a USB interface, and eliminates the need for an external PLL to generate another clock frequency for the audio codec.

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION
R8 (08h) Clocking and Sample Rate Control	6	CLKDIV2	0	Master Clock Divide by 2 1 = MCLK is divided by 2 0 = MCLK is not divided
	5:1	SR [4:0]	00000	Sample Rate Control
	0	USB	0	Clocking Mode Select 1 = USB Mode 0 = 'Normal' Mode

Table 39 Clocking and Sample Rate Control

The clocking of the WM8750JL is controlled using the CLKDIV2, USB, and SR control bits. Setting the CLKDIV2 bit divides MCLK by two internally. The USB bit selects between 'Normal' and USB mode. Each value of SR[4:0] selects one combination of MCLK division ratios and hence one combination of sample rates (see next page). Since all sample rates are generated by dividing MCLK, their accuracy depends on the accuracy of MCLK. If MCLK changes, the sample rates change proportionately.

Note that some sample rates (e.g. 44.1kHz in USB mode) are approximated, i.e. they differ from their target value by a very small amount. This is not audible, as the maximum deviation is only 0.27% (8.0214kHz instead of 8kHz in USB mode). By comparison, a half-tone step corresponds to a 5.9% change in pitch.

The SR[4:0] bits must be set to configure the appropriate ADC and DAC sample rates in both master and slave mode.

Note: When the ADC is configured at a sample rate of 88.2, 88.235 or 96kHZ (SR[4:0]), the ADC right channel data output will be delayed by one sample relative to the left channel data.

MCLK CLKDIV2=0	MCLK CLKDIV2=1	ADC SAMPLE RATE (ADCLRC)	DAC SAMPLE RATE (DACLRC)	USB	SR [4:0]	FILTER TYPE	BCLK (MS=1)
'Normal' Clock Mode ('*' indicates backward compatibility with WM8731)							
12.288 MHz	24.576 MHz	8 kHz (MCLK/1536)	8 kHz (MCLK/1536)	0	00110 *	1	MCLK/4
		8 kHz (MCLK/1536)	48 kHz (MCLK/256)	0	00100 *	1	MCLK/4
		12 kHz (MCLK/1024)	12 kHz (MCLK/1024)	0	01000	1	MCLK/4
		16 kHz (MCLK/768)	16 kHz (MCLK/768)	0	01010	1	MCLK/4
		24 kHz (MCLK/512)	24 kHz (MCLK/512)	0	11100	1	MCLK/4
		32 kHz (MCLK/384)	32 kHz (MCLK/384)	0	01100 *	1	MCLK/4
		48 kHz (MCLK/256)	8 kHz (MCLK/1536)	0	00010 *	1	MCLK/4
		48 kHz (MCLK/256)	48 kHz (MCLK/256)	0	00000 *	1	MCLK/4
		96 kHz (MCLK/128)	96 kHz (MCLK/128)	0	01110 *	3	MCLK/2
11.2896MHz	22.5792MHz	8.0182 kHz (MCLK/1408)	8.0182 kHz (MCLK/1408)	0	10110 *	1	MCLK/4
		8.0182 kHz (MCLK/1408)	44.1 kHz (MCLK/256)	0	10100 *	1	MCLK/4
		11.025 kHz (MCLK/1024)	11.025 kHz (MCLK/1024)	0	11000	1	MCLK/4
		22.05 kHz (MCLK/512)	22.05 kHz (MCLK/512)	0	11010	1	MCLK/4
		44.1 kHz (MCLK/256)	8.0182 kHz (MCLK/1408)	0	10010 *	1	MCLK/4
		44.1 kHz (MCLK/256)	44.1 kHz (MCLK/256)	0	10000 *	1	MCLK/4
		88.2 kHz (MCLK/128)	88.2 kHz (MCLK/128)	0	11110 *	3	MCLK/2
18.432MHz	36.864MHz	8 kHz (MCLK/2304)	8 kHz (MCLK/2304)	0	00111 *	1	MCLK/6
		8 kHz (MCLK/2304)	48 kHz (MCLK/384)	0	00101 *	1	MCLK/6
		12 kHz (MCLK/1536)	12 kHz (MCLK/1536)	0	01001	1	MCLK/6
		16kHz (MCLK/1152)	16 kHz (MCLK/1152)	0	01011	1	MCLK/6
		24kHz (MCLK/768)	24 kHz (MCLK/768)	0	11101	1	MCLK/6
		32 kHz (MCLK/576)	32 kHz (MCLK/576)	0	01101 *	1	MCLK/6
		48 kHz (MCLK/384)	48 kHz (MCLK/384)	0	00001 *	1	MCLK/6
		48 kHz (MCLK/384)	8 kHz (MCLK/2304)	0	00011 *	1	MCLK/6
		96 kHz (MCLK/192)	96 kHz (MCLK/192)	0	01111 *	3	MCLK/3
16.9344MHz	33.8688MHz	8.0182 kHz (MCLK/2112)	8.0182 kHz (MCLK/2112)	0	10111 *	1	MCLK/6
		8.0182 kHz (MCLK/2112)	44.1 kHz (MCLK/384)	0	10101 *	1	MCLK/6
		11.025 kHz (MCLK/1536)	11.025 kHz (MCLK/1536)	0	11001	1	MCLK/6
		22.05 kHz (MCLK/768)	22.05 kHz (MCLK/768)	0	11011	1	MCLK/6
		44.1 kHz (MCLK/384)	8.0182 kHz (MCLK/2112)	0	10011 *	1	MCLK/6
		44.1 kHz (MCLK/384)	44.1 kHz (MCLK/384)	0	10001 *	1	MCLK/6
		88.2 kHz (MCLK/192)	88.2 kHz (MCLK/192)	0	11111 *	3	MCLK/3
USB Mode ('*' indicates backward compatibility with WM8731)							
12.000MHz	24.000MHz	8 kHz (MCLK/1500)	8 kHz (MCLK/1500)	1	00110 *	0	MCLK
		8 kHz (MCLK/1500)	48 kHz (MCLK/250)	1	00100 *	0	MCLK
		8.0214 kHz (MCLK/1496)	8.0214kHz (MCLK/1496)	1	10111 *	1	MCLK
		8.0214 kHz (MCLK/1496)	44.118 kHz (MCLK/272)	1	10101 *	1	MCLK
		11.0259 kHz (MCLK/1088)	11.0259kHz (MCLK/1088)	1	11001	1	MCLK
		12 kHz (MCLK/1000)	12 kHz (MCLK/1000)	1	01000	0	MCLK
		16kHz (MCLK/750)	16kHz (MCLK/750)	1	01010	0	MCLK
		22.0588kHz (MCLK/544)	22.0588kHz (MCLK/544)	1	11011	1	MCLK
		24kHz (MCLK/500)	24kHz (MCLK/500)	1	11100	0	MCLK
		32 kHz (MCLK/375)	32 kHz (MCLK/375)	1	01100 *	0	MCLK
		44.118 kHz (MCLK/272)	8.0214kHz (MCLK/1496)	1	10011 *	1	MCLK
		44.118 kHz (MCLK/272)	44.118 kHz (MCLK/272)	1	10001 *	1	MCLK
		48 kHz (MCLK/250)	8 kHz (MCLK/1500)	1	00010 *	0	MCLK
		48 kHz (MCLK/250)	48 kHz (MCLK/250)	1	00000 *	0	MCLK
		88.235kHz (MCLK/136)	88.235kHz (MCLK/136)	1	11111 *	3	MCLK
		96 kHz (MCLK/125)	96 kHz (MCLK/125)	1	01110 *	2	MCLK

Table 40 Master Clock and Sample Rates

CONTROL INTERFACE

SELECTION OF CONTROL MODE

The WM8750JL is controlled by writing to registers through a serial control interface. A control word consists of 16 bits. The first 7 bits (B15 to B9) are address bits that select which control register is accessed. The remaining 9 bits (B8 to B0) are data bits, corresponding to the 9 bits in each control register. The control interface can operate as either a 3-wire or 2-wire MPU interface. The MODE pin selects the interface format.

MODE	INTERFACE FORMAT
Low	2 wire
High	3 wire

Table 41 Control Interface Mode Selection

3-WIRE SERIAL CONTROL MODE

In 3-wire mode, every rising edge of SCLK clocks in one data bit from the SDIN pin. A rising edge on CSB latches in a complete control word consisting of the last 16 bits.

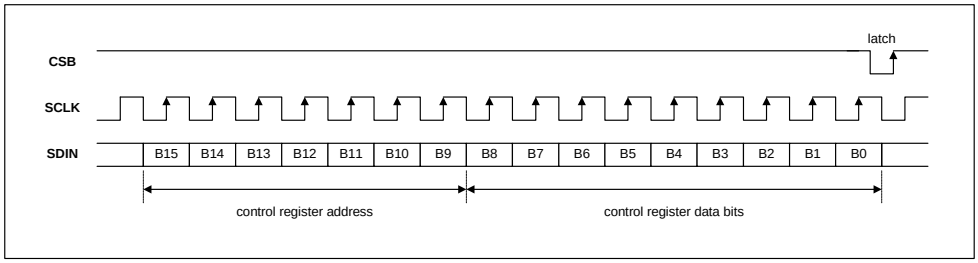


Figure 25 3-Wire Serial Control Interface

2-WIRE SERIAL CONTROL MODE

The WM8750JL supports software control via a 2-wire serial bus. Many devices can be controlled by the same bus, and each device has a unique 7-bit address (this is not the same as the 7-bit address of each register in the WM8750JL).

The WM8750JL operates as a slave device only. The controller indicates the start of data transfer with a high to low transition on SDIN while SCLK remains high. This indicates that a device address and data will follow. All devices on the 2-wire bus respond to the start condition and shift in the next eight bits on SDIN (7-bit address + Read/Write bit, MSB first). If the device address received matches the address of the WM8750JL and the R/W bit is '0', indicating a write, then the WM8750JL responds by pulling SDIN low on the next clock pulse (ACK). If the address is not recognised or the R/W bit is '1', the WM8750JL returns to the idle condition and wait for a new start condition and valid address.

Once the WM8750JL has acknowledged a correct address, the controller sends the first byte of control data (B15 to B8, i.e. the WM8750JL register address plus the first bit of register data). The WM8750JL then acknowledges the first data byte by pulling SDIN low for one clock pulse. The controller then sends the second byte of control data (B7 to B0, i.e. the remaining 8 bits of register data), and the WM8750JL acknowledges again by pulling SDIN low.

The transfer of data is complete when there is a low to high transition on SDIN while SCLK is high. After receiving a complete address and data sequence the WM8750JL returns to the idle state and waits for another start condition. If a start or stop condition is detected out of sequence at any point during data transfer (i.e. SDIN changes while SCLK is high), the device jumps to the idle condition.

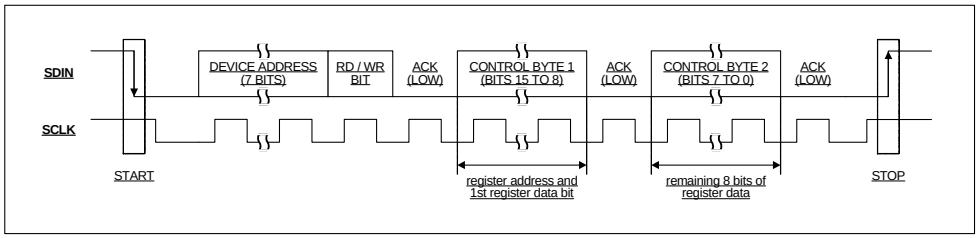


Figure 26 2-Wire Serial Control Interface

The WM8750JL has two possible device addresses, which can be selected using the CSB pin.

CSB STATE	DEVICE ADDRESS
Low	0011010 (0 x 34h)
High	0011011 (0 x 36h)

Table 42 2-Wire MPU Interface Address Selection

POWER SUPPLIES

The WM8750JL can use up to four separate power supplies:

- AVDD / AGND: Analogue supply, powers all analogue functions except the headphone drivers. AVDD can range from 1.8V to 3.6V and has the most significant impact on overall power consumption (except for power consumed in the headphone). A large AVDD slightly improves audio quality.
- HPVDD / HPGND: Headphone supply, powers the headphone drivers. HPVDD is normally tied to AVDD, but it requires separate layout and decoupling capacitors to curb harmonic distortion. If HPVDD is lower than AVDD, the output signal may be clipped.
- DCVDD: Digital core supply, powers all digital functions except the audio and control interfaces. DCVDD can range from 1.42V to 3.6V, and has no effect on audio quality. The return path for DCVDD is DGND, which is shared with DBVDD.
- DBVDD: Digital buffer supply, powers the audio and control interface buffers. This makes it possible to run the digital core at very low voltages, saving power, while interfacing to other digital devices using a higher voltage. DBVDD draws much less power than DCVDD, and has no effect on audio quality. DBVDD can range from 1.8V to 3.6V. The return path for DBVDD is DGND, which is shared with DCVDD.

It is possible to use the same supply voltage on all four. However, digital and analogue supplies should be routed and decoupled separately to keep digital switching noise out of the analogue signal paths.

POWER MANAGEMENT

The WM8750JL has two control registers that allow users to select which functions are active. For minimum power consumption, unused functions should be disabled. To avoid any pop or click noise, it is important to enable or disable functions in the correct order (see Applications Information). VMIDSEL is the enable for the Vmid reference, which defaults to disabled and can be enabled as a 50kΩ potential divider or, for low power maintenance of Vref when all other blocks are disabled, as a 500kΩ potential divider.

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION
R25 (19h) Power Management (1)	8:7	VMIDSEL	00	Vmid divider enable and select 00 – Vmid disabled (for OFF mode) 01 – 50kΩ divider enabled (for playback/record) 10 – 500kΩ divider enabled (for low-power standby) 11 – 5kΩ divider enabled (for fast start-up)
	6	VREF	0	VREF (necessary for all other functions) 0 = Power down 1 = Power up
	5	AINL	0	Analogue in PGA Left 0 = Power down 1 = Power up
	4	AINR	0	Analogue in PGA Right 0 = Power down 1 = Power up
	3	ADCL	0	ADC Left 0 = Power down 1 = Power up
	2	ADCR	0	ADC Right 0 = Power down 1 = Power up
	1	MICB	0	MICBIAS 0 = Power down 1 = Power up
R26 (1Ah) Power Management (2)	8	DACL	0	DAC Left 0 = Power down 1 = Power up
	7	DACR	0	DAC Right 0 = Power down 1 = Power up
	6	LOUT1	0	LOUT1 Output Buffer* 0 = Power down 1 = Power up
	5	ROUT1	0	ROUT1 Output Buffer* 0 = Power down 1 = Power up
	4	LOUT2	0	LOUT2 Output Buffer* 0 = Power down 1 = Power up
	3	ROUT2	0	ROUT2 Output Buffer* 0 = Power down 1 = Power up
	2	MONO	0	MONOOUT Output Buffer and Mono Mixer 0 = Power down 1 = Power up
	1	OUT3	0	OUT3 Output Buffer 0 = Power down 1 = Power up
* The left mixer is enabled when LOUT1=1 or LOUT2=1. The right mixer is enabled when ROUT1=1 or ROUT2=1.				

Table 43 Power Management

STOPPING THE MASTER CLOCK

In order to minimise power consumed in the digital core of the WM8750JL, the master clock may be stopped in Standby and OFF modes. If this cannot be done externally at the clock source, the DIGENB bit (R25, bit 0) can be set to stop the MCLK signal from propagating into the device core. In Standby mode, setting DIGENB will typically provide an additional power saving on DCVDD of 20uA. However, since setting DIGENB has no effect on the power consumption of other system components external to the WM8750JL, it is preferable to disable the master clock at its source wherever possible.

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION
R25 (19h) Additional Control (1)	0	DIGENB	0	Master clock disable 0: master clock enabled 1: master clock disabled

Table 44 ADC and DAC Oversampling Rate Selection

NOTE: Before DIGENB can be set, the control bits ADCL, ADCR, DACL and DACR must be set to zero and a waiting time of 1ms must be observed. Any failure to follow this procedure may prevent DACs and ADCs from re-starting correctly.

SAVING POWER BY REDUCING OVERSAMPLING RATE

The default mode of operation of the ADC and DAC digital filters is in 128x oversampling mode. Under the control of ADCOSR and DACOSR the oversampling rate may be halved. This will result in a slight decrease in noise performance but will also reduce the power consumption of the device. In USB mode ADCOSR must be set to 0, i.e. 128x oversampling.

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION
R24 (18h) Additional Control (2)	1	ADCOSR	0	ADC oversample rate select 1 = 64x (lowest power) 0 = 128x (best SNR)
	0	DACOSR	0	DAC oversample rate select 1 = 64x (lowest power) 0 = 128x (best SNR)

Table 45 ADC and DAC Oversampling Rate Selection

ADCOSR set to '1', 64x oversample mode, is not supported in USB mode (USB=1).

SAVING POWER AT HIGHER SUPPLY VOLTAGES

The analogue supplies to the WM8750JL can run from 1.8V to 3.6V. By default, all analogue circuitry on the device is optimized to run at 3.3V. This set-up is also good for all other supply voltages down to 1.8V. At lower voltages, performance can be improved by increasing the bias current. If low power operation is preferred the bias current can be left at the default setting. This is controlled as shown below.

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION
R23 (17h) Additional Control(1)	7:6	VSEL [1:0]	11	Analogue Bias optimization 00: Highest bias current, optimized for AVDD=1.8V 01: Bias current optimized for AVDD=2.5V 1X: Lowest bias current, optimized for AVDD=3.3V

REGISTER MAP

REGISTER	ADDRESS (Bit 15 – 9)	remarks	Bit[8]	Bit[7]	Bit[6]	Bit[5]	Bit[4]	Bit[3]	Bit[2]	Bit[1]	Bit[0]	default	page ref
R0 (00h)	0000000	Left Input volume	LIVU	LINMUTE	LIZC	LINVOL						010010111	19
R1 (01h)	0000001	Right Input volume	RIVU	RINMUTE	RIZC	RINVOL						010010111	19
R2 (02h)	0000010	LOUT1 volume	LO1VU	LO1ZC	LOUT1VOL[6:0]							001111001	32
R3 (03h)	0000011	ROUT1 volume	RO1VU	RO1ZC	ROUT1VOL[6:0]							001111001	32
R4 (04h)	0000100	Reserved	0	0	0	0	0	0	0	0	0	000000000	-
R5 (05h)	0000101	ADC & DAC Control	ADCDIV2	DACDIV2	ADCPOL[1:0]		HPOR	DACMU	DEEMPH[1:0]		ADCHPD	000001000	21, 26,29
R6 (06h)	0000110	Reserved	0	0	0	0	0	0	0	0	0	000000000	-
R7 (07h)	0000111	Audio Interface	0	BCLKINV	MS	LRSWAP	LRP	WL[1:0]		FORMAT[1:0]		000001010	42
R8 (08h)	0001000	Sample rate	BCM[1:0]		CLKDIV2	SR[4:0]					USB	000000000	43, 44
R9 (09h)	0001001	Reserved	0	0	0	0	0	0	0	0	0	000000000	-
R10 (0Ah)	0001010	Left DAC volume	LDVU	LDACVOL[7:0]								011111111	27
R11 (0Bh)	0001011	Right DAC volume	RDVU	RDACVOL[7:0]								011111111	27
R12 (0Ch)	0001100	Bass control	0	BB	BC	0	0	BASS[3:0]				000001111	28
R13 (0Dh)	0001101	Treble control	0	0	TC	0	0	TRBL[3:0]				000001111	28
R15 (0Fh)	0001111	Reset	writing to this register resets all registers to their default state									not reset	-
R16 (10h)	0010000	3D control	0	MODE3D	3DUC	3DLC	3DDEPTH[3:0]				3DEN	000000000	26
R17 (11h)	0010001	ALC1	ALCSEL[1:0]		MAXGAIN[2:0]			ALCL[3:0]				001111011	24
R18 (12h)	0010010	ALC2	0	ALCZC	0	0	0	HLD[3:0]				000000000	24
R19 (13h)	0010011	ALC3	0	DCY[3:0]				ATK[3:0]				000110010	24
R20 (14h)	0010100	Noise Gate	0	NGTH[4:0]					NGG[1:0]		NGAT	000000000	25
R21 (15h)	0010101	Left ADC volume	LAVU	LADCVOL[7:0]								011000011	22
R22 (16h)	0010110	Right ADC volume	RAVU	RADCVOL[7:0]								011000011	22
R23 (17h)	0010111	Additional control(1)	TSDEN	VSEL[1:0]		DMONOMIX[1:0]		DATSEL[1:0]		DACINV	TOEN	011000000	18, 19, 29, 36
R24 (18h)	0011000	Additional control(2)	OUT3SW[1:0]		HPSWEN	HPSWPOL	ROUT2INV	TRI	LRCM	ADCOSR	DACOSR	000000000	33, 34, 35, 42, 43, 49
R25 (19h)	0011001	Pwr Mgmt (1)	VMIDSEL[1:0]		VREF	AINL	AINR	ADCL	ADCR	MICB	DIGENB	000000000	48
R26 (1Ah)	0011010	Pwr Mgmt (2)	DACL	DACR	LOUT1	ROUT1	LOUT2	ROUT2	MONO	OUT3	0	000000000	48
R27 (1Bh)	0011011	Additional Control (3)	ADCLRM[1:0]		VROI	HPFLREN	0	0	0	0	0	000000000	21, 34, 44
R31 (1Fh)	0011111	ADC input mode	DS	MONOMIX[1:0]		RDCM	LDCM	0	0	0	0	000000000	17
R32 (20h)	0100000	ADCL signal path	0	LINSEL[1:0]		LMICBOOST[1:0]		0	0	0	0	000000000	17
R33 (21h)	0100001	ADCR signal path	0	RINSEL[1:0]		RMICBOOST[1:0]		0	0	0	0	000000000	17
R34 (22h)	0100010	Left out Mix (1)	LD2LO	LI2LO	LI2LOVOL[2:0]			0	LMIXSEL[2:0]			001010000	30
R35 (23h)	0100011	Left out Mix (2)	RD2LO	RI2LO	RI2LOVOL[2:0]			0	0	0	0	001010000	30
R36 (24h)	0100100	Right out Mix (1)	LD2RO	LI2RO	LI2ROVOL[2:0]			0	RMIXSEL[2:0]			001010000	31
R37 (25h)	0100101	Right out Mix (2)	RD2RO	RI2RO	RI2ROVOL[2:0]			0	0	0	0	001010000	31
R38 (26h)	0100110	Mono out Mix (1)	LD2MO	LI2MO	LI2MOVOL[2:0]			0	0	0	0	001010000	31
R39 (27h)	0100111	Mono out Mix (2)	RD2MO	RI2MO	RI2MOVOL[2:0]			0	0	0	0	001010000	31
R40 (28h)	0101000	LOUT2 volume	LO2VU	LO2ZC	LOUT2VOL[6:0]							001111001	33
R41 (29h)	0101001	ROUT2 volume	RO2VU	RO2ZC	ROUT2VOL[6:0]							001111001	33
R42 (2Ah)	0101010	MONOOUT volume	0	MOZC	MOUTVOL[6:0]							001111001	33

DIGITAL FILTER CHARACTERISTICS

The ADC and DAC employ different digital filters. There are 4 types of digital filter, called Type 0, 1, 2 and 3. The performance of Types 0 and 1 is listed in the table below, the responses of all filters is shown in the proceeding pages.

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
ADC Filter Type 0 (USB Mode, 250fs operation)					
Passband	+/- 0.05dB	0		0.416fs	
	-6dB		0.5fs		
Passband Ripple				+/- 0.05	dB
Stopband		0.584fs			
Stopband Attenuation	f > 0.584fs	-60			dB
ADC Filter Type 1 (USB mode, 272fs or Normal mode operation)					
Passband	+/- 0.05dB	0		0.4535fs	
	-6dB		0.5fs		
Passband Ripple				+/- 0.05	dB
Stopband		0.5465fs			
Stopband Attenuation	f > 0.5465fs	-60			dB
High Pass Filter Corner Frequency	-3dB		3.7		Hz
	-0.5dB		10.4		
	-0.1dB		21.6		
DAC Filter Type 0 (USB mode, 250fs operation)					
Passband	+/- 0.03dB	0		0.416fs	
	-6dB		0.5fs		
Passband Ripple				+/-0.03	dB
Stopband		0.584fs			
Stopband Attenuation	f > 0.584fs	-50			dB
DAC Filter Type 1 (USB mode, 272fs or Normal mode operation)					
Passband	+/- 0.03dB	0		0.4535fs	
	-6dB		0.5fs		
Passband Ripple				+/- 0.03	dB
Stopband		0.5465fs			
Stopband Attenuation	f > 0.5465fs	-50			dB

Table 46 Digital Filter Characteristics

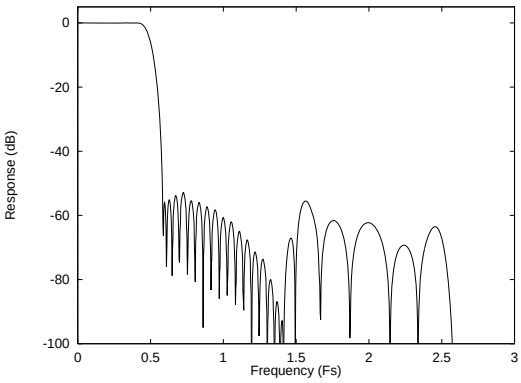
DAC FILTERS		ADC FILTERS	
Mode	**Group Delay**	**Mode**	**Group Delay**
0 (250 USB)	11/FS	0 (250 USB)	13/FS
1 (256/272)	16/FS	1 (256/272)	23/FS
2 (250 USB, 96k mode)	4/FS	2 (250 USB, 96k mode)	4/FS
3 (256/272, 88.2/96k mode)	3/FS	3 (256/272, 88.2/96k mode)	5/FS

Table 47 ADC/DAC Digital Filters Group Delay

TERMINOLOGY

1. Stop Band Attenuation (dB) – the degree to which the frequency spectrum is attenuated (outside audio band)
2. Pass-band Ripple – any variation of the frequency response in the pass-band region

DAC FILTER RESPONSES



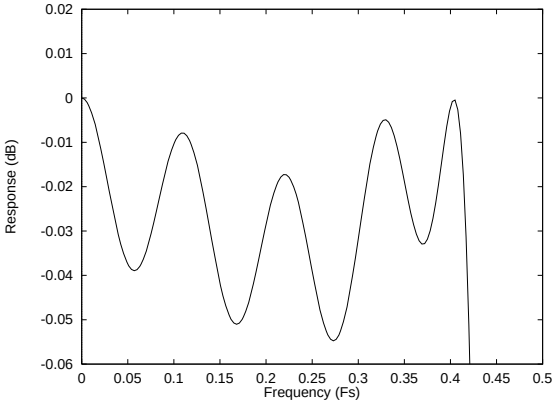
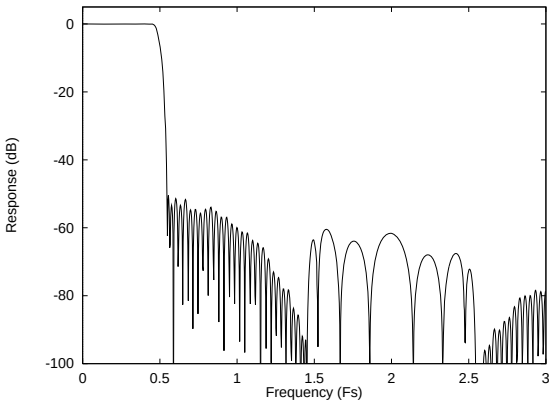


Figure 27 DAC Digital Filter Frequency Response – Type 0 **Figure 28 DAC Digital Filter Ripple – Type 0**



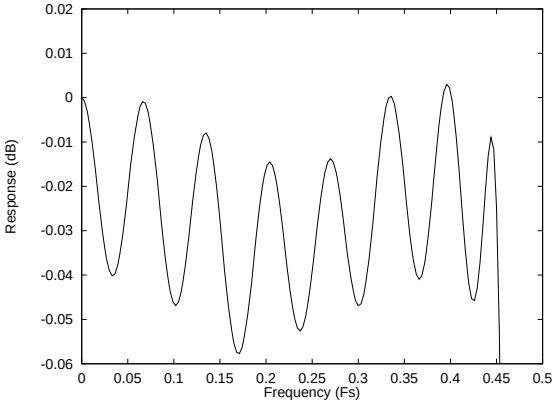
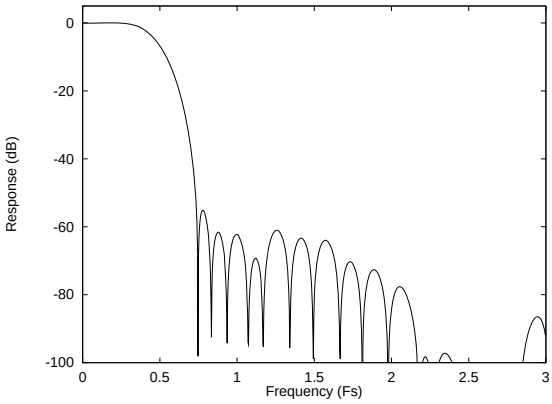


Figure 29 DAC Digital Filter Frequency Response – Type 1 **Figure 30 DAC Digital Filter Ripple – Type 1**



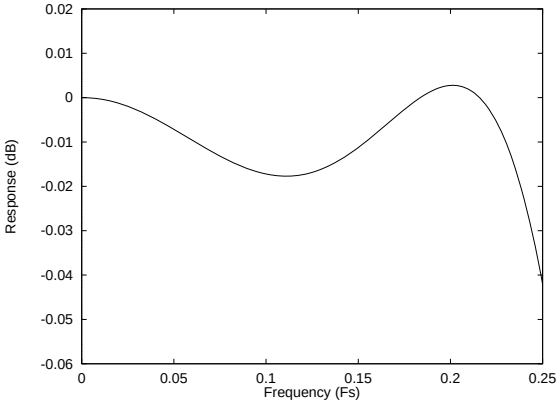


Figure 31 DAC Digital Filter Frequency Response – Type 2 **Figure 32 DAC Digital Filter Ripple – Type 2**

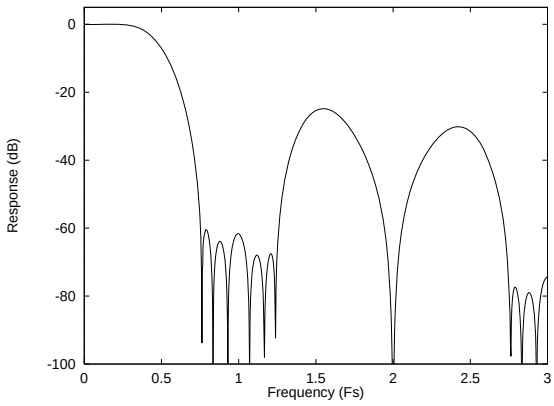


Figure 33 DAC Digital Filter Frequency Response – Type 3

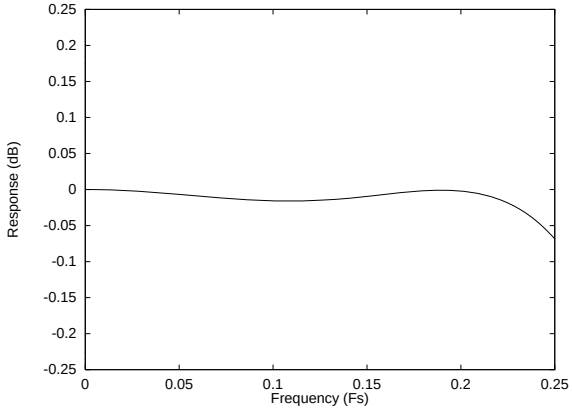


Figure 34 DAC Digital Filter Ripple – Type 3

ADC FILTER RESPONSES

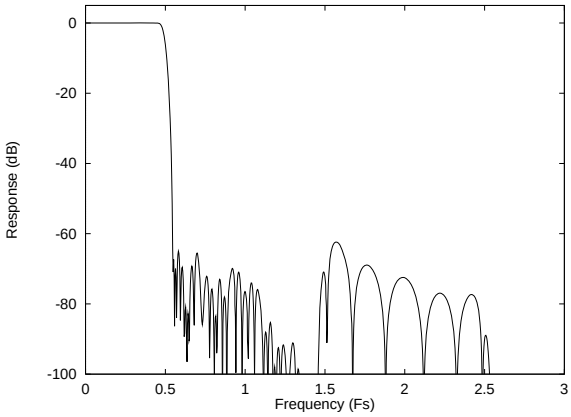


Figure 35 ADC Digital Filter Frequency Response – Type 0

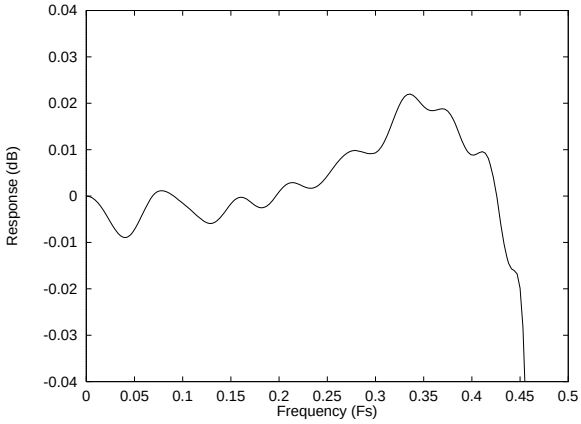


Figure 36 ADC Digital Filter Ripple – Type 0

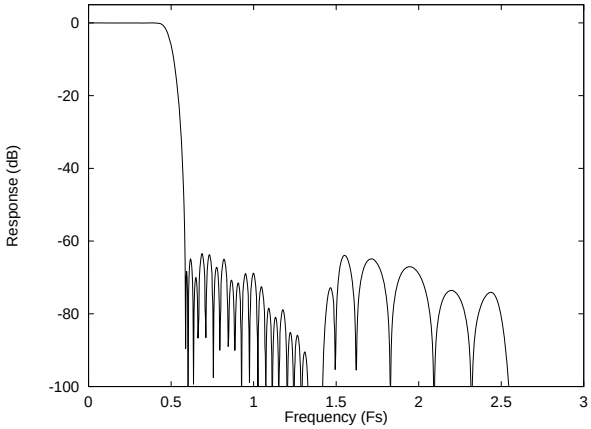


Figure 37 ADC Digital Filter Frequency Response – Type 1

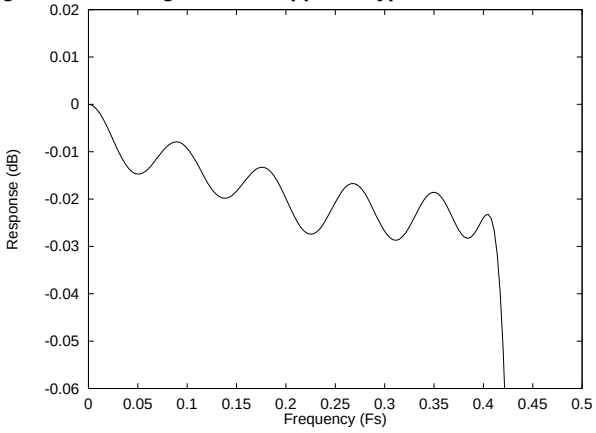


Figure 38 ADC Digital Filter Ripple – Type 1

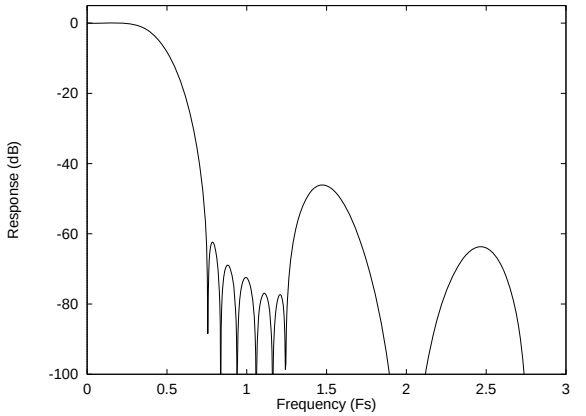


Figure 39 ADC Digital Filter Frequency Response – Type 2

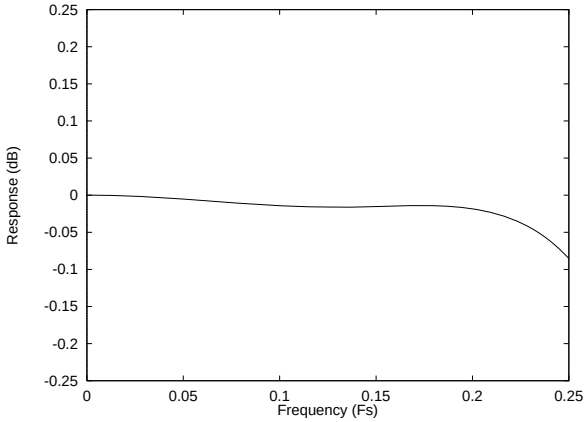


Figure 40 ADC Digital Filter Ripple – Type 2

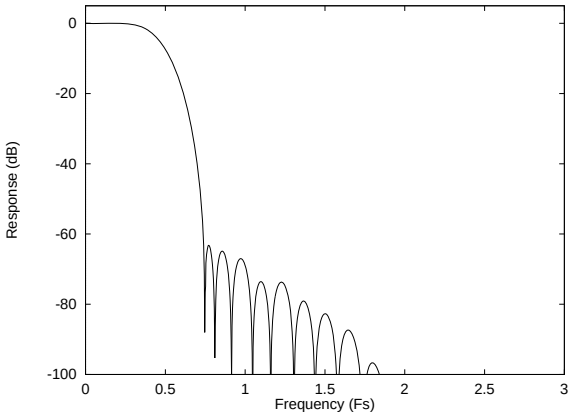


Figure 41 ADC Digital Filter Frequency Response – Type 2

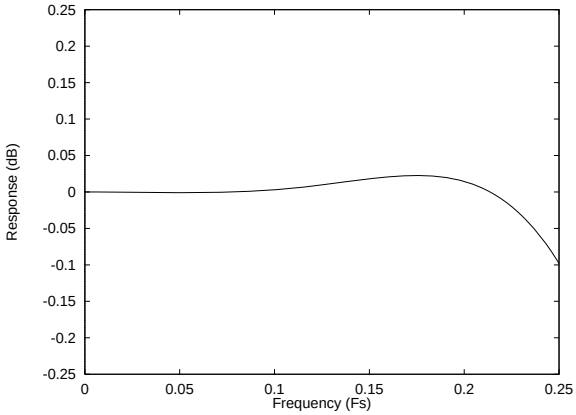


Figure 42 ADC Digital Filter Ripple – Type 3

DE-EMPHASIS FILTER RESPONSES

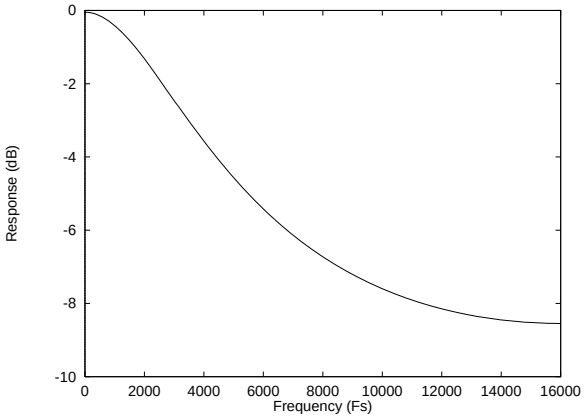


Figure 43 De-emphasis Frequency Response (32kHz)

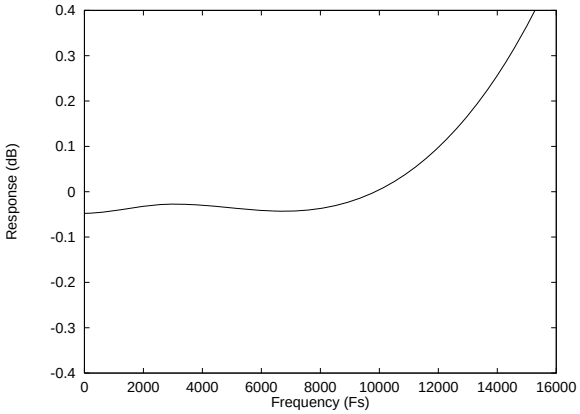


Figure 44 De-emphasis Error (32kHz)

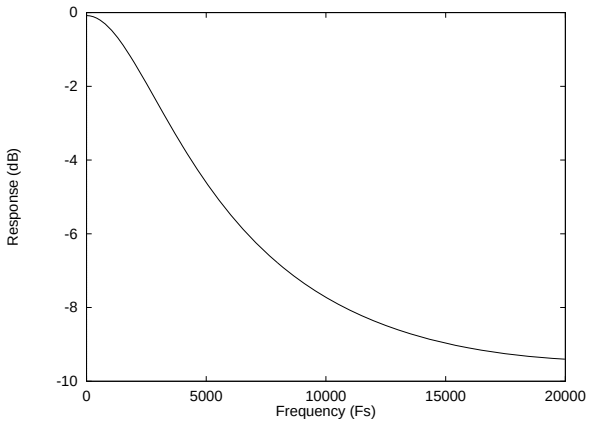


Figure 45 De-emphasis Frequency Response (44.1kHz)

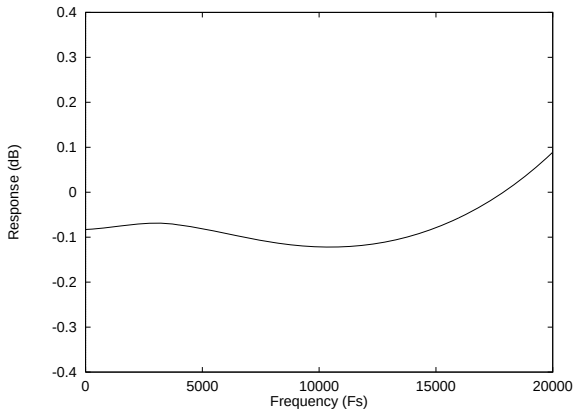


Figure 46 De-emphasis Error (44.1kHz)

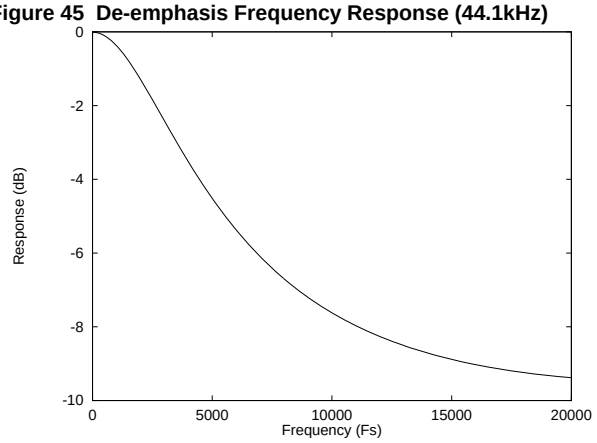


Figure 47 De-emphasis Frequency Response (48kHz)

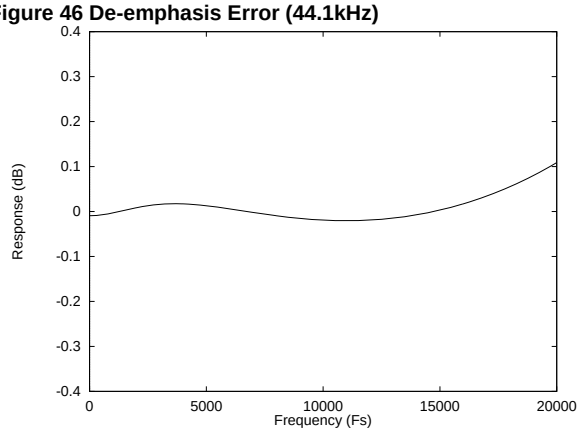


Figure 48 De-emphasis Error (48kHz)

HIGHPASS FILTER

The WM8750JL has a selectable digital highpass filter in the ADC filter path to remove DC offsets. The filter response is characterised by the following polynomial:

$$H(z) = \frac{1 - z^{-1}}{1 - 0.9995z^{-1}}$$

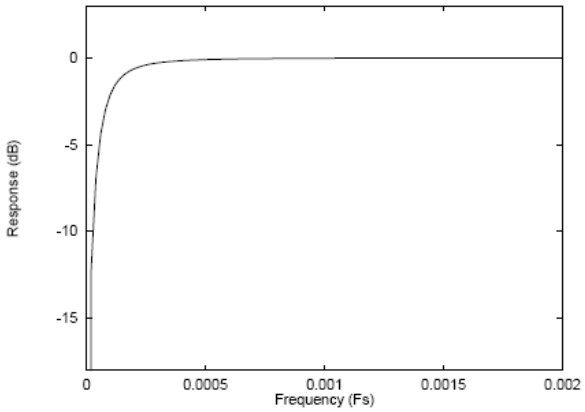
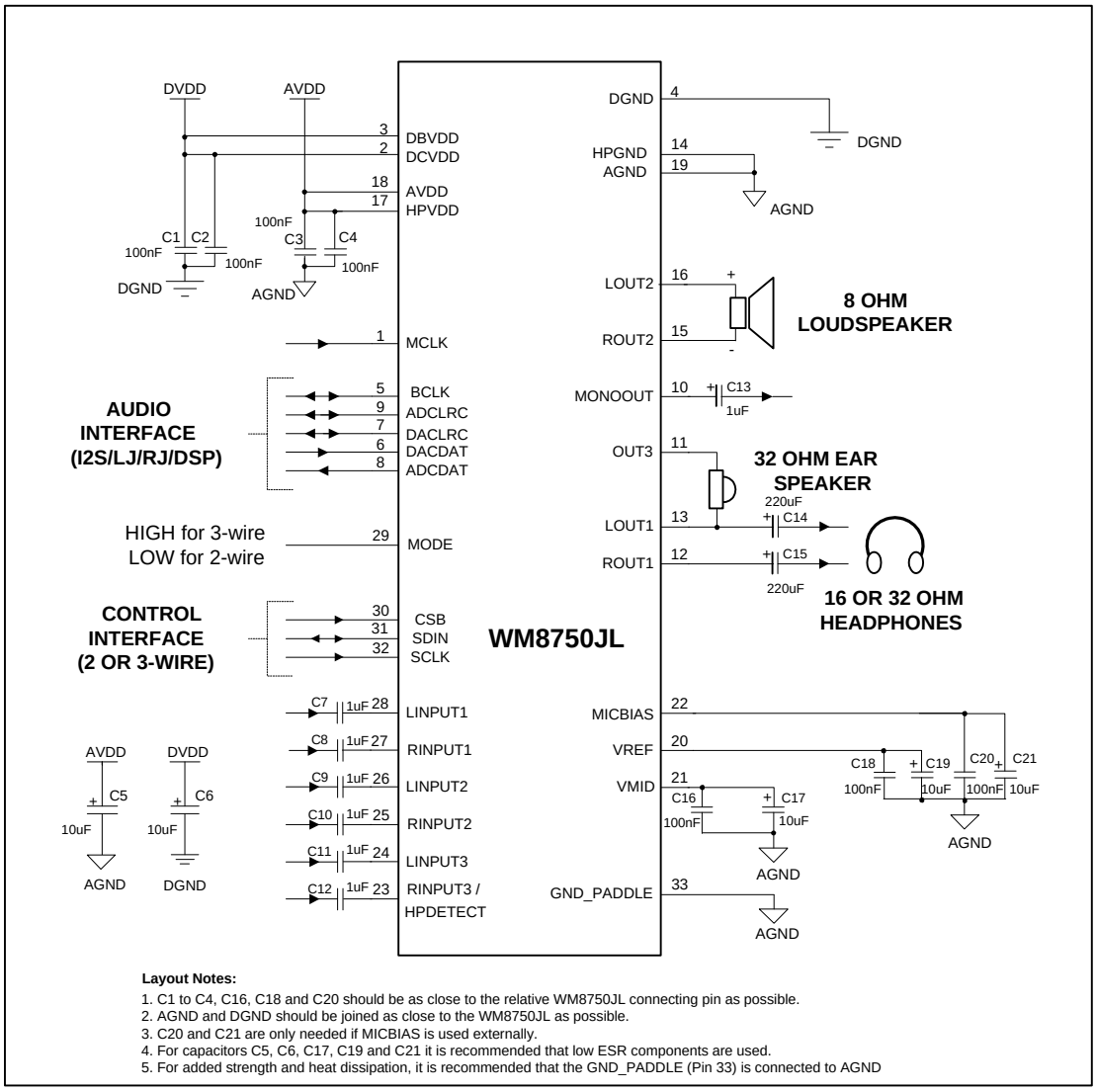


Figure 49 ADC Highpass Filter Response

APPLICATIONS INFORMATION

RECOMMENDED EXTERNAL COMPONENTS



Layout Notes:

1. C1 to C4, C16, C18 and C20 should be as close to the relative WM8750JL connecting pin as possible.
2. AGND and DGND should be joined as close to the WM8750JL as possible.
3. C20 and C21 are only needed if MICBIAS is used externally.
4. For capacitors C5, C6, C17, C19 and C21 it is recommended that low ESR components are used.
5. For added strength and heat dissipation, it is recommended that the GND_PADDLE (Pin 33) is connected to AGND

Figure 50 Recommended External Components Diagram

LINE INPUT CONFIGURATION

When LINPUT1/RINPUT1 or LINPUT2/RINPUT2 are used as line inputs, the microphone boost and ALC functions should normally be disabled.

In order to avoid clipping, the user must ensure that the input signal does not exceed AVDD. This may require a potential divider circuit in some applications. It is also recommended to remove RF interference picked up on any cables using a simple first-order RC filter, as high-frequency components in the input signal may otherwise cause aliasing distortion in the audio band. AC signals with no DC bias should be fed to the WM8750JL through a DC blocking capacitor, e.g. 1μF.

MICROPHONE INPUT CONFIGURATION

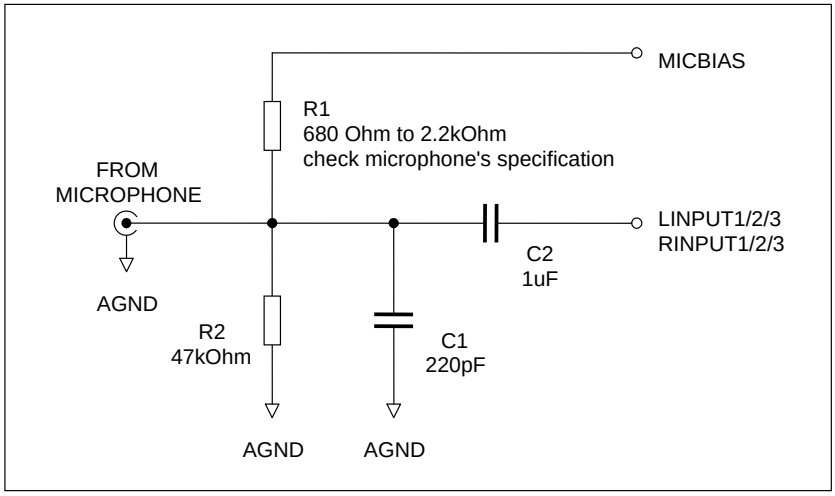


Figure 51 Recommended Circuit for Line Input

For interfacing to a microphone, the ALC function should be enabled and the microphone boost switched on. Microphones held close to a speaker's mouth would normally use the 13dB gain setting, while tabletop or room microphones would need a 29dB boost.

The recommended application circuit is shown above. R1 and R2 form part of the biasing network (refer to Microphone Bias section). R1 connected to MICBIAS is necessary only for electret type microphones that require a voltage bias. R2 should always be present to prevent the microphone input from charging to a high voltage which may damage the microphone on connection. R1 and R2 should be large so as not to attenuate the signal from the microphone, which can have source impedance greater than 2kOhm. C1 together with the source impedance of the microphone and the WM8750JL input impedance forms an RF filter. C2 is a DC blocking capacitor to allow the microphone to be biased at a different DC voltage to the MICIN signal.

MINIMISING POP NOISE AT THE ANALOGUE OUTPUTS

To minimise any pop or click noise when the system is powered up or down, the following procedures are recommended.

POWER UP

- Switch on power supplies. By default the WM8750JL is in Standby Mode, the DAC is digitally muted and the Audio Interface, Line outputs and Headphone outputs are all OFF (DACMU = 1 Power Management registers 1 and 2 are all zeros).
- Enable Vmid and VREF.
- Enable DACs as required
- Enable line and / or headphone output buffers as required.
- Set DACMU = 0 to soft-un-mute the audio DACs.

POWER DOWN

- Set DACMU = 1 to soft-mute the audio DACs.
- Disable all output buffers.
- Switch off the power supplies.

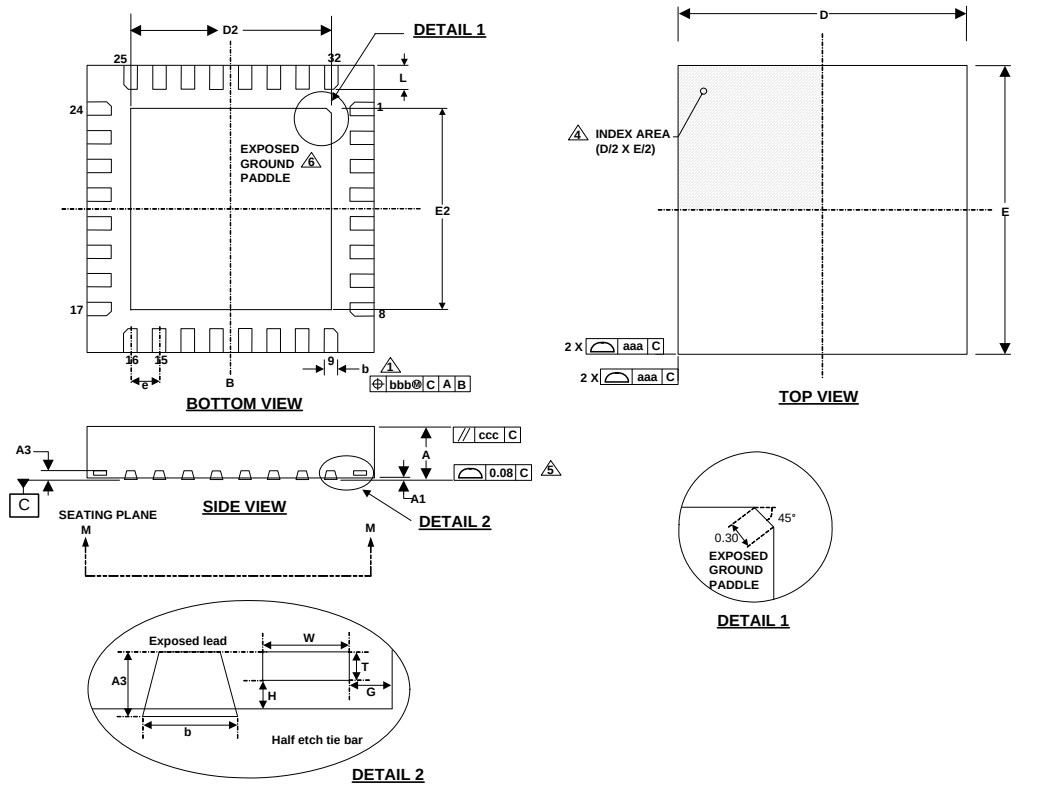
POWER MANAGEMENT EXAMPLES

OPERATION MODE	POWER MANAGEMENT (1)							POWER MANAGEMENT (2)							
			PGAs		ADCs			DACs		Output Buffers					
	VREF	AINL/R	PGL	PGR	ADL	ADR	MBI	DAL	DAR	LO1	RO1	LO2	RO2	MO	HPD
Stereo Headphone Playback	1	0	0	0	0	0	0	1	1	1	1	0	0	0	x
Stereo Line-in Record	1	1	1	1	1	1	0	0	0	0	0	0	0	0	0
Stereo Microphone Record	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0
Mono Microphone Record	1	1	1	0	1	0	1	0	0	0	0	0	0	0	0
Stereo Line-in to Headphone Out	1	1	0	0	0	0	0	0	0	1	1	0	0	0	x
Phone Call	1	1	1	0	0	0	1	0	0	1	1	0	0	1	x
Speaker Phone Call [ROUT2INV = 1]	1	1	1	0	0	0	1	0	0	0	0	1	1	1	0
Record Phone Call [L channel = mic with boost, R channel = RX, enable mono mix]	1	1	1	1	1	1	1	0	0	1	1	0	0	1	x

Table 48 Register Settings for Power Management

PACKAGE DIMENSIONS

FL: 32 PIN QFN PLASTIC PACKAGE 5 x 5 x 0.9 mm BODY, 0.50 mm LEAD PITCH **DM101.A**



Symbols		Dimensions (mm)		
	MIN	NOM	MAX	NOTE
A	0.80	0.90	1.00	
A1	0	0.02	0.05	
A3		0.203 REF		
b	0.18	0.25	0.30	1
D		5.00 BSC		
D2	3.30	3.45	3.60	2
E		5.00 BSC		
E2	3.30	3.45	3.60	2
e		0.50 BSC		
G		0.20		
H		0.1		
L	0.30	0.40	0.50	
T		0.103		
W		0.15		
Tolerances of Form and Position				
aaa	0.15			
bbb	0.10			
ccc	0.10			
REF:	JEDEC, MO-220, VARIATION VHHD-5.			

NOTES:
1. DIMENSION b APPLIES TO METALLIZED TERMINAL AND IS MEASURED BETWEEN 0.15 mm AND 0.30 mm FROM TERMINAL TIP.
2. FALLS WITHIN JEDEC, MO-220, VARIATION VHHD-5.
3. ALL DIMENSIONS ARE IN MILLIMETRES.
4. THE TERMINAL #1 IDENTIFIER AND TERMINAL NUMBERING CONVENTION SHALL CONFORM TO JEDEC 95-1 SPP-002.
5. COPLANARITY APPLIES TO THE EXPOSED HEAT SINK SLUG AS WELL AS THE TERMINALS.
6. REFER TO APPLICATION NOTE WAN_0118 FOR FURTHER INFORMATION REGARDING PCB FOOTPRINTS AND QFN PACKAGE SOLDERING.
7. THIS DRAWING IS SUBJECT TO CHANGE WITHOUT NOTICE.

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REVISION HISTORY

DATE	REV	ORIGINATOR	CHANGES
16/01/12	4.1	JMacD	Order codes updated from WM8750JLGEFL and WM8750JLGEFL/R to WM8750**C**JLGEFL and WM8750**C**JLGEFL/R to reflect change to copper wire bonding.
16/01/12	4.1	JMacD	Package diagram changed to DM101.A