ATO25D1GA

3.3V 1G-BIT
Serial NAND Flash Memory with Quad SPI

Revision History

Revision No.	History	Date	Remark
0.0	Initial Draft	Sep.2012	preliminary
0.1	1. Add one page configuration (page 15) 2. Add OTP Protection Register (page 24) 3. Add Random Data-in Limitation (page 31) 4. Add NOP Description (page 41) 5. Correct the typo (page17; 7.2 Quad SPI Instructions)	Nov. 2012	
0.2	Add operating temperature(page 46)	Apr. 2013	
0.3	Add Package pin map (page 9)	July. 2013	
0.4	Adjust Package(WSON / SOIC 300mil) Image (Page 9)	Aug. 2013	
0.5	Add Industrial operating temperature (Page 39)	Sep. 2013	
0.6	Bit0 of the register OTP register, QE, revised (Page 24)	Mar. 2015	
0.7	WSON package dimension revision (Page 44)	July. 2015	

FEATURES

GENERAL

Serial Peripheral Interface
- Mode 0 and Mode 3

Standard, Quad SPI
- Standard SPI : SCLK, CS#, SI, SO
- Quad SPI : SCLK, CS#, SIO0, SIO1, SIO2/W#, SIO3/Hold#

Single power supply operation
- Full voltage range: 2.7V to 3.6V read, erase and program operations

Organization
- Memory Cell Array : (128M + 4M) x Bytes
- Data Register : (2048 + 64) x Bytes

Automatic Program and Erase
- Page Program : (2048 + 64) x Bytes
- Block Erase : (128K + 4K) x Bytes = 64pages

Page Read Operation
- Page Size : (2048 + 64) Bytes
- Page Read(cell array to page buffer) : 25us(Max.)
- Serial Page Access : 104MHz, 133MHz(C_L=15pF)

Fast Write Cycle Time
- Program time : 200us(Typ.)
- Block Erase time : 2ms(Typ.)

Electronic Identification
- JEDEC standard 1-byte manufacturer ID and 1-byte device ID.

.

Copy-Back PROGRAM Operation
- Fast Page copy without external buffering

Security features
- OTP area, 16K bytes(8 pages)

Hardware Data Protection
- Program / Erase locked during Power transitions.
- W# pin works in conjunction with Status Register Bits to protect specified memory areas. Status Register Block Protection bits (BP2, BP1, BP0) in status register configure parts of memory as read-only

Data Integrity
- Endurance:100K Program/Erase Cycles
- Data Retention : 10 years

Error Management
- Internal ECC code generation
- 1bit/528byte ECC, 1NOP/528byte

Package
- 8-pad 8x6 WSON
- 16-pin SOIC 300 mil

Contents

List of tables

List of figures

1. General Description

The ATO25D1GA is 1G-bit with spare 32Mbit capacity. The device is offered in 3.3V power supply. Its NAND cell provides the most cost-effective solution for the solid state mass storage market. The memory is divided into blocks that can be erased independently so it possible to preserve valid data while old data is erased. The device contains 1024 blocks, composed by 64 pages consisting in two NAND structures of 32series connected Flash Cells. A program operation can be performed in typical 200us on the 2048-bytes and an erase operation can be performed in typical 2ms on a 128K-bytes block. Data in the page can be read out at 25ns cycle time per byte. The on-chip write control automates all program and erase functions including pulse repetition, where required, and internal verification and margining of data. Even the write-intensive systems can take advantage of the ATO25D1GA's extended reliability of 100K program/erase cycles by providing ECC(Error Correction Code) with real time mapping-out algorithm.

ATO25D1GA features a serial peripheral interface and software protocol allowing operation on a simple 3-wire bus while it is in single I/O mode. The three signals are a clock input(SCLK), a serial data input(SI), and a serial data output(SO). Serial access to the device is enabled by CS# input. When it is in four I/O read mode, the SI pin, SO pin, WP# pin and HOLD# pin become SIO0 pin, SIO1 pin, SIO2 pin SIO3 pin for address/dummy bits input and data output. The copy back function allows the optimization of defective blocks management : when a page program operation fails the data can be directly programmed in another page inside the same array section without the time consuming serial data insertion phase. The ATO25D1GA is an optimum solution for large nonvolatile storage applications such as solid state file storage and other portable applications requiring non-volatility.

After program/erase command is issued, auto program/erase algorithms which program/erase and verify the specified page or sector/block locations will be executed. Up to 2Kbytes can be programmed at a time. Pages can be erased in groups of 128KB erase. To provide user with ease of interface, a status register is included to indicate the status of the chip. The status read command can be issued to detect completion status of a program or erase operation via OIP bit. Advanced security features enhance the protection and security functions, please see security features section for more details.

The ATO25D1GA supports JEDEC standard manufacturer and device identification with a 16Kbytes(8 pages) Secured OTP.

Figure 1. Logic Diagram

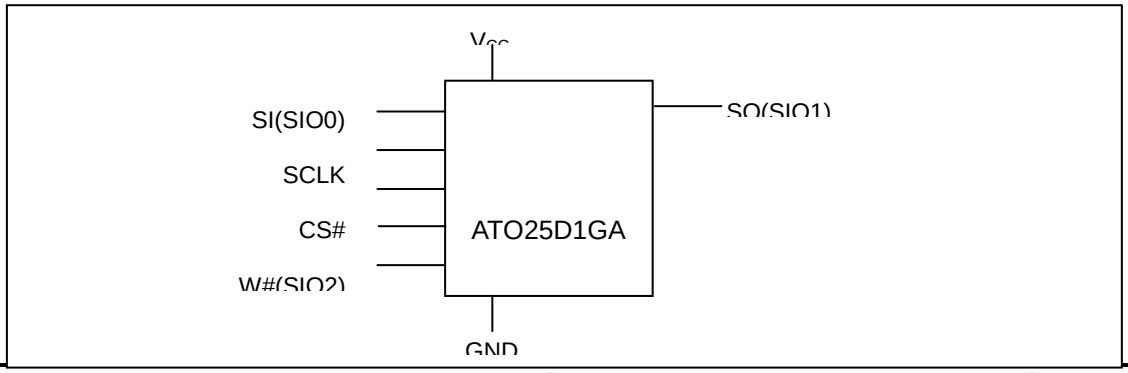
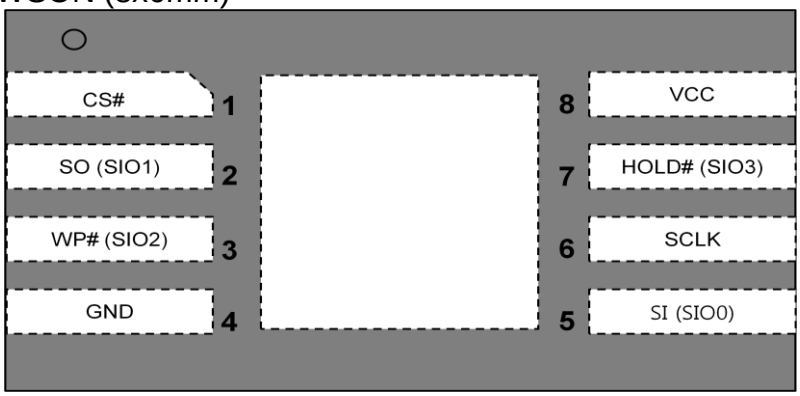


Table 1. Signal names

Signal name	Function	Direction
SCLK	Serial Clock	Input
SI(SIO0)	Serial Data Input(for 1 I/O) Serial Data Input & Output(for 4 I/O)	Input / Output
SO(SIO1)	Serial Data Output(for 1 I/O) Serial Data Input & Output(for 4 I/O)	Input / Output
CS#	Chip Select	Input
W#(SIO2)	Write Protect Serial Data Input & Output(for 4 I/O)	Input / Output
HOLD#(SIO3)	Hold Serial Data Input & Output(for 4 I/O)	Input / Output
VCC	3.3V Supply voltage	
GND	Ground	

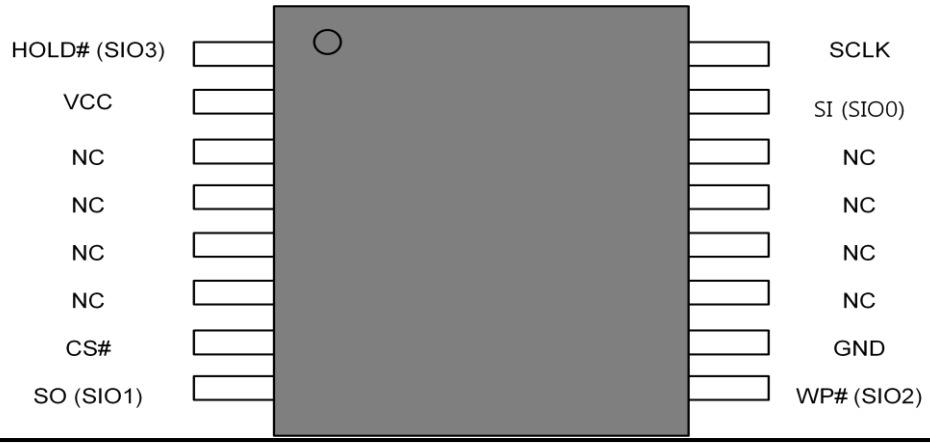
Figure 2. 8 Pad WSON 8x6mm / 16-Pin SOIC 300mil connections

8 Pad WSON (8x6mm)



TOP VIEW

16 Pin SOIC 300mil



TOP VIEW

2 Signal descriptions

2.1 Serial Data output (SO) – SIO1

This output signal is used to transfer data serially out of the device. Data is shifted out on the falling edge of Serial Clock (SCLK) at all read mode. Also, When the device is Quad mode, this pin(SO) is used for SIO1

2.2 Serial Data input (SI) – SIO0

This input signal is used to transfer data serially into the device. It receives instructions, addresses, and the data to be programmed. Values are latched on the rising edge of Serial Clock (SCLK). Also, When the device is Quad mode, this pin(SI) is used for SIO0

2.3 Serial Clock (SCLK)

This input signal provides the timing of the serial interface. Instructions, addresses, or data present at Serial Data Input (SI) are latched on the rising edge of Serial Clock (SCLK). Data on Serial Data Output (SO) changes after the falling edge of Serial Clock (SCLK).

2.4 Chip Select (CS#)

When this input signal is High, the device is deselected and Serial Data Output Pins are at high impedance. Unless an internal Program, Erase or Write Status Register cycle is in progress, the device will be in the Standby mode (this is not the Deep Power-down mode). Driving Chip Select (CS#) Low enables the device, placing it in the active power mode.

After Power-up, a falling edge on Chip Select (CS#) is required prior to the start of any instruction.

2.5 Hold (HOLD#) – SIO3

The Hold (HOLD#) signal is used to pause any serial communications with the device without deselecting the device.

During the Hold condition, the Serial Data Output (SO) is high impedance, and Serial Data Input (SI) and Serial Clock (SCLK) are Don't Care.

To start the Hold condition, the device must be selected, with Chip Select (CS#) driven Low. Also, When the QE bit of Status Register is set for "High", the Hold# function is not available and this pin used for SIO3 in Quad mode.

2.6 Write Protect (W#) – SIO2

The main purpose of this input signal is to freeze the size of the area of memory that is protected against program or erase instructions (as specified by the values in the BP2, BP1 and BP0 bits of the Status Register).
Like the Hold# pin, When the QE bit of Status Register is set for "High", the W# function is not available too, and this pin used for SIO2 in Quad mode.

3 SPI modes

These devices can be driven by a microcontroller with its SPI peripheral running in either of the two following modes:

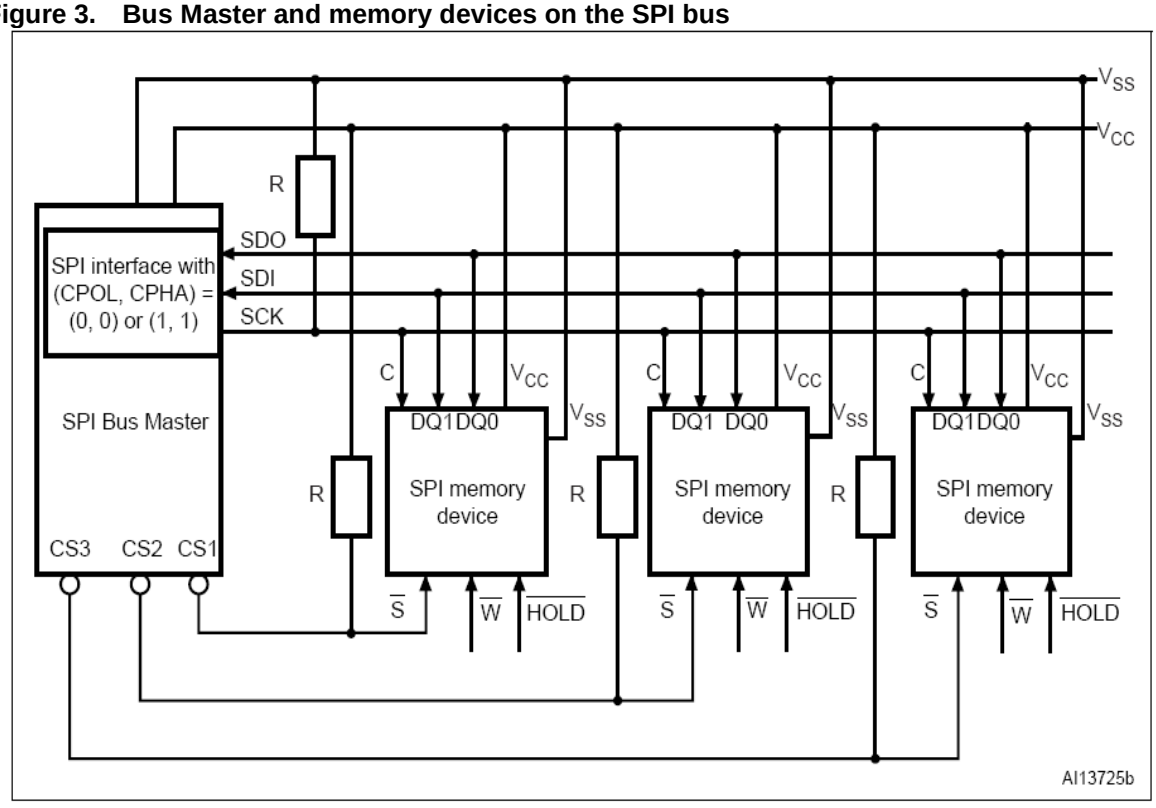
- CPOL=0, CPHA=0
- CPOL=1, CPHA=1

For these two modes, input data is latched in on the rising edge of Serial Clock (SCLK), and output data is available from the falling edge of Serial Clock (SCLK).

The difference between the two modes, as shown in *Figure 4*, is the clock polarity when the bus master is in Standby mode and not transferring data:

- C remains at 0 for (CPOL=0, CPHA=0)
- C remains at 1 for (CPOL=1, CPHA=1)

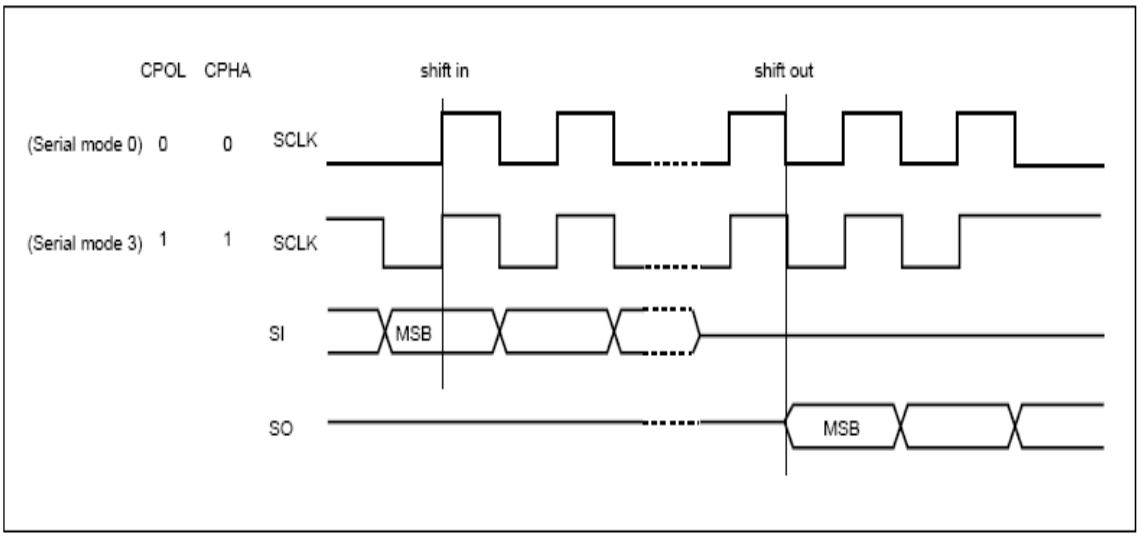
Figure 3. Bus Master and memory devices on the SPI bus



1. The Write Protect (W) and Hold (HOLD) signals should be driven, High or Low as appropriate.

Figure 3 shows an example of three devices connected to an MCU, on an SPI bus. Only one device is selected at a time, so only one device drives the Serial Data Output (SO) line at a time, the other devices are in the high impedance state. Resistors R (represented in *Figure 3*) ensure that the ATO25D1GA is not selected if the Bus Master leaves the CS# line in the high impedance state. As the Bus Master may enter a state where all inputs/outputs are in high impedance at the same time (for example, when the Bus Master is reset), the clock line (SCLK) must be connected to an external pull-down resistor so that, when all inputs/outputs become high impedance, the S line is pulled High while the SCLK line is pulled Low (thus ensuring that CS# and SCLK do not become High at the same time, and so, that the t_{SHCH} requirement is met). The typical value of R is 100 kΩ, assuming that the time constant R*C_p (C_p = parasitic capacitance of the bus line) is shorter than the time during which the Bus Master leaves the SPI bus in high impedance.
Example: C_p = 50 pF, that is R*C_p = 5 µs <=> the application must ensure that the Bus Master never leaves the SPI bus in the high impedance state for a time period shorter than 5µs.

Figure 4. SPI modes supported



4 Data Protection

The environments where non-volatile memory devices are used can be very noisy. No SPI device can operate correctly in the presence of excessive noise. The block lock feature provides the ability to protect the entire device, or ranges of blocks, from the PROGRAM and ERASE operations. After power-up, the device is in the “locked” state, i.e., bits 3, 4, and 5 of the block lock register are set to 1. To unlock all the blocks, or a range of blocks, the SET FEATURES command must be issued with the A0h feature address, including the data bits shown in *Table 6*.. The operation for the SET FEATURES command is shown in *Figure 13* on page 25. When BRWD is set and WP is LOW, none of the writable bits (3, 4, 5, and 7) in the block lock register can be set. Also, when a PROGRAM/ERASE command is issued to a locked block, a status of C0h is returned. When an ERASE command is issued to a locked block, the erase failure, 04h, is returned. When a PROGRAM command is issued to a locked block, program failure, 08h, is returned.

Table 2. Protected area sizes

BP2	BP1	BP0	Protected Rows
0	0	0	None-all unlocked
0	0	1	Upper 1/64 locked
0	1	0	Upper 1/32 locked
0	1	1	Upper 1/16 locked
1	0	0	Upper 1/8 locked
1	0	1	Upper 1/4 locked
1	1	0	Upper 1/2 locked
1	1	1	All locked (default)

For example, if all the blocks need to be unlocked after power-up, the following sequence should be performed:

1. Issue SET FEATURES register write (1Fh)
2. Issue the feature address to unlock the block (A0h)
3. Issue 00h on data bits to unlock all blocks

5 OTP Feature

Additional 16K-byte secured OTP for unique identifier to provide 16K-byte one-time program area for setting device unique serial number – Which may be set by factory or system customer.

The serial device offers a protected, one-time programmable NAND Flash memory area. Ten full pages (2112 bytes per page) are available on the device, and the entire range is guaranteed to be good. Customers can use the OTP area any way they want; typical uses include programming serial numbers, or other data, for permanent storage. To access the OTP feature, the user must issue the SET FEATURES command, followed by feature address B0h. When the OTP is ready for access, pages 02h–09h can be programmed in sequential order. The PROGRAM LOAD (02h) and PROGRAM EXECUTE(10h) commands can be used to program the pages. Also, the PAGE READ (13h) command can be used to read the OTP area. The data bits used in feature address B0h to enable OTP access are shown in the table below.

OTP Access

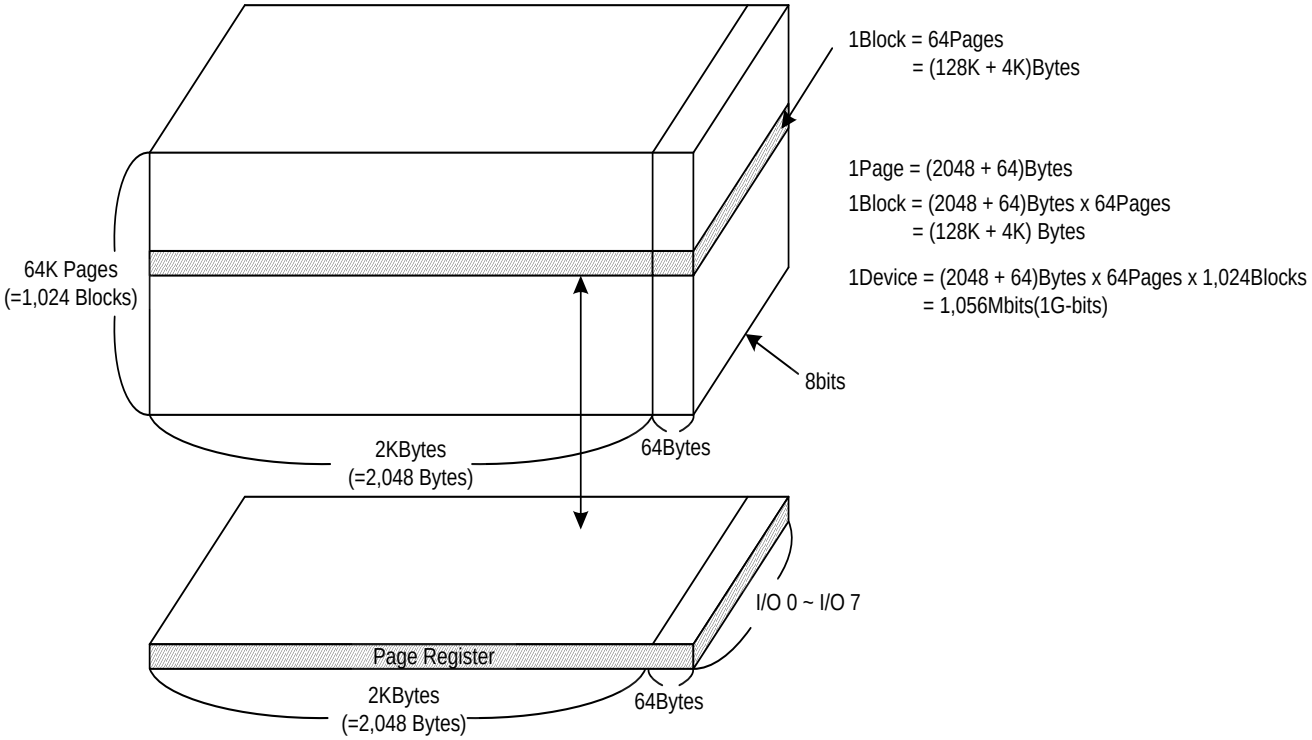
To access OTP, perform the following command sequence:

- Issue the SET FEATURES register write (1Fh)
- Issue the OTP feature address (B0h)
- Issue the PAGE PROGRAM or PAGE READ command

It is important to note that after bits 6 and 7 of the OTP register are set by the user, the OTP area becomes read-only and no further programming is supported.

6 Memory organization

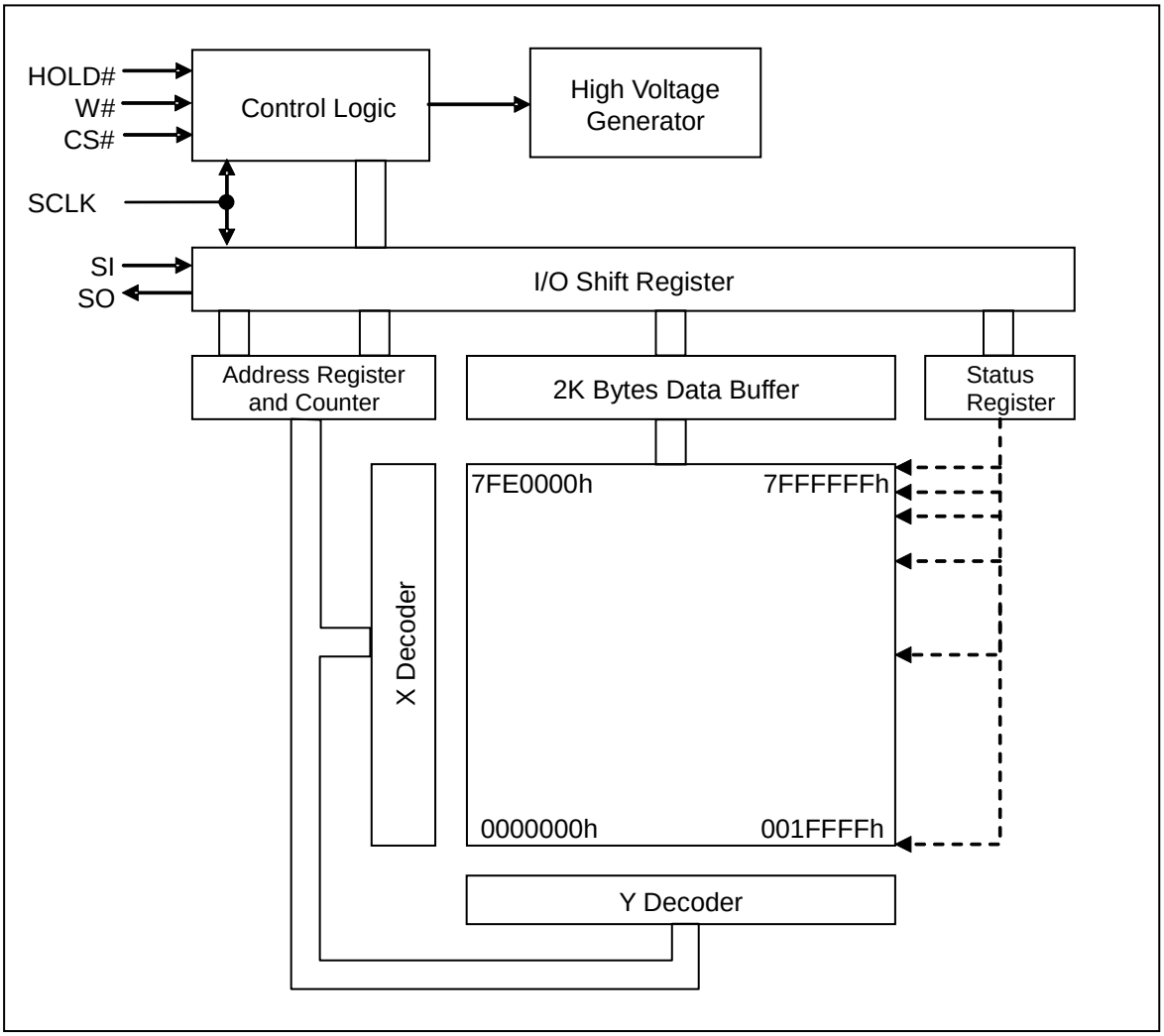
Figure 5. Memory organization



Page(2K Bytes) Configuration

	Main Array(2,048 Bytes)				Spare Array(64 Bytes)			
Area	1	2	3	4	1	2	3	4
Column Address	000h	200h	400h	600h	800h	810h	820h	830h
	1FFh	3FFh	5FFh	7FFh	80Fh	81Fh	82Fh	83Fh

Figure 6. Block diagram



7 FUNCTIONAL DESCRIPTION

7.1 Standard SPI Instructions

The ATO25D1GA is accessed through an SPI compatible bus consisting of four signals: Serial Clock (CLK). Chip Select (CS#), Serial Data Input (SI) and Serial Data Output (SO). Standard SPI instructions use the SI input pin to serially write instructions, addresses or data to the device on the rising edge of CLK. The SO output pin is used to read data or status from the device on the falling edge of SCLK.

SPI bus operation Modes 0 (0, 0) and 3 (1, 1) are supported. The primary difference between Mode 0 and Mode 3 concerns the normal state of the SCLK signal when the SPI bus master is in standby and data is not being transferred to the Serial Flash. For Mode 0 the SCLK signal is normally low on the falling and rising edges of CS#. For Mode 3 the SCLK signal is normally high on the falling and rising edges of CS#.

7.2 Quad SPI Instructions

The ATO25D1GA supports Quad SPI operation when using the “Read from page buffer x4” command. This instruction allows data to be transferred to or from the device six to seven times the rate of ordinary Serial Flash. The Quad Read instruction offers a significant improvement in continuous and random access transfer rates allowing fast code-shadowing to RAM or execution directly from the SPI bus (XIP). When using Quad SPI instruction the SI and SO pins become bidirectional SIO0 and SIO1 and the WP# and HOLD# pins become SIO2 and SIO3 respectively. Quad SPI instructions require the Quad Enable bit (QE) in Status Register to be set.

7.3 Hold condition

The Hold (HOLD#) signal is used to pause any serial communications with the device without resetting the clocking sequence. However, taking this signal Low does not terminate any Write Status Register, Program or Erase cycle that is currently in progress.

To enter the Hold condition, the device must be selected, with Chip Select (CS#) Low.

The Hold condition starts on the falling edge of the Hold (HOLD#) signal, provided that this coincides with Serial Clock (SCLK) being Low (as shown in *Figure 7*).

The Hold condition ends on the rising edge of the Hold (HOLD#) signal, provided that this coincides with Serial Clock (SCLK) being Low.

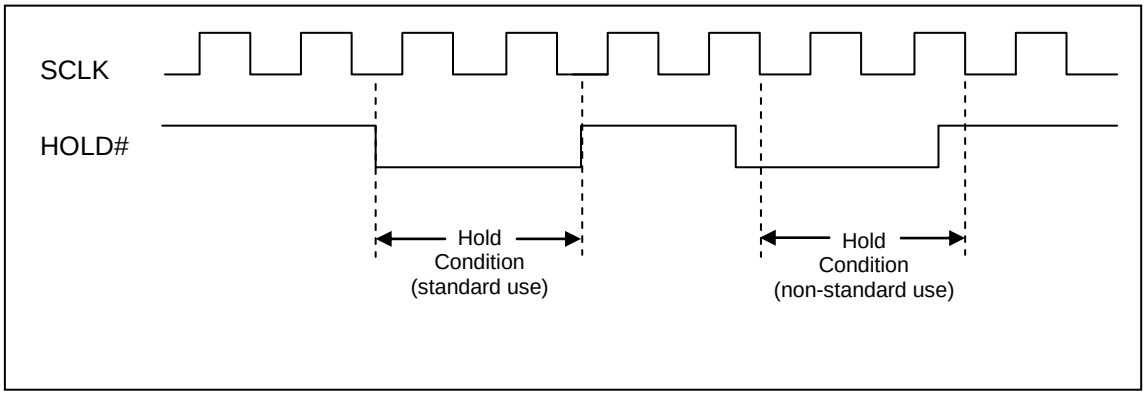
If the falling edge does not coincide with Serial Clock (SCLK) being Low, the Hold condition starts after Serial Clock (SCLK) next goes Low. Similarly, if the rising edge does not coincide with Serial Clock (SCLK) being Low, the Hold condition ends after Serial Clock (SCLK) next goes Low. (This is shown in *Figure 7*).

During the Hold condition, the Serial Data Output (SO) is high impedance, and Serial Data Input (SI) and Serial Clock (SCLK) are Don't Care.

Normally, the device is kept selected, with Chip Select (CS#) driven Low, for the whole duration of the Hold condition. This is to ensure that the state of the internal logic remains unchanged from the moment of entering the Hold condition.

If Chip Select (CS#) goes High while the device is in the Hold condition, this has the effect of resetting the internal logic of the device. To restart communication with the device, it is necessary to drive Hold (HOLD#) High, and then to drive Chip Select (CS#) Low. This prevents the device from going back to the Hold condition.

Figure 7. Hold condition activation



8 Instructions

All instructions, addresses and data are shifted in and out of the device, most significant bit first. Serial Data Input (SI) is sampled on the first rising edge of Serial Clock (SCLK) after Chip Select (CS#) is driven Low. Then, the one-byte instruction code must be shifted in to the device, most significant bit first, on Serial Data input (SI), each bit being latched on the rising edges of Serial Clock (SCLK).

The instruction set is listed in *Table 3*.

All attempts to access the memory array during a Write Status Register cycle, Program cycle or Erase cycle are ignored, and the internal Write Status Register cycle, Program cycle or Erase cycle continues unaffected.

Table 3. Instruction set

Command	Op Code	Address Bytes	Dummy Bytes	Data Bytes	Note
BLOCK ERASE	D8h	3	0	0	
GET FEATURE	0Fh	1	0	1	Refer to Feature Register
SET FEATURE	1Fh	1	0	1	
WRITE DISABLE	04h	0	0	0	
WRITE ENABLE	06h	0	0	0	
PROGRAM LOAD	02h	2	0	1 to 2112	
PROGRAM LOAD x4	32h	2	0	1 to 2112	Command/Address is 1 bit, data is 4 bit
PROGRAM LOAD RANDOM DATA	84h	2	0	1 to 2112	
PROGRAM LOAD RANDOM DATA x4	34h	2	0	1 to 2112	Command/Address is 1 bit, data is 4 bit
PROGRAM EXECUTE	10h	3	0	0	
PAGE READ	13h	3	0	0	
READ FROM PAGE BUFFER	03h, 0Bh	2	1	1 to 2112	
READ FROM PAGE BUFFER x4	6Bh	2	1	1 to 2112	Command/Address is 1 bit, data is 4 bit
READ ID	9Fh	1	0	2	Address is 00h to get JEDEC ID
RESET	FFh	0	0	0	

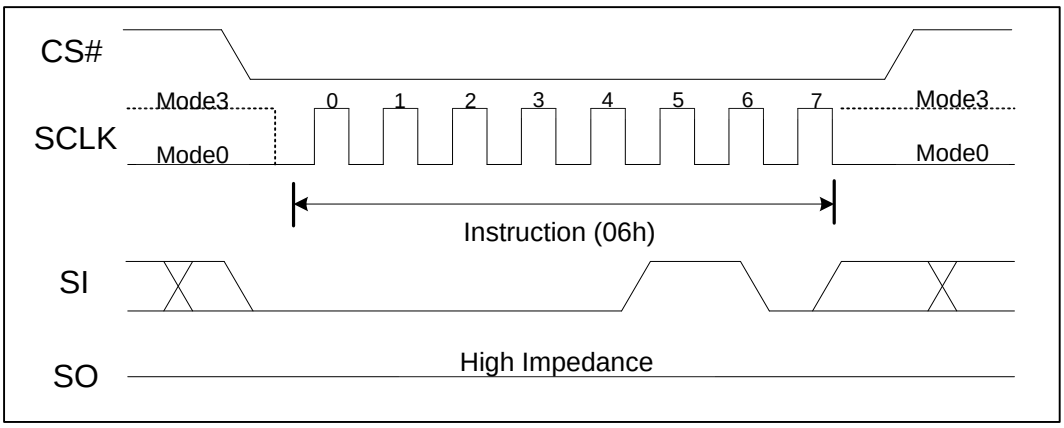
8.1 Write Enable (WREN)

The Write Enable (WREN) instruction (*Figure 8*) sets the Write Enable Latch (WEL) bit.

The Write Enable Latch (WEL) bit must be set prior to every Page Program, Block Erase, and OTP program instruction.

The Write Enable (WREN) instruction is entered by driving Chip Select (CS#) Low, sending the instruction code, and then driving Chip Select (CS#) High.

Figure 8. Write Enable (WREN) instruction sequence



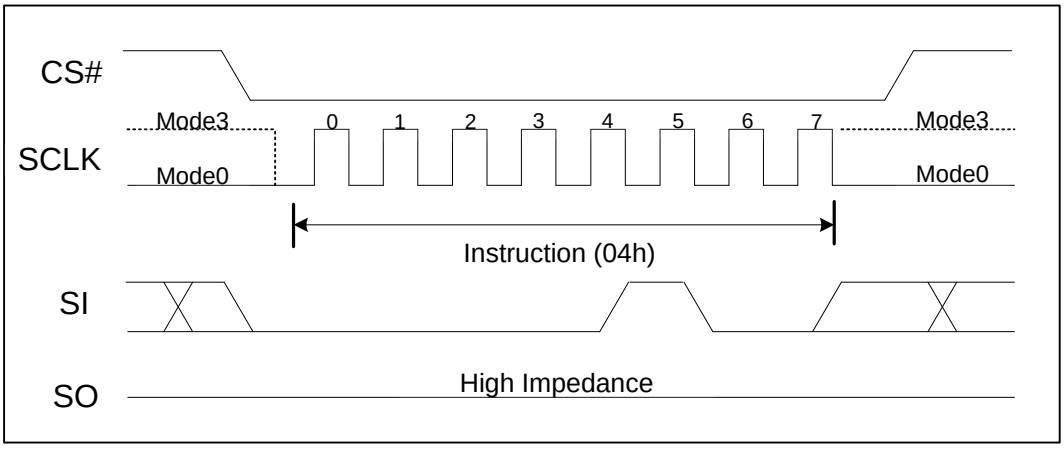
8.2 Write Disable (WRDI)

The Write Disable (WRDI) instruction (*Figure 9*) resets the Write Enable Latch (WEL) bit.

The Write Disable (WRDI) instruction is entered by driving Chip Select (CS#) Low, sending the instruction code, and then driving Chip Select (CS#) High. The Write Enable Latch (WEL) bit is reset under the following conditions:

- Power-up
- Write Disable (WRDI) instruction completion
- OTP program instruction completion
- Page Program (PP) instruction completion
- Block Erase (BE) instruction completion

Figure 9. Write Disable (WRDI) instruction sequence



8.3 Read Identification (RDID)

The READ ID command is used to read the 2 bytes of identifier code programmed into the NAND Flash device. The READ ID command reads a 2-byte table (see below) that includes the Manufacturer ID and the device configuration.

- Manufacturer identification (one byte)
- Device identification (one byte)

Any Read Identification (RDID) instruction while an Erase or Program cycle is in progress is not decoded, and has no effect on the cycle that is in progress.

The instruction sequence is shown in *Figure 10*

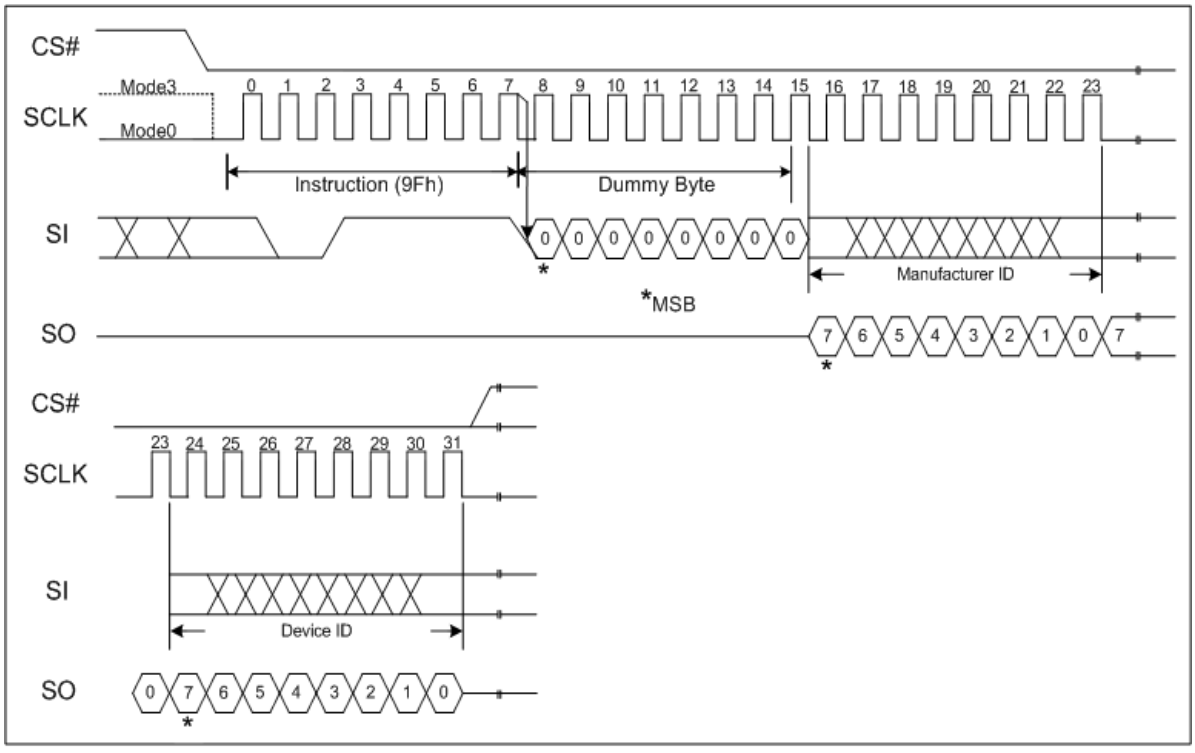
The Read Identification (RDID) instruction is terminated by driving Chip Select (CS#) High at any time during data output.

When Chip Select (CS#) is driven High, the device is put in the Standby Power mode. Once in the Standby Power mode, the device waits to be selected, so that it can receive, decode and execute instructions.

Table 4. Read Identification (RDID) data-out sequence

Instruction	Manufacturer Identification	Device Identification
9Fh	9Bh	12h

Figure 10. Read Identification (RDID) instruction sequence and data-out sequence

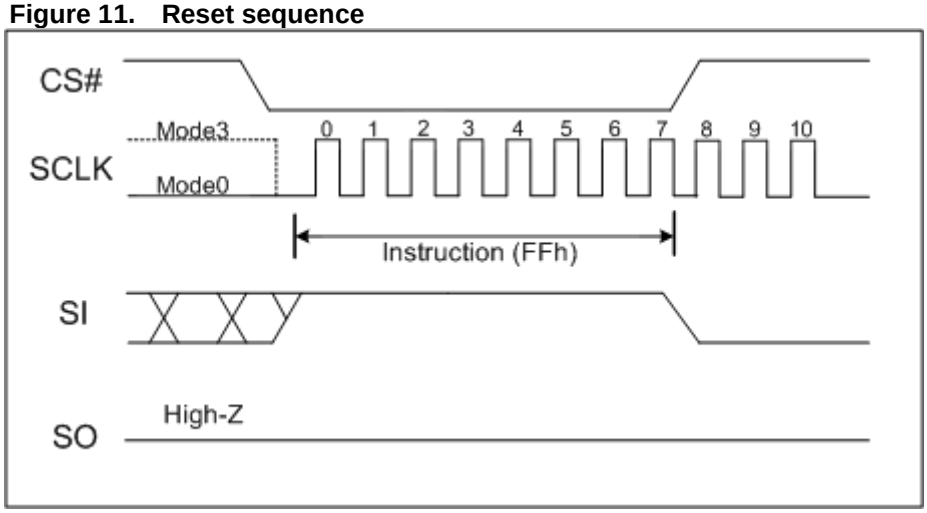


8.4 Software Reset

The Reset operation is used as a system (software) reset that puts the device in normal operating Ready mode.
To reset the ATO25D1GA the host drives CS# low, sends the Reset command(FFH),

A successful command execution will reset the device to SPI stand by read mode, which are their respective default states. A device reset during an active Program and Erase operation aborts the operation, which can cause the data of the targeted address range to be corrupted or lost. Depending on the prior operation, the reset timing may vary. Recovery from a Write operation requires more latency time than recovery from other operations.

Figure 11. Reset sequence



8.5 Feature Operation

The GET FEATURES (0Fh) and SET FEATURES (1Fh) commands are used to alter the device behavior from the default power-on behavior. These commands use a 1-byte feature address to determine which feature is to be read or modified. Features such as OTP and block locking can be enabled or disabled by setting specific bits in feature address A0h and B0h (shown in the following table). The status register is mostly read, except WEL, which is a writable bit with the WRITE ENABLE (06h) command.

Table 5. Status Registers

Register	Address	Data Bits							
		7	6	5	4	3	2	1	0
Block Lock	A0h	BRWD(1)	Reserved	BP2	BP1	BP0	Reserved	Reserved	Reserved
OTP	B0h	OTP Protect	OTP Enable	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved
Status	C0h	Reserved	Reserved	Reserved	Reserved	P_Fail	E_Fail	WEL	OIP

Note: 1. If BRWD is enabled and WP# is LOW, then the block lock register cannot be changed.

8.5.1 OIP bit

The Operation In Progress (OIP) bit indicates whether the memory is busy with a Write Status Register, Program or Erase cycle. When set to 1, such a cycle is in progress, when reset to 0 no such cycle is in progress.

8.5.2 WEL bit

The Write Enable Latch (WEL) bit indicates the status of the internal Write Enable Latch. When set to 1 the internal Write Enable Latch is set, when set to 0 the internal Write Enable Latch is reset and no Write Status Register, Program or Erase instruction is accepted.

8.5.3 BP2, BP1, BP0 bits

The Block Protect (BP2, BP1, BP0) bits define the size of the area to be software protected against Program and Erase instructions. These bits are written with the Set features instruction. When one or both of the Block Protect (BP2, BP1, BP0) bits is set to 1, the relevant memory area becomes protected against Page Program, OTP Program, Block Erase. The Block Protect (BP2, BP1, BP0) bits can be written provided that the Hardware Protected mode has not been set.

8.5.4 P_Fail bit

This bit indicats that a program failure has occurred (P_Fail set to 1). This bit will also be set if the user attempts to program an invalid address or a locked or protected region, including the OTP area. This bit is cleared during the PROGRAM EXECUTE command sequence or a RESET command (P_Fail = 0).

8.5.5 E_Fail bit

This bit indicates that an erase failure has occurred (E_Fail set to 1). This bit will also be set if the user attempts to erase a locked region, or if the ERASE operation fails. This bit is cleared (E_Fail = 0) at the start of the BLOCK ERASE command sequence or the RESET command.

Figure 12. Get Feature Timing

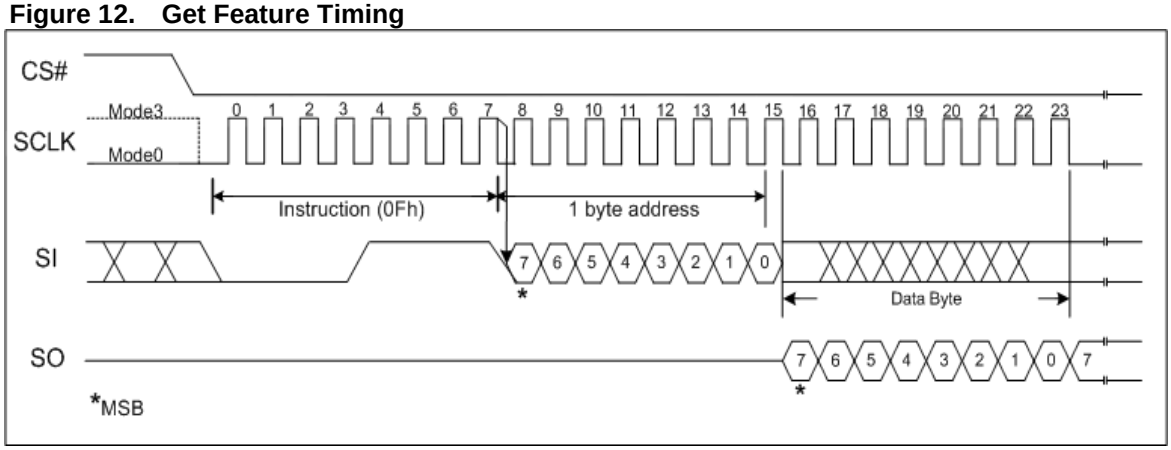
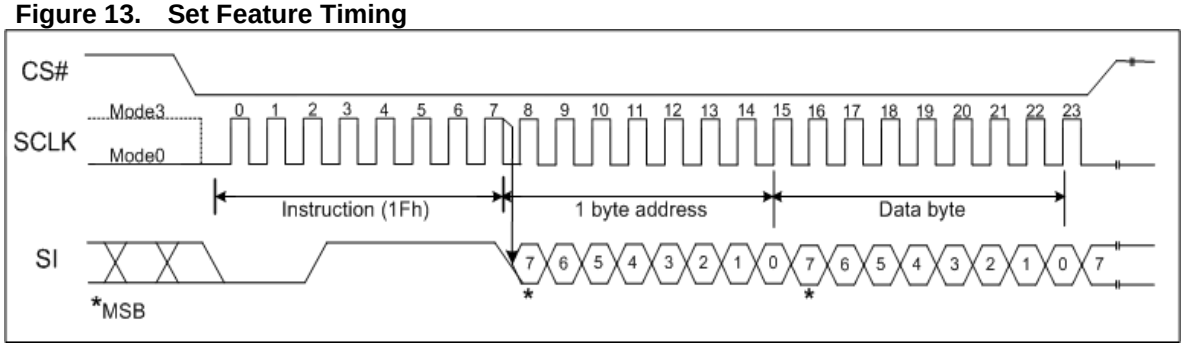


Figure 13. Set Feature Timing



8.6 Page Read(13h)

The PAGE READ (13h) command transfers the data from the NAND Flash array to the page buffer. The command sequence is follows:

- **13h (PAGE READ to page buffer)**
- **0Fh (GET FEATURES command to read the status)**
- **0Bh or 03h (Random data read)**

The PAGE READ command requires a 24-bit address consisting of 8 dummy bits followed by a 16-bit block/page address. After the block/page addresses are registered, the device starts the transfer from the main array to the page buffer, and is busy for tRD time. During this time, the GET FEATURE (0Fh) command can be issued to monitor the status of the operation. Following a status of successful completion, the RANDOM DATA READ (03h or 0Bh) command must be issued in order to read the data out of the page buffer. The RANDOM DATA READ command requires a 16 -bit column address for the starting byte address. The starting byte address can be 0 to 2111, but after the end of the page buffer is reached, the data does not wrap around and SO goes to a High-Z state. Refer to *Figure 14* and *Figure 15* to view the entire READ operation.

Figure 14. Page Read(13h) instruction Timing

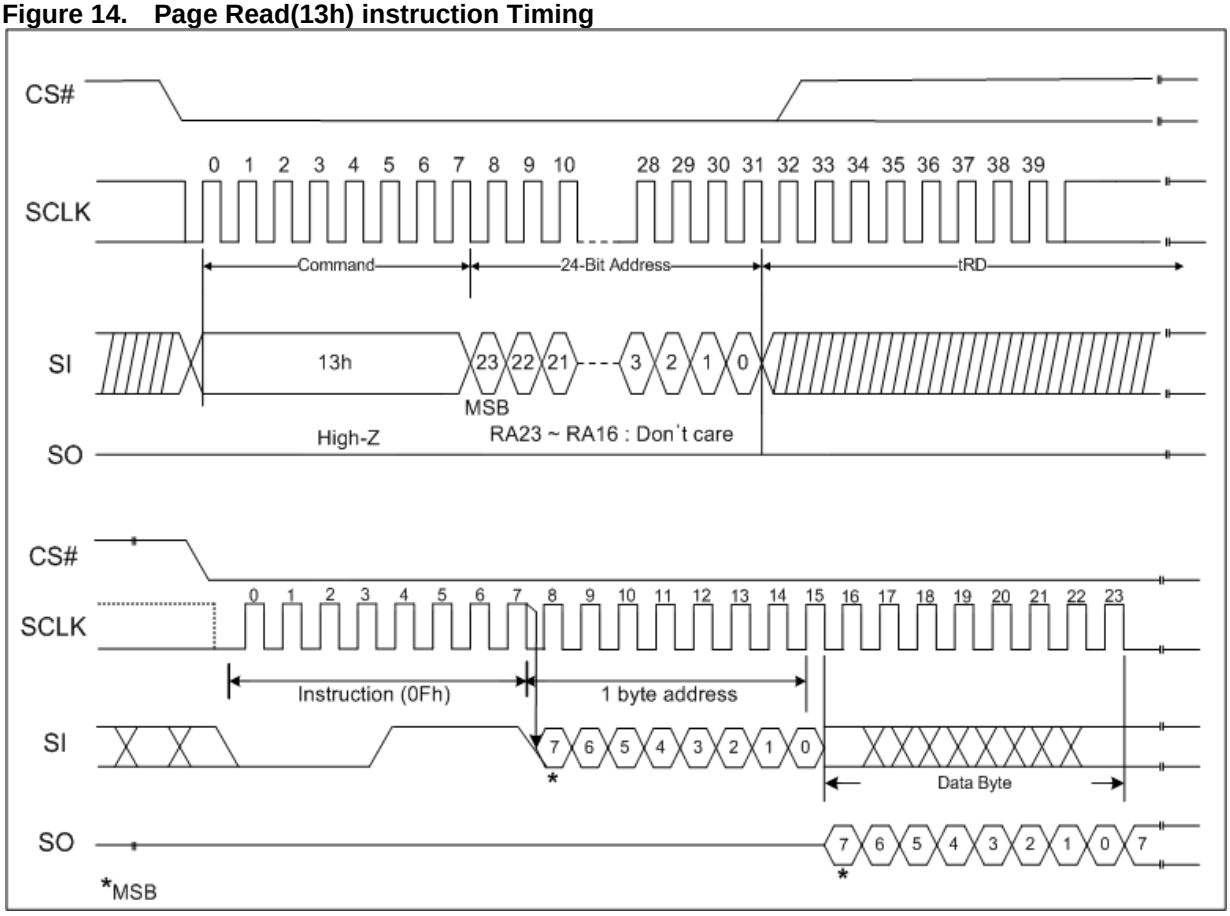


Figure 15. Read From Page Buffer(03h/0Bh) instruction Timing

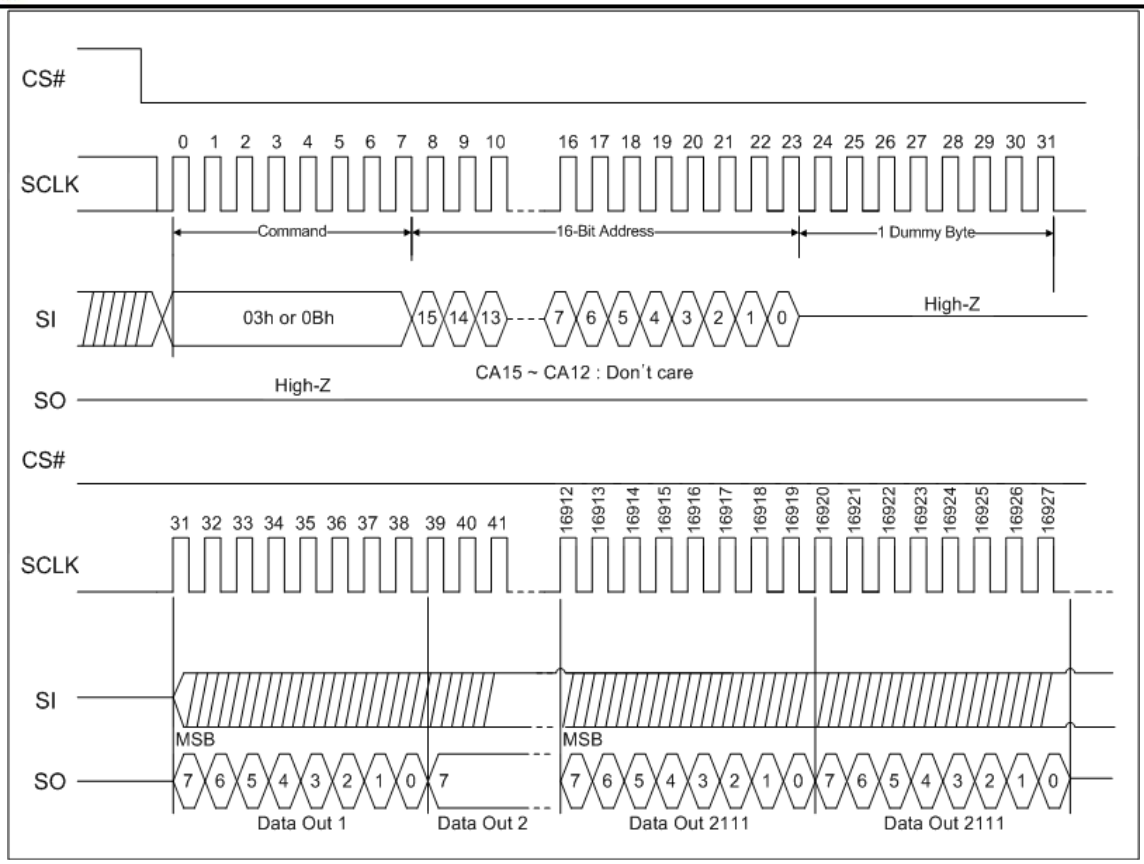
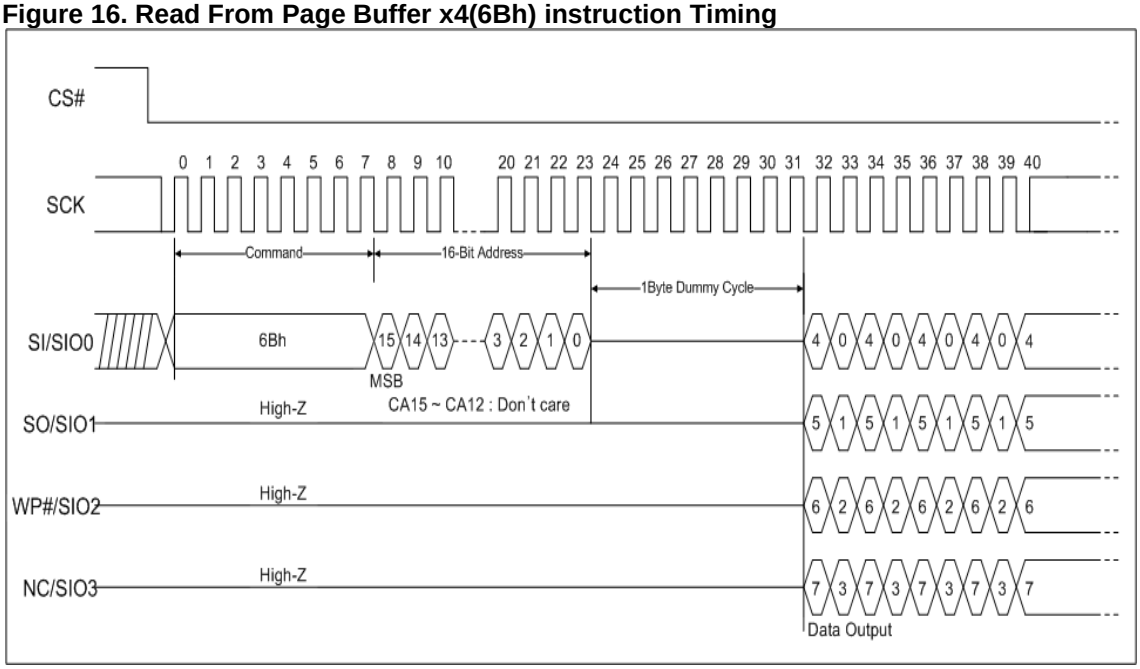


Figure 16. Read From Page Buffer x4(6Bh) instruction Timing



8.7 Page Program

The PAGE PROGRAM operation sequence programs 1 byte to 2112 bytes of data within a page. The page program sequence is as follows:

- **06h (WRITE ENABLE)**
- **02h/32h (PROGRAM LOAD)**
- **10h (PROGRAM EXECUTE)**
- **0Fh (GET FEATURE command to read the status)**

Prior to performing the PROGRAM LOAD operation, a WRITE ENABLE (06h) command must be issued. As with any command that changes the memory contents, the WRITE ENABLE must be executed in order to set the WEL bit. If this command is not issued, then the rest of the program sequence is ignored. WRITE ENABLE must be followed by a PROGRAM LOAD (02h/32h) command. PROGRAM LOAD consists of an 8-bit Op code, followed by a 16-bit column address, then the data bytes to be programmed. The data bytes are loaded into a page buffer that is 2112 bytes long. If more than 2112 bytes are loaded, then those additional bytes are ignored by the page buffer. The command sequence ends when CS goes from LOW to HIGH. *Figure 16* shows the PROGRAM LOAD operation.
After the data is loaded, a PROGRAM EXECUTE (10h) command must be issued to initiate the transfer of data from the page buffer to the main array. PROGRAM EXECUTE consists of an 8-bit Op code, followed by a 24-bit address. After the page/block address is registered, the memory device starts the transfer from the page buffer to the main array, and is busy for tPROG time. During this busy time, the status register can be polled to monitor the status of the operation (refer to the Status Register section). When the operation completes successfully, the next series of data can be loaded with the PROGRAM LOAD command. Only the Get Feature and Reset command are valid while programming is in progress. The number of consecutive partial page programming operation within the same page without an intervening erase operation must not exceed 4 for main array and 4 for spare array. And the device is limited to one partial page program per each area of main or spare array.
(Refer to *Figure 5*)

Figure 17. Program Load(02h) instruction sequence

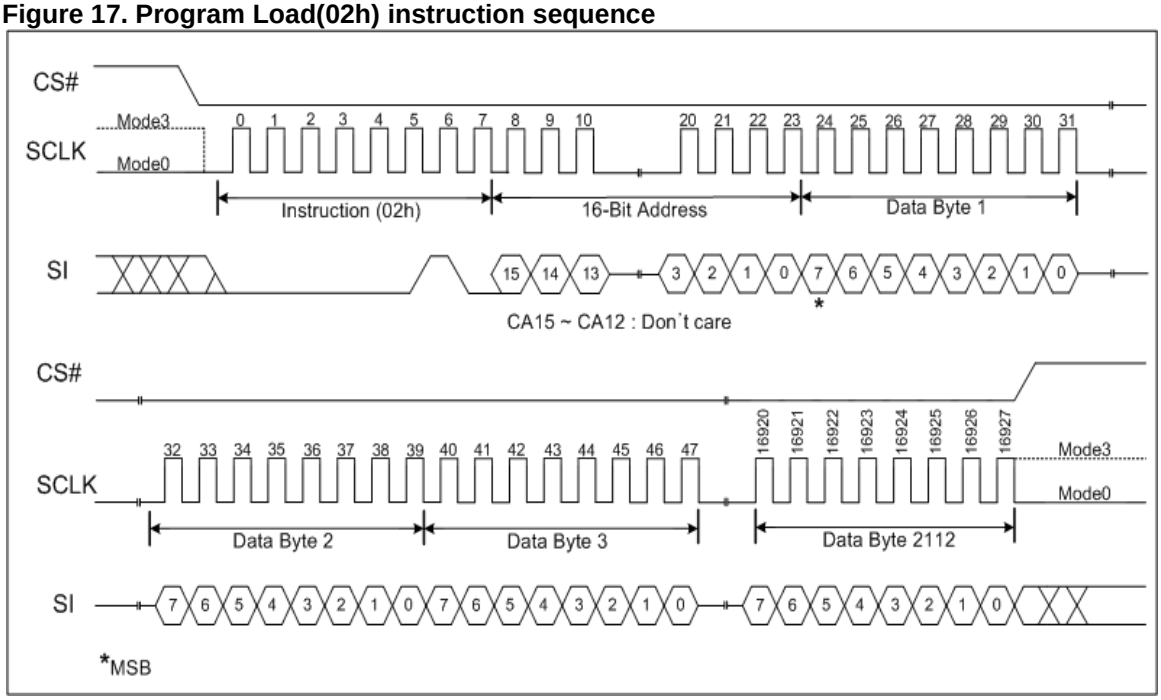


Figure 18. Program Load x4(32h) instruction sequence

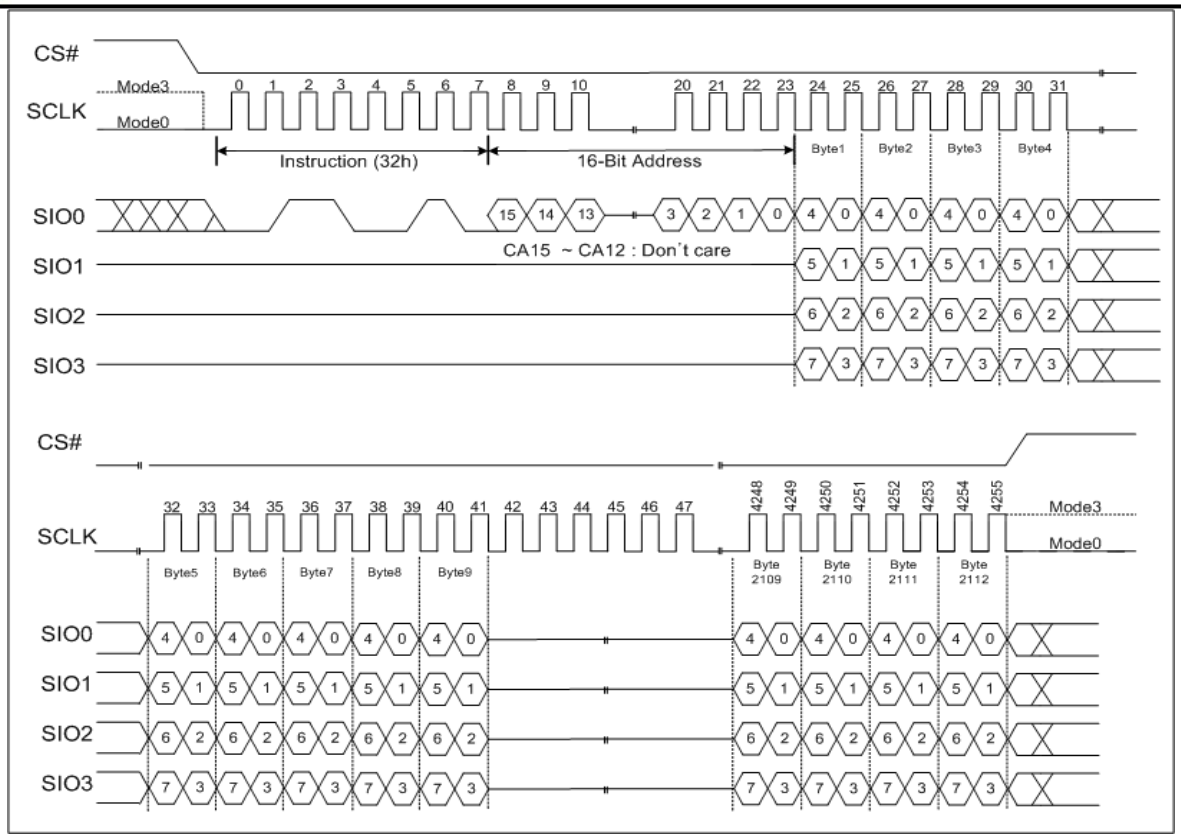
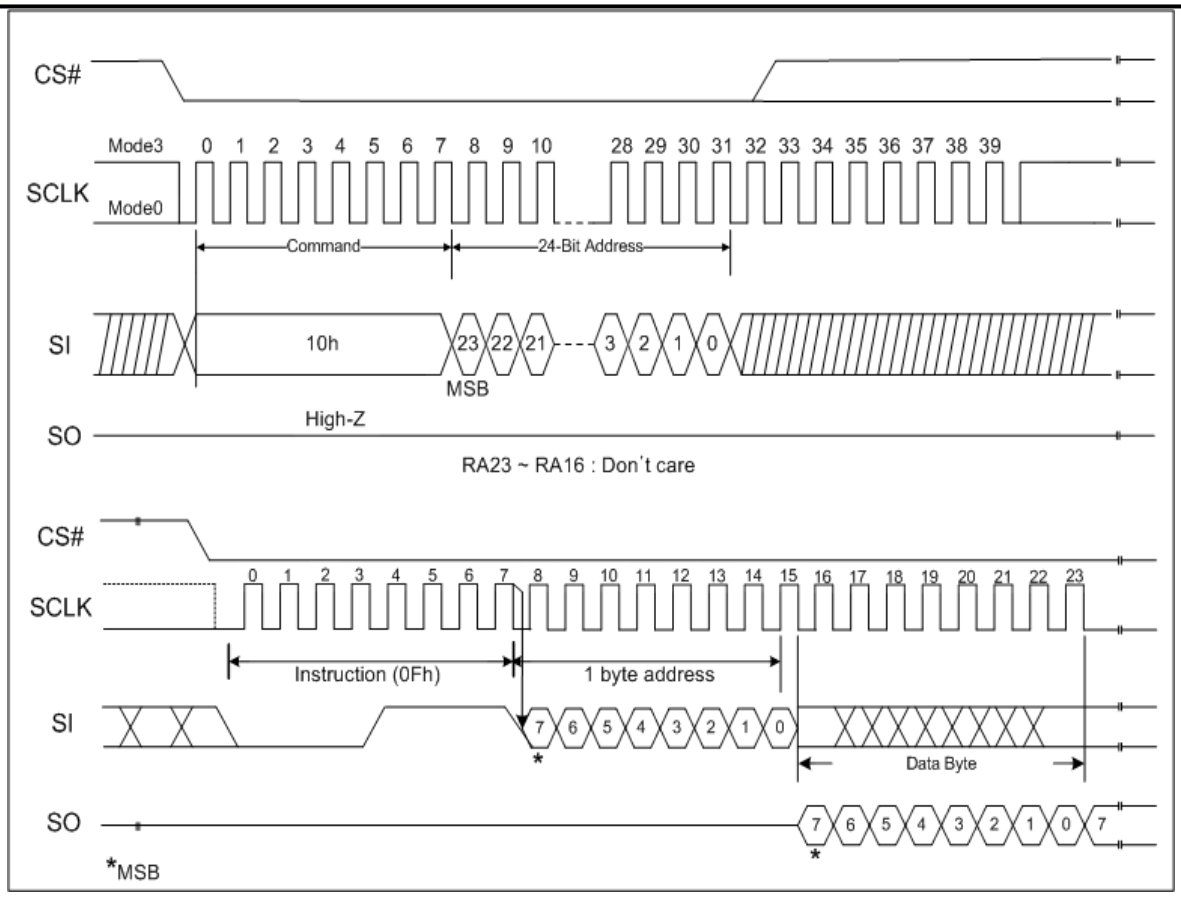


Figure 19. Program Execute(10h) instruction sequence



8.8 Random Data Program

The RANDOM DATA PROGRAM sequence programs or replaces data in a page with existing data. The random data program sequence is as follows:

- **06h (WRITE ENABLE)**
- **84h/34h (PROGRAM LOAD RANDOM DATA)**
- **10h (PROGRAM EXECUTE)**
- **0Fh (GET FEATURE command to read the status)**

Prior to performing a PROGRAM LOAD RANDOM DATA operation, a WRITE ENABLE(06h) command must be issued to change the contents of the memory array. Following a WRITE ENABLE (06) command, a PROGRAM LOAD RANDOM DATA (84h/34h) command must be issued. This command consists of an 8-bit Op code, a 16-bit column address. New data is loaded in the column address provided with the 12 bits. If the random data is not sequential, then another PROGRAM LOAD RANDOM DATA (84h/34h) command must be issued with a new column address. And the device is limited to one program data load per each a fixed length of 8 byte section within a 2112 byte(page).

After the data is loaded, a PROGRAM EXECUTE(10h) command can be issued to start the programming operation.

Figure 20. Program Load Random Data(84h) instruction sequence

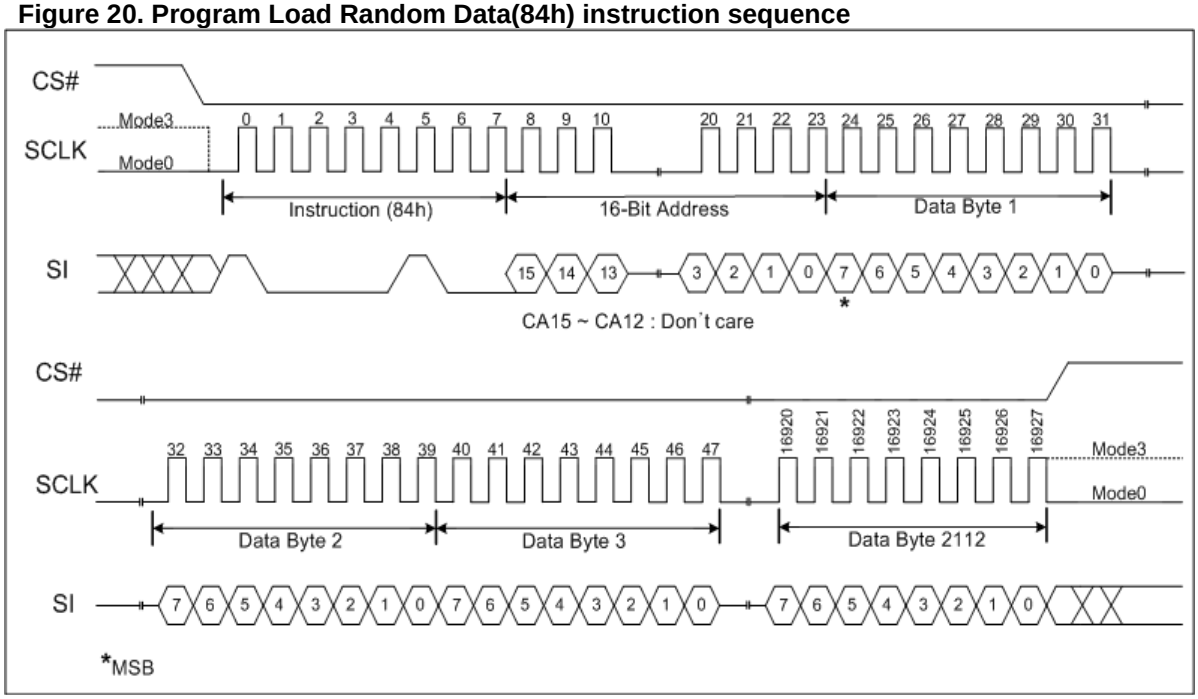
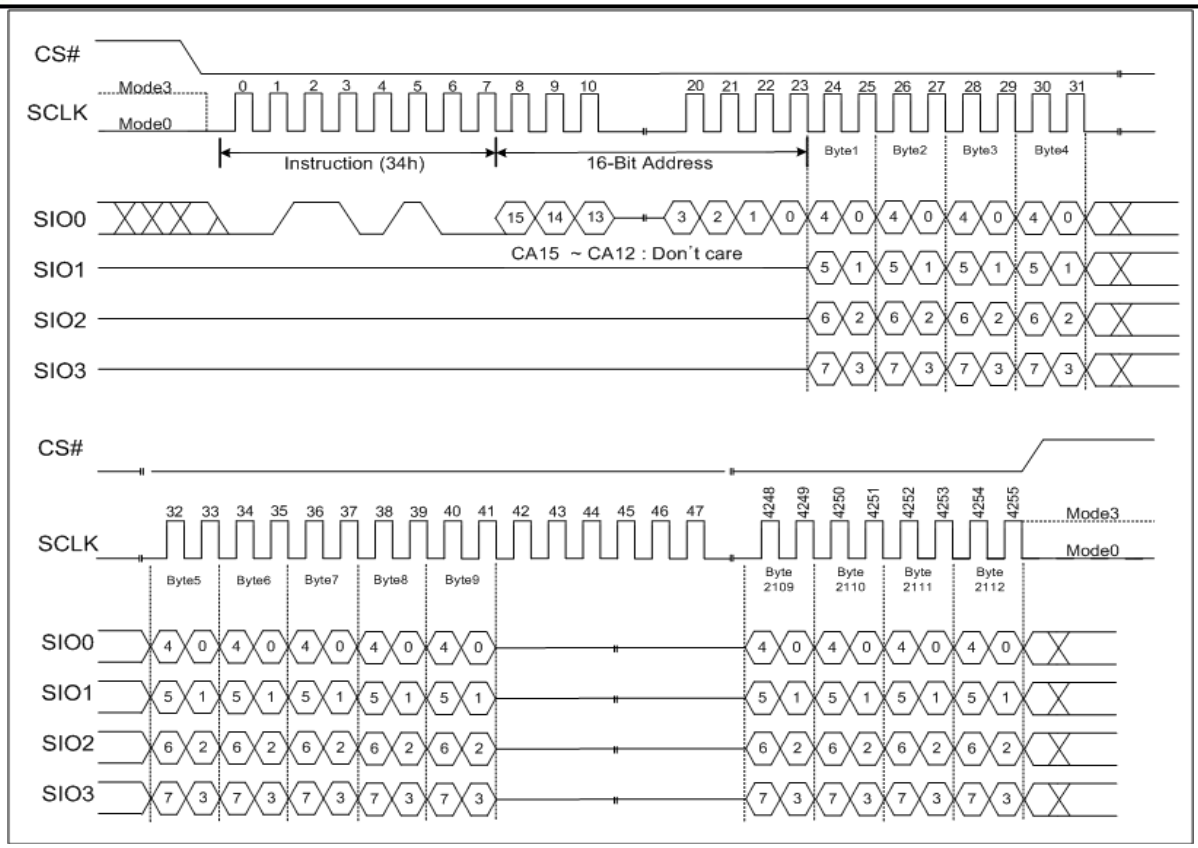


Figure 21. Program Load Random Data x4(34h) instruction sequence



8.9 Copy Back Program

The Copy Back Program command sequence programs or replaces data in a page with existing data. The Copy Back Program command sequence is as follows:

- **13h (PAGE READ to page buffer)**
- **06h (WRITE ENABLE)**
- **10h (PROGRAM EXECUTE)**
- **0Fh (GET FEATURE command to read the status)**

Prior to performing an internal data move operation, the target page content must be read into the page buffer. This is done by issuing a PAGE READ (13h) command. The PAGE READ command must be followed with a WRITE ENABLE (06h) command in order to change the contents of memory array. After the WRITE ENABLE command is issued, a PROGRAM EXECUTE (10h) command can be issued to start the programming operation.

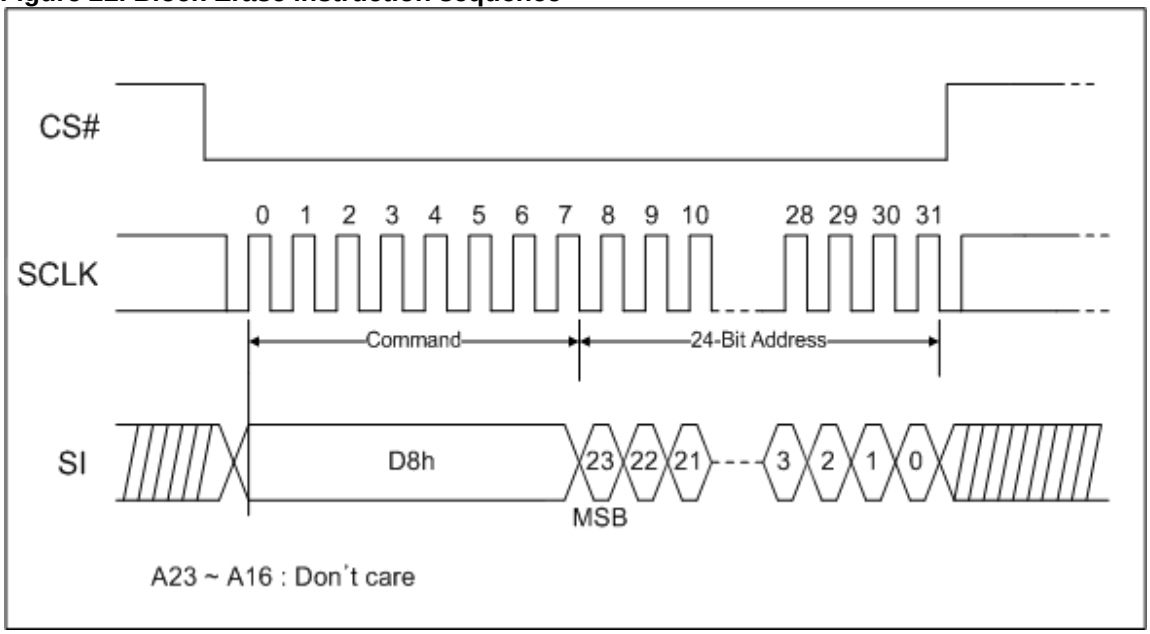
8.10 Block Erase (D8h)

The BLOCK ERASE (D8h) command is used to erase at the block level. The blocks are organized as 64 pages per block, 2112 bytes per page (2048 + 64 bytes). Each block is 132 Kbytes. The BLOCK ERASE command (D8h) operates on one block at a time. The command sequence for the BLOCK ERASE operation is as follows:

- **06h (WRITE ENBALE command)**
- **D8h (BLOCK ERASE command)**
- **0Fh (GET FEATURES command to read the status register)**

Prior to performing the BLOCK ERASE operation, a WRITE ENABLE (06h) command must be issued. As with any command that changes the memory contents, the WRITE ENABLE command must be executed in order to set the WEL bit. If the WRITE ENABLE command is not issued, then the rest of the erase sequence is ignored. A WRITE ENABLE command must be followed by a BLOCK ERASE (D8h) command. This command requires a 24-bit address consisting of 8 dummy bits followed by an 16-bit row address. After the row address is registered, the control logic automatically controls timing and erase-verify operations. The device is busy for tERS time during the BLOCK ERASE operation. The GET FEATURES (0Fh) command can be used to monitor the status of the operation. Only the Get Feature and Reset command are valid while erasing is in progress.

Figure 22. Block Erase instruction sequence



9 Error Management

This NAND Flash device is specified to have the minimum number of valid blocks (NVB) of the total available blocks per die shown in the table below. This means the devices may have blocks that are invalid when shipped from the factory. An invalid block is one that contains at least one page that has more bad bits than can be corrected by the minimum required ECC. Additional bad blocks may develop with use. However, the total number of available blocks will not fall below NVB during the endurance life of the product.

Although NAND Flash memory devices may contain bad blocks, they can be used reliably in systems that provide bad-block management and error-correction algorithms. This ensures data integrity. Internal circuitry isolates each block from other blocks, so the presence of a bad block does not affect the operation of the rest of the NAND Flash array.

NAND Flash devices are shipped from the factory erased. The factory identifies invalid blocks before shipping by attempting to program the bad-block mark into every location in the first page of each invalid block. It may not be possible to program every location in an invalid block with the bad-block mark. However, the first spare area location in each bad block is guaranteed to contain the bad-block mark. See the following table for the bad-block mark.

System software should initially check the first spare area location for non-FFh data on the first page of each block prior to performing any program or erase operations on the NAND Flash device. A bad-block table can then be created, enabling system software to map around these areas. Factory testing is performed under worst-case conditions. Because invalid blocks may be marginal, it may not be possible to recover the bad-block marking if the block is erased. The 1st block, which is placed on 00h block address, is guaranteed to be a valid block up to 1K program/erase cycles.

Table 6. Error Management Details

Description	Requirement
Minimum number of valid blocks (Nvb)	1004
Total available blocks per die	1024
First spare area location	Byte 2048
Bad block mark	00h

10 Power-up and Power-down

At Power-up and Power-down, the device must not be selected (that is Chip Select (S) must follow the voltage applied on V_{CC}) until V_{CC} reaches the correct value:

- V_{CC}(min) at Power-up, and then for a further delay of t_{VSL}
- V_{SS} at Power-down

To avoid data corruption and inadvertent write operations during Power-up, a Power On Reset (POR) circuit is included. The logic inside the device is held reset while V_{CC} is less than the POR threshold value, V_{WI} – all operations are disabled, and the device does not respond to any instruction.

Moreover, the device ignores all Write Enable (WREN), Page Program, Block Erase (BE), OTP Program instructions until a time delay of t_{PUW} has elapsed after the moment that V_{CC} rises above the V_{WI} threshold. However, the correct operation of the device is not guaranteed if, by this time, V_{CC} is still below V_{CC}(min). No Write Status Register, Program or Erase instructions should be sent until the later of:

- t_{PUW} after V_{CC} passed the V_{WI} threshold
- t_{VSL} after V_{CC} passed the V_{CC}(min) level

These values are specified in *Table 8*.

If the delay, t_{VSL}, has elapsed, after V_{CC} has risen above V_{CC}(min), the device can be selected for READ instructions even if the t_{PUW} delay is not yet fully elapsed. At Power-up, the device is in the following state:

- The device is in the Standby mode (not the Deep Power-down mode).
- The Write Enable Latch (WEL) bit is reset.
- The Operation In Progress (OIP) bit is reset.

Normal precautions must be taken for supply rail decoupling, to stabilize the V_{CC} feed. Each device in a system should have the V_{CC} rail decoupled by a suitable capacitor close to the package pins. (Generally, this capacitor is of the order of 100 nF).

At Power-down, when V_{CC} drops from the operating voltage, to below the Power On Reset (POR) threshold value, V_{WI}, all operations are disabled and the device does not respond to any instruction. (The designer needs to be aware that if a Power-down occurs while a Write, Program or Erase cycle is in progress, some data corruption can result.)

Figure 23. Power-up timing

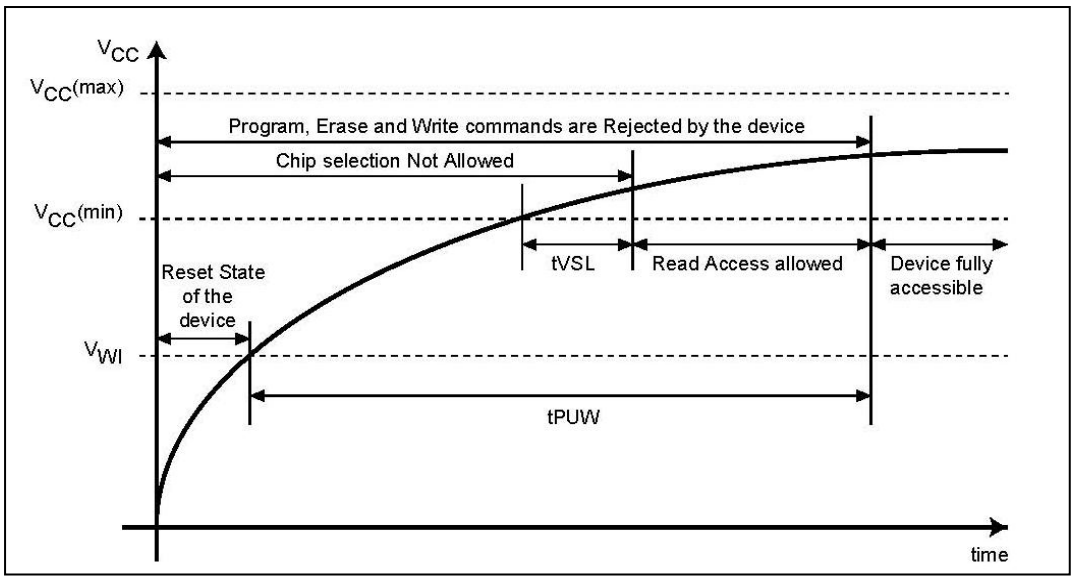


Table 7. Power-up timing and V_{WI} threshold

Symbol	Parameter	Min.	Max.	Unit
t_{VSL}(1)	VCC(min) to S low	10		µs
t_{PUW}(1)	Time delay to Write instruction	1	10	ms
V_{WI}(1)	Write Inhibit voltage	1	2	V

1. These parameters are characterized only.

11 Initial delivery state

The device is delivered with the memory array erased: all bits are set to 1 (each byte contains FFh). The Status Register contains 00h (all Status Register bits are 0).

12 Maximum rating

Stressing the device above the rating listed in the absolute maximum ratings table may cause permanent damage to the device. These are stress ratings only and operation of the device at these or any other conditions above those indicated in the operating sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability. Refer also to relevant quality documents.

Table 8. Absolute maximum ratings

Symbol	Parameter	Min.	Max.	Unit
T_{STG}	Storage temperature	–65	150	°C
T_{LEAD}	Lead temperature during soldering		see (0)	°C
V_{IO}	Input and output voltage (with respect to ground)	–0.6	V_{CC} + 0.4	V
V_{CC}	Supply voltage	–0.6	4.6	V
V_{ESD}	Electrostatic discharge voltage (Human Body model) (1)	–2000	2000	V

0. Compliant with JEDEC Std J-STD-020C (for small body, Sn-Pb or Pb assembly)
1. JEDEC Std JESD22-A114A (C1=100 pF, R1=1500 Ω, R2=500 Ω)

13 DC and AC parameters

This section summarizes the operating and measurement conditions, and the DC and AC characteristics of the device. The parameters in the DC and AC Characteristic tables that follow are derived from tests performed under the Measurement Conditions summarized in the relevant tables. Designers should check that the operating conditions in their circuit match the measurement conditions when relying on the quoted parameters.

Table 9. Operating conditions

Symbol	Parameter		Min.	Max.	Unit
V_{CC}	Supply voltage		2.7	3.6	V
T_A	Ambient operating temperature	E(Extended)	-30	85	°C
		C(Commercial)	0	70	°C
		I (Industrial)	-40	85	°C

Table 10. Data retention and endurance

Parameter	Condition	Min.	Max.	Unit
Erase/Program cycles			100,000	cycles per sector
Data Retention			10	years

Table 11. AC measurement conditions

Symbol	Parameter	Min.	Max.	Unit
C_L	Load capacitance	30(15pF/133MHz)		pF
	Input rise and fall times		5	ns
	Input pulse voltages	0.2V_{CC} to 0.8V_{CC}		V
	Input timing reference voltages	0.3V_{CC} to 0.7V_{CC}		V
	Output timing reference voltages	V_{CC} / 2		V

1. Output Hi-Z is defined as the point where data out is no longer driven.

Figure 24. AC measurement I/O waveform

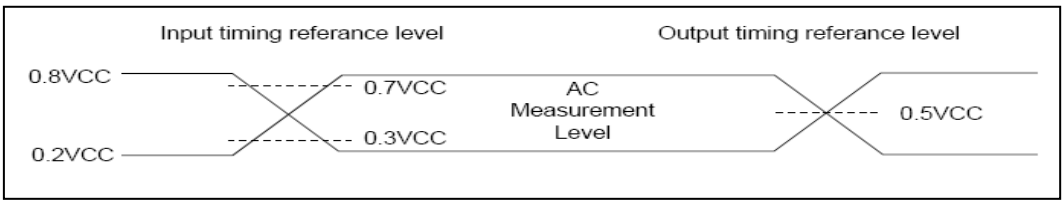


Table 12. Capacitance[1]

Symbol	Parameter	Test condition	Min.	Max.	Unit
C_{OUT}	Output capacitance (Q)	V_{OUT} = 0 V		8	pF
C_{IN}	Input capacitance (other pins)	V_{IN} = 0 V		6	pF

1. Sampled only, not 100% tested, at T_A = 25 °C and a frequency of 20 MHz.

Table 13. DC characteristics

Symbol	Parameter	Test condition (in addition to those in *Table9*)	Min.	Max.	Unit
I_{LI}	Input leakage current			± 2	µA
I_{LO}	Output leakage current			± 2	µA
I_{CC1}	Standby current	CS# = V_{CC}, V_{IN} = V_{SS} or V_{CC}	1	50	µA
I_{CC2}	Deep Power-down current	CS# = V_{CC}, V_{IN} = V_{SS} or V_{CC}	1	15	µA
I_{CC3}	Operating current (READ)	SCLK = 0.1V_{CC} / 0.9.V_{CC} at 104 MHz, Q = open	10	20	mA
		SCLK = 0.1V_{CC} / 0.9.V_{CC} at 33 MHz, Q = open	8	12	mA
I_{CC4}	Operating current (Program)	CS# = V_{CC}	10	20	mA
I_{CC5}	Operating current (Block Erase)	CS# = V_{CC}	10	20	mA
V_{IL}	Input low voltage		-0.5	0.2xV_{CC}	V
V_{IH}	Input high voltage		0.8xV_{CC}	Vcc + 0.4	V
V_{OL}	Output low voltage	I_{OL} = 1.6mA		0.2	V
V_{OH}	Output high voltage	I_{OH} = –100 µA	V_{CC} – 0.2		V

Table 14. AC characteristics (104 MHz operation)

Test conditions specified in *Table9* and *Table11*						
Symbol	**Alt.**	**Parameter**	**Min.**	**Typ.(1)**	**Max.**	**Unit**
f_Q	fQ	Clock frequency for the following instructions: Read, Page Program, Block Erase, WREN, WRDI, RDID, Get Feature, Set Feature	D.C.		104	MHz
tRD	tR	Page Read time (cell array to page buffer)			25	us
t_{CH}(2)	tCLH	Clock High time	4.5			ns
t_{CL}(2)	tCLL	Clock Low time	4.5			ns
t_{CLCH}(3)		Clock Rise time(4) (peak to peak)	0.1			V/ns
t_{CHCL}(3)		Clock Fall time(3) (peak to peak)	0.1			V/ns
t_{SLCH}	tCSS	CS# active setup time (relative to C)	5			ns
t_{CHSL}		CS# not active hold time (relative to C)	7			ns
t_{DVCH}	tDSU	Data In setup time	3			ns
t_{CHDX}	tDH	Data In hold time	5			ns
t_{CHSH}		CS# active hold time (relative to C)	5			ns
t_{SHCH}		CS# not active setup time (relative to C)	5			ns
t_{SHSL}	tCSH	CS# deselect time	30			ns
t_{SHQZ}(3)	tDIS	Output disable time			8	ns
t_{CLQV}	tV	Clock Low to Output Valid(30pF)			8	ns
t_{CLQV2}	tV2	Clock Low to Output Valid(15pF)			6	ns
t_{CLQX}	tHO	Output hold time	0			ns
t_{HLCH}		HOLD setup time (relative to C)	5			ns
t_{CHHH}		HOLD hold time (relative to C)	5			ns
t_{HHCH}		HOLD setup time (relative to C)	5			ns
t_{CHHL}		HOLD hold time (relative to C)	5			ns
t_{HHQX}(3)	tLZ	HOLD to Output Low-Z			8	ns
t_{HLQZ}(3)	tHZ	HOLD to Output High-Z			8	ns
t_{WHSL}(5)		Write Protect setup time	20			ns
t_{SHWL}(5)		Write Protect hold time	100			ns
t_{DP}(3)		CS# High to Deep Power-down mode			10	µs
t_{PP}		Page Program time		200	500	us
t_{BE}		Block Erase time		2	3	ms
tRST		After Reset, Recovery time for RD/PGM/Erase	Max 5us/10us/500us			µs
NOP		Number of partial programming operation supported.	Main		4	
			Spare		4	

1 Typical values given for TA = 25°C.
2 tCH + tCL must be greater than or equal to 1/ fC
3 Value guaranteed by characterization, not 100% tested in production.
4 Expressed as a slew-rate.

Figure 25. Serial input timing

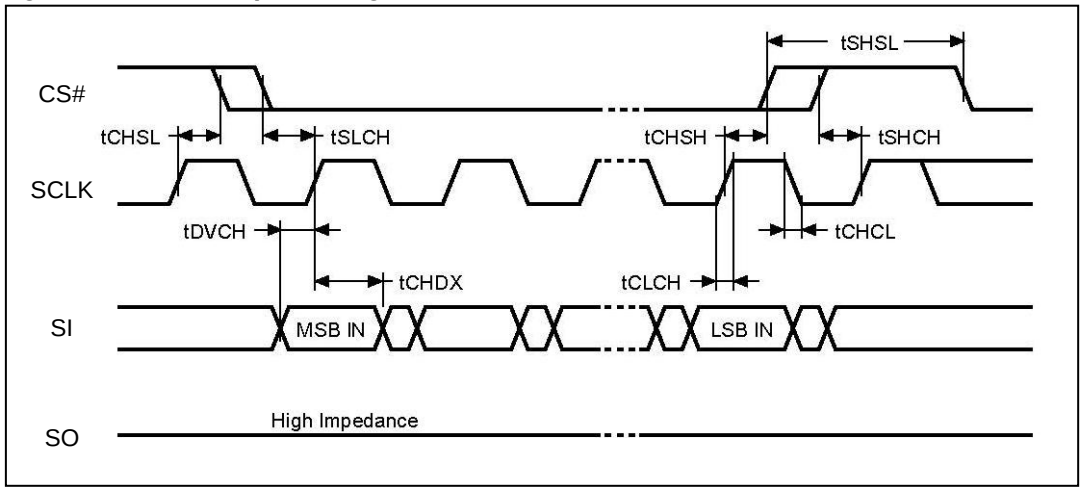


Figure 26. Write protect setup and hold timing

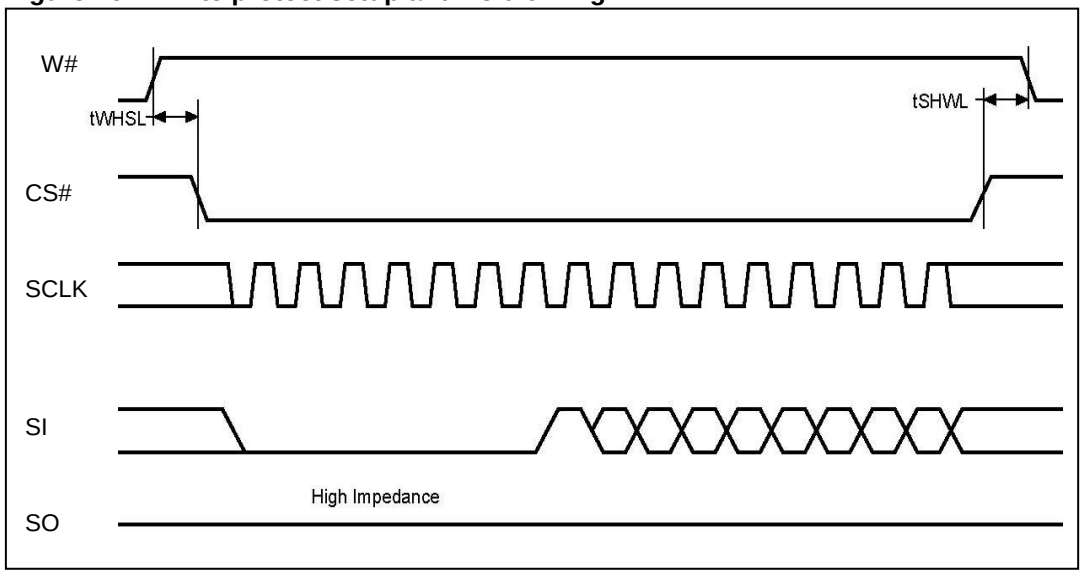


Figure 27. Hold timing

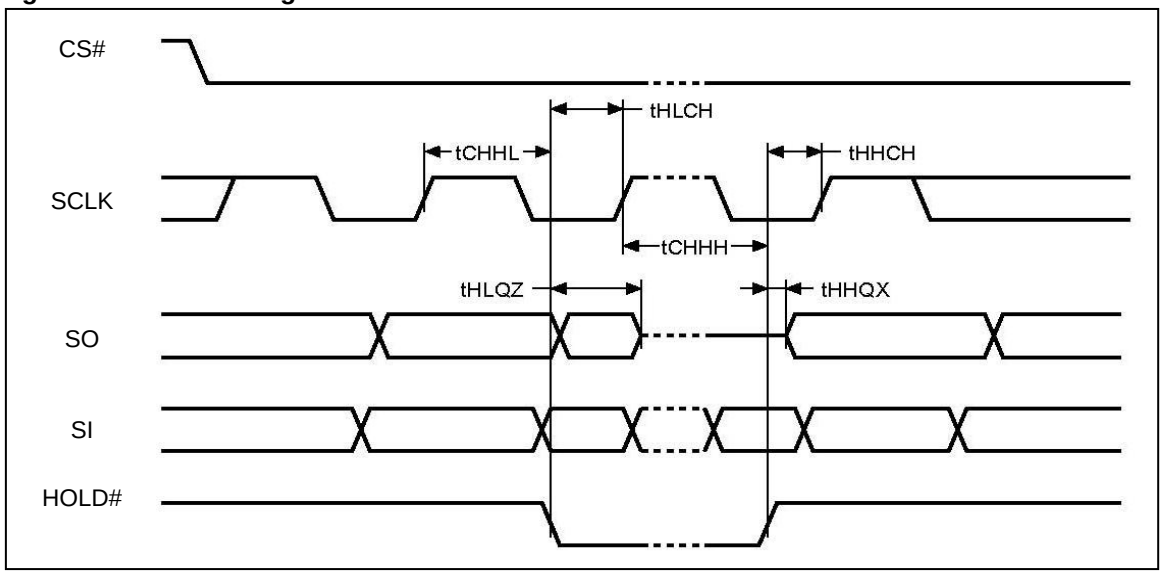
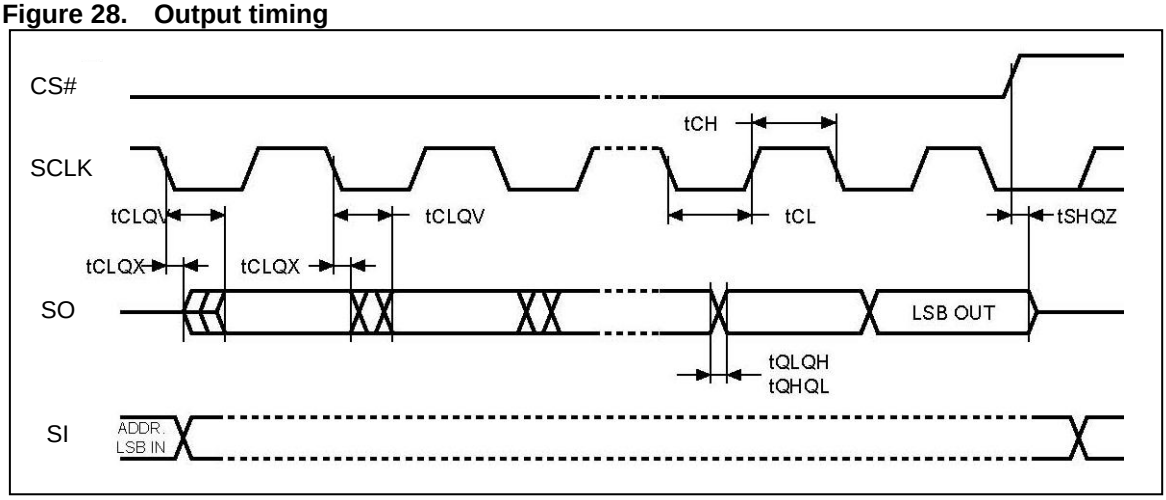


Figure 28. Output timing



14 Package mechanical

Figure 29. 8-Contact 8x6mm WSON

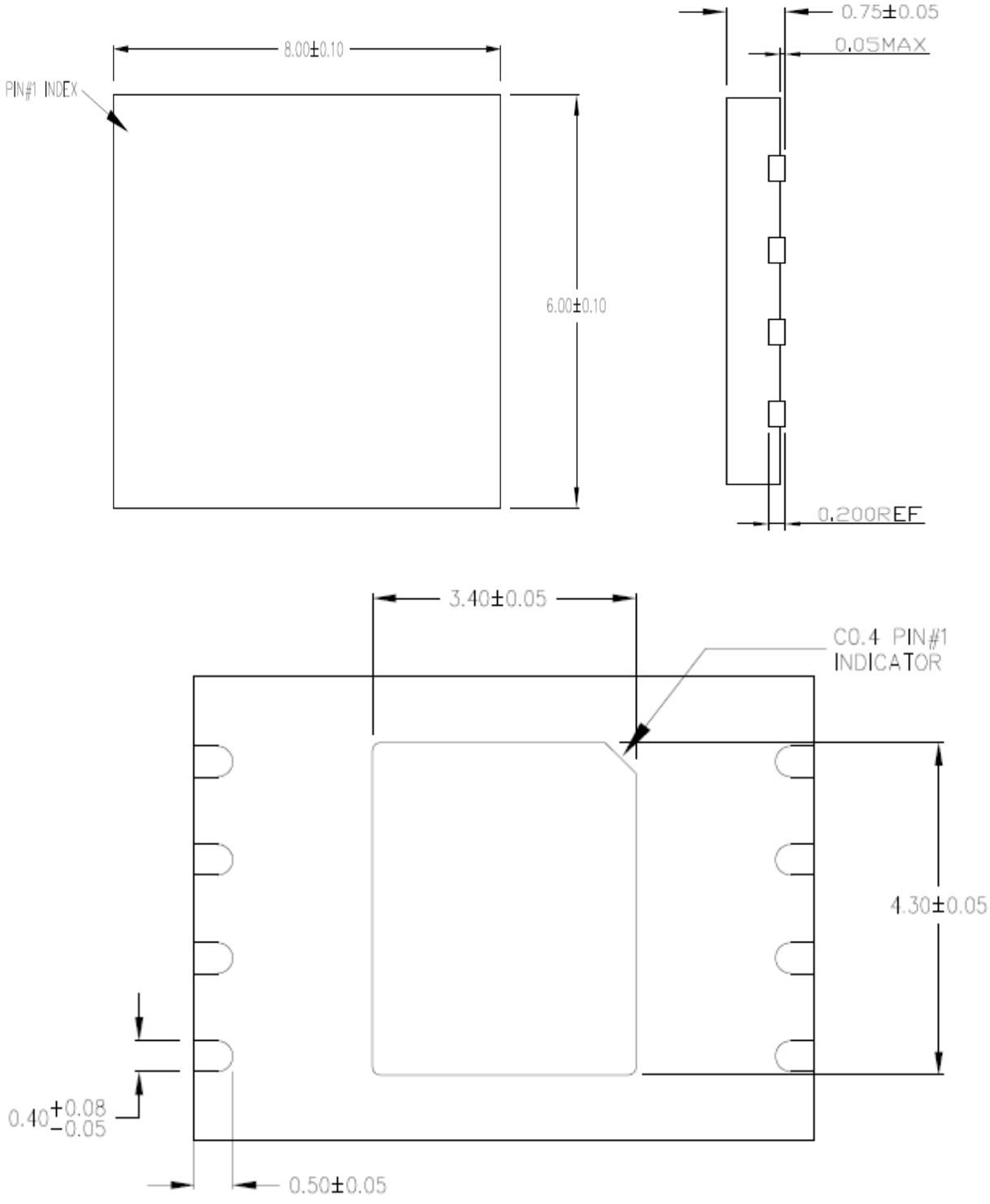
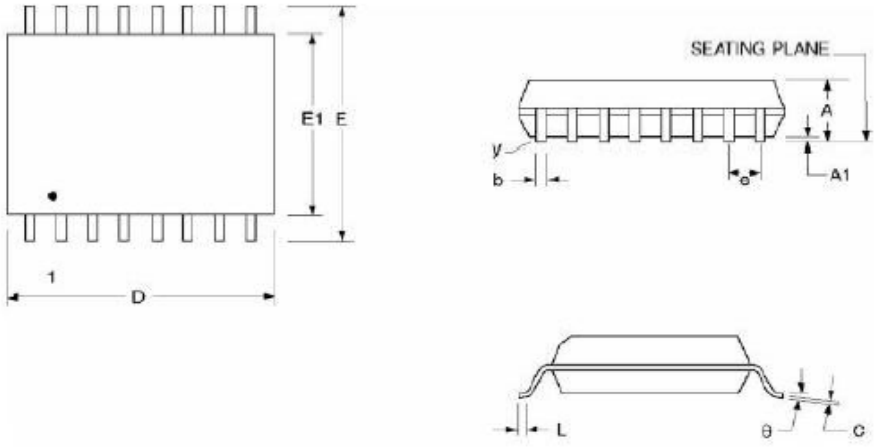


Figure 30. 16-Pin SOIC 300-mil



SYMBOL	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	2.36	2.64	0.093	0.104
A1	0.10	0.30	0.005	0.012
b	0.33	0.51	0.013	0.020
C	0.18	0.28	0.007	0.000
D(3)	10.08	10.49	0.397	0.413
E	10.01	10.64	0.394	0.419
E1(3)	7.39	7.59	0.291	0.299
e(2)	1.27BSC		0.050	
L	0.39	1.27	0.015	0.050
θ	0°	8°	0°	8°
y	---	0.076	---	0.003

Notes:
1. Controlling dimensions: inches, unless otherwise specified.
2. BSC = Basic lead spacing between centers.
3. Dimensions D and E1 do not include mold flash protrusions and should be measured from the bottom of the package.

15 Part Numbering

Table 15. Ordering information

ATO 25 D 1G A – X X X

Package Type

A = 8-pin SOIC 208mil
B = 16-pin SOIC 300mil
C = 8-pad WSON 6x5mml
D = 8-pad WSON 8x6mm
W=Wafer

Temperature Range

C = 0℃ ~ 70℃
E = -30℃ ~ 85℃
I = -45℃ ~ 85℃

Speed

30 = 30MHz
75 = 75MHz
10 = 104MHz

Generation

A = 1st Gen.
B = 2nd Gen.
C = 3rd Gen.

Device Density

512 / 1G = 512Mbit / 1Gbit

Operating Voltage

F = 1.8V Single voltage. 1.65V ~ 2V
D = 3.0V Single voltage. 2.7V ~ 3.6V
R = 3.0V Single Regulated voltage. 3.0V ~ 3.6V

Device Type

25 = SPI interface Serial Flash Memory

Manufacture Company

ATO = ATO Solution Flash Memory