



12N90

Preliminary

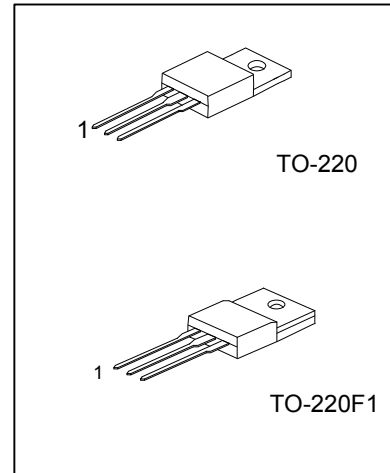
Power MOSFET

12A, 900V N-CHANNEL POWER MOSFET

DESCRIPTION

The UTC **12N90** is an N-channel enhancement mode power MOSFET using UTC's advanced technology to provide customers with planar stripe and DMOS technology. This technology is specialized in allowing a minimum on-state resistance and superior switching performance. It also can withstand high energy pulse in the avalanche and commutation mode.

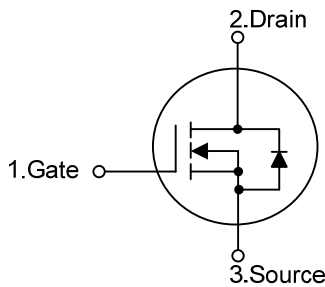
The UTC **12N90** is universally applied in high efficiency switch mode power supply.



FEATURES

- * $R_{DS(on)} = 0.95\Omega @ V_{GS} = 10V$
- * High switching speed
- * 100% avalanche tested

SYMBOL



ORDERING INFORMATION

Ordering Number		Package	Pin Assignment			Packing
Lead Free	Halogen Free		1	2	3	
12N90L-TA3-T	12N90G-TA3-T	TO-220	G	D	S	Tube
12N90L-TF1-T	12N90G-TF1-T	TO-220F1	G	D	S	Tube

Note: Pin Assignment: G: Gate D: Drain S: Source

12N90L - TA3 - T	(1) Packing Type	(1) T: Tube
	(2) Package Type	(2) TA3: TO-220, TF1: TO-220F1
	(3) Lead Free	(3) G: Halogen Free, L: Lead Free

■ ABSOLUTE MAXIMUM RATINGS ($T_C = 25^\circ\text{C}$ unless otherwise specified)

PARAMETER		SYMBOL	RATINGS	UNIT
Drain-Source Voltage		V_{DSS}	900	V
Gate-Source Voltage		V_{GSS}	± 30	V
Drain Current	Continuous ($T_C=25^\circ\text{C}$)	I_D	12	A
	Pulsed (Note 2)	I_{DM}	48	A
Avalanche Current (Note 2)		I_{AR}	12	A
Power Dissipation	TO-220	P_D	225	W
	TO-220F1		51	W
Junction Temperature		T_J	+150	$^\circ\text{C}$
Storage Temperature		T_{STG}	-55~+150	$^\circ\text{C}$

Note: 1. Absolute maximum ratings are those values beyond which the device could be permanently damaged.

Absolute maximum ratings are stress ratings only and functional device operation is not implied.

2. Repetitive Rating: Pulse width limited by maximum junction temperature

■ THERMAL DATA

PARAMETER		SYMBOL	RATINGS	UNIT
Junction to Ambient		θ_{JA}	62.5	$^\circ\text{C/W}$
Junction to Case	TO-220	θ_{JC}	0.56	$^\circ\text{C/W}$
	TO-220F1		2.43	$^\circ\text{C/W}$

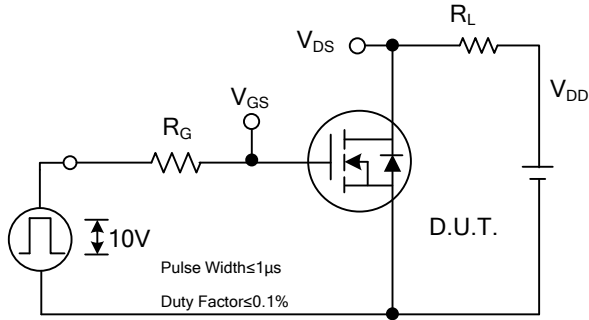
■ ELECTRICAL CHARACTERISTICS ($T_C = 25^\circ\text{C}$ unless otherwise specified)

PARAMETER		SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNIT	
OFF CHARACTERISTICS								
Drain-Source Breakdown Voltage		BV_{DSS}	$I_D=250\mu\text{A}, V_{GS}=0\text{V}$	900			V	
Breakdown Voltage Temperature Coefficient		$\Delta BV_{DSS}/\Delta T_J$	$I_D=250\mu\text{A}$, Referenced to 25°C		1.0		$\text{V}/^\circ\text{C}$	
Drain-Source Leakage Current		I_{DSS}	$V_{DS}=900\text{V}, V_{GS}=0\text{V}$			10	μA	
			$V_{DS}=720\text{V}, T_C=125^\circ\text{C}$			100		
Gate- Source Leakage Current	Forward	I_{GSS}	$V_{GS}=+30\text{V}, V_{DS}=0\text{V}$			100	nA	
	Reverse		$V_{GS}=-30\text{V}, V_{DS}=0\text{V}$			-100	nA	
ON CHARACTERISTICS								
Gate Threshold Voltage		$V_{GS(TH)}$	$V_{DS}=V_{GS}, I_D=250\mu\text{A}$	3.0		5.0	V	
Static Drain-Source On-State Resistance		$R_{DS(ON)}$	$V_{GS}=10\text{V}, I_D=6\text{A}$		0.8	0.95	Ω	
DYNAMIC PARAMETERS								
Input Capacitance		C_{ISS}	$V_{GS}=0\text{V}, V_{DS}=25\text{V}, f=1.0\text{MHz}$		4200		pF	
Output Capacitance		C_{OSS}				315		pF
Reverse Transfer Capacitance		C_{RSS}				90		pF
SWITCHING PARAMETERS								
Total Gate Charge		Q_G	$V_{GS}=10\text{V}, V_{DS}=720\text{V}, I_D=12\text{A}$ (Note 1, 2)		123	155	nC	
Gate to Source Charge		Q_{GS}			27	45	nC	
Gate to Drain Charge		Q_{GD}			49	80	nC	
Turn-ON Delay Time		$t_{D(ON)}$	$V_{DD}=450\text{V}, I_D=12\text{A}, R_G=25\Omega$ (Note 1, 2)		18	50	ns	
Rise Time		t_R			12	50	ns	
Turn-OFF Delay Time		$t_{D(OFF)}$			51	100	ns	
Fall-Time		t_F			18	50	ns	
SOURCE- DRAIN DIODE RATINGS AND CHARACTERISTICS								
Maximum Body-Diode Continuous Current		I_S				12	A	
Maximum Body-Diode Pulsed Current		I_{SM}				48	A	
Drain-Source Diode Forward Voltage		V_{SD}	$I_S=12\text{A}, V_{GS}=0\text{V}$			1.4	V	
Body Diode Reverse Recovery Time		t_{rr}	$V_{GS}=0\text{V}, I_S=12\text{A}$,		1000		ns	
Body Diode Reverse Recovery Charge		Q_{RR}	$di_f/dt=100\text{A}/\mu\text{s}$ (Note 1)		17.0		μC	

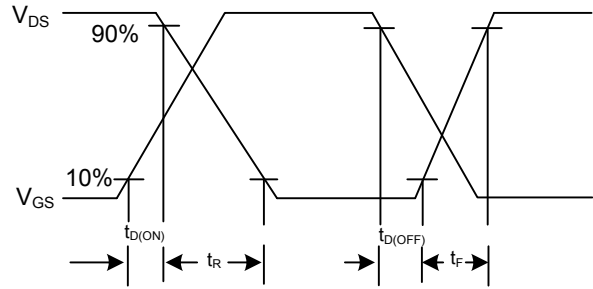
Note: 1. Pulse Test: Pulse width $\leq 300\mu\text{s}$, Duty cycle $\leq 2\%$

2. Essentially independent of operating temperature

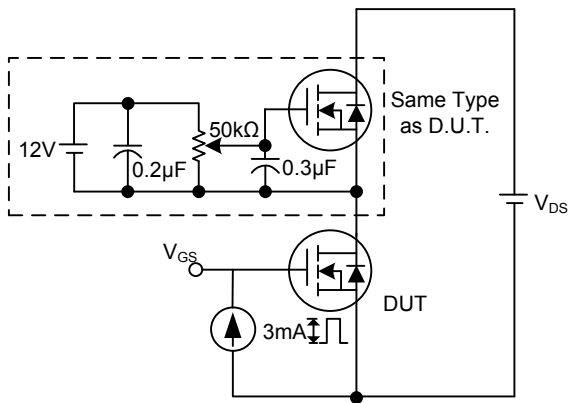
■ TEST CIRCUITS AND WAVEFORMS



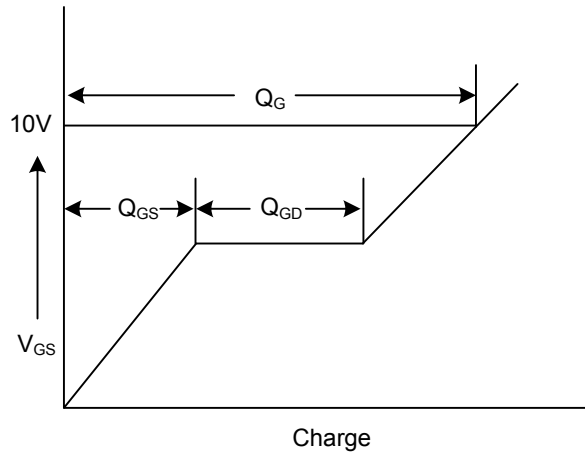
Switching Test Circuit



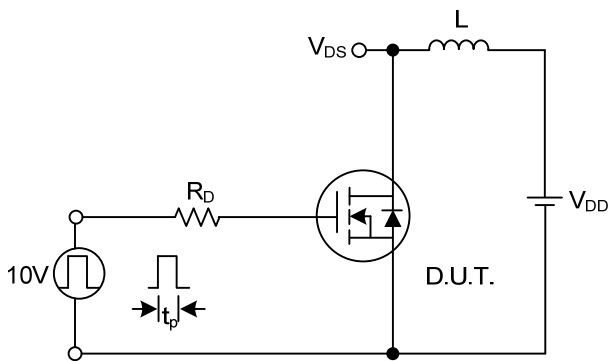
Switching Waveforms



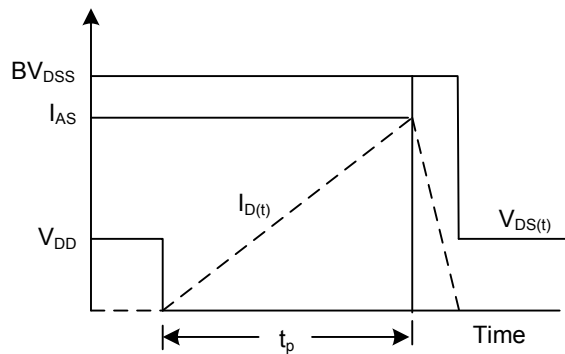
Gate Charge Test Circuit



Gate Charge Waveform

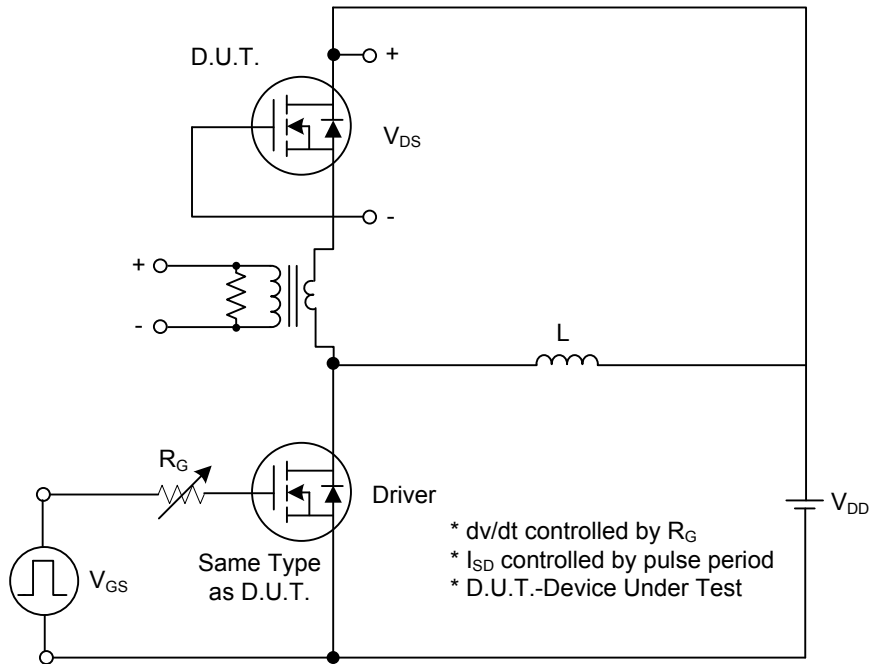


Unclamped Inductive Switching Test Circuit

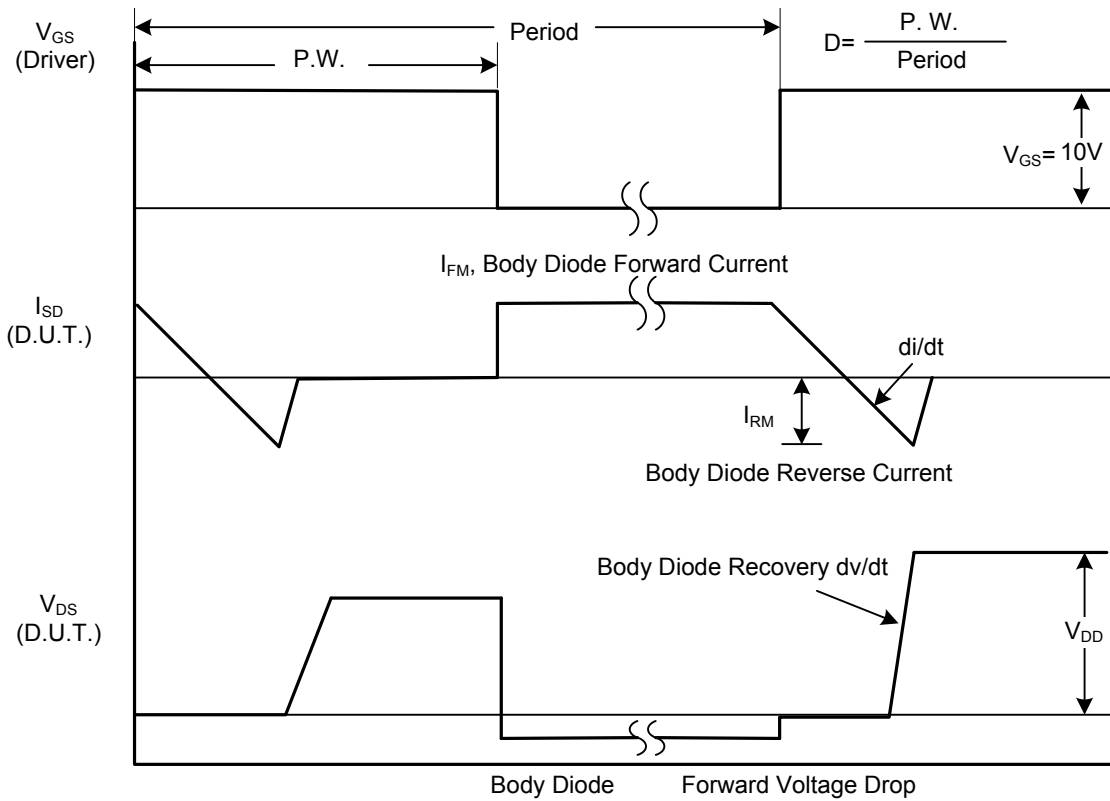


Unclamped Inductive Switching Waveforms

■ TEST CIRCUITS AND WAVEFORMS(Cont.)



Peak Diode Recovery dv/dt Test Circuit



Peak Diode Recovery dv/dt Waveforms

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