Stacked Multi-chip Package (MCP) 1 M X 8 Bit / 512K X 16 Bit Boot Sector Flash Memory and 128K x 8 Low Voltage CMOS SRAM

Preliminary

Document Title

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Revision History

Rev.	History	Issue Date	Remark
0.0	Initial issue	March 25, 2005	Preliminary

AMIC

A81L801

Stacked Multi-chip Package (MCP) 1 M X 8 Bit / 512K X 16 Bit Boot Sector Flash Memory and 128K x 8 Bit Low Voltage CMOS SRAM

Preliminary

MCP Features

- Single power supply operation 2.7 to 3.6 volt
- High Performance
  - Access time as fast as 70ns
- Package
  - 69-Ball FBGA (8x11x1.4 mm)
- Industrial operating temperature range: -25°C to 85°C for –I

Flash Features

- Single power supply operation
  - Full voltage range: 2.7 to 3.6 volt read and write operations for battery-powered applications
- Access times:
  - 70 (max.)
- Current:
  - 9 mA typical active read current
  - 20 mA typical program/erase current
  - 200 nA typical CMOS standby
  - 200 nA Automatic Sleep Mode current
- Flexible sector architecture
  - 16 Kbyte/ 8 KbyteX2/ 32 Kbyte/ 64 KbyteX15 sectors
  - 8 Kword/ 4 KwordX2/ 16 Kword/ 32 KwordX15 sectors
  - Any combination of sectors can be erased
  - Supports full chip erase
  - Sector protection:
    A hardware method of protecting sectors to prevent any inadvertent program or erase operations within that sector. Temporary Sector Unprotect feature allows code changes in previously locked sectors
- Extended operating temperature range: -25°C ~ +85°C for –I series
- Unlock Bypass Program Command
  - Reduces overall programming time when issuing multiple program command sequence
- Top or bottom boot block configurations available
- Embedded Algorithms
  - Embedded Erase algorithm will automatically erase the entire chip or any combination of designated sectors and verify the erased sectors
  - Embedded Program algorithm automatically writes and verifies data at specified addresses
- Typical 100,000 program/erase cycles per sector
- 20-year data retention at 125°C
  - Reliable operation for the life of the system
- $\overline{\text{Data}}$ Polling and toggle bits
  - Provides a software method of detecting completion of program or erase operations
- Ready / $\overline{\text{BUSY}}$ pin (RY / $\overline{\text{BY}}$)
  - Provides a hardware method of detecting completion of program or erase operations
- Erase Suspend/Erase Resume
  - Suspends a sector erase operation to read data from, or program data to, a non-erasing sector, then resumes the erase operation
- Hardware reset pin ($\overline{\text{RESET}}$)
  - Hardware method to reset the device to reading array data

LP SRAM Features

- Power supply range: 2.7V to 3.6V
- Access times: 70 ns (max.)
- Current:
  Very low power version: Operating: 30mA(max.)
  Standby: 5uA (max.)
- Full static operation, no clock or refreshing required
- All inputs and outputs are directly TTL-compatible
- Common I/O using three-state output
- Output enable and two chips enable inputs for easy application
- Data retention voltage: 2.0V (min.)

General Description

The Flash memory of A81L801 is an 8Mbit, 3.0 volt-only memory organized as 1,048,576 bytes of 8 bits or 524,288 words of 16 bits each. The 8 bits of data appear on I/O_0 - I/O_7; the 16 bits of data appear on I/O_0~I/O_{15}. The A81L801 is offered in 69-ball TFBGA package. This device is designed to be programmed in-system with the standard system 3.0 volt VCC supply. Additional 12.0 volt VPP is not required for in-system write or erase operations. However, the A81L801 can also be programmed in standard EPROM programmers.

The Flash memory of A81L801 has the first toggle bit, I/O_6, which indicates whether an Embedded Program or Erase is in progress, or it is in the Erase Suspend. Besides the I/O_6 toggle bit, the Flash memory of A81L801 also has a second toggle bit, I/O_2, to indicate whether the addressed sector is being selected for erase. The A81L801 also offers the ability to program in the Erase Suspend mode. The standard A81L801 offers access times of 70 and 90ns, allowing high-speed microprocessors to operate without wait states. To eliminate bus contention the device has separate chip enables ($\overline{CE_F}$, and $\overline{CE_S}$), write enable ($\overline{WE}$) and output enable ($\overline{OE}$) controls.

The device requires only a single 3.0 volt power supply for both read and write functions. Internally generated and regulated voltages are provided for the program and erase operations.

The Flash memory of A81L801 is entirely software command set compatible with the JEDEC single-power-supply Flash standard. Commands are written to the command register using standard microprocessor write timings. Register contents serve as input to an internal state-machine that controls the erase and programming circuitry. Write cycles also internally latch addresses and data needed for the programming and erase operations. Reading data out of the device is similar to reading from other Flash or EPROM devices.

Device programming occurs by writing the proper program command sequence. This initiates the Embedded Program algorithm - an internal algorithm that automatically times the program pulse widths and verifies proper program margin.

Device erasure occurs by executing the proper erase command sequence. This initiates the Embedded Erase algorithm - an internal algorithm that automatically preprograms the array (if it is not already programmed) before executing the erase operation. During erase, the device automatically times the erase pulse widths and verifies proper erase margin. The Unlock Bypass mode facilitates faster programming times by requiring only two write cycles to program data instead of four.

The host system can detect whether a program or erase operation is complete by observing the RY / $\overline{BY}$ pin, or by reading the I/O_7 ($\overline{Data}$ Polling) and I/O_6 (toggle) status bits. After a program or erase cycle has been completed, the device is ready to read array data or accept another command.

The sector erase architecture allows memory sectors to be erased and reprogrammed without affecting the data contents of other sectors. The Flash memory of A81L801 is fully erased when shipped from the factory.

The hardware sector protection feature disables operations for both program and erase in any combination of the sectors of memory. This can be achieved via programming equipment.

The Erase Suspend/Erase Resume feature enables the user to put erase on hold for any period of time to read data from, or program data to, any other sector that is not selected for erasure. True background erase can thus be achieved.

The hardware $\overline{RESET}$ pin terminates any operation in progress and resets the internal state machine to reading array data. The $\overline{RESET}$ pin may be tied to the system reset circuitry. A system reset would thus also reset the device, enabling the system microprocessor to read the boot-up firmware from the Flash memory.

The A81L801 device offers two power-saving features. When addresses have been stable for a specified amount of time, the device enters the automatic sleep mode. The system can also place the device into the standby mode. Power consumption is greatly reduced in both these modes.

Pin Configurations

■ 69-Ball FBGA
Top View



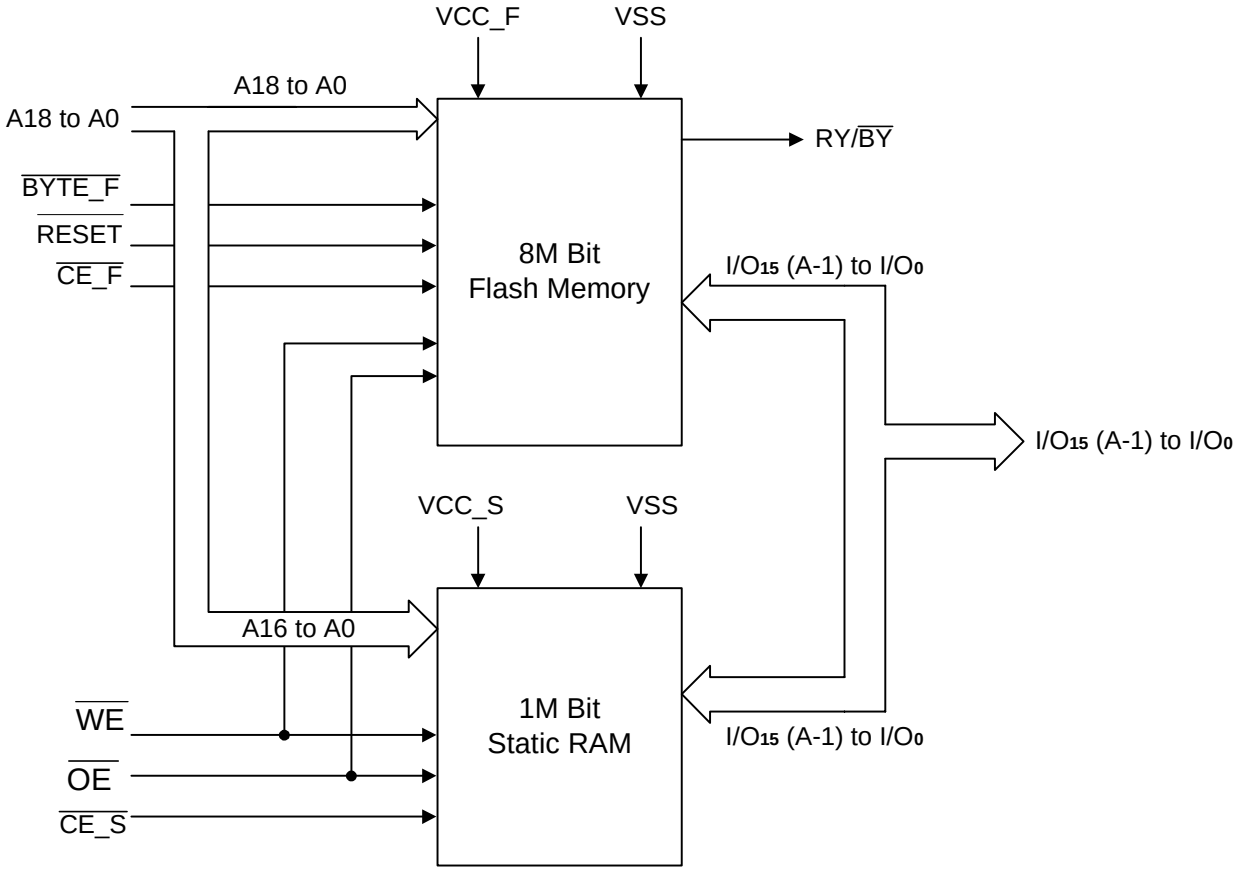
Special Handling Instructions for FBGA Package

Special handling is required for Flash Memory products in FBGA packages.
Flash memory devices in FBGA packages may be damaged if exposed to ultrasonic cleaning methods. The package and/or data integrity may be compromised if the package body is exposed to temperatures above 150°C for prolonged periods of time

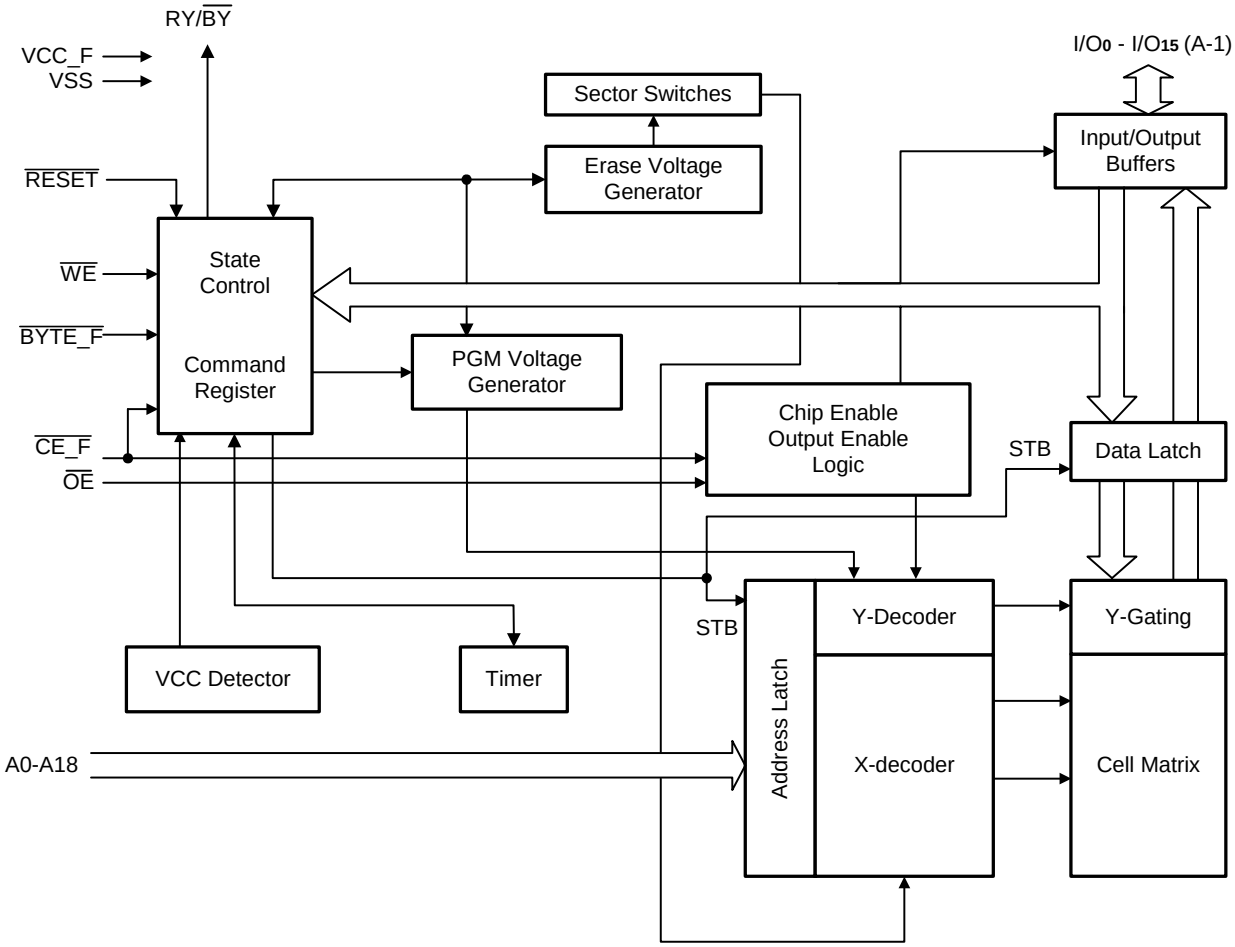
Product Information Guide

Part Number		A81L801
Speed Options	Standard Voltage Range: VCC_F/VCC_S=2.7-3.6V	**70**
Max Access Time (ns)		70
$\overline{CE_F}$ / $\overline{CE_S}$ Access (ns)		70
$\overline{OE}$ Access (ns)		40

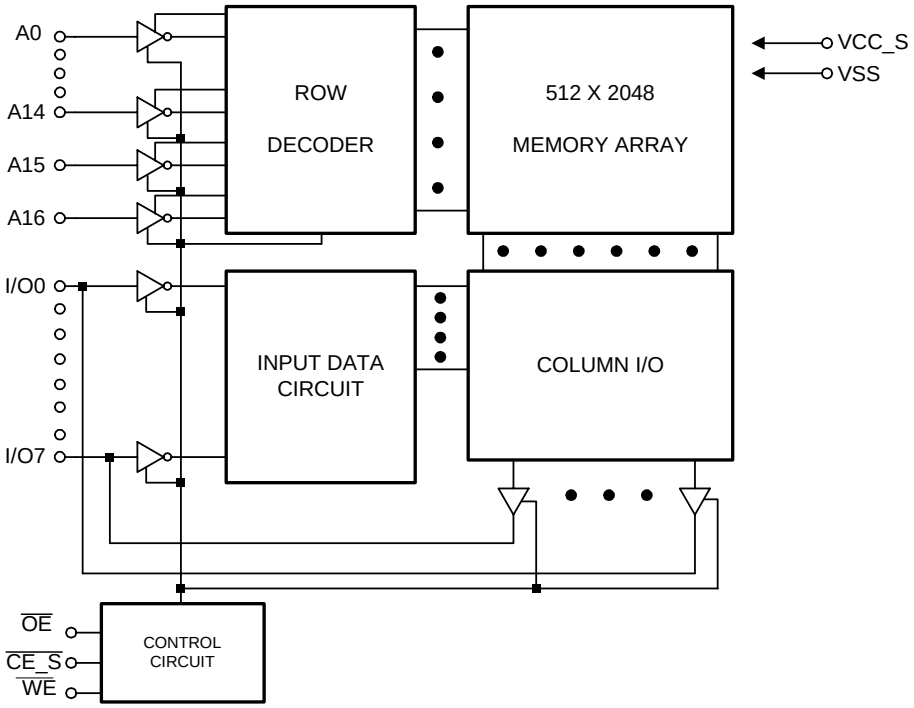
MCP Block Diagram



Flash Memory Block Diagram



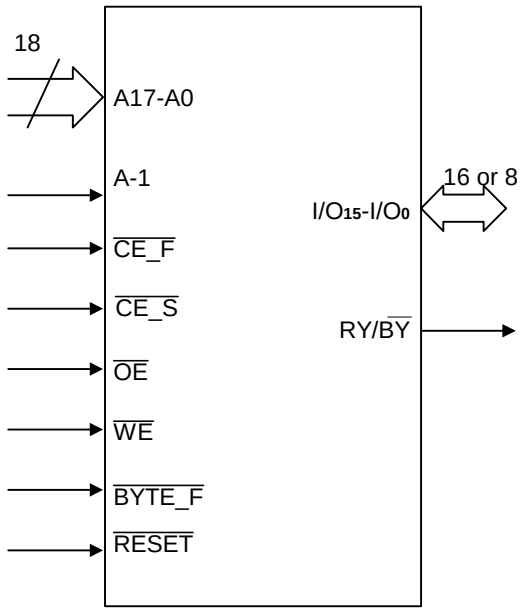
SRAM Block Diagram



Pin Description

Pin No.	Description
A18-A0	18 Address Inputs (Common)
I/O_{14} - I/O_0	15 Data Inputs/Outputs (Common)
I/O_{15} (A-1)	I/O_{15} Data Input/Output, Word Mode A-1 LSB Address Input, Byte Mode
$\overline{CE_F}$	Chip Enable (Flash)
$\overline{CE_S}$	Chip Enable (SRAM)
$\overline{OE}$	Output Enable (Common)
$\overline{WE}$	Write Enable (Common)
RY/$\overline{BY}$	Ready/$\overline{BUSY}$ - Output
$\overline{RESET}$	Hardware Reset Pin, Active Low
$\overline{BYTE_F}$	Select Byte Mode or Word Mode
VCC_F	Power Supply (Flash)
VCC_S	Power Supply (SRAM)
VSS	Device Ground (Common)
NC	Pin Not Connected Internally

Logic Symbol



Absolute Maximum Ratings*

Storage Temperature Plastic Packages. . . . . .-65°C to + 150°C
Ambient Temperature with Power Applied . . . -55°C to + 125°C
Voltage with Respect to Ground VCC_F/VCC_S . . . . (Note 1)
. . . . . -0.5V to +4.0V
A9, $\overline{OE}$ & $\overline{RESET}$ (Note 2) . . . . . -0.5 to +12.5V
All other pins (Note 1) . . . . . -0.5V to VCC_F/VCC_ S + 0.5V
Output Short Circuit Current (Note 3) 200mA

Notes:

1. Minimum DC voltage on input or I/O pins is -0.5V. During voltage transitions, input or I/O pins may undershoot VSS to -2.0V for periods of up to 20ns. Maximum DC voltage on input and I/O pins is VCC_F/VCC_S +0.5V. During voltage transitions, input or I/O pins may overshoot to VCC_F/VCC_S +2.0V for periods up to 20ns.
2. Minimum DC input voltage on A9, $\overline{OE}$ and $\overline{RESET}$ is -0.5V. During voltage transitions, A9, $\overline{OE}$ and $\overline{RESET}$ may overshoot VSS to -2.0V for periods of up to 20ns. Maximum DC input voltage on A9 is +12.5V which may overshoot to 14.0V for periods up to 20ns.
3. No more than one output is shorted at a time. Duration of the short circuit should not be greater than one second.

*Comments

Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to this device. These are stress ratings only. Functional operation of this device at these or any other conditions above those indicated in the operational sections of this specification is not implied or intended. Exposure to the absolute maximum rating conditions for extended periods may affect device reliability.

Operating Ranges

Commercial (C) Devices

Ambient Temperature (T_A) . . . . . 0°C to +70°C

Extended Range Devices

Ambient Temperature (T_A)
For – I series . . . . . -25°C to + 85°C

VCC Supply Voltages

VCC_F/VCC_S ..... +2.7V to +3.6V
Operating ranges define those limits between which the functionally of the device is guaranteed.

Device Bus Operations

This section describes the requirements and use of the device bus operations, which are initiated through the internal command register. The command register itself does not occupy any addressable memory location. The register is composed of latches that store the commands, along with the address and data information needed to execute the command. The contents of the register serve as inputs to the internal state machine. The state machine outputs dictate the function of the device. The appropriate device bus operations table lists the inputs and control levels required, and the resulting output. The following subsections describe each of these operations in further detail.

Table 1.1 Device Bus Operations—Flash Word Mode $\overline{BYTE_F}$ = V_{IH}

Operation (Notes 1,2)	$\overline{CE_F}$	$\overline{CE_S}$	$\overline{OE}$	$\overline{WE}$	A0-A18	$\overline{RESET}$	I/O_7-I/O_0	I/O_{15}-I/O_8
Read from Flash	L	H	L	H	A_{IN}	H	D_{OUT}	D_{OUT}
Standby	H	H	X	X	X	H	High-Z	High-Z
Output Disable	L	H	H	H	X	H	High-Z	High-Z
Write to Flash (Program/Erase)	L	H	H	L	A_{IN}	H	D_{IN}	D_{IN}
Sector Protect	L	H	H	⎍	Sector Address, A6=L, A1=H, A0=L	H	D_{IN}	X
Sector Unprotect	L	H	L	L	Sector Address, A6=L, A1=H, A0=L	H	D_{IN}	X
Temporary Sector Unprotection	X	H	X	X	A_{IN}	V_{ID}	D_{IN}	X
Flash Reset (Hardware) / Standby	X	H	X	X	X	L	High-Z	High-Z
Boot Block Sector Write Protect	X	H	X	X	X	X	X	X
Read from SRAM	H	L	L	H	A_{IN}	H	D_{OUT}	D_{OUT}
							High-Z	D_{OUT}
							D_{OUT}	High-Z
Write to SRAM	H	L	H	L	A_{IN}	H	D_{IN}	D_{IN}
							High-Z	D_{IN}
							D_{IN}	High-Z

Legend:
L = Logic Low = V_{IL}, H = Logic High = V_{IH}, V_{ID} = 11.5-12.5V, ⎍ = Pulse input, X = Don't Care, D_{IN} = Data In, D_{OUT} = Data Out

Notes:
1. Other operations except for those indicated in this column are inhibited.
2. Do not apply $\overline{CE_F}$ = V_{IL}, $\overline{CE_S}$ = V_{IL} at the same time.

Table 1.2 Device Bus Operations—Flash Word Mode $\overline{BYTE_F}$ = V_{IL}

Flash Operation (Notes 1,2)	$\overline{CE_F}$	$\overline{CE_S}$	$\overline{OE}$	$\overline{WE}$	**I/O_{15} (A-1)**	**A0-A18**	$\overline{RESET}$	**I/O_7-I/O_0**	**I/O_{14}-I/O_8**
Read from Flash	L	H	L	H	A-1	A_{IN}	H	D_{OUT}	High-Z
Standby	H	H	X	X	X	X	H	High-Z	High-Z
Output Disable	L	H	H	H	X	X	H	High-Z	High-Z
Write to Flash (Program/Erase)	L	H	H	L	A-1	A_{IN}	H	D_{IN}	High-Z
Sector Protect	L	H	V_{ID}	⊓⊔	L	Sector Address, A6=L, A1=H, A0=L	V_{ID}	X	High-Z
Sector Unprotect	L	H	L	H	L	Sector Address, A6=L, A1=H, A0=L	V_{ID}	Code	High-Z
Temporary Sector Unprotection	X	H	X	X	X	A_{IN}	V_{ID}	X	High-Z
Flash Reset (Hardware)/ Standby	X	H	X	X	X	X	L	High-Z	High-Z
Boot Block Sector Write Protect	X	H	X	X	X	X	X	X	High-Z
Read from SRAM	H	L	L	H	D_{OUT}	A0	H	D_{OUT}	D_{OUT}
					D_{OUT}			High-Z	High-Z
					High-z			D_{OUT}	D_{OUT}
Write to SRAM	H	L	H	L	D_{IN}	A0	H	D_{IN}	D_{IN}
					D_{IN}			High-Z	High-Z
					High-z			D_{IN}	D_{IN}

Legend:
L = Logic Low = V_{IL}, H = Logic High = V_{IH}, V_{ID} = 11.5-12.5V, ⊓⊔ = Pulse input, X = Don't Care, D_{IN} = Data In, D_{OUT} = Data Out

Notes:
1. Other operations except for those indicated in this column are inhibited.
2. Do not apply $\overline{CE_F}$ = V_{IL}, $\overline{CE_S}$ = V_{IL} at the same time.

Word/Byte Configuration

The $\overline{BYTE_F}$ pin determines whether the I/O pins I/O_{15}-I/O_0 operate in the byte or word configuration. If the $\overline{BYTE_F}$ pin is set at logic "1", the device is in word configuration, I/O_{15}-I/O_0 are active and controlled by $\overline{CE_F}$ and $\overline{OE}$.

If the $\overline{BYTE_F}$ pin is set at logic "0", the device is in byte configuration, and only I/O_0-I/O_7 are active and controlled by $\overline{CE_F}$ and $\overline{OE}$. I/O_8-I/O_{14} are tri-stated, and I/O_{15} pin is used as an input for the LSB (A-1) address function.

Requirements for Reading Array Data

To read array data from the outputs, the system must drive the $\overline{CE_F}$ and $\overline{OE}$ pins to V_{IL}. $\overline{CE_F}$ is the power control and selects the device. $\overline{OE}$ is the output control and gates array data to the output pins. $\overline{WE}$ should remain at V_{IH} all the time during read operation. The $\overline{BYTE_F}$ pin determines whether the device outputs array data in words and bytes. The internal state machine is set for reading array data upon device power-up, or after a hardware reset. This ensures that no spurious alteration of the memory content occurs during the power transition. No command is necessary in this mode to obtain array data. Standard microprocessor read cycles that assert valid addresses on the device address inputs produce valid data on the device data outputs. The device remains enabled for read access until the command register contents are altered.

See "Reading Array Data" for more information. Refer to the AC Read Operations table for timing specifications and to the Read Operations Timings diagram for the timing waveforms, I_{CC1} in the DC Characteristics table represents the active current specification for reading array data.

Writing Commands/Command Sequences

To write a command or command sequence (which includes programming data to the device and erasing sectors of memory), the system must drive $\overline{WE}$ and $\overline{CE_F}$ to V_{IL}, and $\overline{OE}$ to V_{IH}. For program operations, the $\overline{BYTE_F}$ pin determines whether the device accepts program data in bytes or words, Refer to "Word/Byte Configuration" for more information. The device features an Unlock Bypass mode to facilitate faster programming. Once the device enters the Unlock Bypass mode, only two write cycles are required to program a word or byte, instead of four. The "

Word / Byte Program Command Sequence" section has details on programming data to the device using both standard and Unlock Bypass command sequence. An erase operation can erase one sector, multiple sectors, or the entire device. The Sector Address Tables indicate the address range that each sector occupies. A "sector address" consists of the address inputs required to uniquely select a sector. See the "Command Definitions" section for details on erasing a sector or the entire chip, or suspending/resuming the erase operation.

After the system writes the auto-select command sequence, the device enters the auto-select mode. The system can then read auto-select codes from the internal register (which is separate from the memory array) on I/O_7 - I/O_0. Standard read cycle timings apply in this mode. Refer to the "Auto-select Mode" and "Auto-select Command Sequence" sections for more information.

I_{CC2} in the DC Characteristics table represents the active current specification for the write mode. The "AC Characteristics" section contains timing specification tables and timing diagrams for write operations.

Program and Erase Operation Status

During an erase or program operation, the system may check the status of the operation by reading the status bits on I/O_7 - I/O_0. Standard read cycle timings and I_{CC} read specifications apply. Refer to "Write Operation Status" for more information, and to each AC Characteristics section for timing diagrams.

Standby Mode

When the system is not reading or writing to the device, it can place the device in the standby mode. In this mode, current consumption is greatly reduced, and the outputs are placed in the high impedance state, independent of the $\overline{OE}$ input.

The device enters the CMOS standby mode when the $\overline{CE_F}$ & $\overline{RESET}$ pins are both held at VCC_F ± 0.3V. (Note that this is a more restricted voltage range than V_{IH}.) If $\overline{CE_F}$ and $\overline{RESET}$ are held at V_{IH}, but not within VCC_F ± 0.3V, the device will be in the standby mode, but the standby current will be greater. The device requires the standard access time (t_{CE}) before it is ready to read data.

If the device is deselected during erasure or programming, the device draws active current until the operation is completed.

I_{CC3} and I_{CC4} in the DC Characteristics tables represent the standby current specification.

Automatic Sleep Mode

The automatic sleep mode minimizes Flash device energy consumption. The device automatically enables this mode when addresses remain stable for t_{ACC} +30ns. The automatic sleep mode is independent of the $\overline{CE_F}$, $\overline{WE}$ and $\overline{OE}$ control signals. Standard address access timings provide new data when addresses are changed. While in sleep mode, output data is latched and always available to the system. I_{CC4} in the DC Characteristics table represents the automatic sleep mode current specification.

Output Disable Mode

When the $\overline{OE}$ input is at V_{IH}, output from the device is disabled. The output pins are placed in the high impedance state.

$\overline{RESET}$: Hardware Reset Pin

The $\overline{RESET}$ pin provides a hardware method of resetting the device to reading array data. When the system drives the $\overline{RESET}$ pin low for at least a period of t_{RP}, the device immediately terminates any operation in progress, tri-states all data output pins, and ignores all read/write attempts for the duration of the $\overline{RESET}$ pulse. The device also resets the internal state machine to reading array data. The operation that was interrupted should be reinitiated once the device is ready to accept another command sequence, to ensure data integrity.

Current is reduced for the duration of the $\overline{RESET}$ pulse. When $\overline{RESET}$ is held at VSS ± 0.3V, the device draws CMOS standby current (I_{CC4}). If $\overline{RESET}$ is held at V_{IL} but not within VSS ± 0.3V, the standby current will be greater.

The $\overline{\text{RESET}}$ pin may be tied to the system reset circuitry. A system reset would thus also reset the Flash memory, enabling the system to read the boot-up firmware from the Flash memory.

If $\overline{\text{RESET}}$ is asserted during a program or erase operation, the RY/$\overline{\text{BY}}$ pin remains a "0" (busy) until the internal reset operation is complete, which requires a time t_{READY} (during Embedded Algorithms). The system can thus monitor RY/$\overline{\text{BY}}$ to determine whether the reset operation is complete. If $\overline{\text{RESET}}$ is asserted when a program or erase operation is not executing (RY/$\overline{\text{BY}}$ pin is "1"), the reset operation is completed within a time of t_{READY} (not during Embedded Algorithms). The system can read data t_{RH} after the $\overline{\text{RESET}}$ pin return to V_{IH}.

Refer to the AC Characteristics tables for $\overline{\text{RESET}}$ parameters and diagram.

Table 2. A81L801 Top Boot Block Sector Address Table

Sector	A18	A17	A16	A15	A14	A13	A12	Sector Size (Kbytes/ Kwords)	Address Range (in hexadecimal)	
									Byte Mode (x 8)	Word Mode (x16)
SA0	0	0	0	0	X	X	X	64/32	00000h - 0FFFFh	00000h - 07FFFh
SA1	0	0	0	1	X	X	X	64/32	10000h - 1FFFFh	08000h - 0FFFFh
SA2	0	0	1	0	X	X	X	64/32	20000h - 2FFFFh	10000h - 17FFFh
SA3	0	0	1	1	X	X	X	64/32	30000h - 3FFFFh	18000h - 1FFFFh
SA4	0	1	0	0	X	X	X	64/32	40000h - 4FFFFh	20000h - 27FFFh
SA5	0	1	0	1	X	X	X	64/32	50000h - 5FFFFh	28000h - 2FFFFh
SA6	0	1	1	0	X	X	X	64/32	60000h - 6FFFFh	30000h - 37FFFh
SA7	0	1	1	1	X	X	X	64/32	70000h - 7FFFFh	38000h - 3FFFFh
SA8	1	0	0	0	X	X	X	64/32	80000h - 8FFFFh	40000h - 47FFFh
SA9	1	0	0	1	X	X	X	64/32	90000h - 9FFFFh	48000h - 4FFFFh
SA10	1	0	1	0	X	X	X	64/32	A0000h - AFFFFh	50000h - 57FFFh
SA11	1	0	1	1	X	X	X	64/32	B0000h - BFFFFh	58000h - 5FFFFh
SA12	1	1	0	0	X	X	X	64/32	C0000h - CFFFFh	60000h - 67FFFh
SA13	1	1	0	1	X	X	X	64/32	D0000h - DFFFFh	68000h - 6FFFFh
SA14	1	1	1	0	X	X	X	64/32	E0000h - EFFFFh	70000h - 77FFFh
SA15	1	1	1	1	0	X	X	32/16	F0000h - F7FFFh	78000h - 7BFFFh
SA16	1	1	1	1	1	0	0	8/4	F8000h - F9FFFh	7C000h - 7CFFFh
SA17	1	1	1	1	1	0	1	8/4	FA000h - FBFFFh	7D000h - 7DFFFh
SA18	1	1	1	1	1	1	X	16/8	FC000h - FFFFFh	7E000h - 7FFFFh

Note:
Address range is A18: A_{-1} in byte mode and A18: A0 in word mode. See "Word/Byte Configuration" section.

Table 3. A81L801 Bottom Boot Block Sector Address Table

Sector	A18	A17	A16	A15	A14	A13	A12	Sector Size (Kbytes/ Kwords)	Address Range (in hexadecimal)	
									Byte Mode (x 8)	Word Mode (x16)
SA0	0	0	0	0	0	0	X	16/8	00000h - 03FFFh	00000 - 01FFF
SA1	0	0	0	0	0	1	0	8/4	04000h - 05FFFh	02000 - 02FFF
SA2	0	0	0	0	0	1	1	8/4	06000h - 07FFFh	03000 - 03FFF
SA3	0	0	0	0	1	X	X	32/16	08000h - 0FFFFh	04000 - 07FFF
SA4	0	0	0	1	X	X	X	64/32	10000h - 1FFFFh	08000 - 0FFFF
SA5	0	0	1	0	X	X	X	64/32	20000h – 2FFFFh	10000 - 17FFF
SA6	0	0	1	1	X	X	X	64/32	30000h - 3FFFFh	18000 - 1FFFF
SA7	0	1	0	0	X	X	X	64/32	40000h - 4FFFFh	20000 - 27FFF
SA8	0	1	0	1	X	X	X	64/32	50000h - 5FFFFh	28000 - 2FFFF
SA9	0	1	1	0	X	X	X	64/32	60000h - 6FFFFh	30000 - 37FFF
SA10	0	1	1	1	X	X	X	64/32	70000h - 7FFFFh	38000 - 3FFFF
SA11	1	0	0	0	X	X	X	64/32	80000h - 8FFFFh	40000 - 47FFF
SA12	1	0	0	1	X	X	X	64/32	90000h - 9FFFFh	48000 - 4FFFF
SA13	1	0	1	0	X	X	X	64/32	A0000h - AFFFFh	50000 - 57FFF
SA14	1	0	1	1	X	X	X	64/32	B0000h - BFFFFh	58000 - 5FFFF
SA15	1	1	0	0	X	X	X	64/32	C0000h - CFFFFh	60000 - 67FFF
SA16	1	1	0	1	X	X	X	64/32	D0000h - DFFFFh	68000 - 6FFFF
SA17	1	1	1	0	X	X	X	64/32	E0000h - EFFFFh	70000 - 77FFF
SA18	1	1	1	1	X	X	X	64/32	F0000h - FFFFFh	78000 - 7FFFF

Note:
Address range is A18: A_{-1} in byte mode and A18: A0 in word mode. See “Word/Byte Configuration” section.

Autoselect Mode

The autoselect mode provides manufacturer and device identification, and sector protection verification, through identifier codes output on I/O7 - I/O0. This mode is primarily intended for programming equipment to automatically match a device to be programmed with its corresponding programming algorithm. However, the autoselect codes can also be accessed in-system through the command register.

When using programming equipment, the autoselect mode requires V_{ID} (11.5V to 12.5 V) on address pin A9. Address pins A6, A1, and A0 must be as shown in autoselect Codes (High Voltage Method) table. In addition, when verifying sector protection, the sector address must appear on the appropriate highest order address bits. Refer to the corresponding Sector Address Tables. The Command Definitions table shows the remaining address bits that are don't care. When all necessary bits have been set as required, the programming equipment may then read the corresponding identifier code on I/O7 - I/O0.To access the autoselect codes in-system, the host system can issue the autoselect command via the command register, as shown in the Command Definitions table. This method does not require V_{ID}. See "Command Definitions" for details on using the autoselect mode.

Table 4. A81L801 Autoselect Codes (High Voltage Method)

Description	Mode	$\overline{CE_F}$	$\overline{OE}$	$\overline{WE}$	A18 to A12	A11 to A10	A9	A8 to A7	A6	A5 to A2	A1	A0	I/O_8 to I/O_{15}	I/O_7 to I/O_0
Manufacturer ID: AMIC		L	L	H	X	X	V_{ID}	X	L	X	L	L	X	37h
Device ID: A81L801 (Top Boot Block)	Word	L	L	H	X	X	V_{ID}	X	L	X	L	H	B3h	1Ah
	Byte												X	1Ah
Device ID: A81L801 (Bottom Boot Block)	Word	L	L	H	X	X	V_{ID}	X	L	X	L	H	B3h	9Bh
	Byte												X	9Bh
Continuation ID		L	L	H	X	X	V_{ID}	X	L	X	H	H	X	7Fh
Sector Protection Verification		L	L	H	SA	X	V_{ID}	X	L	X	H	L	X	01h (protected)
													X	00h (unprotected)

L=Logic Low= V_{IL}, H=Logic High=V_{IH}, SA=Sector Address, X=Don't Care, $\overline{CE_S}$ = V_{IH}

Note: The autoselect codes may also be accessed in-system via command sequences.

Sector Protection/Unprotection

The hardware sector protection feature disables both program and erase operations in any sector. The hardware sector unprotection features re-enables both program and erase operations in previously protected sectors.
It is possible to determine whether a sector is protected or unprotected. See “Autoselect Mode” for details.
Sector protection / unprotection can be implemented via two methods. The primary method requires VID on the $\overline{\text{RESET}}$ pin only, and can be implemented either in-system or via programming equipment. Figure 2 shows the algorithm and the Sector Protect / Unprotect Timing Diagram illustrates the timing waveforms for this feature. This method uses standard microprocessor bus cycle timing. For sector unprotect, all unprotected sectors must first be protected prior to the first sector unprotect write cycle. The alternate method must be implemented using programming equipment. The procedure requires a high voltage (V_{ID}) on address pin A9 and the control pins.
The device is shipped with all sectors unprotected.
It is possible to determine whether a sector is protected or unprotected. See "Autoselect Mode" for details.

Hardware Data Protection

The requirement of command unlocking sequence for programming or erasing provides data protection against inadvertent writes (refer to the Command Definitions table). In addition, the following hardware data protection measures prevent accidental erasure or programming, which might otherwise be caused by spurious system level signals during V_{CC} power-up transitions, or from system noise. The device is powered up to read array data to avoid accidentally writing data to the array.

Write Pulse "Glitch" Protection

Noise pulses of less than 5ns (typical) on $\overline{\text{OE}}$, $\overline{\text{CE_F}}$ or $\overline{\text{WE}}$ do not initiate a write cycle.

Logical Inhibit

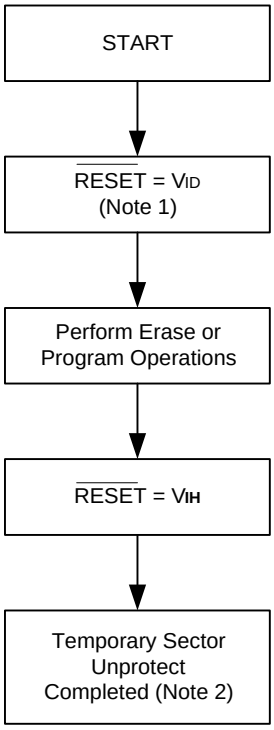
Write cycles are inhibited by holding any one of $\overline{\text{OE}}$ =V_{IL}, $\overline{\text{CE_F}}$ = V_{IH} or $\overline{\text{WE}}$ = V_{IH}. To initiate a write cycle, $\overline{\text{CE_F}}$ and $\overline{\text{WE}}$ must be a logical zero while $\overline{\text{OE}}$ is a logical one.

Power-Up Write Inhibit

If $\overline{\text{WE}}$ = $\overline{\text{CE_F}}$ = V_{IL} and $\overline{\text{OE}}$ = V_{IH} during power up, the device does not accept commands on the rising edge of $\overline{\text{WE}}$. The internal state machine is automatically reset to reading array data on the initial power-up.

Temporary Sector Unprotect

This feature allows temporary unprotection of previous protected sectors to change data in-system. The Sector Unprotect mode is activated by setting the $\overline{\text{RESET}}$ pin to V_{ID}. During this mode, formerly protected sectors can be programmed or erased by selecting the sector addresses. Once V_{ID} is removed from the $\overline{\text{RESET}}$ pin, all the previously protected sectors are protected again. Figure 1 shows the algorithm, and the Temporary Sector Unprotect diagram shows the timing waveforms, for this feature.



Notes:
1. All protected sectors unprotected.
2. All previously protected sectors are protected once again.

Figure 1. Temporary Sector Unprotect Operation

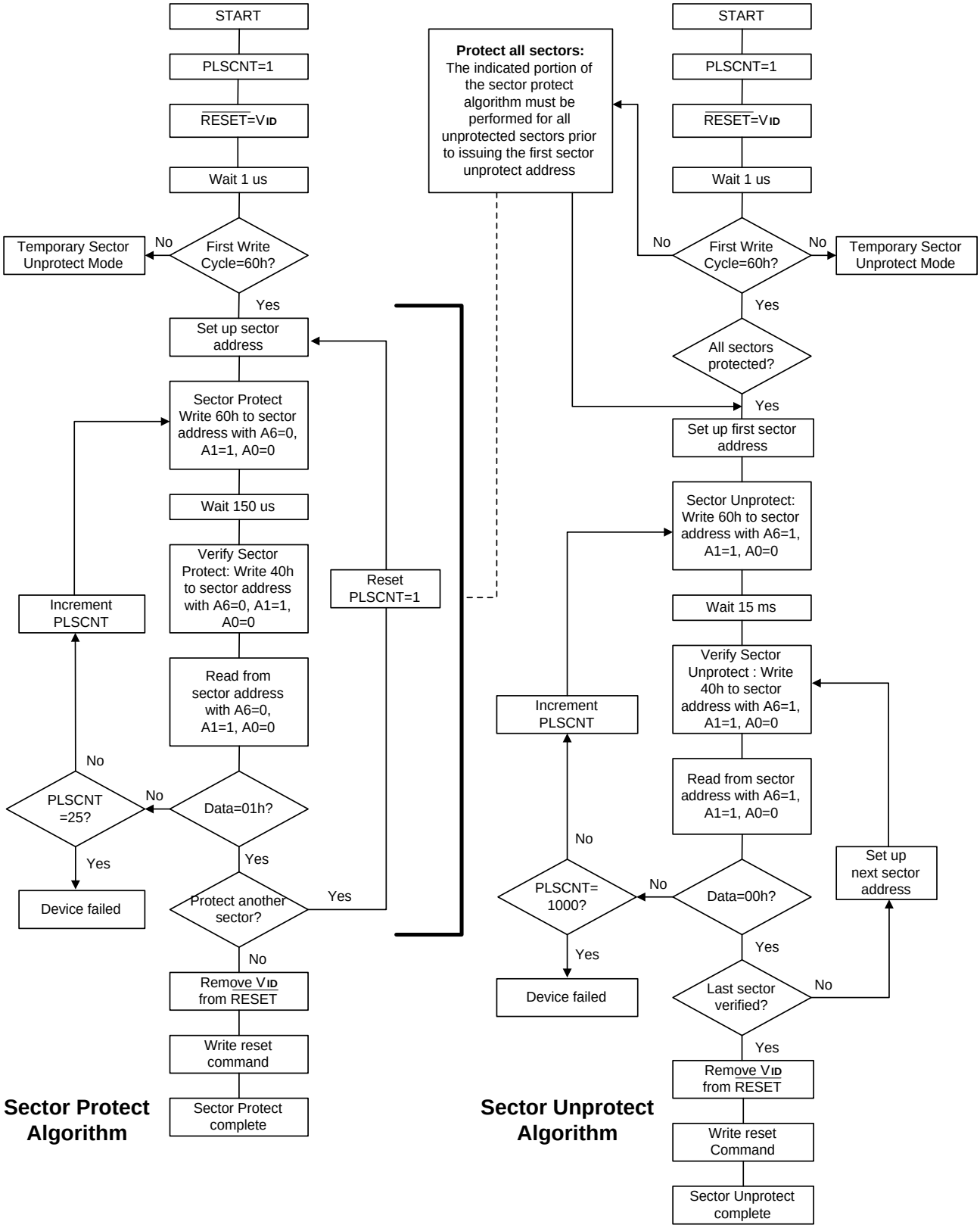


Figure 2. In-System Sector Protect/Unprotect Algorithms

Command Definitions

Writing specific address and data commands or sequences into the command register initiates device operations. The Command Definitions table defines the valid register command sequences. Writing incorrect address and data values or writing them in the improper sequence resets the device to reading array data.

All addresses are latched on the falling edge of $\overline{WE}$ or $\overline{CE_F}$, whichever happens later. All data is latched on the rising edge of $\overline{WE}$ or $\overline{CE_F}$, whichever happens first. Refer to the appropriate timing diagrams in the "AC Characteristics" section.

Reading Array Data

The device is automatically set to reading array data after device power-up. No commands are required to retrieve data. The device is also ready to read array data after completing an Embedded Program or Embedded Erase algorithm. After the device accepts an Erase Suspend command, the device enters the Erase Suspend mode. The system can read array data using the standard read timings, except that if it reads at an address within erase-suspended sectors, the device outputs status data. After completing a programming operation in the Erase Suspend mode, the system may once again read array data with the same exception. See "Erase Suspend/Erase Resume Commands" for more information on this mode.

The system must issue the reset command to re-enable the device for reading array data if I/O_5 goes high, or while in the autoselect mode. See the "Reset Command" section, next.

See also "Requirements for Reading Array Data" in the "Device Bus Operations" section for more information. The Read Operations table provides the read parameters, and Read Operation Timings diagram shows the timing diagram.

Reset Command

Writing the reset command to the device resets the device to reading array data. Addresses bits are don't care for this command. The reset command may be written between the sequence cycles in an erase command sequence before erasing begins. This resets the device to reading array data. Once erasure begins, however, the device ignores reset commands until the operation is complete.

The reset command may be written between the sequence cycles in a program command sequence before programming begins. This resets the device to reading array data (also applies to programming in Erase Suspend mode). Once programming begins, however, the device ignores reset commands until the operation is complete.

The reset command may be written between the sequence cycles in an autoselect command sequence. Once in the autoselect mode, the reset command must be written to return to reading array data (also applies to autoselect during Erase Suspend).

If I/O_5 goes high during a program or erase operation, writing the reset command returns the device to reading array data (also applies during Erase Suspend).

Autoselect Command Sequence

The autoselect command sequence allows the host system to access the manufacturer and devices codes, and determine whether or not a sector is protected. The Command Definitions table shows the address and data requirements. This method is an alternative to that shown in the Autoselect Codes (High Voltage Method) table, which is intended for PROM programmers and requires V_{ID} on address bit A9.

The autoselect command sequence is initiated by writing two unlock cycles, followed by the autoselect command. The device then enters the autoselect mode, and the system may read at any address any number of times, without initiating another command sequence.

A read cycle at address XX00h retrieves the manufacturer code and another read cycle at XX03h retrieves the continuation code. A read cycle at address XX01h returns the device code. A read cycle containing a sector address (SA) and the address 02h in returns 01h if that sector is protected, or 00h if it is unprotected. Refer to the Sector Address tables for valid sector addresses.

The system must write the reset command to exit the autoselect mode and return to reading array data.

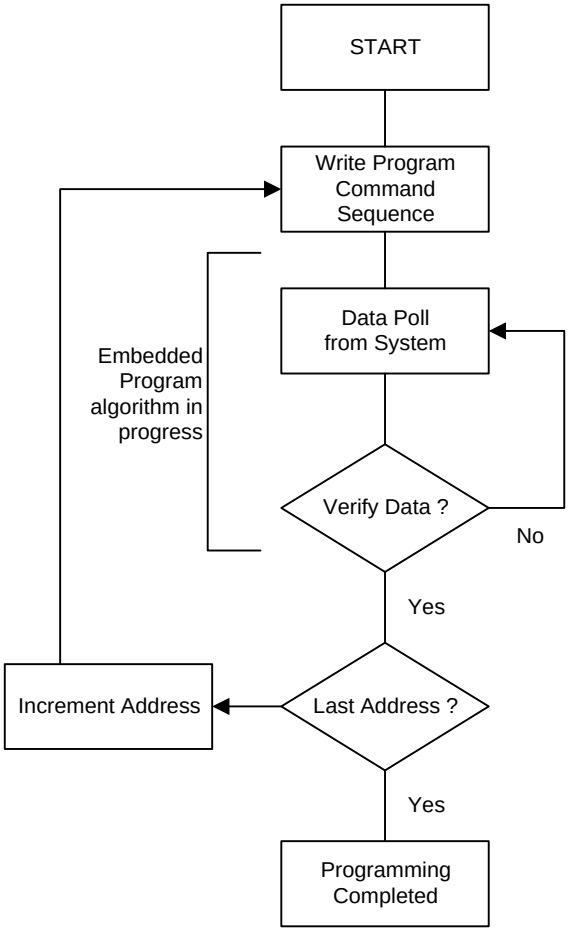
Word/Byte Program Command Sequence

The system may program the device by word or byte, depending on the state of the $\overline{BYTE_F}$ pin. Programming is a four-bus-cycle operation. The program command sequence is initiated by writing two unlock write cycles, followed by the program set-up command. The program address and data are written next, which in turn initiate the Embedded Program algorithm. The system is not required to provide further controls or timings. The device automatically provides internally generated program pulses and verify the programmed cell margin. Table 5 shows the address and data requirements for the byte program command sequence.

When the Embedded Program algorithm is complete, the device then returns to reading array data and addresses are longer latched. The system can determine the status of the program operation by using I/O_7, I/O_6, or RY/$\overline{BY}$. See “White Operation Status” for information on these status bits.

Any commands written to the device during the Embedded Program Algorithm are ignored. Note that a hardware reset immediately terminates the programming operation. The Byte Program command sequence should be reinitiated once the device has reset to reading array data, to ensure data integrity.

Programming is allowed in any sequence and across sector boundaries. A bit cannot be programmed from a “0” back to a “1”. Attempting to do so may halt the operation and set I/O5 to “1”, or cause the $\overline{Data}$ Polling algorithm to indicate the operation was successful. However, a succeeding read will show that the data is still “0”. Only erase operations can convert a “0” to a “1”.



Note : See the appropriate Command Definitions table for program command sequence.

Figure 3. Program Operation

Unlock Bypass Command Sequence

The unlock bypass feature allows the system to program bytes or words to the device faster than using the standard program command sequence. The unlock bypass command sequence is initiated by first writing two unlock cycles. This is followed by a third write cycle containing the unlock bypass command, 20h. The device then enters the unlock bypass mode. A two-cycle unlock bypass program command sequence is all that is required to program in this mode. The first cycle in this sequence contains the unlock bypass program command, A0h; the second cycle contains the program address and data. Additional data is programmed in the same manner. This mode dispenses with the initial two unlock cycles required in the standard program command sequence, resulting in faster total programming time. Table 5 shows the requirements for the command sequence.

During the unlock bypass mode, only the Unlock Bypass Program and Unlock Bypass Reset commands are valid. To exit the unlock bypass mode, the system must issue the two-cycle unlock bypass reset command sequence. The first cycle must contain the data 90h; the second cycle the data 00h. Addresses are don't care for both cycle. The device returns to reading array data.

Figure 3 illustrates the algorithm for the program operation. See the Erase/Program Operations in "AC Characteristics" for parameters, and to Program Operation Timings for timing diagrams.

Chip Erase Command Sequence

Chip erase is a six-bus-cycle operation. The chip erase command sequence is initiated by writing two unlock cycles, followed by a set-up command. Two additional unlock write cycles are then followed by the chip erase command, which in turn invokes the Embedded Erase algorithm. The device does not require the system to preprogram prior to erase. The Embedded Erase algorithm automatically preprograms and verifies the entire memory for an all zero data pattern prior to electrical erase. The system is not required to provide any controls or timings during these operations. The Command Definitions table shows the address and data requirements for the chip erase command sequence.

Any commands written to the chip during the Embedded Erase algorithm are ignored. The system can determine the status of the erase operation by using I/O_7, I/O_6, or I/O_2. See "Write Operation Status" for information on these status bits. When the Embedded Erase algorithm is complete, the device returns to reading array data and addresses are no longer latched.

Figure 4 illustrates the algorithm for the erase operation. See the Erase/Program Operations tables in "AC Characteristics" for parameters, and to the Chip/Sector Erase Operation Timings for timing waveforms.

Sector Erase Command Sequence

Sector erase is a six-bus-cycle operation. The sector erase command sequence is initiated by writing two unlock cycles, followed by a set-up command. Two additional unlock write cycles are then followed by the address of the sector to be erased, and the sector erase command. The Command Definitions table shows the address and data requirements for the sector erase command sequence.

The device does not require the system to preprogram the memory prior to erase. The Embedded Erase algorithm automatically programs and verifies the sector for an all zero data pattern prior to electrical erase. The system is not required to provide any controls or timings during these operations.

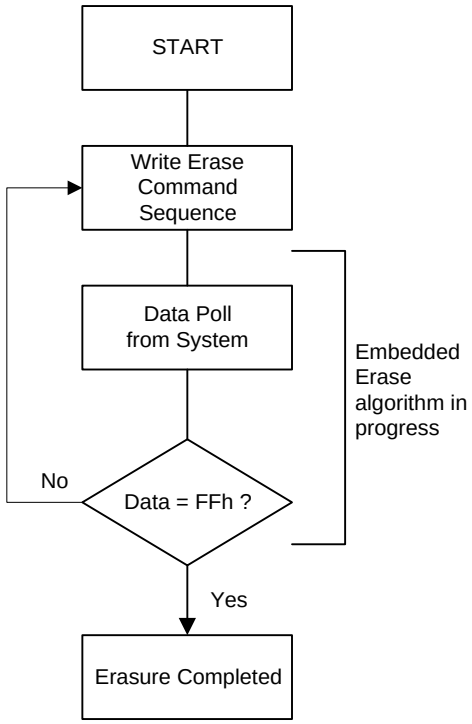
After the command sequence is written, a sector erase time-out of 50μs begins. During the time-out period, additional sector addresses and sector erase commands may be written. Loading the sector erase buffer may be done in any sequence, and the number of sectors may be from one sector to all sectors. The time between these additional cycles must be less than 50μs, otherwise the last address and command might not be accepted, and erasure may begin. It is recommended that processor interrupts be disabled during this time to ensure all commands are accepted. The interrupts can be re-enabled after the last Sector Erase command is written. If the time between additional sector erase commands can be assumed to be less than 50μs, the system need not monitor I/O_3. Any command other than Sector Erase or Erase Suspend during the time-out period resets the device to reading array data. The system must rewrite the command sequence and any additional sector addresses and commands.

The system can monitor I/O_3 to determine if the sector erase timer has timed out. (See the " I/O_3: Sector Erase Timer"

section.) The time-out begins from the rising edge of the final $\overline{WE}$ pulse in the command sequence.
Once the sector erase operation has begun, only the Erase Suspend command is valid. All other commands are ignored.
When the Embedded Erase algorithm is complete, the device returns to reading array data and addresses are no longer latched. The system can determine the status of the erase operation by using I/O7, I/O6, or I/O2. Refer to "Write Operation Status" for information on these status bits.
4 illustrates the algorithm for the erase operation. Refer to the Erase/Program Operations tables in the "AC Characteristics" section for parameters, and to the Sector Erase Operations Timing diagram for timing waveforms.

Erase Suspend/Erase Resume Commands

The Erase Suspend command allows the system to interrupt a sector erase operation and then read data from, or program data to, any sector not selected for erasure. This command is valid only during the sector erase operation, including the 50μs time-out period during the sector erase command sequence. The Erase Suspend command is ignored if written during the chip erase operation or Embedded Program algorithm. Writing the Erase Suspend command during the Sector Erase time-out immediately terminates the time-out period and suspends the erase operation. Addresses are "don't cares" when writing the Erase Suspend command.
When the Erase Suspend command is written during a sector erase operation, the device requires a maximum of 20μs to suspend the erase operation. However, when the Erase Suspend command is written during the sector erase time-out, the device immediately terminates the time-out period and suspends the erase operation.
After the erase operation has been suspended, the system can read array data from or program data to any sector not selected for erasure. (The device "erase suspends" all sectors selected for erasure.) Normal read and write timings and command definitions apply. Reading at any address within erase-suspended sectors produces status data on I/O7 - I/O0. The system can use I/O7, or I/O6 and I/O2 together, to determine if a sector is actively erasing or is erase-suspended. See "Write Operation Status" for information on these status bits.
After an erase-suspended program operation is complete, the system can once again read array data within non-suspended sectors. The system can determine the status of the program operation using the I/O7 or I/O6 status bits, just as in the standard program operation. See "Write Operation Status" for more information.
The system may also write the autoselect command sequence when the device is in the Erase Suspend mode. The device allows reading autoselect codes even at addresses within erasing sectors, since the codes are not stored in the memory array. When the device exits the autoselect mode, the device reverts to the Erase Suspend mode, and is ready for another valid operation. See "Autoselect Command Sequence" for more information.
The system must write the Erase Resume command (address bits are "don't care") to exit the erase suspend mode and continue the sector erase operation. Further writes of the Resume command are ignored. Another Erase Suspend command can be written after the device has resumed erasing.



Note :
1. See the appropriate Command Definitions table for erase command sequences.
2. See "I/O3 : Sector Erase Timer" for more information.

Figure 4. Erase Operation

Table 5. A81L801 Command Definitions

Command Sequence (Note 1)			Cycles	Bus Cycles (Notes 2 - 5)													
				First		Second		Third		Fourth		Fifth		Sixth	
				Addr	Data	Addr	Data	Addr	Data	Addr	Data	Addr	Data	Addr	Data
Read (Note 6)			1	RA	RD										
Reset (Note 7)			1	XXX	F0										
Autoselect (Note 8)	**Manufacturer ID**	Word	4	555	AA	2AA	55	555	90	X00	37				
		Byte		AAA		555		AAA							
	Device ID, Top Boot Block	Word	4	555	AA	2AA	55	555	90	X01	B31A				
		Byte		AAA		555		AAA		X02	1A				
	Device ID, Bottom Boot Block	Word	4	555	AA	2AA	55	555	90	X01	B39B				
		Byte		AAA		555		AAA		X02	9B				
	Continuation ID	Word	4	555	AA	2AA	55	555	90	X03	7F				
		Byte		AAA		555		AAA		X06					
	Sector Protect Verify (Note 9)	Word	4	555	AA	2AA	55	555	90	(SA) X02	XX00				
											XX01				
		Byte		AAA		555		AAA		(SA) X04	00				
											01				
Program		Word	4	555	AA	2AA	55	555	A0	PA	PD				
		Byte		AAA		555		AAA							
Unlock Bypass		Word	3	555	AA	2AA	55	555	20						
		Byte		AAA		555		AAA							
Unlock Bypass Program (Note 10)			2	XXX	A0	PA	PD								
Unlock Bypass Reset (Note 11)			2	XXX	90	XXX	00								
Chip Erase		Word	6	555	AA	2AA	55	555	80	555	AA	2AA	55	555	10
		Byte		AAA		555		AAA		AAA		555		AAA	
Sector Erase		Word	6	555	AA	2AA	55	555	80	555	AA	2AA	55	SA	30
		Byte		AAA		555		AAA		AAA		555			
Erase Suspend (Note 12)			1	XXX	B0										
Erase Resume (Note 13)			1	XXX	30										

Legend:
X = Don't care
RA = Address of the memory location to be read.
RD = Data read from location RA during read operation.
PA = Address of the memory location to be programmed. Addresses latch on the falling edge of the $\overline{WE}$ or $\overline{CE_F}$ pulse, whichever happens later.
PD = Data to be programmed at location PA. Data latches on the rising edge of $\overline{WE}$ or $\overline{CE_F}$ pulse, whichever happens first.
SA = Address of the sector to be verified (in autoselect mode) or erased. Address bits A18 - A12 select a unique sector.
Note:
1. See Table 1 for description of bus operations.
2. All values are in hexadecimal.
3. Except when reading array or autoselect data, all bus cycles are write operation.
4. Data bits I/O_{15}~I/O_8 are don't care for unlock and command cycles.
5. Address bits A18 - A11 are don't cares for unlock and command cycles, unless SA or PA required.
6. No unlock or command cycles required when reading array data.
7. The Reset command is required to return to reading array data when device is in the autoselect mode, or if I/O_5 goes high (while the device is providing status data).
8. The fourth cycle of the autoselect command sequence is a read cycle.
9. The data is 00h for an unprotected sector and 01h for a protected sector. See "Autoselect Command Sequence" for more information.
10. The Unlock Bypass command is required prior to the Unlock Bypass Program command.
11. The Unlock Bypass Reset command is required to return to reading array data when the device is in the unlock bypass mode.
12. The system may read and program in non-erasing sectors, or enter the autoselect mode, when in the Erase Suspend mode.
13. The Erase Resume command is valid only during the Erase Suspend mode.

Write Operation Status

Several bits, I/O2, I/O3, I/O5, I/O6, I/O7, RY/$\overline{BY}$ are provided in the A81L801 to determine the status of a write operation in the flash memory. Table 6 and the following subsections describe the functions of these status bits. I/O7, I/O6 and RY/$\overline{BY}$ each offer a method for determining whether a program or erase operation is complete or in progress. These three bits are discussed first.

I/O7: $\overline{Data}$ Polling

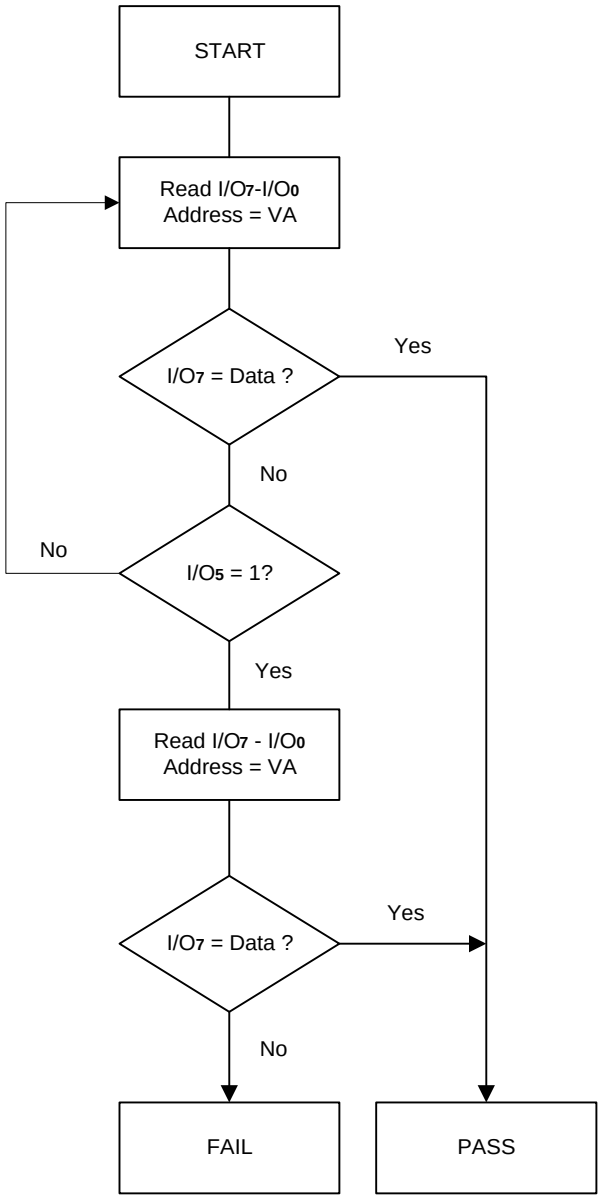
The $\overline{Data}$ Polling bit, I/O7, indicates to the host system whether an Embedded Algorithm is in progress or completed, or whether the device is in Erase Suspend. $\overline{Data}$ Polling is valid after the rising edge of the final $\overline{WE}$ pulse in the program or erase command sequence.

During the Embedded Program algorithm, the device outputs on I/O7 the complement of the datum programmed to I/O7. This I/O7 status also applies to programming during Erase Suspend. When the Embedded Program algorithm is complete, the device outputs the datum programmed to I/O7. The system must provide the program address to read valid status information on I/O7. If a program address falls within a protected sector, $\overline{Data}$ Polling on I/O7 is active for approximately 2μs, then the device returns to reading array data.

During the Embedded Erase algorithm, $\overline{Data}$ Polling produces a "0" on I/O7. When the Embedded Erase algorithm is complete, or if the device enters the Erase Suspend mode, $\overline{Data}$ Polling produces a "1" on I/O7.This is analogous to the complement/true datum output described for the Embedded Program algorithm: the erase function changes all the bits in a sector to "1"; prior to this, the device outputs the "complement," or "0." The system must provide an address within any of the sectors selected for erasure to read valid status information on I/O7.

After an erase command sequence is written, if all sectors selected for erasing are protected, $\overline{Data}$ Polling on I/O7 is active for approximately 100μs, then the device returns to reading array data. If not all selected sectors are protected, the Embedded Erase algorithm erases the unprotected sectors, and ignores the selected sectors that are protected.

When the system detects I/O7 has changed from the complement to true data, it can read valid data at I/O7 - I/O0 on the following read cycles. This is because I/O7 may change asynchronously with I/O0 - I/O6 while Output Enable ($\overline{OE}$) is asserted low. The $\overline{Data}$ Polling Timings (During Embedded Algorithms) in the "AC Characteristics" section illustrates this. Table 6 shows the outputs for $\overline{Data}$ Polling on I/O7. Figure 5 shows the $\overline{Data}$ Polling algorithm.



Note :
1. VA = Valid address for programming. During a sector erase operation, a valid address is an address within any sector selected for erasure. During chip erase, a valid address is any non-protected sector address.
2. I/O7 should be rechecked even if I/O5 = "1" because I/O7 may change simultaneously with I/O5.

Figure 5. $\overline{Data}$ Polling Algorithm

RY/$\overline{BY}$: Read/$\overline{Busy}$

The RY/$\overline{BY}$ is a dedicated, open-drain output pin that indicates whether an Embedded algorithm is in progress or complete. The RY/$\overline{BY}$ status is valid after the rising edge of the final $\overline{WE}$ pulse in the command sequence. Since RY/$\overline{BY}$ is an open-drain output, several RY/$\overline{BY}$ pins can be tied together in parallel with a pull-up resistor to VCC.
If the output is low (Busy), the device is actively erasing or programming. (This includes programming in the Erase Suspend mode.) If the output is high (Ready), the device is ready to read array data (including during the Erase Suspend mode), or is in the standby mode.
Table 6 shows the outputs for RY/$\overline{BY}$. Refer to "$\overline{RESET}$ Timings", "Timing Waveforms for Program Operation" and "Timing Waveforms for Chip/Sector Erase Operation" for more information.

I/O6: Toggle Bit I

Toggle Bit I on I/O6 indicates whether an Embedded Program or Erase algorithm is in progress or complete, or whether the device has entered the Erase Suspend mode. Toggle Bit I may be read at any address, and is valid after the rising edge of the final $\overline{WE}$ pulse in the command sequence (prior to the program or erase operation), and during the sector erase time-out.
During an Embedded Program or Erase algorithm operation, successive read cycles to any address cause I/O6 to toggle. (The system may use either $\overline{OE}$ or $\overline{CE_F}$ to control the read cycles.) When the operation is complete, I/O6 stops toggling.
After an erase command sequence is written, if all sectors selected for erasing are protected, I/O6 toggles for approximately 100μs, then returns to reading array data. If not all selected sectors are protected, the Embedded Erase algorithm erases the unprotected sectors, and ignores the selected sectors that are protected.
The system can use I/O6 and I/O2 together to determine whether a sector is actively erasing or is erase-suspended. When the device is actively erasing (that is, the Embedded Erase algorithm is in progress), I/O6 toggles. When the device enters the Erase Suspend mode, I/O6 stops toggling. However, the system must also use I/O2 to determine which sectors are erasing or erase-suspended. Alternatively, the system can use I/O7 (see the subsection on " I/O7: $\overline{Data}$ Polling").
If a program address falls within a protected sector, I/O6 toggles for approximately 2μs after the program command sequence is written, then returns to reading array data.
I/O6 also toggles during the erase-suspend-program mode, and stops toggling once the Embedded Program algorithm is complete.
The Write Operation Status table shows the outputs for Toggle Bit I on I/O6. Refer to Figure 6 for the toggle bit algorithm, and to the Toggle Bit Timings figure in the "AC Characteristics" section for the timing diagram. The I/O2 vs. I/O6 figure shows the differences between I/O2 and I/O6 in graphical form. See also the subsection on " I/O2: Toggle Bit II".

I/O2: Toggle Bit II

The "Toggle Bit II" on I/O2, when used with I/O6, indicates whether a particular sector is actively erasing (that is, the Embedded Erase algorithm is in progress), or whether that sector is erase-suspended. Toggle Bit II is valid after the rising edge of the final $\overline{WE}$ pulse in the command sequence.
I/O2 toggles when the system reads at addresses within those sectors that have been selected for erasure. (The system may use either $\overline{OE}$ or $\overline{CE_F}$ to control the read cycles.) But I/O2 cannot distinguish whether the sector is actively erasing or is erase-suspended. I/O6, by comparison, indicates whether the device is actively erasing, or is in Erase Suspend, but cannot distinguish which sectors are selected for erasure. Thus, both status bits are required for sector and mode information. Refer to Table 6 to compare outputs for I/O2 and I/O6.
Figure 6 shows the toggle bit algorithm in flowchart form, and the section " I/O2: Toggle Bit II" explains the algorithm. See also the " I/O6: Toggle Bit I" subsection. Refer to the Toggle Bit Timings figure for the toggle bit timing diagram. The I/O2 vs. I/O6 figure shows the differences between I/O2 and I/O6 in graphical form.

Reading Toggle Bits I/O6, I/O2

Refer to Figure 6 for the following discussion. Whenever the system initially begins reading toggle bit status, it must read I/O7 - I/O0 at least twice in a row to determine whether a toggle bit is toggling. Typically, a system would note and store the value of the toggle bit after the first read. After the second read, the system would compare the new value of the toggle bit with the first. If the toggle bit is not toggling, the device has completed the program or erase operation. The system can read array data on I/O7 - I/O0 on the following read cycle.
However, if after the initial two read cycles, the system determines that the toggle bit is still toggling, the system also should note whether the value of I/O5 is high (see the section on I/O5). If it is, the system should then determine again whether the toggle bit is toggling, since the toggle bit may have stopped toggling just as I/O5 went high. If the toggle bit is no longer toggling, the device has successfully completed the program or erase operation. If it is still toggling, the device did not complete the operation successfully, and the system must write the reset command to return to reading array data.
The remaining scenario is that the system initially determines that the toggle bit is toggling and I/O5 has not gone high. The system may continue to monitor the toggle bit and I/O5 through successive read cycles, determining the status as described in the previous paragraph. Alternatively, it may choose to perform other system tasks. In this case, the system must start at the beginning of the algorithm when it returns to determine the status of the operation (top of Figure 6).

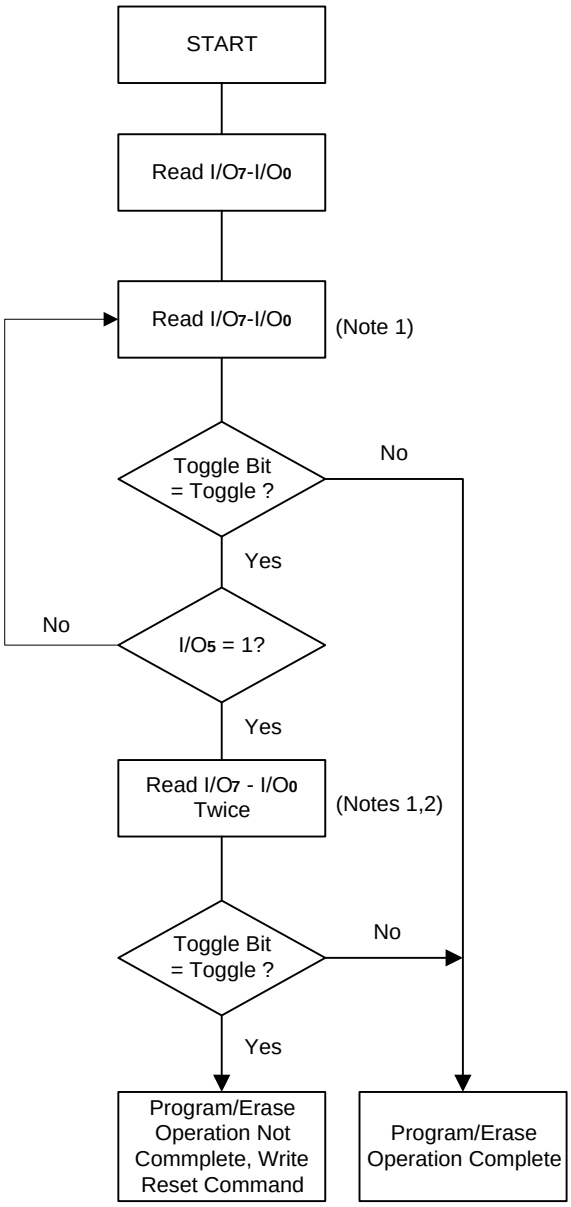
I/O5: Exceeded Timing Limits

I/O5 indicates whether the program or erase time has exceeded a specified internal pulse count limit. Under these conditions I/O5 produces a "1." This is a failure condition that indicates the program or erase cycle was not successfully completed.
The I/O5 failure condition may appear if the system tries to program a "1 "to a location that is previously programmed to "0." Only an erase operation can change a "0" back to a "1." Under this condition, the device halts the operation, and when the operation has exceeded the timing limits, I/O5 produces a "1."
Under both these conditions, the system must issue the reset command to return the device to reading array data.

I/O3: Sector Erase Timer

After writing a sector erase command sequence, the system may read I/O3 to determine whether or not an erase operation has begun. (The sector erase timer does not apply to the chip erase command.) If additional sectors are selected for erasure, the entire time-out also applies after each additional sector erase command. When the time-out is complete, I/O3 switches from "0" to "1." The system may ignore I/O3 if the system can guarantee that the time between additional sector erase commands will always be less than 50μs. See also the "Sector Erase Command Sequence" section.

After the sector erase command sequence is written, the system should read the status on I/O7 ($\overline{\text{Data}}$ Polling) or I/O6 (Toggle Bit I) to ensure the device has accepted the command sequence, and then read I/O3. If I/O3 is "1", the internally controlled erase cycle has begun; all further commands (other than Erase Suspend) are ignored until the erase operation is complete. If I/O3 is "0", the device will accept additional sector erase commands. To ensure the command has been accepted, the system software should check the status of I/O3 prior to and following each subsequent sector erase command. If I/O3 is high on the second status check, the last command might not have been accepted. Table 6 shows the outputs for I/O3.



Notes :
1. Read toggle bit twice to determine whether or not it is toggling. See text.
2. Recheck toggle bit because it may stop toggling as I/O5 changes to "1". See text.

Figure 6. Toggle Bit Algorithm

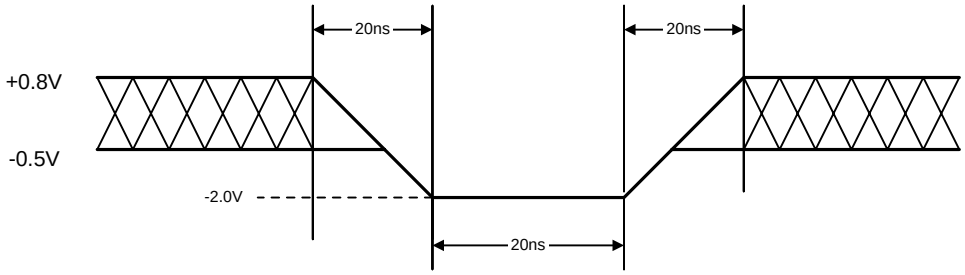
Table 6. Write Operation Status

Operation		I/O_7 (Note 1)	I/O_6	I/O_5 (Note 2)	I/O_3	I/O_2 (Note 1)	RY/$\overline{BY}$
Standard Mode	Embedded Program Algorithm	$\overline{I/O_7}$	Toggle	0	N/A	No toggle	0
	Embedded Erase Algorithm	0	Toggle	0	1	Toggle	0
Erase Suspend Mode	Reading within Erase Suspended Sector	1	No toggle	0	N/A	Toggle	1
	Reading within Non-Erase Suspended Sector	Data	Data	Data	Data	Data	1
	Erase-Suspend-Program	$\overline{I/O_7}$	Toggle	0	N/A	N/A	0

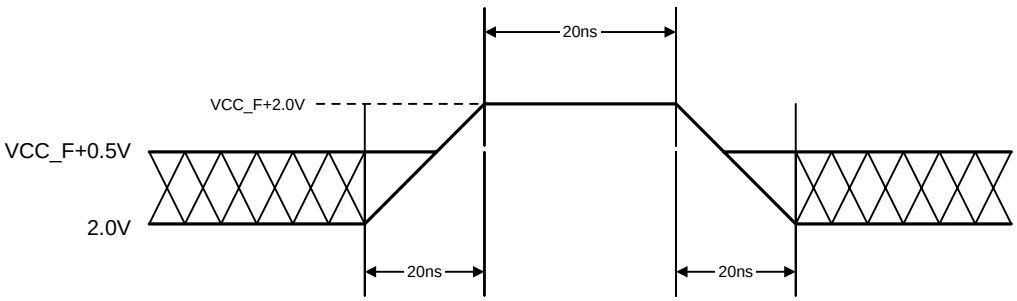
Notes:

1. I/O_7 and I/O_2 require a valid address when reading status information. Refer to the appropriate subsection for further details.
2. I/O_5 switches to "1" when an Embedded Program or Embedded Erase operation has exceeded the maximum timing limits. See "I/O_5: Exceeded Timing Limits" for more information.

Maximum Negative Input Overshoot



Maximum Positive Input Overshoot



DC Characteristics

CMOS Compatible (T_A=0°C to 70°C or -25°C to + 85°C for –I)

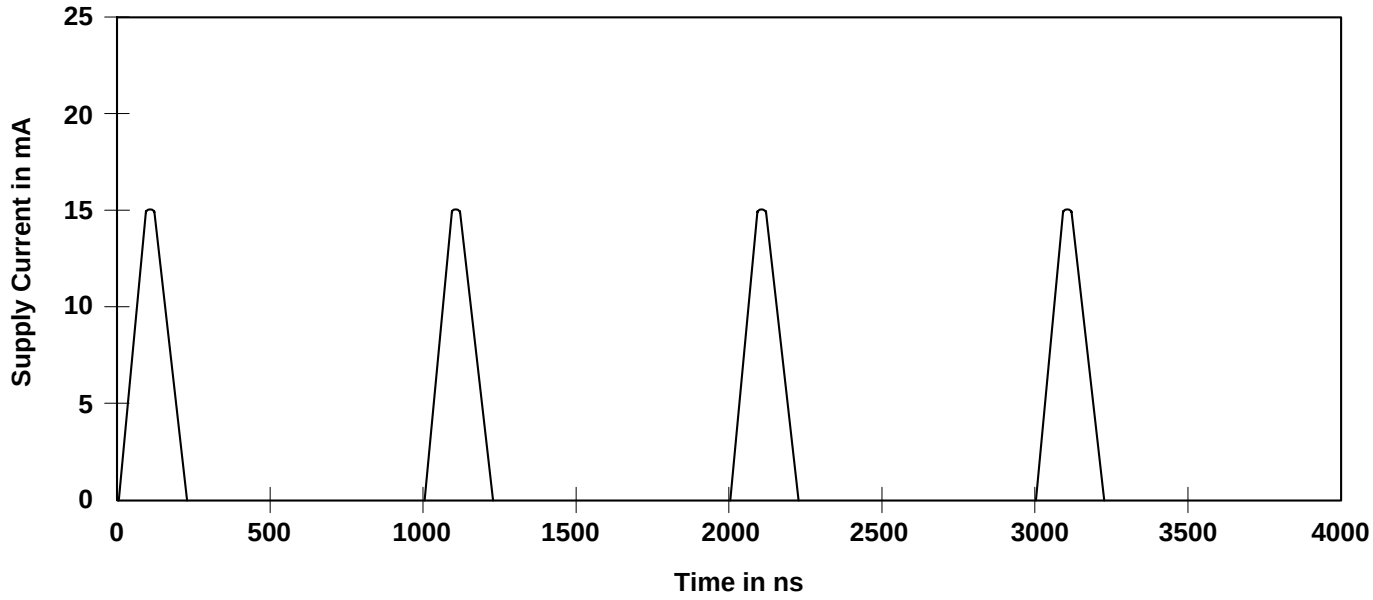
Parameter Symbol	Parameter Description	Test Description		Min.	Typ.	Max.	Unit
I_{LI}	Input Load Current	VIN = VSS to VCC_F. VCC_F = VCC_F Max				±1.0	µA
I_{LIT}	A9 Input Load Current	VCC_F = VCC_F Max, A9 =12.5V				35	µA
I_{LO}	Output Leakage Current	V_{OUT} = VSS to VCC_F. VCC_F = VCC_F Max				±1.0	µA
I_{CC1}	VCC_F Active Read Current (Notes 1, 2)	$\overline{CE_F}$ = V_{IL}, $\overline{OE}$ = V_{IH} Byte Mode	5 MHz		9	16	mA
			1 MHz		2	4	
		$\overline{CE_F}$ = V_{IL}, $\overline{OE}$ = V_{IH} Word Mode	5 MHz		9	16	
			1 MHz		2	4	
I_{CC2}	VCC_F Active Write (Program/Erase) Current (Notes 2, 3, 4)	$\overline{CE_F}$ = V_{IL}, $\overline{OE}$ =V_{IH}			20	30	mA
I_{CC3}	VCC_F Standby Current (Note 2)	$\overline{CE_F}$ = V_{IH}, $\overline{RESET}$= VCC_F ± 0.3V			0.2	5	µA
I_{CC4}	VCC_F Standby Current During Reset (Note 2)	$\overline{RESET}$= VSS ± 0.3V			0.2	5	µA
I_{CC5}	Automatic Sleep Mode (Note 2, 4, 5)	V_{IH} = VCC_F ± 0.3V; V_{IL} = VSS ± 0.3V			0.2	5	µA
V_{IL}	Input Low Level			-0.5		0.8	V
V_{IH}	Input High Level			0.7 x VCC_F		VCC_F + 0.3	V
V_{ID}	Voltage for Autoselect and Temporary Unprotect Sector	VCC_F = 3.3 V		11.5		12.5	V
V_{OL}	Output Low Voltage	I_{OL} = 4.0mA, VCC_F = VCC_F Min				0.45	V
V_{OH1}	Output High Voltage	I_{OH} = -2.0 mA, VCC_F = VCC_F Min		0.85 x VCC_F			V
V_{OH2}		I_{OH} = -100 µA, VCC_F = VCC_F Min		VCC_F - 0.4			V

Notes:

1. The I_{CC} current listed is typically less than 2 mA/MHz, with $\overline{OE}$ at V_{IH}. Typical VCC_F is 3.0V.
2. Maximum I_{CC} specifications are tested with VCC_F = VCC_F max.
3. I_{CC} active while Embedded Algorithm (program or erase) is in progress.
4. Automatic sleep mode enables the low power mode when addresses remain stable for t_{ACC} + 30ns. Typical sleep mode current is 200nA.
5. Not 100% tested.

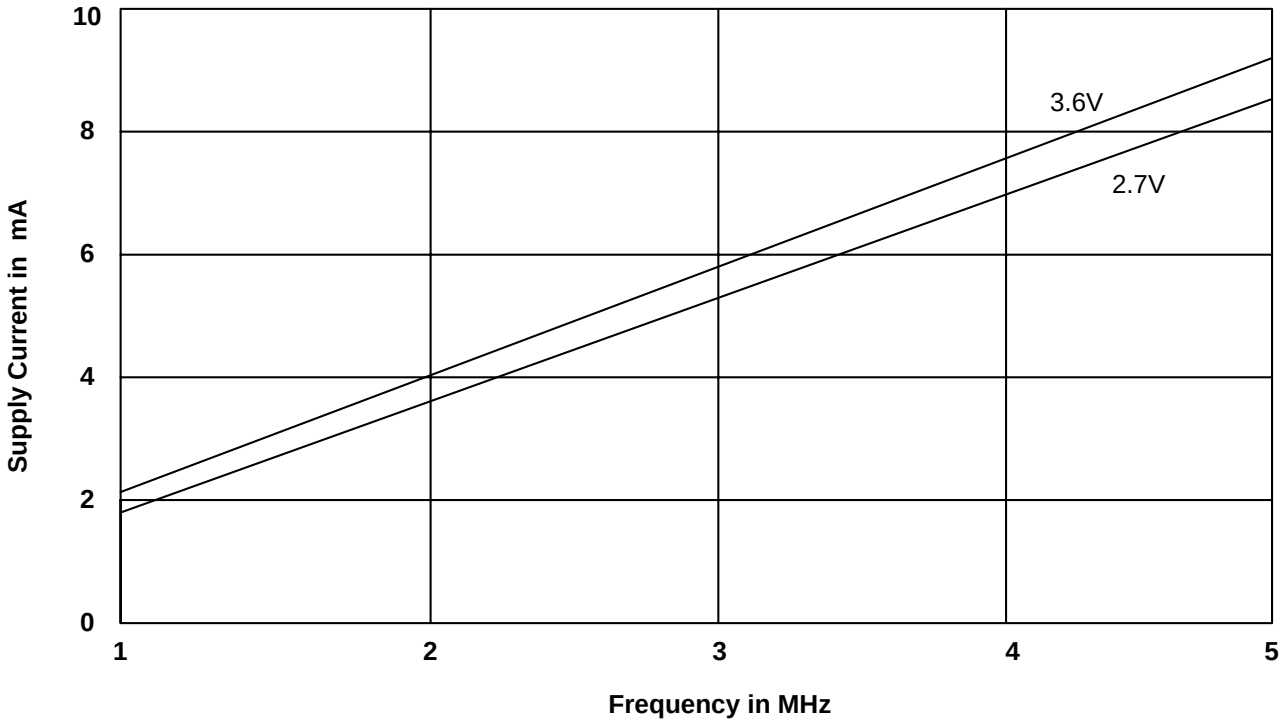
DC Characteristics (continued)

Zero Power Flash



Note: Addresses are switching at 1MHz

I_{CC1} Current vs. Time (Showing Active and Automatic Sleep Currents)



Note : T = 25°C

Typical I_{CC1} vs. Frequency

AC Characteristics

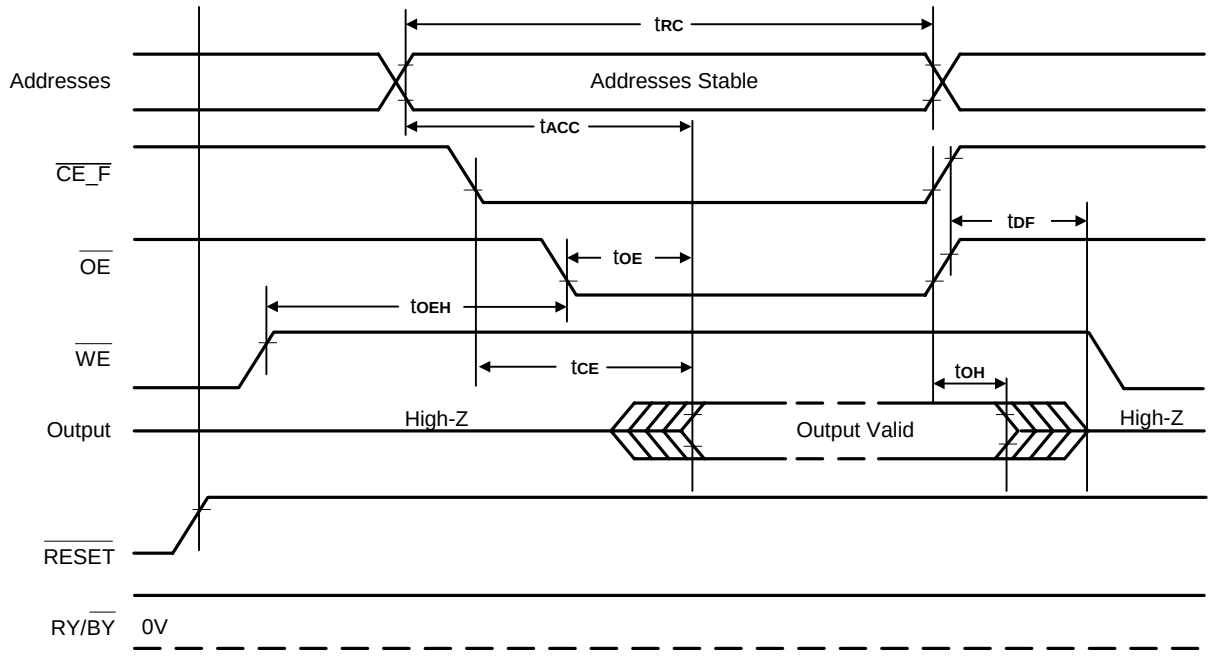
Read Only Operations (T_A=0°C to 70°C or -25°C to + 85°C for –I)

Parameter Symbols		Description		Test Setup		Speed	Unit
JEDEC	Std					-70	
t_{AVAV}	t_{RC}	Read Cycle Time (Note 1)			Min.	70	ns
t_{AVQV}	t_{ACC}	Address to Output Delay		$\overline{CE_F}$ = V_{IL} $\overline{OE}$ = V_{IL}	Max.	70	ns
t_{ELQV}	T_{CE_F}	Chip Enable to Output Delay		$\overline{OE}$ = V_{IL}	Max.	70	ns
t_{GLQV}	t_{OE}	Output Enable to Output Delay			Max.	30	ns
	t_{OEH}	Output Enable Hold Time (Note 1)	Read		Min.	0	ns
			Toggle and $\overline{Data}$ Polling		Min.	10	ns
t_{EHQZ}	t_{DF}	Chip Enable to Output High Z (Notes 1)			Max.	25	ns
t_{GHQZ}	t_{DF}	Output Enable to Output High Z (Notes 1)				25	ns
t_{AXQX}	t_{OH}	Output Hold Time from Addresses, $\overline{CE}$ or $\overline{OE}$, Whichever Occurs First (Note 1)			Min.	0	ns

Notes:

1. Not 100% tested.
2. See Test Conditions and Test Setup for test specifications.

Timing Waveforms for Read Only Operation



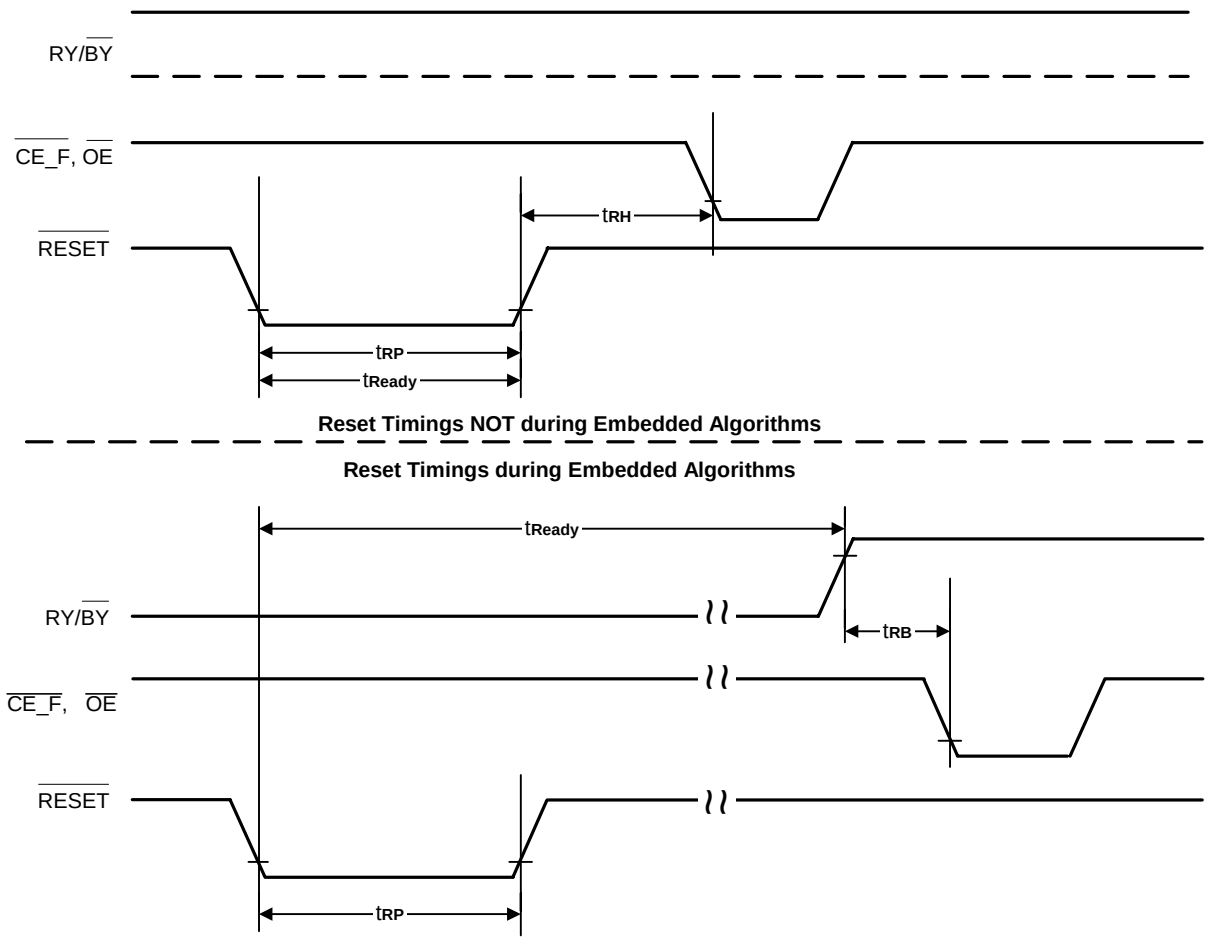
AC Characteristics

Hardware Reset ($\overline{RESET}$) (T_A=0°C to 70°C or -25°C to + 85°C for –I)

Parameter		Description	Test Setup		All Speed Options	Unit
JEDEC	Std					
	t_{READY}	$\overline{RESET}$ Pin Low (During Embedded Algorithms) to Read or Write (See Note)		Max	20	µs
	t_{READY}	$\overline{RESET}$ Pin Low (Not During Embedded Algorithms) to Read or Write (See Note)		Max	500	ns
	t_{RP}	$\overline{RESET}$ Pulse Width		Min	500	ns
	t_{RH}	$\overline{RESET}$ High Time Before Read (See Note)		Min	50	ns
	t_{RB}	RY/$\overline{BY}$ Recovery Time		Min	0	ns
	t_{RPD}	$\overline{RESET}$ Low to Standby Mode		Min	20	µs

Note: Not 100% tested.

$\overline{RESET}$ Timings

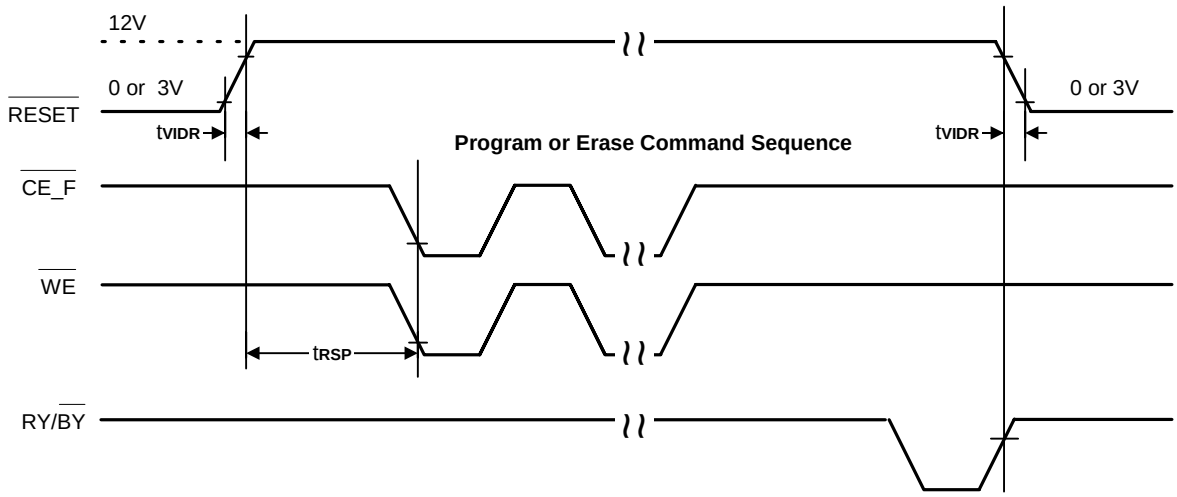


Temporary Sector Unprotect (T_A=0°C to 70°C or -25°C to + 85°C for –I)

Parameter		Description		All Speed Options	Unit
JEDEC	Std				
	t_{VIDR}	V_{ID} Rise and Fall Time (See Note)	Min	500	ns
	t_{RSP}	$\overline{\text{RESET}}$ Setup Time for Temporary Sector Unprotect	Min	4	µs

Note: Not 100% tested.

Temporary Sector Unprotect Timing Diagram

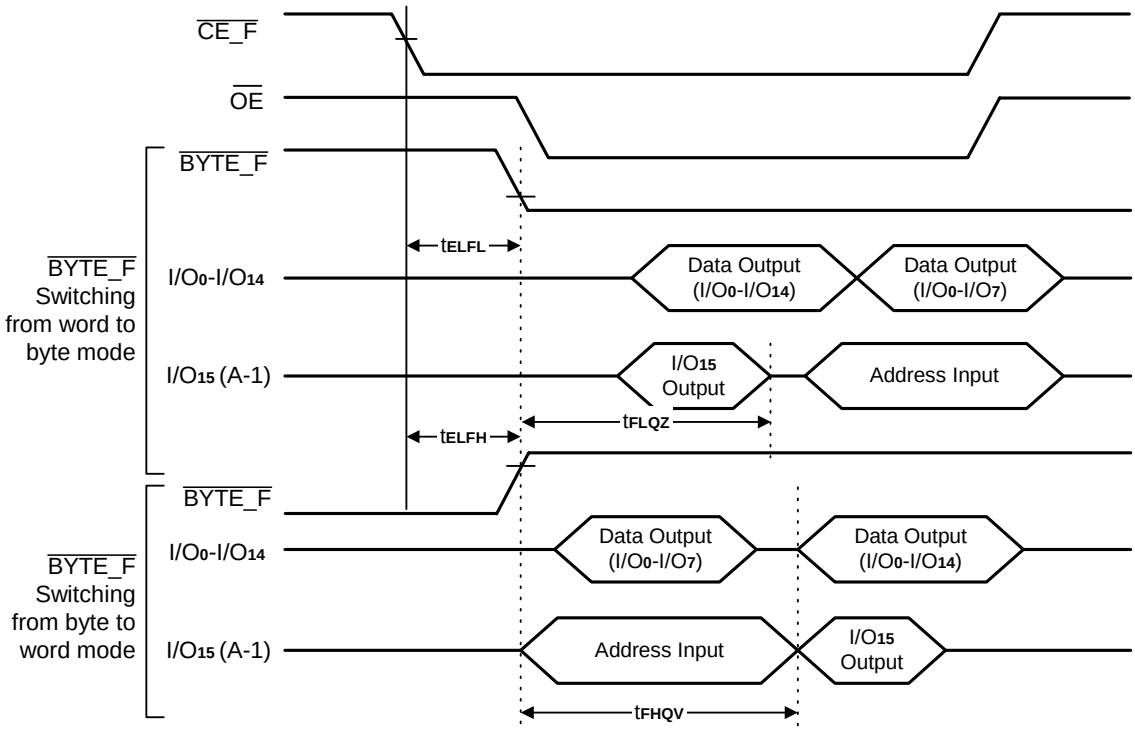


AC Characteristics

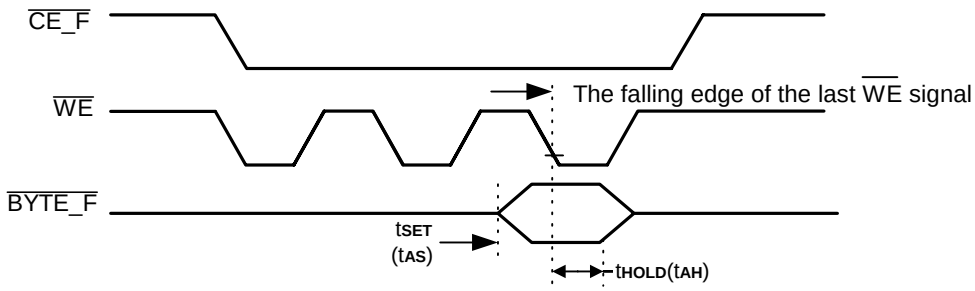
Word/Byte Configuration ($\overline{BYTE_F}$) (T_A=0°C to 70°C or -25°C to + 85°C for – I)

Parameter		Description		Speed Option	Unit
JEDEC	Std			-70	
	t_{ELFL}/t_{ELFH}	$\overline{CE_F}$ to $\overline{BYTE_F}$ Switching Low or High	Max	5	ns
	t_{FLQZ}	$\overline{BYTE_F}$ Switching Low to Output High-Z	Max	25	ns
	t_{HQV}	$\overline{BYTE_F}$ Switching High to Output Active	Min	70	ns

$\overline{BYTE_F}$ Timings for Read Operations



$\overline{BYTE_F}$ Timings for Write Operations



Note:
Refer to the Erase/Program Operations table for t_{AS} and t_{AH} specifications.

AC Characteristics

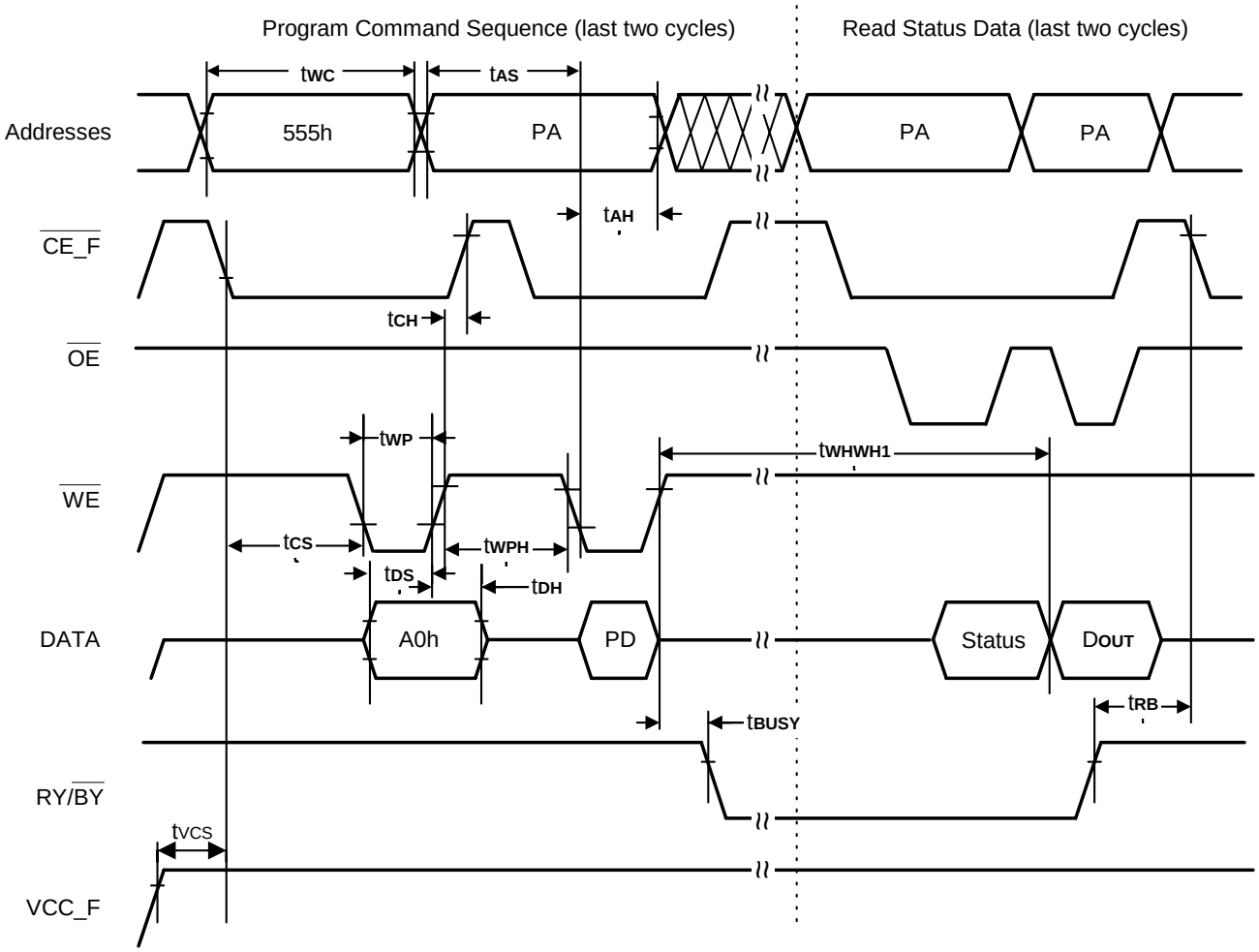
Erase and Program Operations (T_A=0°C to 70°C or -25°C to + 85°C for –I)

Parameter		Description			Speed	Unit
JEDEC	Std				-70	
t_{AVAV}	t_{WC}	Write Cycle Time (Note 1)		Min.	70	ns
t_{AVWL}	t_{AS}	Address Setup Time		Min.	0	ns
t_{WLAX}	t_{AH}	Address Hold Time		Min.	45	ns
t_{DVWH}	t_{DS}	Data Setup Time		Min.	35	ns
t_{WHDX}	t_{DH}	Data Hold Time		Min.	0	ns
	t_{OES}	Output Enable Setup Time		Min.	0	ns
t_{GHWL}	t_{GHWL}	Read Recover Time Before Write ($\overline{OE}$ high to $\overline{WE}$ low)		Min.	0	ns
t_{ELWL}	t_{CS}	$\overline{CE_F}$ Setup Time		Min.	0	ns
t_{WHEH}	t_{CH}	$\overline{CE_F}$ Hold Time		Min.	0	ns
t_{WLWH}	t_{WP}	Write Pulse Width		Min.	35	ns
t_{WHWL}	t_{WPH}	Write Pulse Width High		Min.	30	ns
t_{WHWH1}	t_{WHWH1}	Byte Programming Operation (Note 2)	Byte	Typ.	5	µs
			Word	Typ.	7	
t_{WHWH2}	t_{WHWH2}	Sector Erase Operation (Note 2)		Typ.	0.7	sec
	t_{VCS}	VCC_F Set Up Time (Note 1)		Min.	50	µs
	t_{RB}	Recovery Time from RY/$\overline{BY}$		Min	0	ns
	t_{BUSY}	Program/Erase Valid to RY/$\overline{BY}$ Delay		Min	90	ns

Notes:

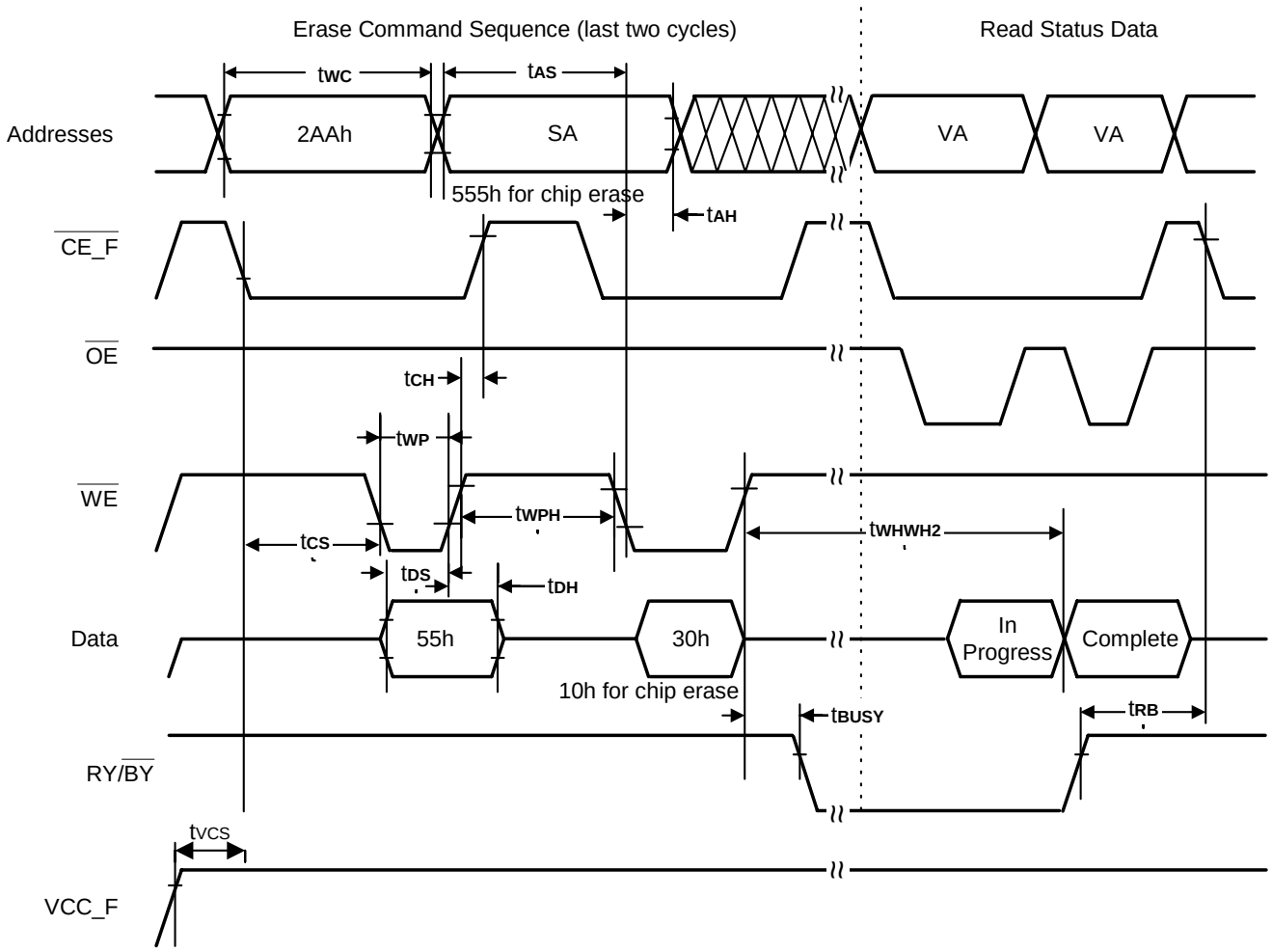
1. Not 100% tested.
2. See the "Erase and Programming Performance" section for more information.

Timing Waveforms for Program Operation



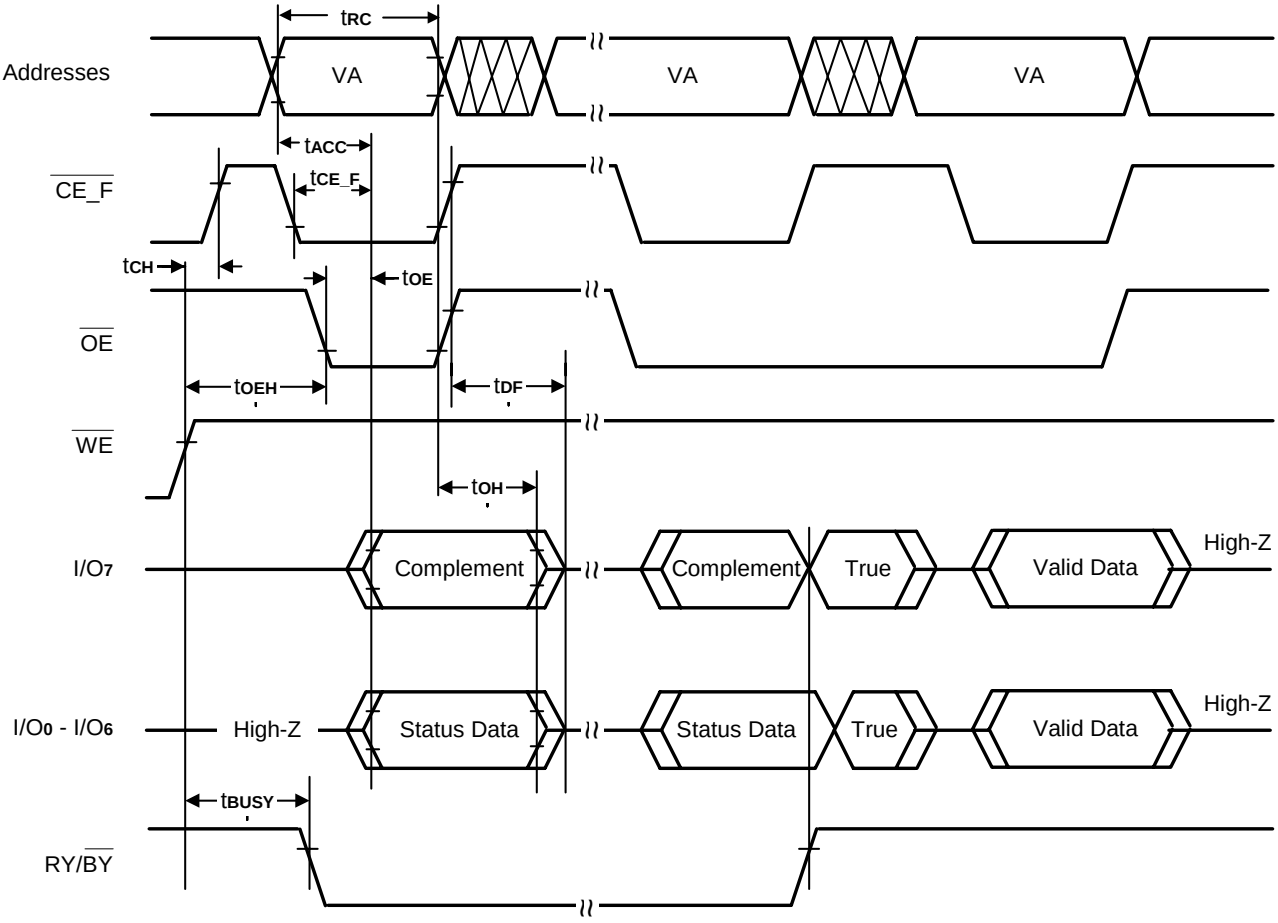
Note :
1. PA = program addrss, PD = program data, Dout is the true data at the program address.
2. Illustration shows device in word mode.

Timing Waveforms for Chip/Sector Erase Operation



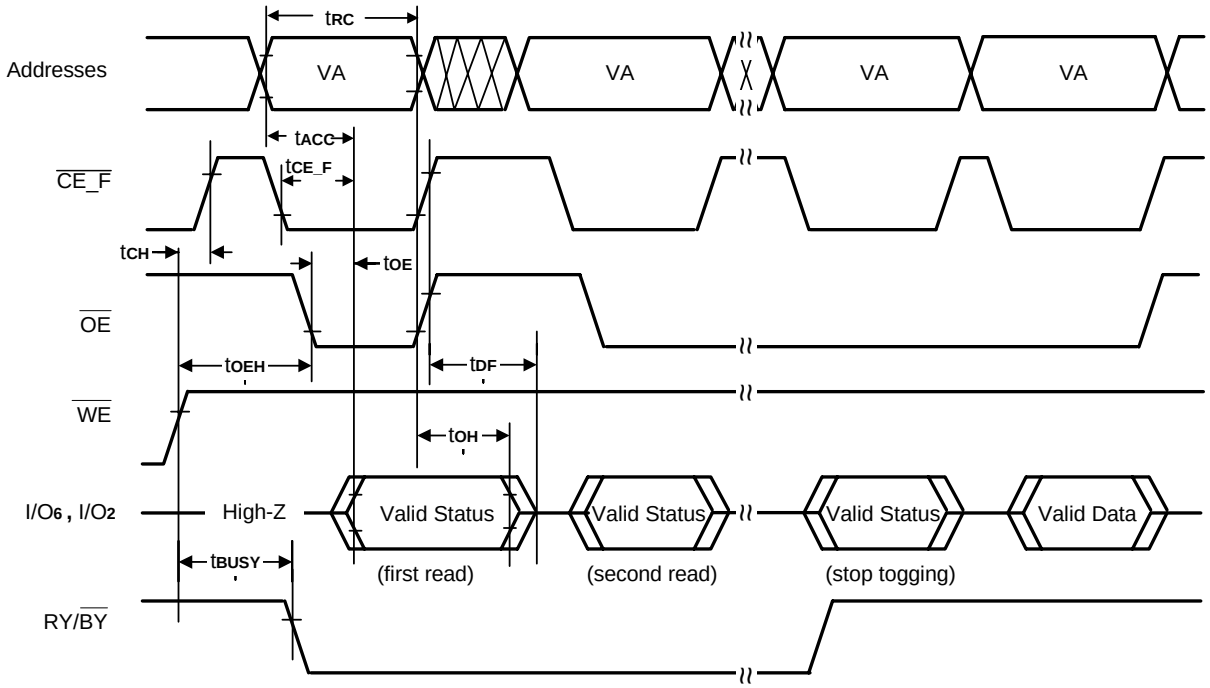
Note :
1. SA = Sector Address (for Sector Erase), VA = Valid Address for reading status data (see "Write Operaion Ststus").
2. Illustratin shows device in word mode.

Timing Waveforms for $\overline{\text{Data}}$ Polling (During Embedded Algorithms)



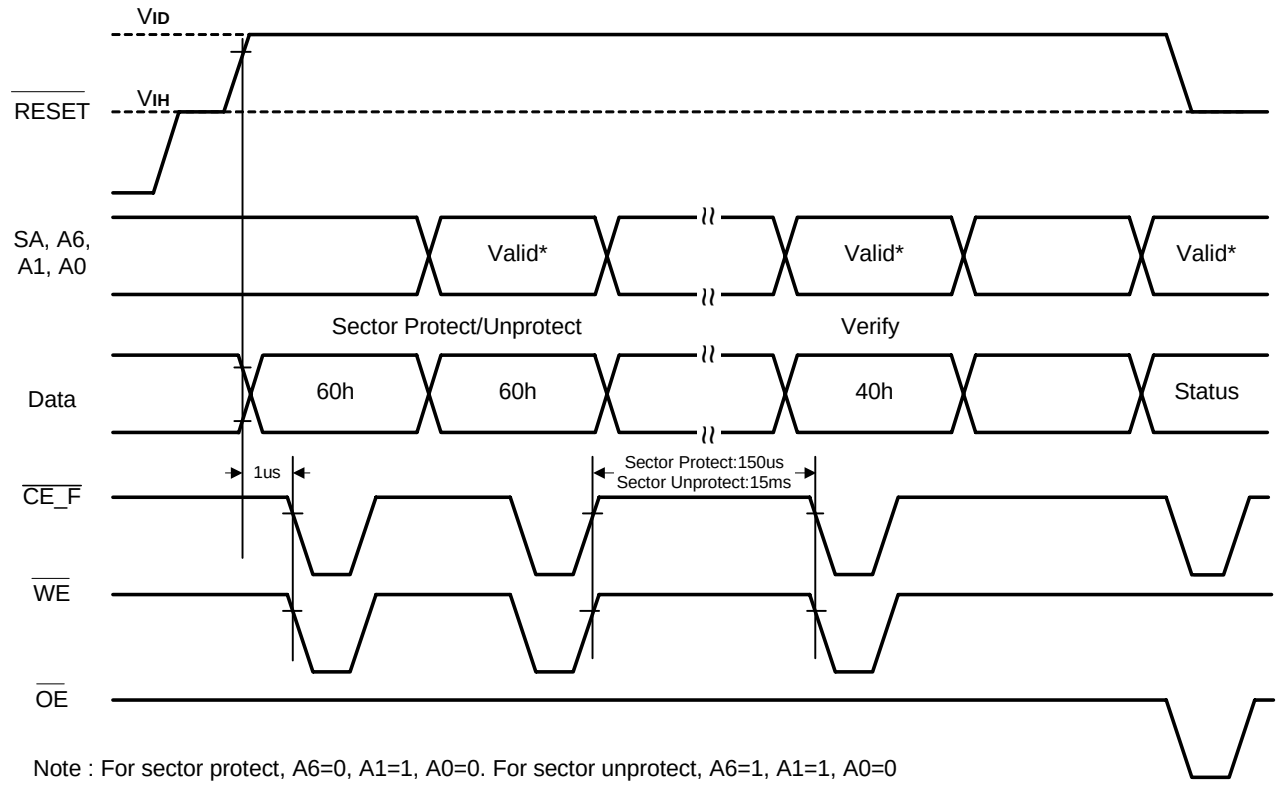
Note : VA = Valid Address. Illustation shows first status cycle after command sequence, last status read cycle, and array data read cycle.

Timing Waveforms for Toggle Bit (During Embedded Algorithms)



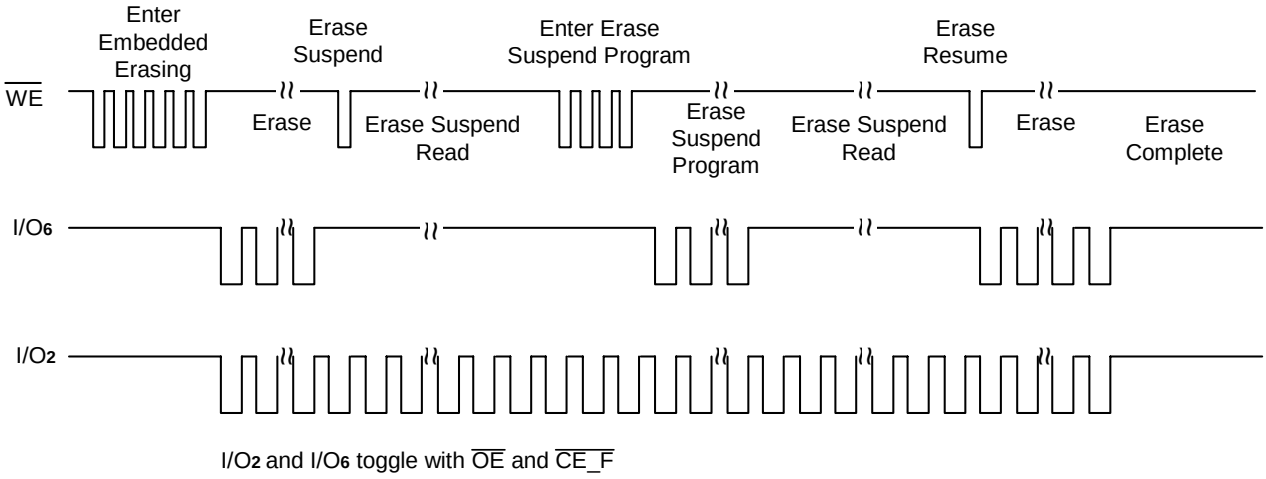
Note: VA = Valid Address; not required for I/O6. Illustration shows first two status cycle after command sequence, last status read cycle, and array data read cycle.

Timing Waveforms for Sector Protect/Unprotect



Note : For sector protect, A6=0, A1=1, A0=0. For sector unprotect, A6=1, A1=1, A0=0

Timing Waveforms for I/O2 vs. I/O6



Note : Both I/O6 and I/O2 toggle with $\overline{OE}$ or $\overline{CE_F}$. See the text on I/O6 and I/O2 in the section "Write Operation Status" for more information.

AC Characteristics

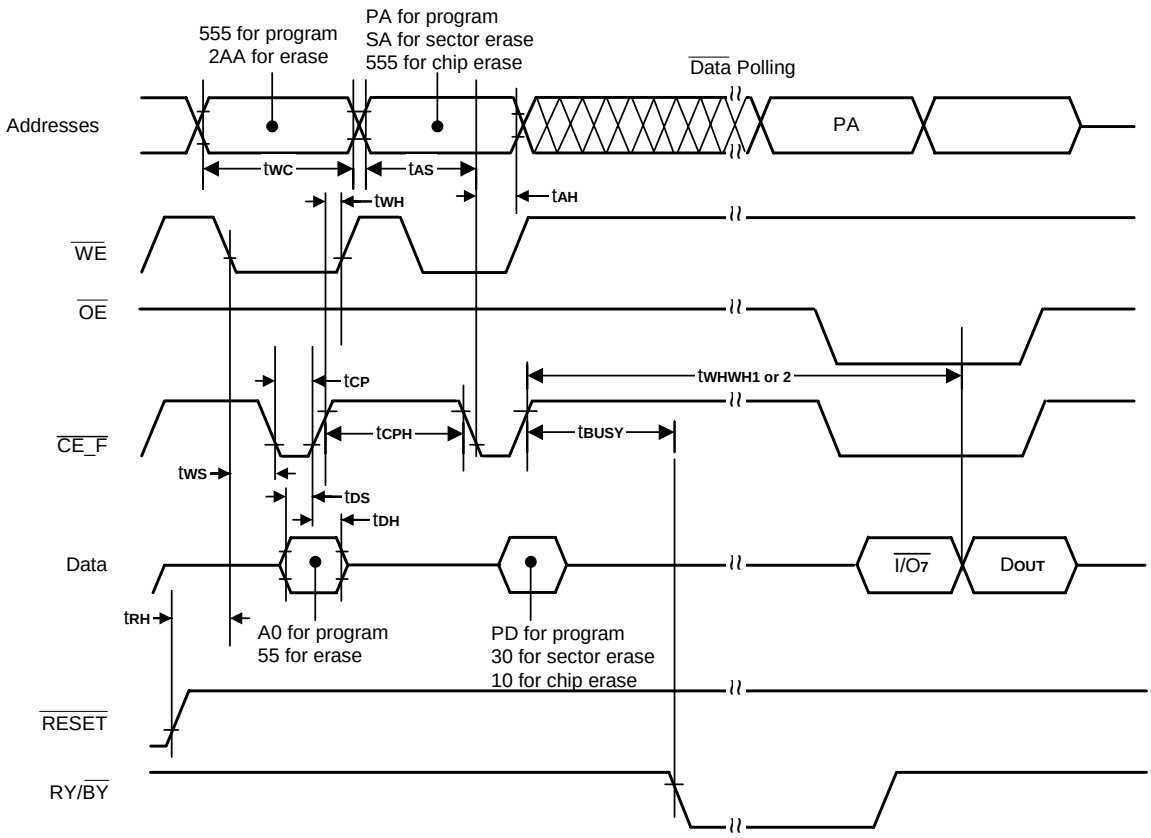
Erase and Program Operations

Alternate $\overline{CE_F}$ Controlled Writes (T_A=0°C to 70°C or -25°C to + 85°C for –I)

Parameter		Description		Speed	Unit
JEDEC	Std			-70	
t_{AVAV}	t_{WC}	Write Cycle Time (Note 1)	Min.	70	ns
t_{AVEL}	t_{AS}	Address Setup Time	Min.	0	ns
t_{ELAX}	t_{AH}	Address Hold Time	Min.	45	ns
t_{DVEH}	t_{DS}	Data Setup Time	Min.	35	ns
t_{EHDX}	t_{DH}	Data Hold Time	Min.	0	ns
	t_{OES}	Output Enable Setup Time	Min.	0	ns
t_{GHEL}	t_{GHEL}	Read Recover Time Before Write ($\overline{OE}$ High to $\overline{WE}$ Low)	Min.	0	ns
t_{WLEL}	t_{WS}	$\overline{WE}$ Setup Time	Min.	0	ns
t_{EHWH}	t_{WH}	$\overline{WE}$ Hold Time	Min.	0	ns
t_{ELEH}	t_{CP}	$\overline{CE}$ Pulse Width	Min.	35	ns
t_{EHEL}	t_{CPH}	$\overline{CE}$ Pulse Width High	Min.	30	ns
t_{WHWH1}	t_{WHWH1}	Programming Operation (Note 2) — Byte	Typ.	5	µs
		Word	Typ.	7	
t_{WHWH2}	t_{WHWH2}	Sector Erase Operation (Note 2)	Typ.	0.7	sec

Notes:
1. Not 100% tested.
2. See the "Erase and Programming Performance" section for more information.

Timing Waveforms for Alternate $\overline{CE_F}$ Controlled Write Operation



Note :
1. PA = Program Address, PD = Program Data, SA = Sector Address, $\overline{I/O7}$ = Complement of Data Input, D_{OUT} = Array Data.
2. Figure indicates the last two bus cycles of the command sequence.

Erase and Programming Performance

Parameter		Typ. (Note 1)	Max. (Note 2)	Unit	Comments
Sector Erase Time		1.0	8	sec	Excludes 00h programming prior to erasure
Chip Erase Time		35		sec	
Byte Programming Time		35	300	µs	Excludes system-level overhead (Note 5)
Word Programming Time		12	500	µs	
Chip Programming Time (Note 3)	Byte Mode	11	33	sec	
	Word Mode	7.2	21.6	sec	

Notes:
1. Typical program and erase times assume the following conditions: 25°C, 3.0V VCC_F, 10,000 cycles. Additionally, programming typically assumes checkerboard pattern.
2. Under worst case conditions of 90°C, VCC_F = 2.7V, 100,000 cycles.
3. The typical chip programming time is considerably less than the maximum chip programming time listed, since most bytes program faster than the maximum byte program time listed. If the maximum byte program time given is exceeded, only then does the device set I/O_5 = 1. See the section on I/O_5 for further information.
4. In the pre-programming step of the Embedded Erase algorithm, all bytes are programmed to 00h before erasure.
5. System-level overhead is the time required to execute the four-bus-cycle command sequence for programming. See Table 5 for further information on command definitions.
6. The device has a guaranteed minimum erase and program cycle endurance of 10,000 cycles.

SRAM

DC Electrical Characteristics (TA = -25°C to +85°C, VCC_S = 2.7V to 3.6V, GND = 0V)

Symbol	Parameter	70ns		Unit	Conditions
		Min.	Max.		
$\lvert I_{LI} \rvert$	Input Leakage Current	-	1	μA	V_{IN} = GND to VCC_S
$\lvert I_{LO} \rvert$	Output Leakage Current	-	1	μA	$\overline{CE_S}$ = V_{IH} or $\overline{OE}$ = V_{IH} or $\overline{WE}$ = V_{IL} $V_{I/O}$ = GND to VCC_S
I_{CC}	Active Power Supply Current	-	3	mA	$\overline{CE_S}$ = V_{IL} $I_{I/O}$ = 0mA
I_{CC1}	Dynamic Operating Current	-	30	mA	Min. Cycle, Duty = 100% $\overline{CE_S}$ = V_{IL}, CE2 = V_{IH} $I_{I/O}$ = 0mA
I_{CC2}		-	3	mA	$\overline{CE_S}$ = V_{IL} V_{IH} = VCC_S, V_{IL} = 0V f = 1 MHz, $I_{I/O}$ = 0mA
I_{SB}	Standby Power Supply Current	-	0.5	mA	VCC_S ≤ 3.3V, $\overline{CE_S}$ = V_{IH}
I_{SB1}		-	5	μA	VCC_S ≤ 3.3V, $\overline{CE_S}$ ≥ VCC_S - 0.2V or V_{IN} ≥ 0V
V_{OL}	Output Low Voltage	-	0.4	V	I_{OL} = 2.1mA
V_{OH}	Output High Voltage	2.2	-	V	I_{OH} = -1.0mA

Truth Table

Mode	$\overline{CE_S}$	$\overline{OE}$	$\overline{WE}$	I/O Operation	Supply Current
Standby	H	X	X	High Z	I_{SB}, I_{SB1}
	X	X	X	High Z	I_{SB}, I_{SB1}
Output Disable	L	H	H	High Z	I_{CC}, I_{CC1}, I_{CC2}
Read	L	L	H	D_{OUT}	I_{CC}, I_{CC1}, I_{CC2}
Write	L	X	L	D_{IN}	I_{CC}, I_{CC1}, I_{CC2}

Note: X = H or L

Capacitance (T_A = 25°C, f = 1.0MHz)

Symbol	Parameter	Min.	Max.	Unit	Conditions
C_{IN}*	Input Capacitance		6	pF	V_{IN} = 0V
$C_{I/O}$*	Input/Output Capacitance		8	pF	$V_{I/O}$ = 0V

*** These parameters are sampled and not 100% tested.**

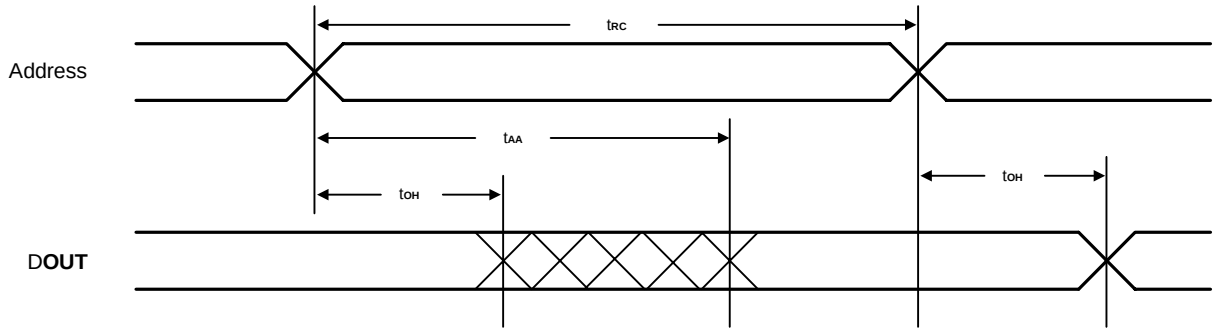
AC Characteristics (T_A = -25°C to +85°C, VCC_S = 2.7V to 3.6V)

Symbol	Parameter		70 ns		Unit
			Min.	Max.	
Read Cycle					
t_{RC}	Read Cycle Time		70	-	ns
t_{AA}	Address Access Time		-	70	ns
t_{ACE1_S}	Chip Enable Access Time	$\overline{CE_S}$	-	70	ns
t_{OE}	Output Enable to Output Valid		-	35	ns
t_{CLZ1}	Chip Enable to Output in Low Z	$\overline{CE_S}$	10	-	ns
t_{OLZ}	Output Enable to Output in Low Z		5	-	ns
t_{CHZ1}	Chip Disable to Output in High Z	$\overline{CE_S}$	0	25	ns
t_{OHZ}	Output Disable to Output in High Z		0	25	ns
t_{OH}	Output Hold from Address Change		10	-	ns
Write Cycle					
t_{WC}	Write Cycle Time		70	-	ns
t_{CW}	Chip Enable to End of Write		60	-	ns
t_{AS}	Address Setup Time		0	-	ns
t_{AW}	Address Valid to End of Write		60	-	ns
t_{WP}	Write Pulse Width		50	-	ns
t_{WR}	Write Recovery Time		0	-	ns
t_{WHZ}	Write to Output in High Z		0	25	ns
t_{DW}	Data to Write Time Overlap		30	-	ns
t_{DH}	Data Hold from Write Time		0	-	ns
t_{OW}	Output Active from End of Write		5	-	ns

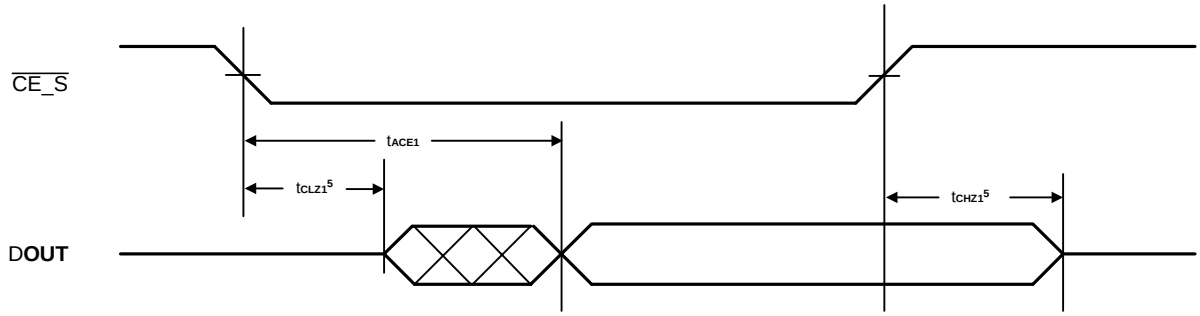
Notes: t_{CHZ1}, t_{OHZ}, and t_{WHZ} are defined as the time at which the outputs achieve the open circuit condition and are not referred to output voltage levels.

SRAM Timing Waveforms

Read Cycle 1 (1, 2, 4)

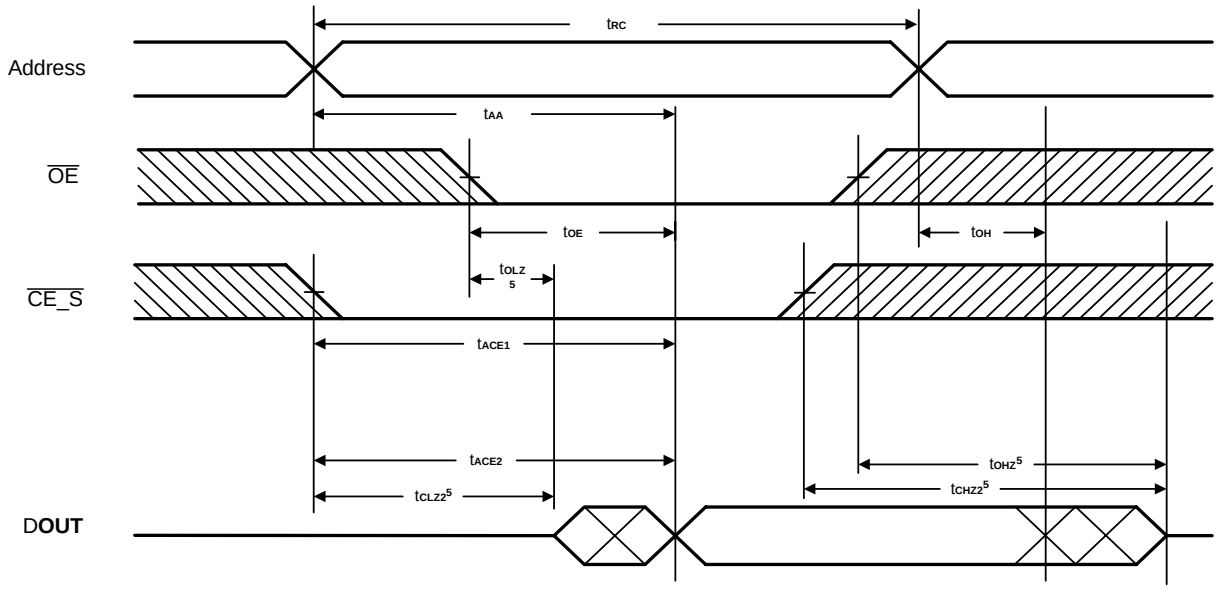


Read Cycle 2 (1, 3, 4, 6)



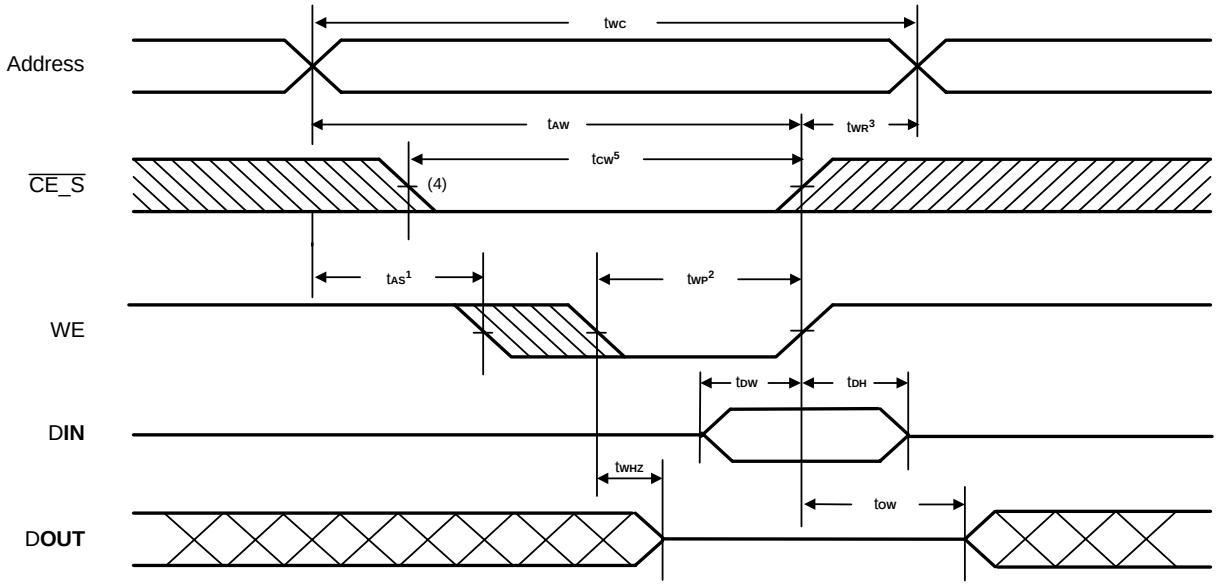
Timing Waveforms (continued)

Read Cycle 3 (1)



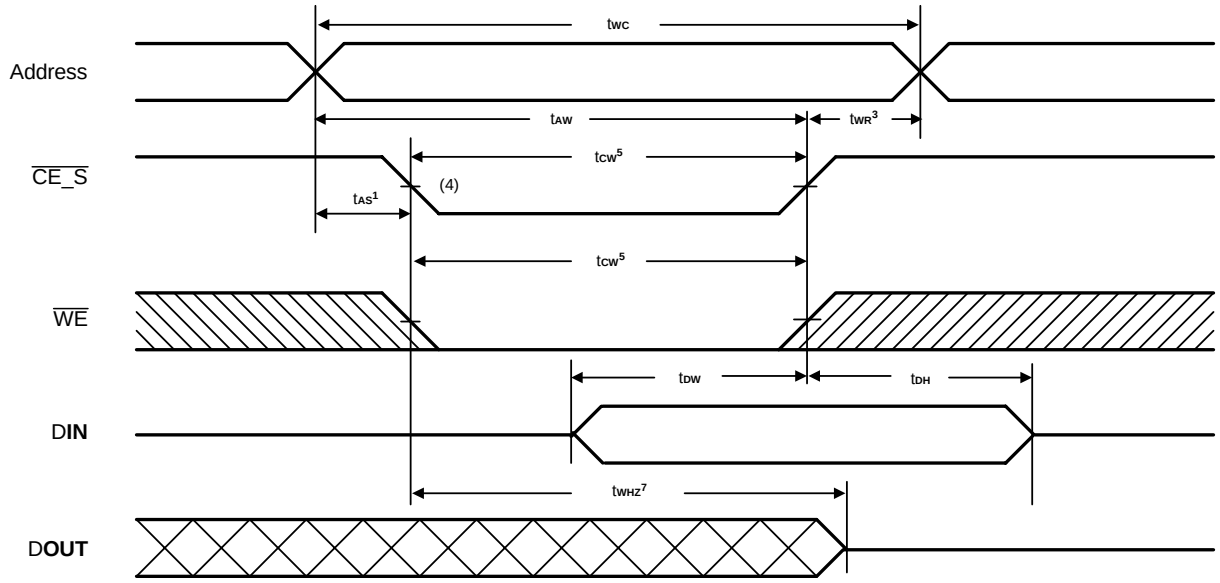
Notes: 1. $\overline{WE}$ is high for Read Cycle.
2. Device is continuously enabled $\overline{CE_S}$ = V_{IL}.
3. Address valid prior to or coincident with $\overline{CE_S}$ transition low.
4. $\overline{OE}$ = V_{IL}.
5. Transition is measured ±500mV from steady state. This parameter is sampled and not 100% tested.
6. $\overline{CE_S}$ is low.

Write Cycle 1 (6)
(Write Enable Controlled)



Timing Waveforms (continued)

Write Cycle 2
(Chip Enable Controlled)



Notes: 1. t_{AS} is measured from the address valid to the beginning of Write.
2. A Write occurs during the overlap (t_{WP}) of a low $\overline{CE_S}$, and a low $\overline{WE}$.
3. t_{WR} is measured from the earliest of $\overline{CE_S}$ or $\overline{WE}$ going high going low to the end of the Write cycle.
4. If the $\overline{CE_S}$ low transition occurs simultaneously with the $\overline{WE}$ low transition or after the $\overline{WE}$ transition, outputs remain in a high impedance state.
5. t_{CW} is measured from the later of $\overline{CE_S}$ going low going high to the end of Write.
6. $\overline{OE}$ is continuously low. ($\overline{OE}$ = V_{IL})
7. Transition is measured ±500mV from steady state. This parameter is sampled and not 100% tested.

AC Test Conditions

Input Pulse Levels	0.4V to 2.4V
Input Rise and Fall Time	5 ns
Input and Output Timing Reference Levels	1.5V
Output Load	See Figures 7 and 8

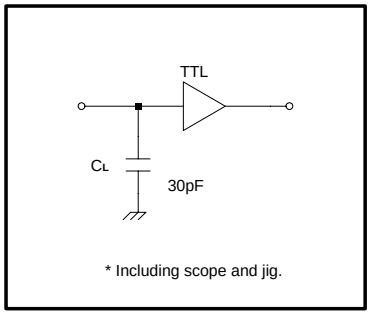


Figure 7. Output Load

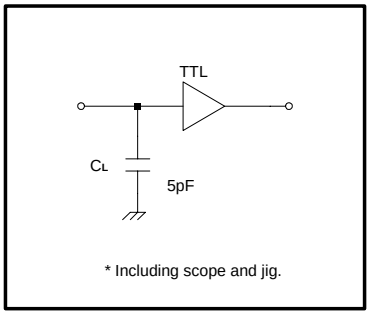


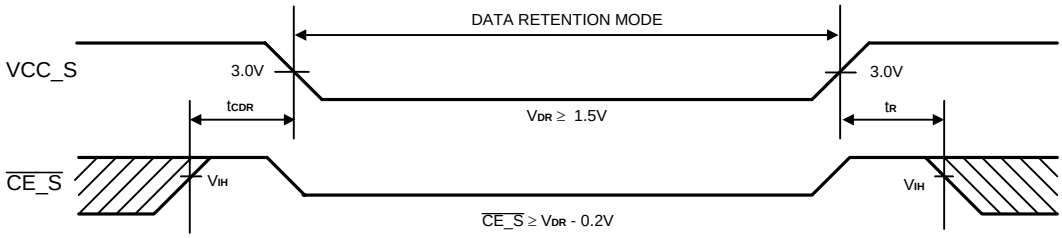
Figure 8. Output Load for t_{CLZ1}, t_{CLZ2}, t_{OHZ}, t_{OLZ}, t_{CHZ1} t_{WHZ}, and t_{OW}

Retention Characteristics (T_A = -25°C to 85°C)

Symbol	Parameter	Min.	Max.	Unit	Conditions
V_{DR1}	VCC for Data Retention	2.0	3.6	V	$\overline{CE_S}$ ≥ VCC_S - 0.2V
I_{CCDR1}	Data Retention Current	-	1*	μA	VCC_S = 1.5V, $\overline{CE_S}$ ≥ VCC - 0.2V, V_{IN} ≥ 0V
I_{CCDR2}		-	1*	μA	VCC_S = 1.5V, V_{IN} ≥ 0V
t_{CDR}	Chip Disable to Data Retention Time	0	-	ns	See Retention Waveform
t_R	Operation Recovery Time	5	-	ms	

* 55 ns – 70 ns I_{CCDR}: max. 1μA at T_A = 0°C to + 40°C

Low VCC Data Retention Waveform (1) ($\overline{CE_S}$ Controlled)



Ordering Information

Top Boot Sector Flash & SRAM

Part No.	Access Time (ns)	Active Read Current Typ. (mA)	Program/Erase Current Typ. (mA)	Standby Current Typ. (μA)	Package
A81L801TG-70	70	9	20	0.2	69-ball FBGA
A81L801TG-70F					69-ball Pb-Free FBGA
A81L801TG-70I					69-ball FBGA
A81L801TG-70IF					69-ball Pb-Free FBGA

Note: Industrial operating temperature range: -25°C to 85°C for –I

Bottom Boot Sector Flash & SRAM

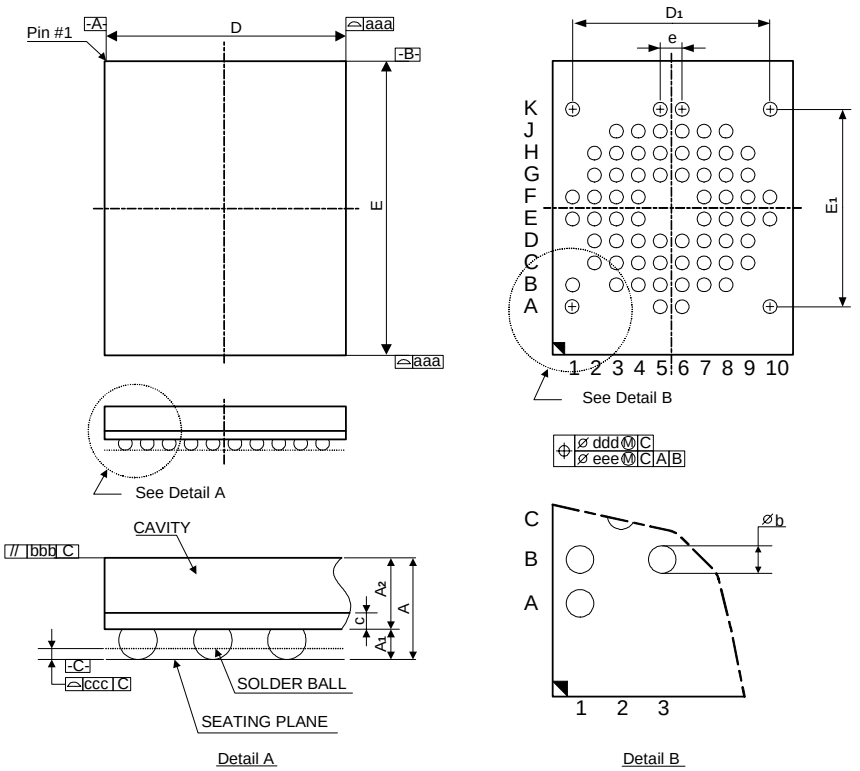
Part No.	Access Time (ns)	Active Read Current Typ. (mA)	Program/Erase Current Typ. (mA)	Standby Current Typ. (μA)	Package
A81L801UG-70	70	9	20	0.2	69-ball FBGA
A81L801UG-70F					69-ball Pb-Free FBGA
A81L801UG-70I					69-ball FBGA
A81L801UG-70IF					69-ball Pb-Free FBGA

Note: Industrial operating temperature range: -25°C to 85°C for –I

Package Information

69LD STF BGA (8 x 11mm) Outline Dimensions

unit: mm



Symbol	Dimensions in mm			Dimensions in inches		
	Min	Nom	Max	Min	Nom	Max
A	-	-	1.40	-	-	0.055
A1	0.25	0.30	0.35	0.010	0.012	0.014
A2	0.91	0.96	1.01	0.036	0.038	0.040
c	0.22	0.26	0.30	0.009	0.010	0.012
D	7.90	8.00	8.10	0.311	0.315	0.319
E	10.90	11.00	11.10	0.429	0.433	0.437
D1	-	7.20	-	-	0.283	-
E1	-	7.20	-	-	0.283	-
e	-	0.80	-	-	0.031	-
b	0.35	0.40	0.45	0.14	0.16	0.18
aaa	0.15			0.006		
bbb	0.20			0.008		
ccc	0.12			0.005		
ddd	0.15			0.006		
eee	0.08			0.003		
MD/ME	10/10			10/10		

Notes:

1. PRIMARY DATUM C AND SEATING PLANE ARE DEFINED BY THE SPHERICAL CROWNS OF THE SOLDER BALLS.
2. DIMENSION b IS MEASURED AT THE MAXIMUM SOLDER BALL DIAMETER, PARALLEL TO PRIMARY DATUM C.
3. THERE SHALL BE A MINIMUM CLEARANCE OF 0.25mm BETWEEN THE EDGE OF THE SOLDER BALL AND THE BODY EDGE.
4. REFERENCE DOCUMENT : JEDEC MO-219
5. THE PATTERN OF PIN 1 FIDUCIAL IS FOR REFERENCE ONLY.