ISL88041

Quad Voltage Monitor

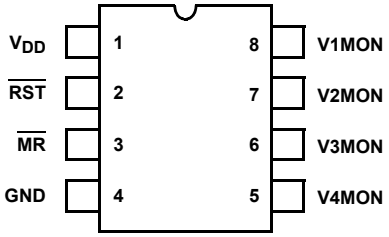
FN9229
Rev 2.00
April 29, 2010

The ISL88041 is a quad voltage-monitoring supervisor designed to monitor voltages ≥0.7V. Low voltage detection circuitry protects the user 's system from low voltage conditions, resetting the system when any of the monitored power supply voltages V1MON-V4MON fall below their respective minimum voltage thresholds. The reset signal remains asserted until all of these voltages return to proper operating levels and stabilize.

Each rail's VMON point is independently adjustable by using an external resistor divider. The VMON inputs will ignore transients of less than 30µs on the monitored supplies, and the $\overline{RST}$ output is guaranteed to be valid down to V_{DD} = 1V. The $\overline{RST}$ output is open-drain to allow ORing of multiple signals and interfacing to a wide range of logic levels. Also, the $\overline{MR}$ input allows the user to assert reset when this input is pulled low.

Pinout

ISL88041
(8 LD SOIC)
TOP VIEW



Features

- Quad Voltage Monitoring
- Adjustable Voltage Inputs Monitor Voltages ≥0.7V
- Active-Low $\overline{RST}$ Output
- Manual Reset Capability
- Reset Signal Valid Down to V_{DD} = 1V
- Integrated 20kΩ Pull-Up Resistor on $\overline{RST}$
- Glitch Immunity on Voltage Monitoring Inputs
- Pb-Free (RoHS Compliant)

Applications

- Graphics Cards
- Multi Voltage DSPs and Processors
- µP Voltage Monitoring
- Embedded Control Systems
- Intelligent Instruments
- Medical Equipment
- Network Routers
- Portable Battery-Powered Equipment
- Set-Top Boxes
- Telecommunications Systems

Ordering Information

PART NUMBER (Note)	PART MARKING	TEMP. RANGE (°C)	PACKAGE (Pb-Free)	PKG. DWG. #
ISL88041IBZ*	88041 IBZ	-40 to +85	8 Ld SOIC (Pb-free)	M8.15

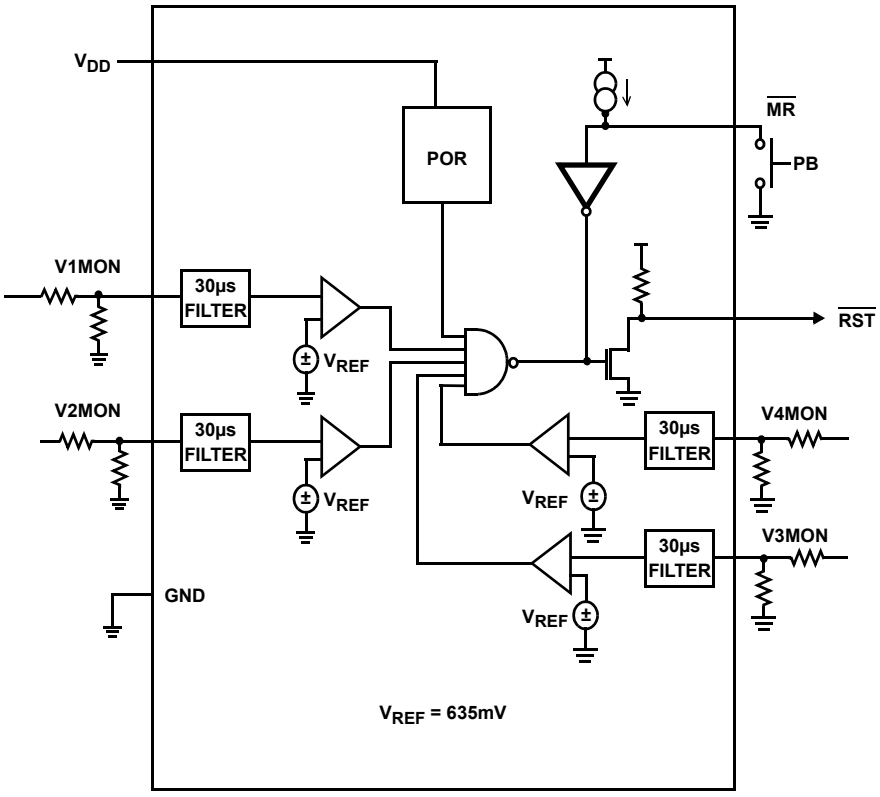
*Add "-T" suffix for tape and reel. Please refer to TB347 for details on reel specifications.

NOTE: These Intersil Pb-free plastic packaged products employ special Pb-free material sets, molding compounds/die attach materials, and 100% matte tin plate plus anneal (e3 termination finish, which is RoHS compliant and compatible with both SnPb and Pb-free soldering operations). Intersil Pb-free products are MSL classified at Pb-free peak reflow temperatures that meet or exceed the Pb-free requirements of IPC/JEDEC J STD-020.

Pin Descriptions

ISL88041	PIN NAME	FUNCTION DESCRIPTION
1	V_{DD}	Bias IC from nominal 2.7V to 4V.
2	$\overline{RST}$	Active-Low Open Drain Reset Output. Internal 20kΩ pull-up resistor to V_{DD}.
3	$\overline{MR}$	Active Low Open Drain $\overline{MR}$ Input has a 10µA pull-up to V_{DD}.
4	GND	Ground.
5	V4MON	Fourth Adjustable Undervoltage Monitor Input
6	V3MON	Third Adjustable Undervoltage Monitor Input
7	V2MON	Second Adjustable Undervoltage Monitor Input
8	V1MON	First Adjustable Undervoltage Monitor Input

Functional Block Diagram



Absolute Maximum Ratings

V_{DD} . . . . . +5.5V
VMON, $\overline{RST}$, $\overline{MR}$ . . . . . -0.3V to V_{DD}+0.3V
ESD Classification . . . . . 4kV (HBM)

Operating Conditions

V_{DD} Supply Voltage Range . . . . . +2.7V to +4V
Temperature Range (T_A) . . . . . -40°C to +85°C

Thermal Information

Thermal Resistance (Typical, Note 1)	θ_{JA} (°C/W)
8 Ld SOIC	108

Maximum Junction Temperature . . . . . +150°C
Maximum Storage Temperature Range . . . . . -65°C to +150°C
Pb-Free Reflow Profile. . . . . .see link below
http://www.intersil.com/pbfree/Pb-FreeReflow.asp

CAUTION: Do not operate at or near the maximum ratings listed for extended periods of time. Exposure to such conditions may adversely impact product reliability and result in failures not covered by warranty.

NOTES:

1. θ_{JA} is measured in free air with the component mounted on a high effective thermal conductivity test board. See Tech Brief TB379 for details.
2. All voltages are relative to GND, unless otherwise specified.

Electrical Specifications

V_{DD} = 3.3V, T_A = T_J = -40°C to +85°C, Unless Otherwise Specified.

SYMBOL	PARAMETER	TEST CONDITIONS	MIN (Note 3)	TYP	MAX (Note 3)	UNIT
BIAS						
V_{DD}	Supply Voltage Range		2.7		4.0	V
I_{DD}	V_{DD} Supply Current	VMON > V_{REF}		165	1000	µA
V_{DD_LO}	V_{DD} Lock Out	V_{DD} low to high		2.6		V
V_{DD_LOR}	V_{DD} Lock Out Reset	V_{DD} high to low		2.4		V
VMON						
V_{REF}	Adj. Reset Threshold Voltage		619	635	651	mV
$V_{REFHYST}$	Hysteresis of V_{REF}			10		mV
V_{REF_RNG}	Range	V_{REF} (max) - V_{REF} (min)		1.8		mV
t_{FIL}	Glitch Filter Duration	VMON glitch to $\overline{RST}$ low Filter		30		µs
$\overline{RESET}$						
I_{PD}	Pull-down Current	$\overline{RST}$ = 0.5V		2		mA
R_{PU}	Internal Pull-up Resistance			20		kΩ
V_{OL}	Output Low	V_{DD} = 1V		0.05	0.1	V
t_{RPD}	V_{TH} to Reset Asserted Delay	Last valid input = V_{TH} to $\overline{RST}$ release		1.5		µs
MANUAL RESET						
V_{MR}	$\overline{MR}$ Input Voltage	$\overline{MR}$ low to high threshold	0.4V_{DD}	0.5V_{DD}	0.6V_{DD}	V
V_{MRHYST}	Hysteresis of V_{MR}			0.065		V
I_{PU}	Pull-up Current	$\overline{MR}$ = 0.5V		10		µA
t_{MD}	$\overline{MR}$ to Deassert Reset Out Delay	$\overline{MR}$ high to $\overline{RST}$ release		50		ns
t_{MR}	$\overline{MR}$ to Assert Reset Out Delay	$\overline{MR}$ low to $\overline{RST}$ pulling low		15		ns

NOTE:

3. Parameters with MIN and/or MAX limits are 100% tested at +25°C, unless otherwise specified. Temperature limits established by characterization and are not production tested.

ISL88041 Description and Operation

The ISL88041 is a four voltage detection IC designed to monitor multiple voltages ≥0.7V. This IC is suitable for microprocessors or industrial system applications providing both reset and manual reset functions.

V_{DD} Lock Out

Applying power to the ISL88041 V_{DD} activates a lock out circuit which disables the reporting function until V_{DD} rises to ~2.6V. As V_{DD} bias is applied the $\overline{RST}$ output is held low before V_{DD} = 1V. If V_{DD} falls below ~2.4V the lock out of monitoring and reporting functions is invoked.

Low Voltage Monitoring

Once biased to 2.7V the IC continuously monitors and reports from one to four voltages independently through external resistor dividers comparing each VMON pin voltage to a nominal internal 0.635V reference. Once all VMON input voltages rise above this threshold, the $\overline{RST}$ output is immediately deasserted by being released to be pulled high via its internal 20kΩ (or optional external) pull resistor to V_{DD} indicating that all the minimum voltage conditions have been met (see Figure 4). The $\overline{RST}$ output is open-drain to allow ORing of signals and interfacing to a range of logic levels. Once any VMON input falls below its respective user-set threshold, the $\overline{RST}$ output is pulled low after the glitch filter delay (t_{FIL}) as the VMON inputs are designed to reject short undervoltage transients of approximately 30µs (see Figure 5). The user can customize the individual rail undervoltage threshold (V_{TRIP}) by connecting individual VMON pins to an external resistor divider according to the Equation 1:

$$V_{TRIP} = 0.635V(R1 + R2)/R2 \quad \text{(EQ. 1)}$$

See Figure 8 for a typical application configuration.

Manual Reset

The manual-reset input ($\overline{MR}$) allows the user to trigger a reset by using a push-button switch or by signaling the input low. Reset is asserted and deasserted immediately upon $\overline{MR}$ transitioning through $\overline{MR}_{VTH}$, see Figures 6 and 7.

Figure 1 is the operational timing diagram.

Using the ISL88041EVAL1

The ISL88041EVAL1 is the evaluation platform for this product and illustrates the flexibility and simplicity of monitoring four separate voltages. The $\overline{RST}$ output can be monitored once the V_{DD}, GND, and appropriate 3.3V, 2.5V, 1.8V and 1.2V supply voltage inputs are properly biased as labeled. A Manual Reset ($\overline{MR}$) input is also available for evaluation.

The circuit as shown in Figures 10 and 11 has resistor dividers chosen to monitor for an undervoltage threshold level of 89% of the 4 nominal voltages. Figure 1 illustrates the expected behavior and Figures 4 through 7 illustrate the actual IC performance in the ISL88041EVAL1.

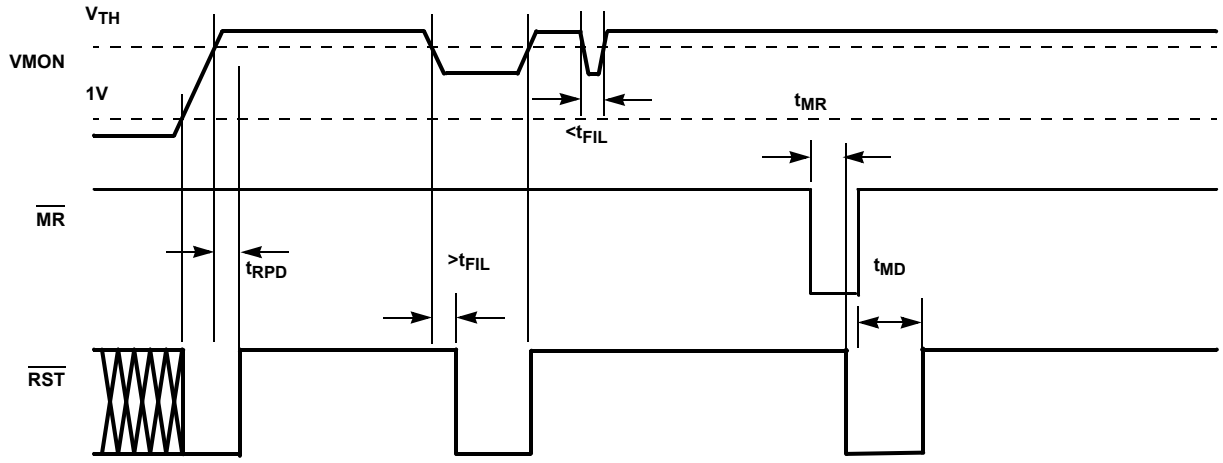


FIGURE 1. ISL88041 OPERATIONAL TIMING DIAGRAM

Typical Performance Curves

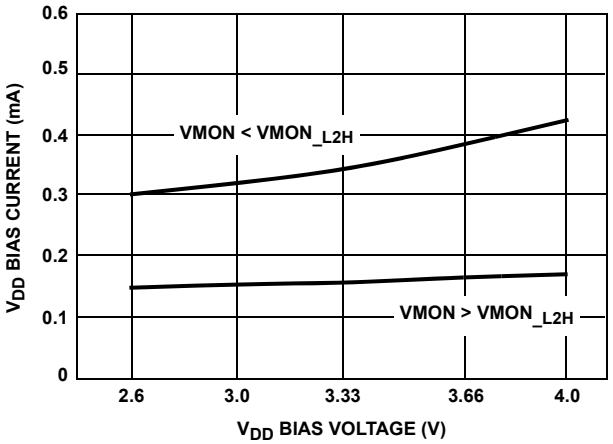


Figure 2 illustrates the idle and active bias currents levels.

FIGURE 2. V_{DD} CURRENT vs V_{DD} VOLTAGE

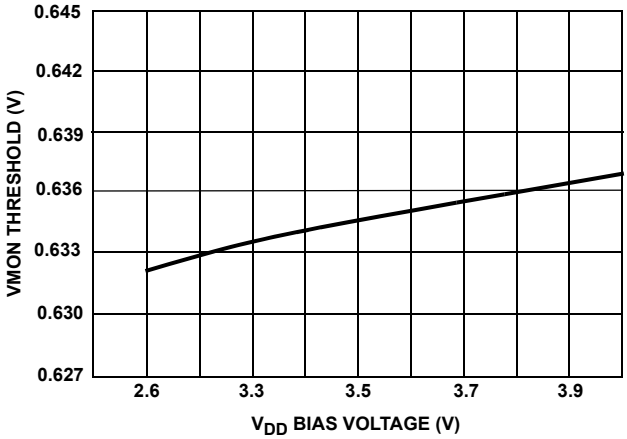


Figure 3 shows the VMON threshold shift over the bias range, demonstrating a PSRR of 105dB.

FIGURE 3. VMON THRESHOLD vs V_{DD} VOLTAGE

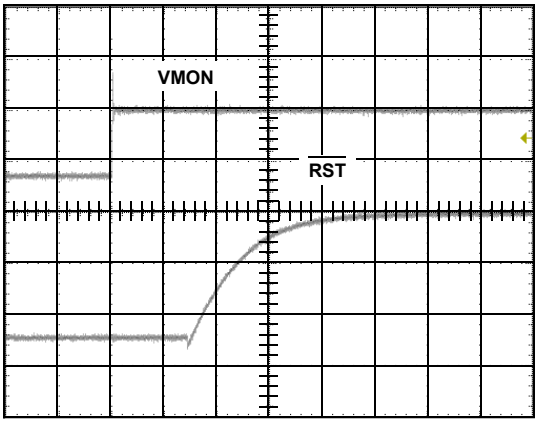


FIGURE 4. VMON HIGH TO RST HIGH

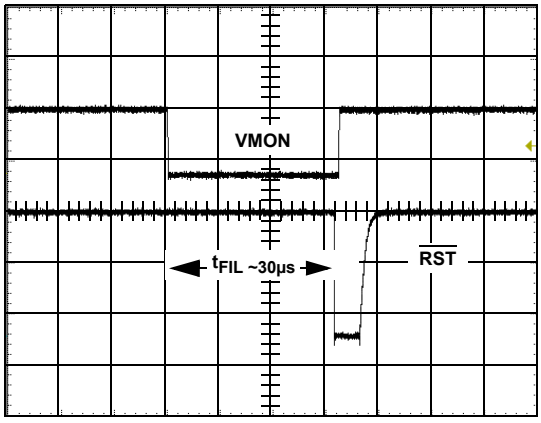


FIGURE 5. VMON LOW TO RST LOW

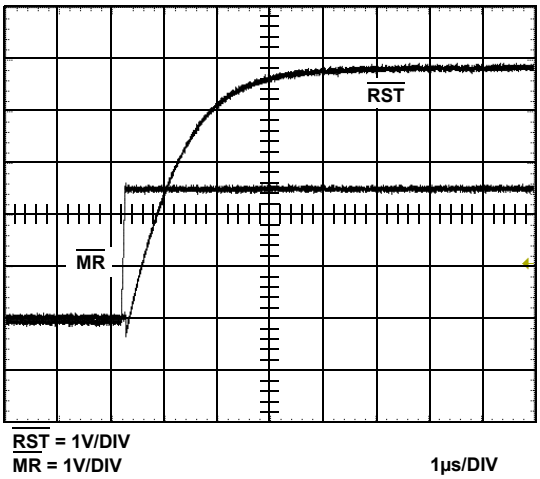


FIGURE 6. MR HIGH TO RST HIGH

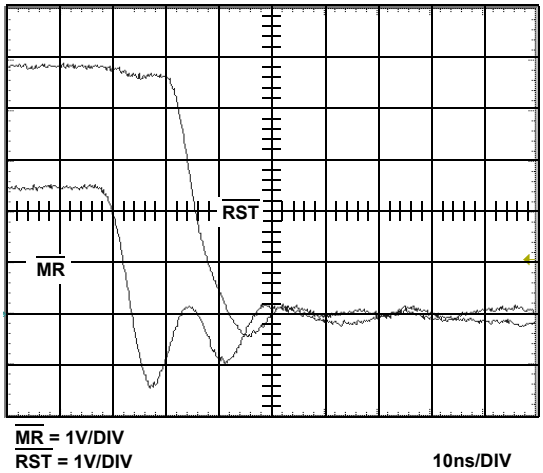


FIGURE 7. MR LOW TO RST LOW

Typical Performance Curves (Continued)

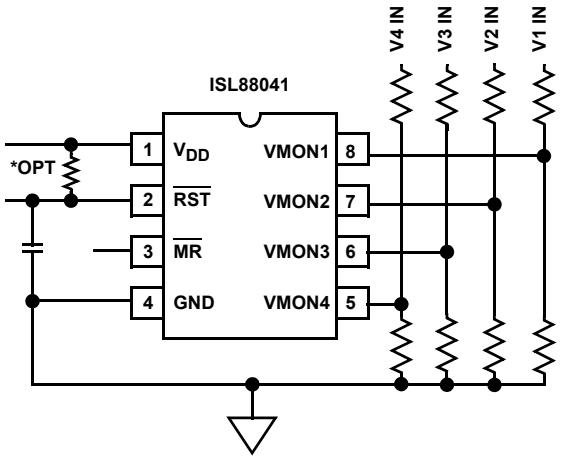


FIGURE 8. ISL88041 TYPICAL APPLICATION SCHEMATIC

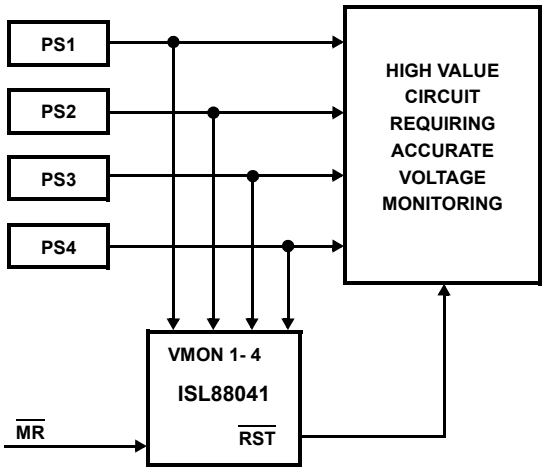


FIGURE 9. TYPICAL ISL88041 APPLICATION DIAGRAM

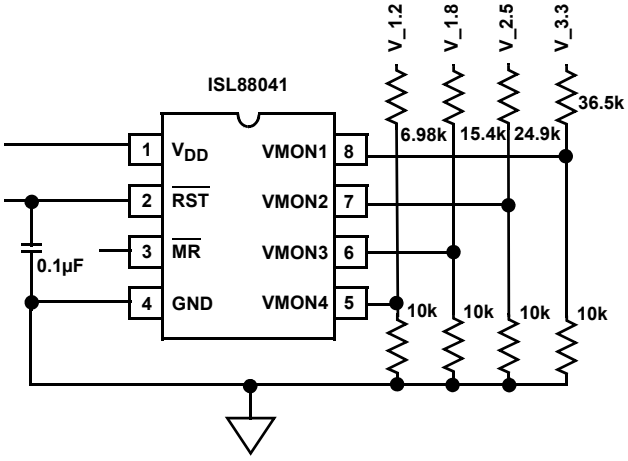


FIGURE 10. ISL88041EVAL1 SCHEMATIC

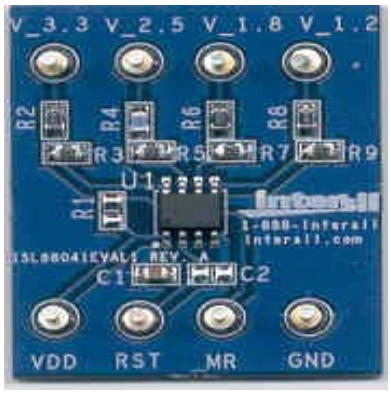
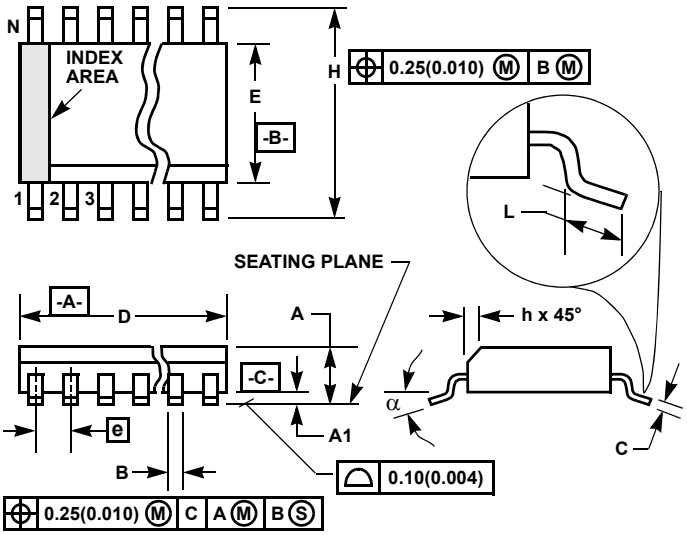


FIGURE 11. ISL88041EVAL1 PHOTO

Small Outline Plastic Packages (SOIC)



NOTES:

1. Symbols are defined in the “MO Series Symbol List” in Section 2.2 of Publication Number 95.
2. Dimensioning and tolerancing per ANSI Y14.5M-1982.
3. Dimension “D” does not include mold flash, protrusions or gate burrs. Mold flash, protrusion and gate burrs shall not exceed 0.15mm (0.006 inch) per side.
4. Dimension “E” does not include interlead flash or protrusions. Interlead flash and protrusions shall not exceed 0.25mm (0.010 inch) per side.
5. The chamfer on the body is optional. If it is not present, a visual index feature must be located within the crosshatched area.
6. “L” is the length of terminal for soldering to a substrate.
7. “N” is the number of terminal positions.
8. Terminal numbers are shown for reference only.
9. The lead width “B”, as measured 0.36mm (0.014 inch) or greater above the seating plane, shall not exceed a maximum value of 0.61mm (0.024 inch).
10. Controlling dimension: MILLIMETER. Converted inch dimensions are not necessarily exact.

M8.15 (JEDEC MS-012-AA ISSUE C)
8 LEAD NARROW BODY SMALL OUTLINE PLASTIC PACKAGE

SYMBOL	INCHES		MILLIMETERS		NOTES
	MIN	MAX	MIN	MAX	
A	0.0532	0.0688	1.35	1.75	-
A1	0.0040	0.0098	0.10	0.25	-
B	0.013	0.020	0.33	0.51	9
C	0.0075	0.0098	0.19	0.25	-
D	0.1890	0.1968	4.80	5.00	3
E	0.1497	0.1574	3.80	4.00	4
e	0.050 BSC		1.27 BSC		-
H	0.2284	0.2440	5.80	6.20	-
h	0.0099	0.0196	0.25	0.50	5
L	0.016	0.050	0.40	1.27	6
N	8		8		7
α	0°	8°	0°	8°	-

Rev. 1 6/05

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