380 MHz, 25 mA, Triple 2:1 Multiplexers

AD8183/AD8185

FEATURES

Fully Buffered Inputs and Outputs
Fast Channel-to-Channel Switching: 15 ns
High Speed
380 MHz Bandwidth (–3 dB) 200 mV p-p
310 MHz Bandwidth (–3 dB) 2 V p-p
1000 V/μs Slew Rate G = +1, 2 V Step
1150 V/μs Slew Rate G = +2, 2 V Step
Fast Settling Time of 15 ns to 0.1%
Low Power: 25 mA
Excellent Video Specifications (R_L = 150 Ω)
Gain Flatness of 0.1 dB to 90 MHz
0.01% Differential Gain Error
0.02° Differential Phase Error
Low All-Hostile Crosstalk –84 dB @ 5 MHz
–54 dB @ 50 MHz
Low Channel-to-Channel Crosstalk –56 dB @ 100 MHz
High "OFF" Isolation of –100 dB @ 10 MHz
Low Cost
Fast High Impedance Output Disable Feature for Connecting Multiple Devices

APPLICATIONS

Pixel Switching for "Picture-In-Picture"
Switching RGB in LCD and Plasma Displays
RGB Video Switchers and Routers

FUNCTIONAL BLOCK DIAGRAM

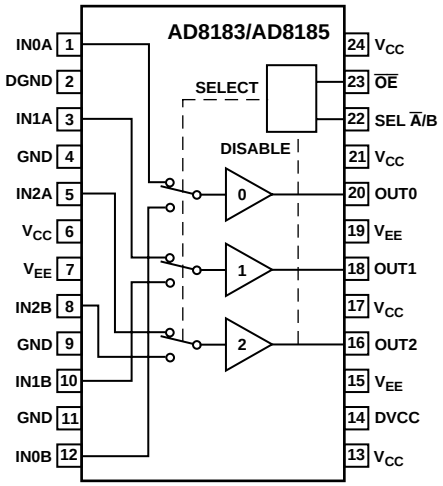


Table I. Truth Table

SEL $\overline{A}$/B	$\overline{OE}$	OUT
0	0	INA
1	0	INB
0	1	High Z
1	1	High Z

PRODUCT DESCRIPTION

The AD8183 (G = +1) and AD8185 (G = +2) are high speed triple 2:1 multiplexers. They offer –3 dB signal bandwidth up to 380 MHz, along with slew rate of 1000 V/μs. With better than –90 dB of channel-to-channel crosstalk and isolation at 10 MHz, they are useful in many high-speed applications. The differential gain and differential phase errors of 0.01% and 0.02° respectively, along with 0.1 dB flatness to 90 MHz make the AD8183 and AD8185 ideal for professional video and RGB multiplexing. They offer 15 ns channel-to-channel switching time, making them an excellent choice for switching video signals, while consuming less than 25 mA on ±5 V supply voltages.

Both devices offer a high speed disable feature that can set the output into a high impedance state. This allows the building of larger input arrays while minimizing "OFF" channel output loading. They operate on voltage supplies of ±5 V and are offered in a 24-lead TSSOP package.

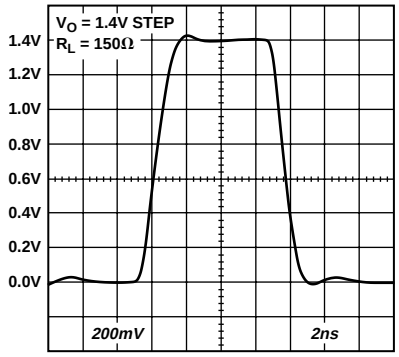


Figure 1. AD8185 Pulse Response; R_L = 150 Ω

REV. 0

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AD8183/AD8185–SPECIFICATIONS (T_A = 25°C, V_S = ±5 V, R_L = 1 kΩ unless otherwise noted)

Parameter	Condition	Min	Typ	Max	Unit
DYNAMIC PERFORMANCE					
–3 dB Bandwidth (Small Signal)	V_{OUT} = 200 mV p-p	250/300	590/360		MHz
	V_{OUT} = 200 mV p-p, R_L = 150 Ω	200/250	380/320		MHz
–3 dB Bandwidth (Large Signal)	V_{OUT} = 2 V p-p	250/300	530/350		MHz
	V_{OUT} = 2 V p-p, R_L = 150 Ω	200/250	310/300		MHz
0.1 dB Bandwidth	V_{OUT} = 200 mV p-p		90/60		MHz
	V_{OUT} = 200 mV p-p, R_L = 150 Ω		100/160		MHz
Slew Rate	2 V Step		1000/1150		V/µs
Settling Time to 0.1%	2 V Step, R_L = 150 Ω		15		ns
NOISE/DISTORTION PERFORMANCE					
Differential Gain	NTSC or PAL, 150 Ω		0.01		%
Differential Phase	NTSC or PAL, 150 Ω		0.02		Degrees
All-Hostile Crosstalk, RTI	f = 5 MHz, AD8185: R_L = 150 Ω		–84/–72		dB
	f = 50 MHz, AD8185: R_L = 150 Ω		–54/–50		dB
Channel-to-Channel Crosstalk, RTI	f = 100 MHz, AD8185: R_L = 150 Ω		–56/–54		dB
OFF Isolation	f = 10 MHz, R_L = 150 Ω		–100		dB
Voltage Noise, RTI	f = 10 kHz to 30 MHz		28/15		nV/√Hz
DC PERFORMANCE					
Voltage Gain Error	No Load		0.20	0.25/0.85	%
Input Offset Voltage, RTI			5	25/40	mV
	T_{MIN} to T_{MAX}		10		mV
Input Offset Voltage Matching, RTI	Channel-to-Channel		1	25/40	mV
Input Offset Drift, RTI			15		µV/°C
Input Bias Current			6/10	10/15	µA
INPUT CHARACTERISTICS					
Input Resistance		4/1	8/5		MΩ
Input Capacitance	Channel Enabled		1		pF
	Channel Disabled		1.5		pF
Input Voltage Range			±3.0/±1.5		V
OUTPUT CHARACTERISTICS					
Output Voltage Swing	R_L = 1 kΩ	±2.90	±3.25		V
	R_L = 150 Ω	±2.65	±2.95		V
Short Circuit Current			60		mA
Output Resistance	Enabled		0.3		Ω
	Disabled	4/1	8/3		MΩ
Output Capacitance	Disabled		4/6.5		pF
POWER SUPPLY					
Operating Range		±4.5		±5.5	V
Power Supply Rejection Ratio	+PSRR +V_S = +4.5 V to +5.5 V, –V_S = –5 V	58/62	66/72		dB
	–PSRR –V_S = –4.5 V to –5.5 V, +V_S = +5 V	52/60	56/68		dB
Quiescent Current	All Channels "ON"		25	30	mA
	All Channels "OFF"		3/7	5/10	mA
	T_{MIN} to T_{MAX}; All Channels "ON"		25		mA
SWITCHING CHARACTERISTICS					
Switch Time	Channel-to-Channel				
50% Logic to 50% Output Settling	IN0 = +1 V, IN1 = –1 V		15		ns
$\overline{\text{ENABLE}}$ to Channel ON Time					
50% Logic to 50% Output Settling	INPUT = 1 V		20		ns
$\overline{\text{ENABLE}}$ to Channel OFF Time					
50% Logic to 50% Output Settling	INPUT = 1 V		45		ns
Channel Switching Transient (Glitch)	All Inputs Grounded		50/70		mV
DIGITAL INPUTS					
Logic "1" Voltage	SEL $\overline{\text{A}}$/B and $\overline{\text{OE}}$ Inputs	2.0			V
Logic "0" Voltage	SEL $\overline{\text{A}}$/B and $\overline{\text{OE}}$ Inputs			0.8	V
Logic "1" Input Current	SEL $\overline{\text{A}}$/B and $\overline{\text{OE}}$ = 4 V		10		nA
Logic "0" Input Current	SEL $\overline{\text{A}}$/B and $\overline{\text{OE}}$ = 0.4 V		0.5		µA
OPERATING TEMPERATURE RANGE					
Temperature Range	Operating (Still Air)	–40		+85	°C
θ_{JA}	Operating (Still Air)		128		°C/W
θ_{JC}	Operating		42		°C/W

Specifications subject to change without notice.

ABSOLUTE MAXIMUM RATINGS[1]

Supply Voltage . . . . . 12.0 V
DVCC to V_{CC} . . . . . ±0.2 V
Internal Power Dissipation[2, 3]
AD8183/AD8185 24-Lead TSSOP (RU) . . . . . 1 W
Input Voltage
IN0A, IN0B, IN1A, IN1B, IN2A, IN2B . . . . . $V_{EE} \le V_{IN} \le V_{CC}$
SELECT $\overline{A}$/B, $\overline{OE}$ . . . . . DGND $\le V_{IN} \le V_{CC}$
Output Short Circuit Duration . . . . . Indefinite[3]
Storage Temperature Range . . . . . –65°C to +150°C
Lead Temperature Range (Soldering 10 sec) . . . . . 300°C

NOTES

[1]Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only; functional operation of the device at these or any other conditions above those indicated in the operational section of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

[2]Specification is for device in free air (T_A = 25°C).

[3]24-lead plastic TSSOP; θ_{JA} = 128°C/W. Maximum internal power dissipation (P_D) should be derated for ambient temperature (T_A) such that $P_D < (150°C–T_A)/\theta_{JA}$.

ORDERING GUIDE

Model	Temperature Range	Package Description	Package Option
AD8183ARU	–40°C to +85°C	24-Lead Plastic TSSOP	RU-24
AD8185ARU	–40°C to +85°C	24-Lead Plastic TSSOP	RU-24
AD8183-EVAL		Evaluation Board	
AD8185-EVAL		Evaluation Board	

MAXIMUM POWER DISSIPATION

The maximum power that can be safely dissipated by the AD8183/AD8185 is limited by the associated rise in junction temperature. The maximum safe junction temperature for plastic encapsulated devices is determined by the glass transition temperature of the plastic, approximately 150°C. Temporarily exceeding this limit may cause a shift in parametric performance due to a change in the stresses exerted on the die by the package. Exceeding a junction temperature of 175°C for an extended period can result in device failure.

While the AD8183/AD8185 is internally short circuit protected, this may not be sufficient to guarantee that the maximum junction temperature (150°C) is not exceeded under all conditions. To ensure proper operation, it is necessary to observe the maximum power derating curves shown in Figure 2.

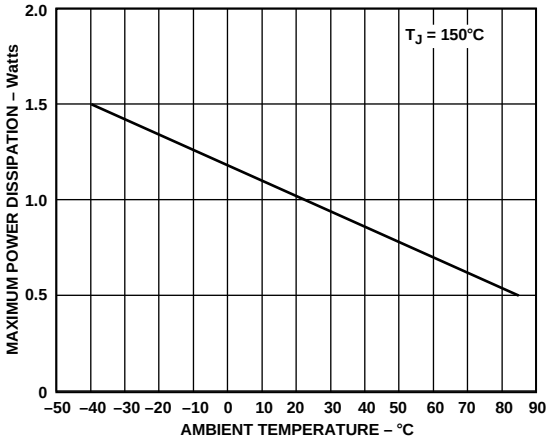
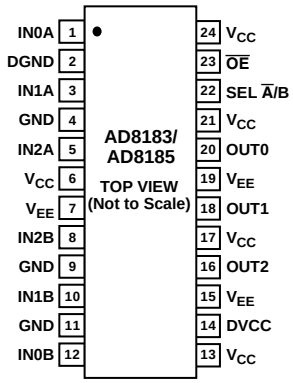


Figure 2. Maximum Power Dissipation vs. Temperature

PIN CONFIGURATION



CAUTION

ESD (electrostatic discharge) sensitive device. Electrostatic charges as high as 4000 V readily accumulate on the human body and test equipment and can discharge without detection. Although the AD8183/AD8185 features proprietary ESD protection circuitry, permanent damage may occur on devices subjected to high energy electrostatic discharges. Therefore, proper ESD precautions are recommended to avoid performance degradation or loss of functionality.



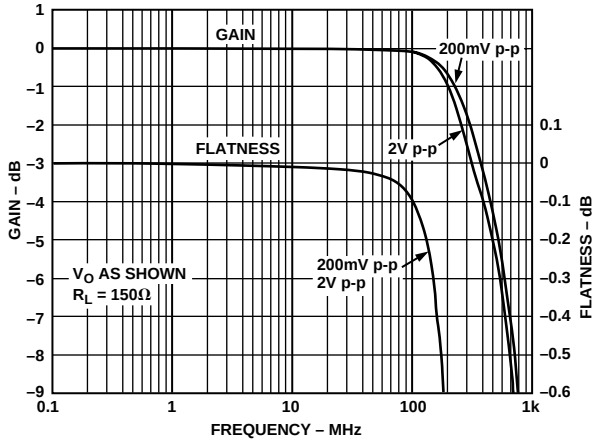


Figure 3. AD8183 Frequency Response; R_L = 150 Ω

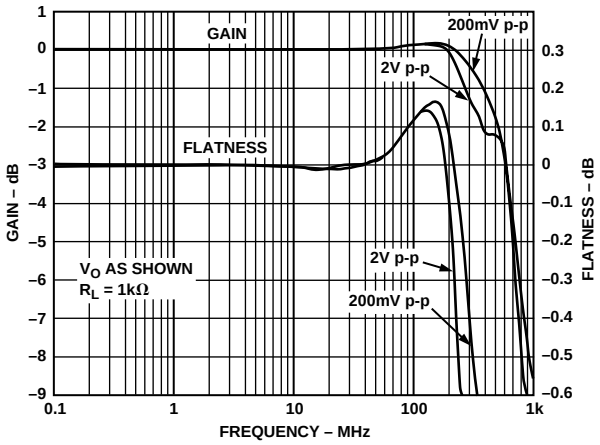


Figure 4. AD8183 Frequency Response; R_L = 1 kΩ

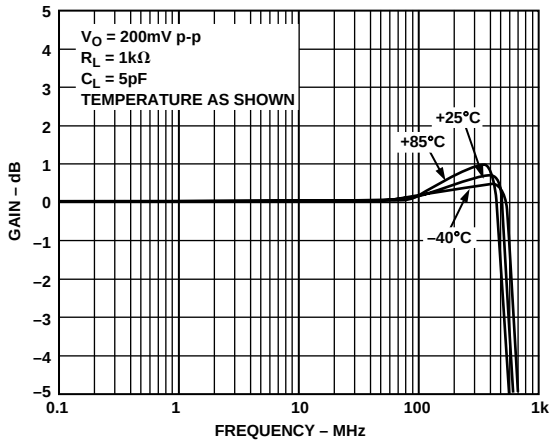


Figure 5. AD8183 Frequency Response vs. Temperature

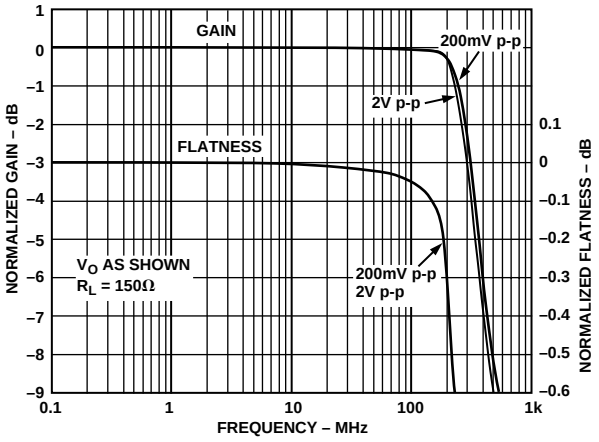


Figure 6. AD8185 Frequency Response; R_L = 150 Ω

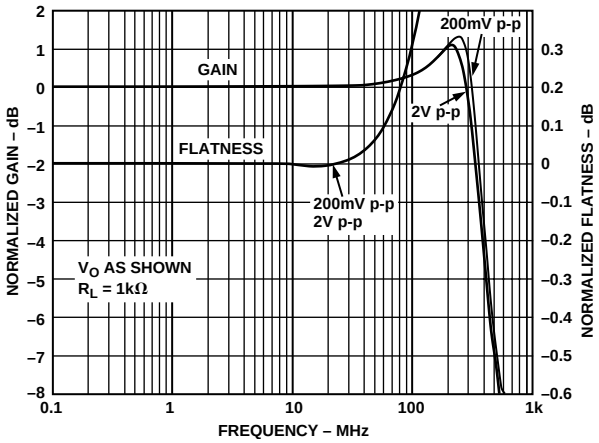


Figure 7. AD8185 Frequency Response; R_L = 1 kΩ

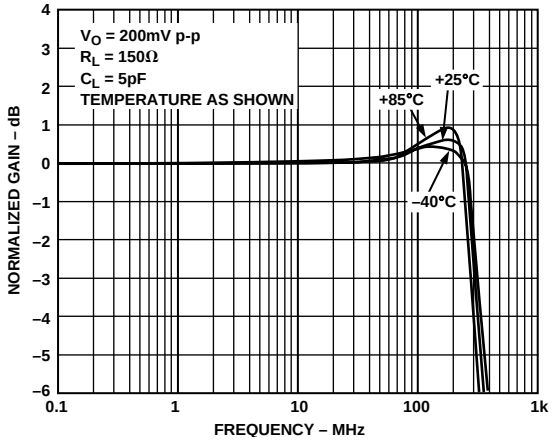


Figure 8. AD8185 Frequency Response vs. Temperature

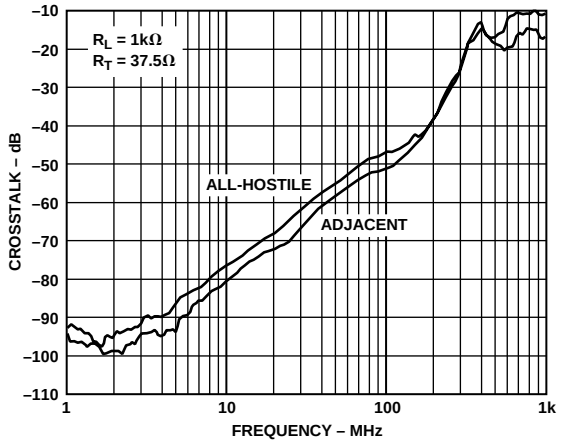


Figure 9. AD8183 Crosstalk vs. Frequency

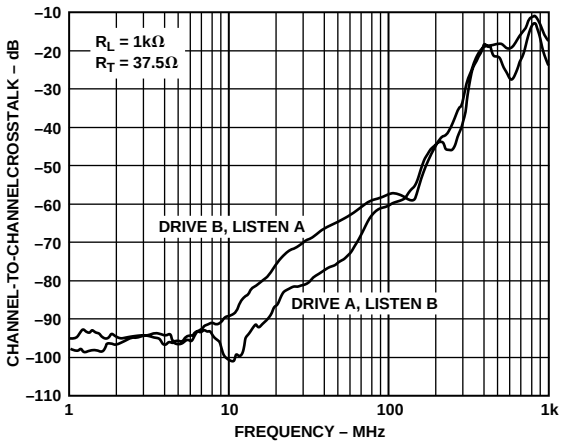


Figure 10. AD8183 Channel-to-Channel Crosstalk vs. Frequency

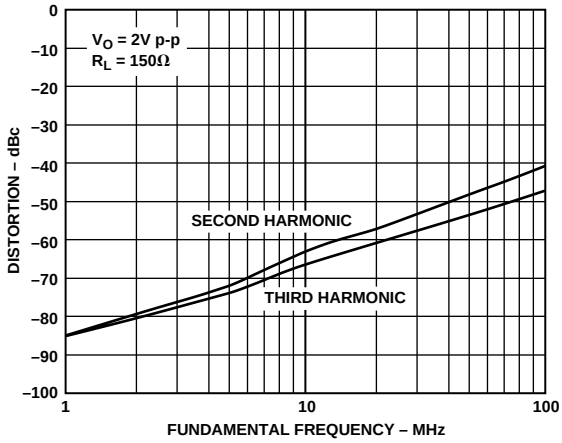


Figure 11. AD8183 Distortion vs. Frequency

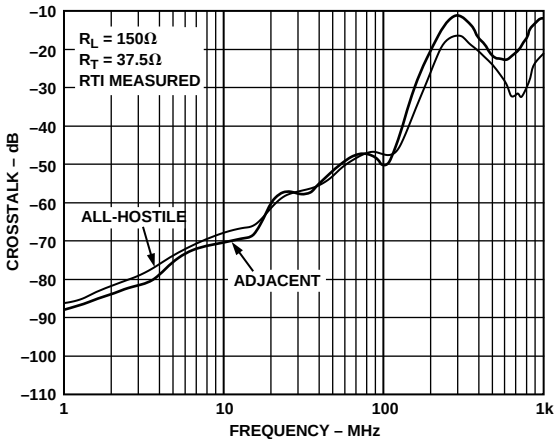


Figure 12. AD8185 Crosstalk vs. Frequency

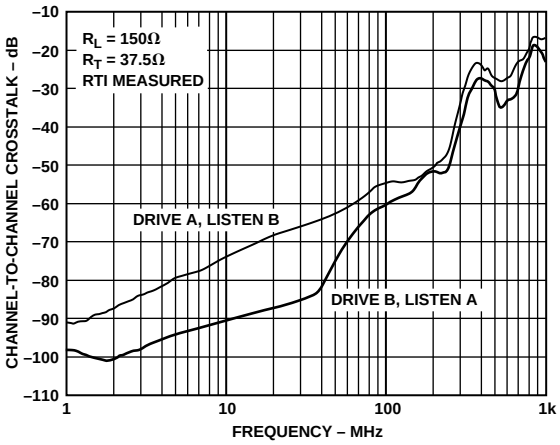


Figure 13. AD8185 Channel-to-Channel Crosstalk vs. Frequency

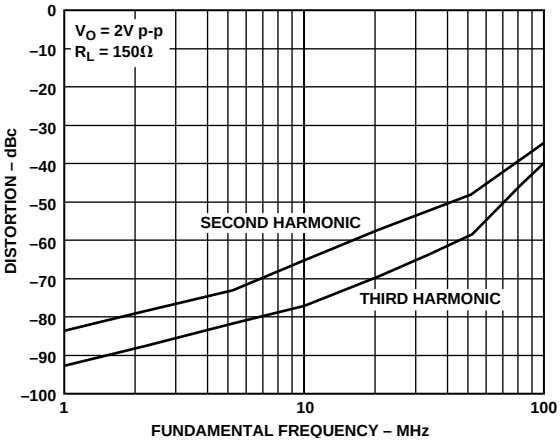


Figure 14. AD8185 Distortion vs. Frequency

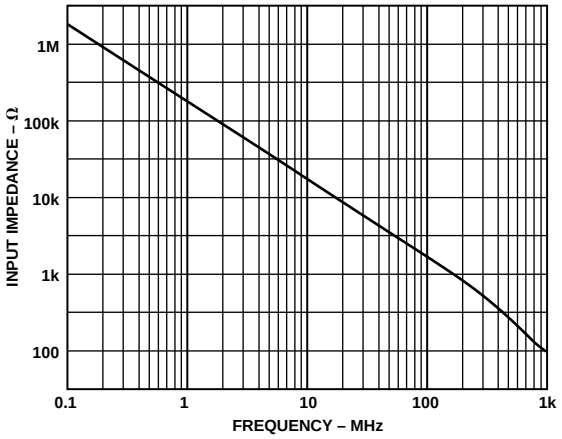


Figure 15. AD8183 Input Impedance vs. Frequency

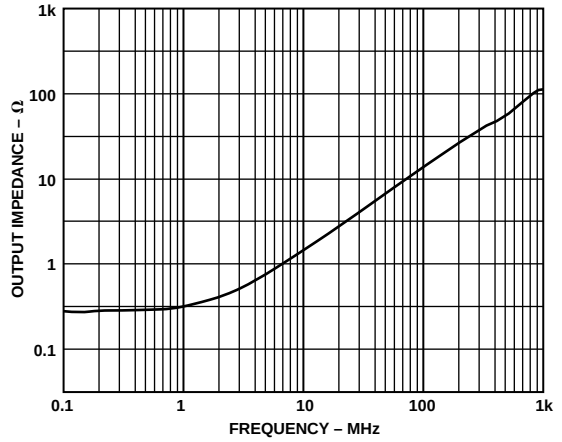


Figure 16. AD8183 Output Impedance vs. Frequency; Enabled

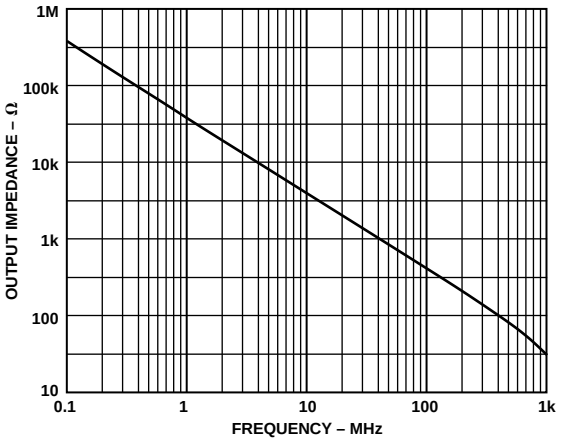


Figure 17. AD8183 Output Impedance, vs. Frequency; Disabled

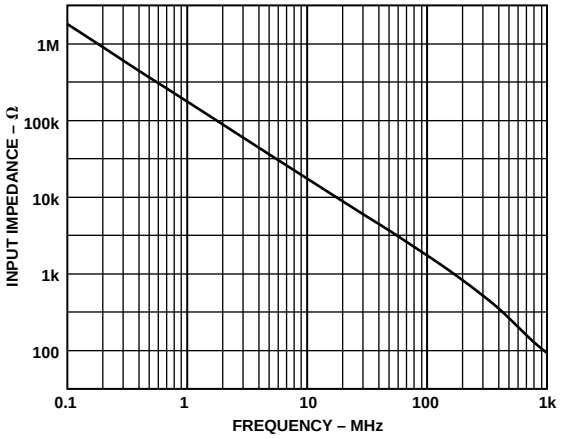


Figure 18. AD8185 Input Impedance vs. Frequency

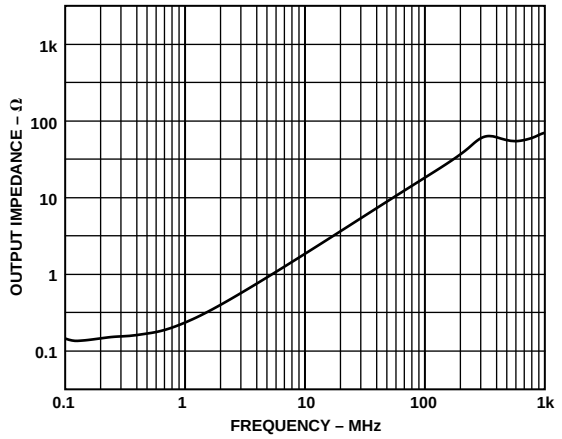


Figure 19. AD8185 Output Impedance vs. Frequency; Enabled

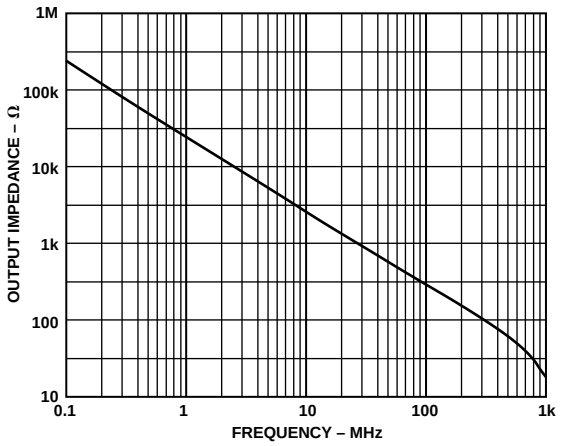


Figure 20. AD8185 Output Impedance vs. Frequency; Disabled

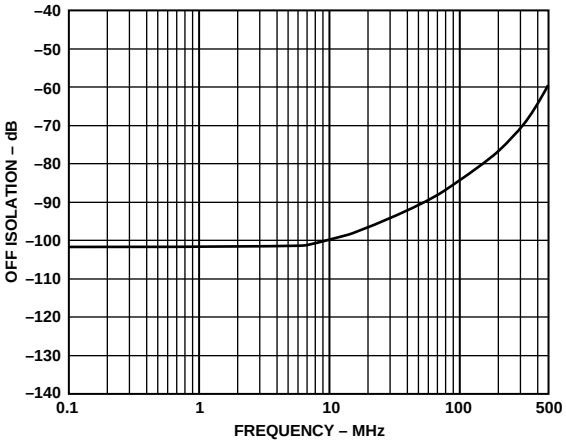


Figure 21. AD8183 Off Isolation, Input–Output

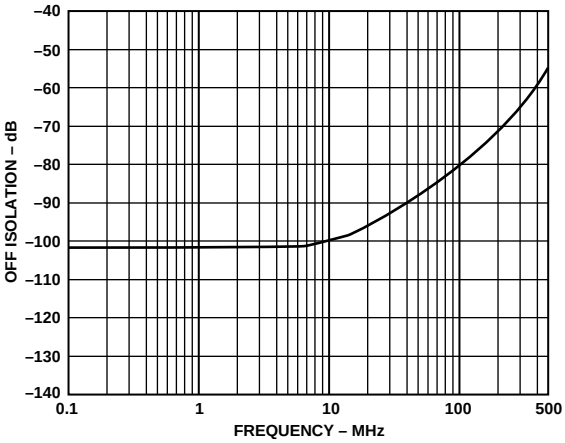


Figure 24. AD8185 Off Isolation, Input–Output

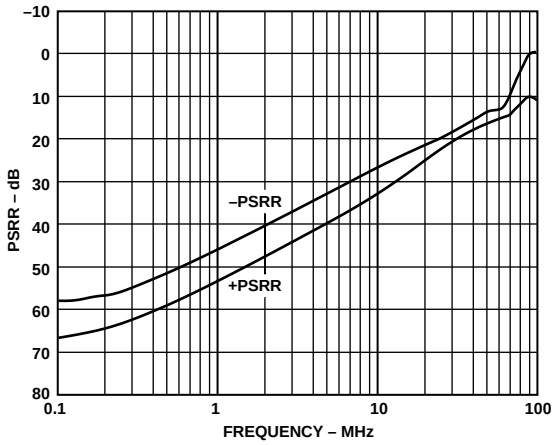


Figure 22. AD8183 PSRR vs. Frequency

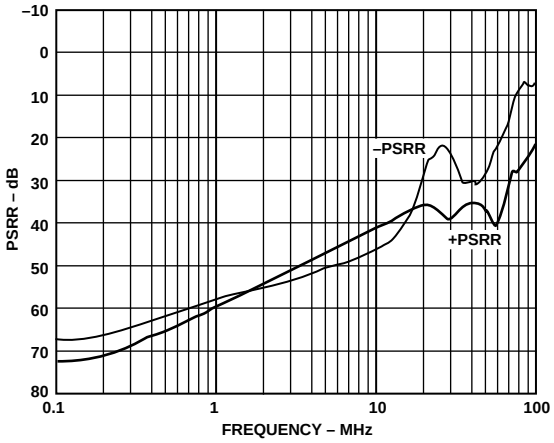


Figure 25. AD8185 PSRR vs. Frequency

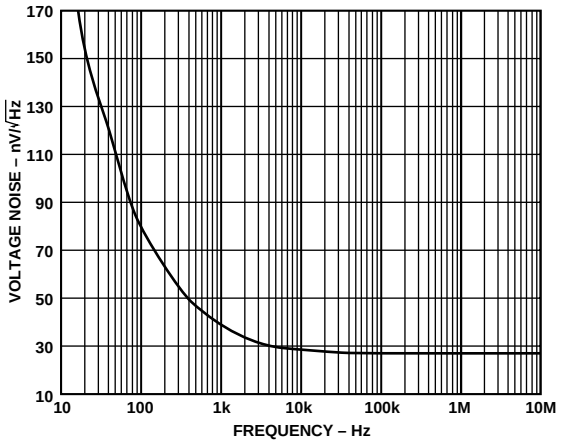


Figure 23. AD8183 Voltage Noise vs. Frequency

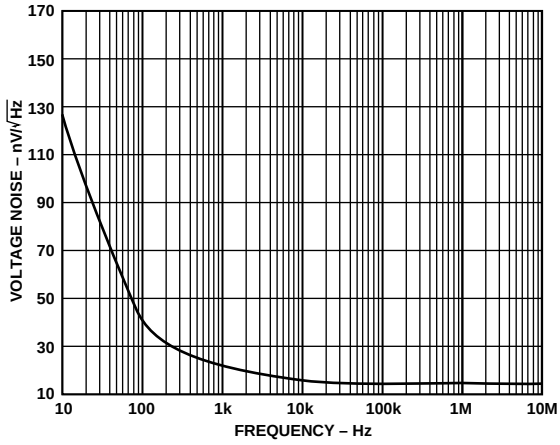


Figure 26. AD8185 RTI Voltage Noise vs. Frequency

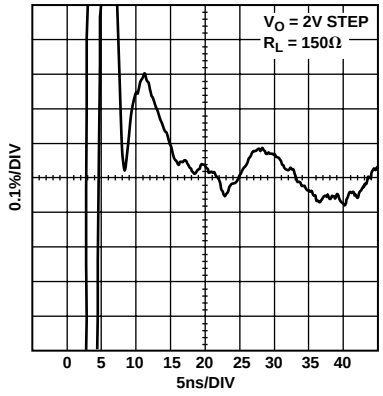


Figure 27. AD8183 0.1% Settling Time

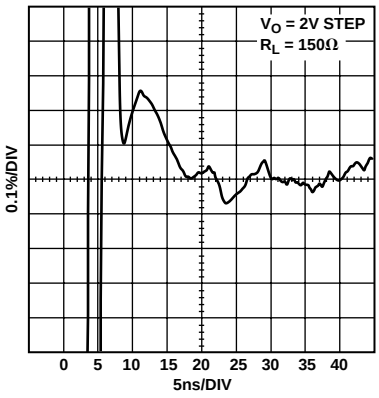


Figure 30. AD8185 0.1% Settling Time

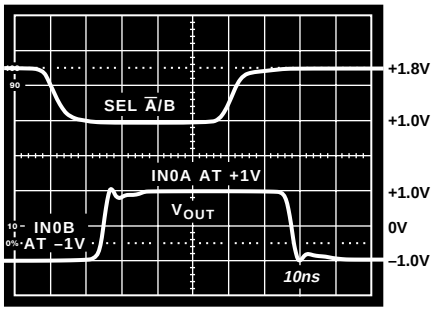


Figure 28. AD8183 Channel-to-Channel Switching Time

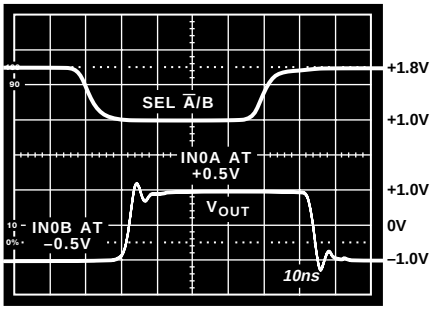


Figure 31. AD8185 Channel-to-Channel Switching Time

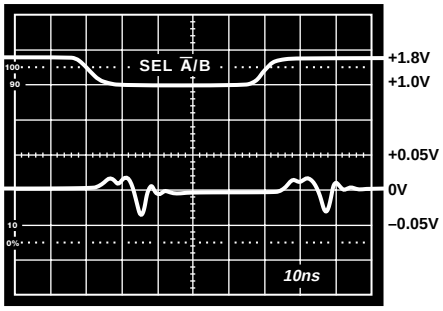


Figure 29. AD8183 Channel-to-Channel Switching Transient (Glitch)

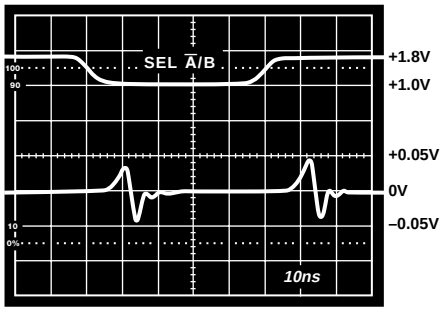


Figure 32. AD8185 Channel-to-Channel Switching Transient (Glitch)

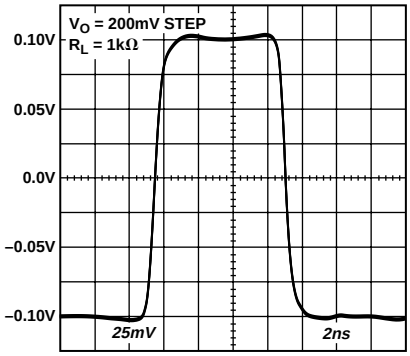


Figure 33. AD8183 Small Signal Pulse Response; R_L = 1 kΩ

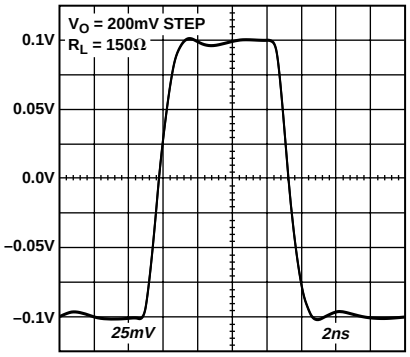


Figure 36. AD8185 Small Signal Pulse Response; R_L = 150 Ω

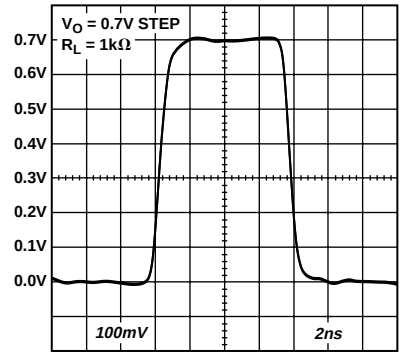


Figure 34. AD8183 Video Amplitude Pulse Response; R_L = 1 kΩ

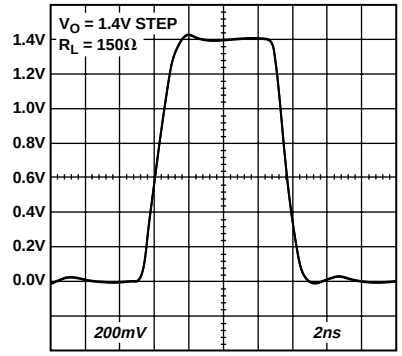


Figure 37. AD8185 Video Amplitude Pulse Response; R_L = 150 Ω

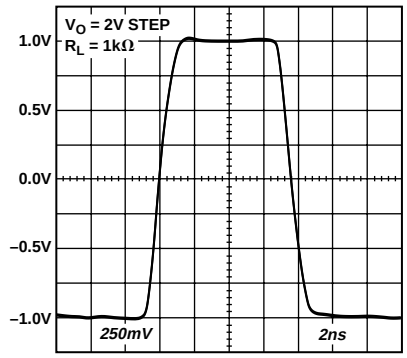


Figure 35. AD8183 Large Signal Pulse Response; R_L = 1 kΩ

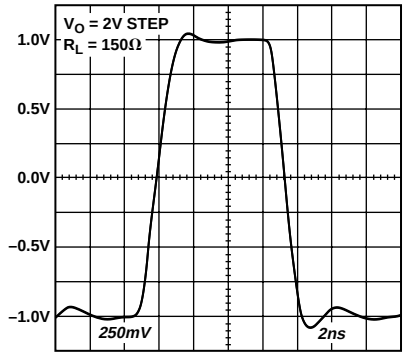


Figure 38. AD8185 Large Signal Pulse Response; R_L = 150 Ω

THEORY OF OPERATION

The AD8183 (G = +1) and AD8185 (G = +2) are triple-output, 2:1 multiplexers with TTL-compatible global input switching and output enable control. Optimized for selecting between two RGB (red, green, blue) video sources, the devices have high peak slew rates, maintaining their bandwidth for large signals. Additionally, the multiplexers are compensated for high phase margin, minimizing overshoot for good pixel resolution. The multiplexers also have video specifications that are suitable for switching NTSC or PAL composite signals.

The multiplexers are organized as three independent channels, each with two input transconductance stages and one output transimpedance stage. The appropriate input transconductance stages are selected via one logic pin (SELECT $\overline{A}$/B), such that all three outputs switch input connections simultaneously. The unused input stages are disabled with a "t-switch" scheme to provide excellent crosstalk isolation between "on" and "off" inputs. No additional input buffering is necessary, resulting in low input capacitance and high input impedance without additional signal degradation.

The transconductance stages, NPN differential pairs, source signal current into the folded cascode output stages. Each output stage contains a compensating network and emitter follower output buffer. Internal voltage feedback sets the gain with the AD8183 being configured as a unity gain follower, and the AD8185 as a gain-of-two amplifier with a feedback network. This architecture provides drive for a reverse-terminated video load (150 Ω) with low differential gain and phase error for relatively low power consumption. Careful chip design and layout allow excellent crosstalk isolation between channels.

One logic pin $\overline{OE}$ controls whether the three outputs are enabled, or disabled to a high-impedance state. The high impedance disable allows larger matrices to be built when busing the outputs together. Also, when not in use the outputs can be disabled to reduce power consumption. In the case of the AD8185 (G = +2), a feedback isolation scheme is used so that the impedance of the gain-of-two feedback network does not load the output.

Note that full power bandwidth for an undistorted sinusoidal signal is often calculated using peak slew rate from the equation:

$$Full\ Power\ Bandwidth = \frac{Peak\ Slew\ Rate}{(2 \times \pi \times Sinusoid\ Amplitude)}$$

Peak slew rate is not the same as average slew rate (25% to 75%) as typically specified. For a natural response, peak slew rate may be 2.7 times larger than average slew rate. Therefore, calculating a full power bandwidth with a specified average slew rate will give a pessimistic result.

APPLICATIONS

Driving Capacitive Loads

When driving a large capacitive load, most amplifiers will exhibit peaking/ringing in pulse response. To minimize peaking, and to ensure stability for larger values of capacitive loads, a small resistor, R_S, can be added between the output and the load capacitor, C_L. This is shown in Figure 39.

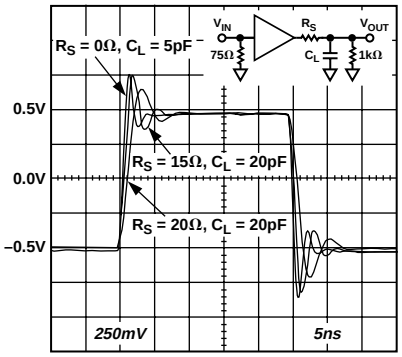


Figure 39. Pulse Responses Driving Capacitive Loads

Power Supply and Layout Considerations

The AD8183 and AD8185 are very high performance muxes that require attention to several important design details to realize their specified performance. Good high-frequency layout rules must be carefully observed.

A good design will start with a solid ground plane. All the GND pins of the part(s) should be directly connected to it. In addition, bypass capacitors should be connected from each supply pin (V_{CC} and V_{EE}) to the ground plane. It is suggested to use 0.01 μF surface-mount chip capacitors as close to the IC as possible to provide high-frequency bypassing.

For lower frequency bypassing, higher value tantalum capacitors—at least 10 μF—should be provided from both V_{CC} and V_{EE} to ground. These do not have to be as close to the IC pins, because parasitic inductance is not as big a factor at low frequencies.

Please refer to AD8183/AD8185 *Evaluation Board Operation Guide* for further information.

Crosstalk

In normal operation the AD8183 and AD8185 will have signals at some of the input pins that are not switched to appear at the output. In addition, several signal paths will in general be active at one time. In any system that has high-frequency signals that are brought together in close proximity, there will be inevitable crosstalk, whereby some fraction of the undesired signals will appear at the outputs. This can result, for example, in ghost images in an RGB monitor muxing application.

The AD8183 and AD8185 are capable of excellent low-crosstalk performance. However, in order to realize the best possible crosstalk performance, certain design details should be followed. Most of the low-crosstalk specification is inherent in the part and will result from observing the power supply and layout consideration discussed above. This is because each of the input and output pins are separated by at least either a supply pin or a ground pin.

This package architecture helps the crosstalk performance in at least three ways. First, the supply and ground pins provide extra physical separation between the input- and output-signal pins. Physical separation is a very effective technique for reducing crosstalk.

Second, the supply and ground pins are at ac ground, and therefore provide a degree of shielding between the signals. This works for both capacitive crosstalk, which is due to voltages on the signals, and inductive crosstalk, which is due to currents that flow through the signal paths.

Third, the additional power and ground pins also yield lower impedance on the power and ground lines, and therefore minimize the effects of shared impedances on crosstalk.

Signal routing is also important for keeping crosstalk low. Shielding and separation should be used for signals that must run parallel over some length on the PC board. If signals must cross, the trace widths should be kept narrow, and the signals should cross at right angles to minimize the capacitance between the traces.

4:1 RGB Multiplexer

For selecting among four RGB sources to drive a monitor, two AD8185s can be combined to make a 4:1 RGB multiplexer. A circuit for this is shown in Figure 40. Each RGB source is connected to either the three "A" or "B" inputs of one of the AD8185s. In addition, all R signals are tied to "0" inputs, all G signals are tied to "1" inputs, and all B signals are tied to "2" inputs. All of these input signals should be terminated with the standard 75 Ω to ground very close to the IC pins.

Each of the outputs of the AD8185 has a series 75 Ω resistor to provide a back termination for the monitor load. Whichever device is selected will drive the output signal through its three termination resistors. When terminated by the monitor, the voltage of these signals will be attenuated by a factor of two. This is normalized by the gain-of-two of the AD8185.

Unlike many gain-of-two circuits, the impedance of the AD8185 is very high when it is disabled. This is due to a proprietary circuit that disconnects the feedback network from a low impedance when the part is disabled.

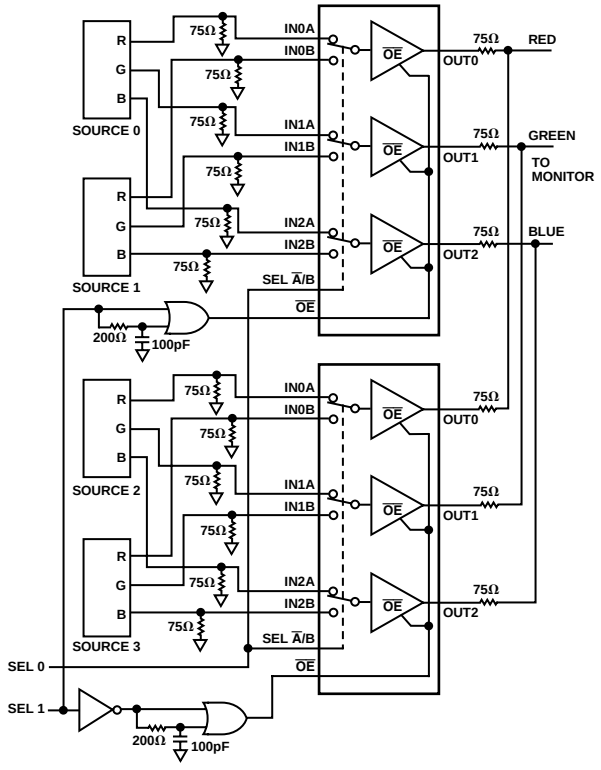


Figure 40. 4:1 RGB Multiplexer

Two control bits are required to select the input source for the RGB signals. One is applied to each of the SEL A/B inputs of each device to select between the two input sources for that device. The other bit controls the $\overline{OE}$ inputs of the two devices. A delay circuit is provided for each device to ensure that the outputs of one device are disabled before the outputs of the other are enabled.

If the RGB signals contain the sync information, such as a sync-on-Green, this circuit is all that is necessary for the full 4:1 RGB mux. However, if sync is carried on separate signals, such as in PCs, the sync signals can be multiplexed through a digital multiplexer that operates from the same SEL signals.

The RC in the $\overline{OE}$ circuit is to ensure "Break-Before-Make" operation. Using the values shown, a 20 ns time constant is created. This will delay the enabling of the outputs of the new selection until after the other devices' outputs are disabled. This time can be shortened or eliminated if the system can tolerate the glitches caused by simultaneously enabled outputs.

EVALUATION BOARD

POWER AND GROUND

There are three power supply pins on the board. "V_{CC}" is +5 V analog, "V_{EE}" is –5 V analog, and "DVCC" is +5 V digital. These three power supply pins should be connected to good quality, low noise supplies. If the same ±5 V power supply is used for both analog and digital, separate cables should be run from the power supply to the evaluation board's analog and digital power supply pins.

Three 10 μF tantalum capacitors (C1–C3) are located under the power connector to decouple the power supplies as they first enter the board. As the three supplies get close to the part, they are again decoupled with 0.1 μF ceramic capacitors (C4–C6). Finally, each power pin of the device is locally decoupled with a 0.01 μF ceramic capacitor (C7–C15).

The board has a separate analog and digital ground plane. With the jumper at W5 installed, these two ground planes are tied together on the board. Generally, this jumper should remain installed.

INPUTS AND OUTPUTS

The evaluation board has been carefully laid out to demonstrate the high speed performance of the device. Optimized for video applications, all signal inputs are terminated with 75 Ω resistors to ground (R1–R6). The three outputs are backterminated with 75 Ω series resistors (R12–R14). Stripline techniques are used to achieve a 75 Ω characteristic impedance on the input and output lines. See Figure 41 for the arrangement of the PCB layers.

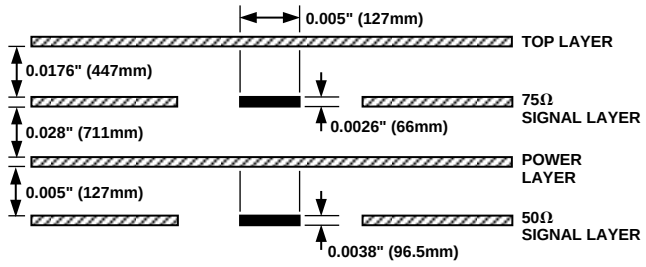


Figure 41. PCB Dimensions

In addition, 75 Ω BNC connectors are used on the six inputs (J1–J6) and three outputs (J7–J9). The connectors are arranged in a crescent around the device. This results in all the input and output signal traces having the same length. Unused regions of the multilayer board are filled up with ground planes. As a

result, the input and output traces, in addition to having a controlled impedance, are well shielded.

SEL $\overline{A}$/B AND $\overline{OE}$

SEL $\overline{A}$/B (Pin 22 of the device) allows the A or B inputs to be selected.

When SEL $\overline{A}$/B is at logic low, (equal to or less than 0.8 V), inputs 0A, 1A and 2A are directed to OUTPUTs 0, 1, and 2, respectively. When SEL $\overline{A}$/B is at logic high, (equal to or greater than 2.0 V), inputs 0B, 1B, and 2B are directed to OUTPUTs 0, 1, and 2, respectively.

There are two ways to provide SEL $\overline{A}$/B to the device: using a jumper or a BNC connection. With the jumper in the W4 position, SEL $\overline{A}$/B is tied to ground. This selects the A inputs.

With the jumper in the W3 position, SEL $\overline{A}$/B is tied to 5 V, through pull up resistor R15. This selects the B inputs.

If faster use of SEL $\overline{A}$/B is desired, the 50 Ω BNC connector at J10 can be used. If J10 is used, there must NOT be a jumper on W3 and W4. Microstrip line techniques provide a 50 Ω characteristic impedance from J10 to the device. Please refer to Figure 41 for the arrangement of the PCB layers. If J10 is used, the user may wish to install a 50 Ω termination resistor at R10.

$\overline{OE}$ (Pin 23 of the device) allows the three outputs to be enabled or disabled. When $\overline{OE}$ is at logic low, (equal to or less than 0.8 V), Outputs 0, 1, and 2 are enabled. When $\overline{OE}$ is at logic high, (equal to or greater than 2.0 V), Outputs 0, 1, and 2 are disabled (placed into a high impedance state).

Once again, there are two different ways to provide $\overline{OE}$ to the device: using a jumper or a BNC connection. With the jumper in the W2 position, $\overline{OE}$ is tied to ground. This enables the outputs. With the jumper in the W1 position, $\overline{OE}$ is tied to 5 V, through pull-up resistor R16. This selects "Hi Z," or high impedance, and the outputs are disabled.

If faster use of $\overline{OE}$ is desired, the 50 Ω BNC connector at J11 can be used. If J11 is used, there must NOT be a jumper on W1 and W2. Microstrip line techniques provide a 50 Ω characteristic impedance from J11 to the device. Please refer to Figure 41 for the arrangement of the PCB layers. If J11 is used, the user may wish to install a 50 Ω termination resistor at R11.

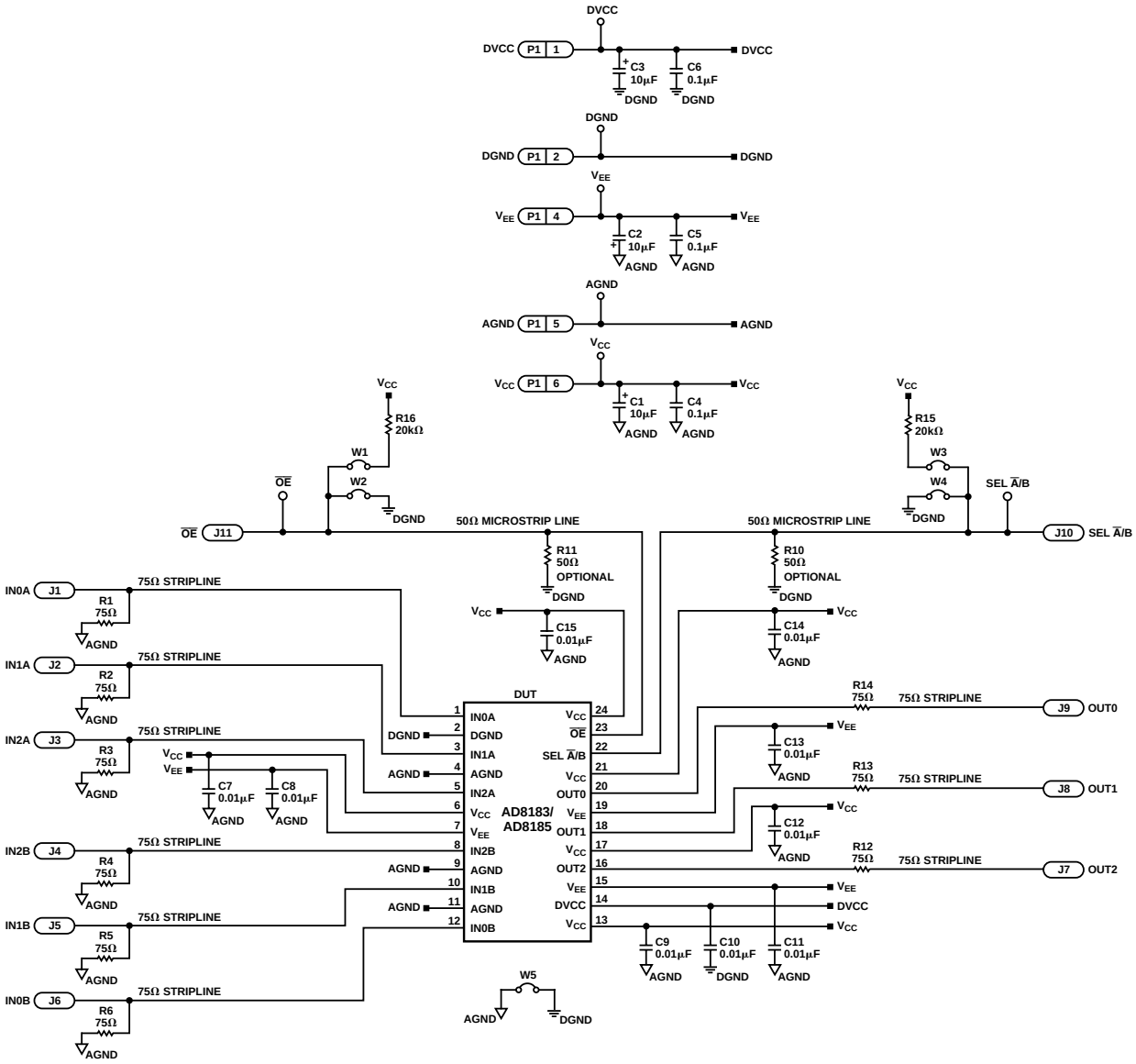


Figure 42. Evaluation Board Schematic

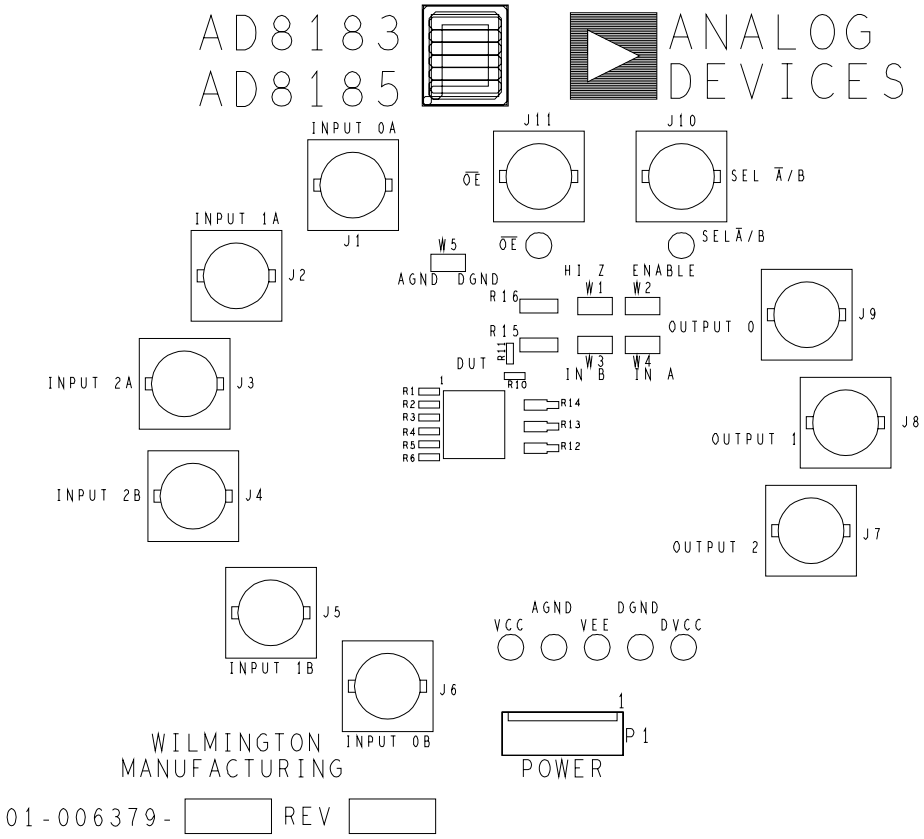


Figure 43. Component Side Silkscreen

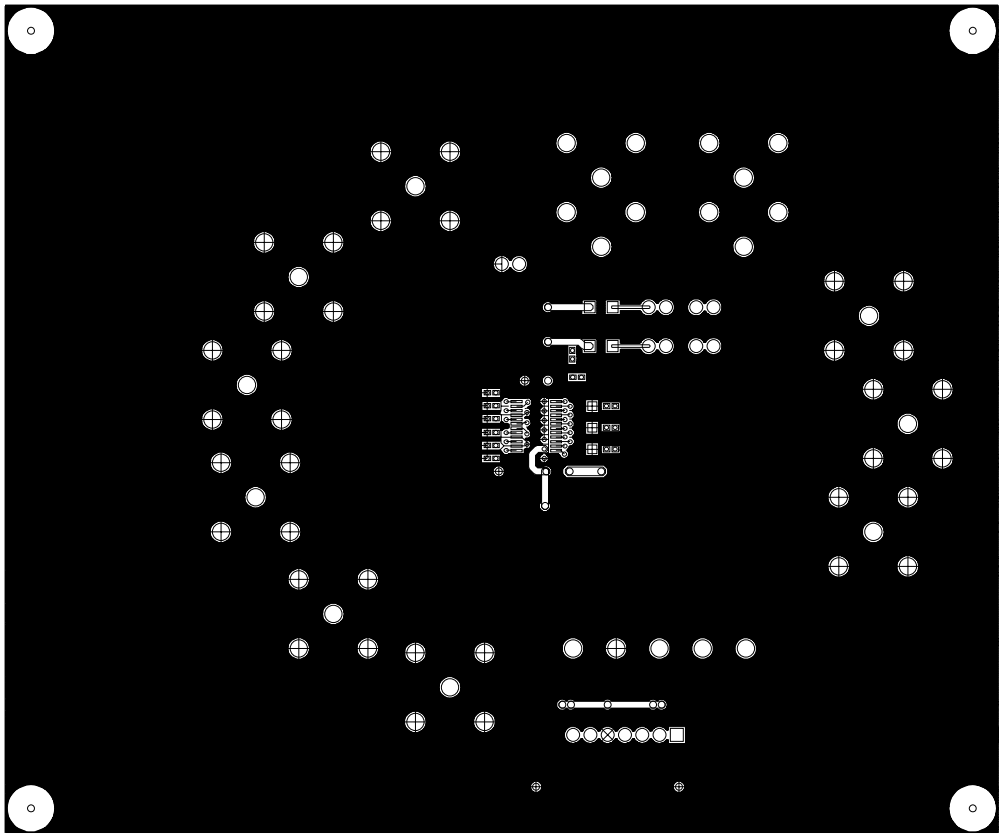


Figure 44. Board Layout (Component Side)

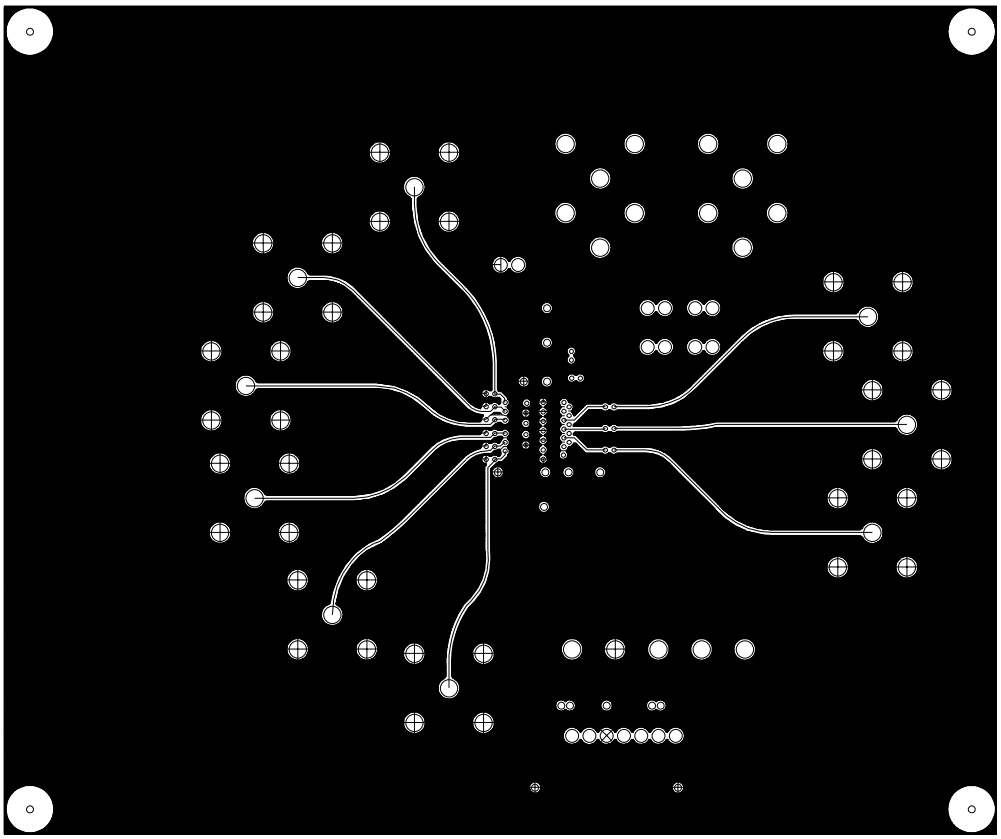


Figure 45. Board Layout (75 Ω Signal Layer)

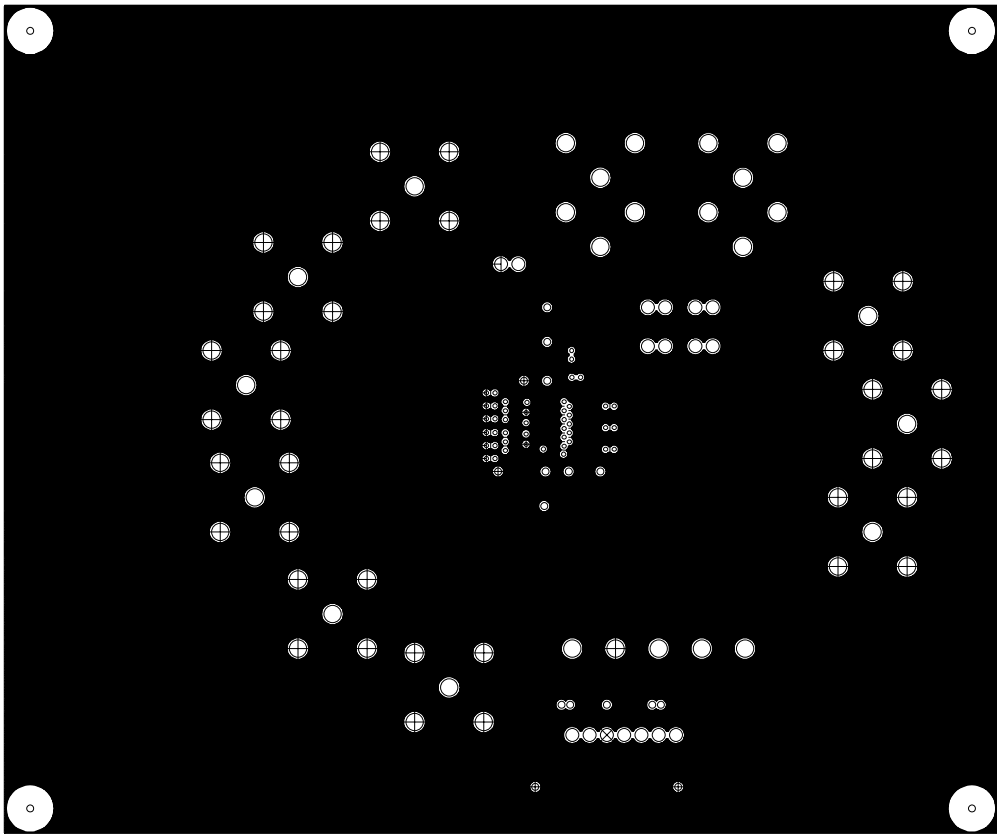


Figure 46. Board Layout (Ground Plane)

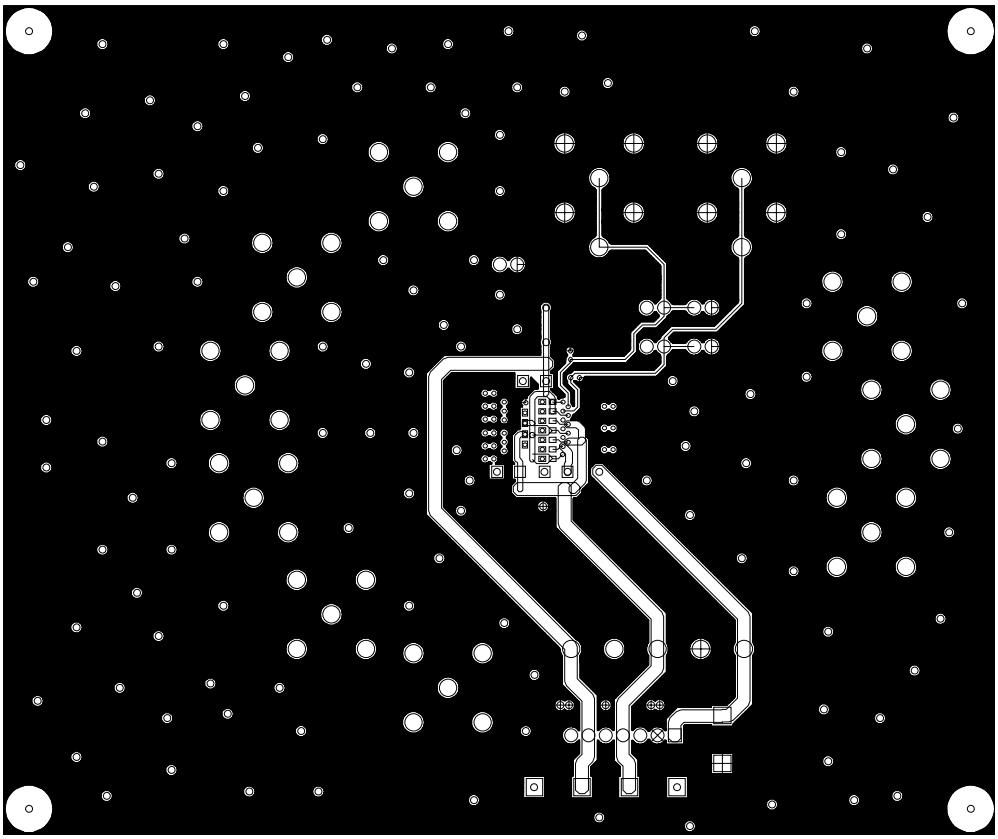


Figure 47. Board Layout (Circuit Side;) 50 Ω Signal Layer

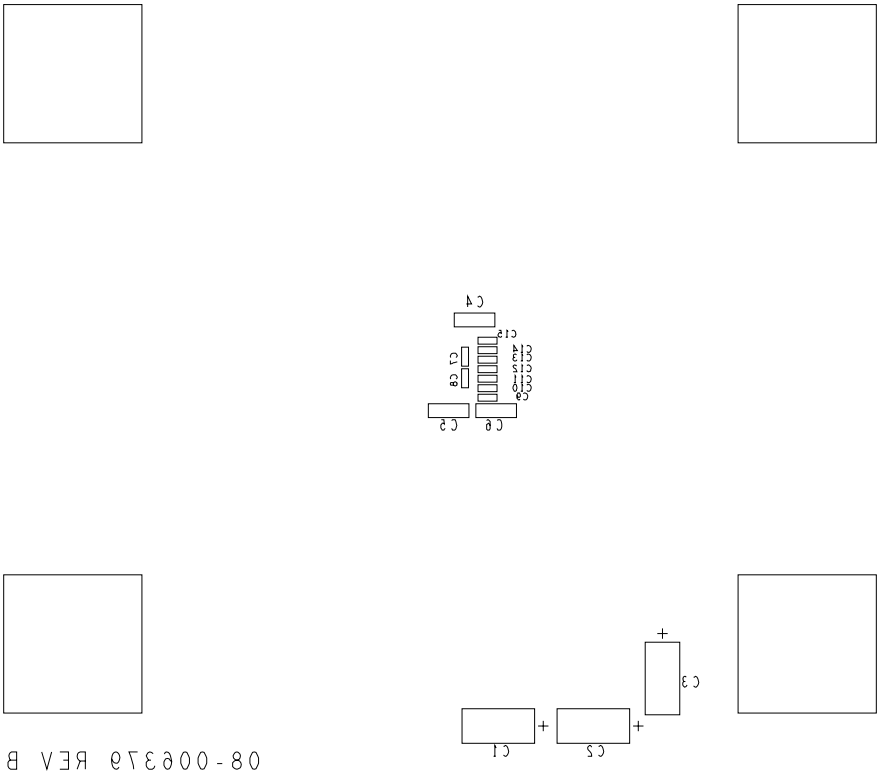
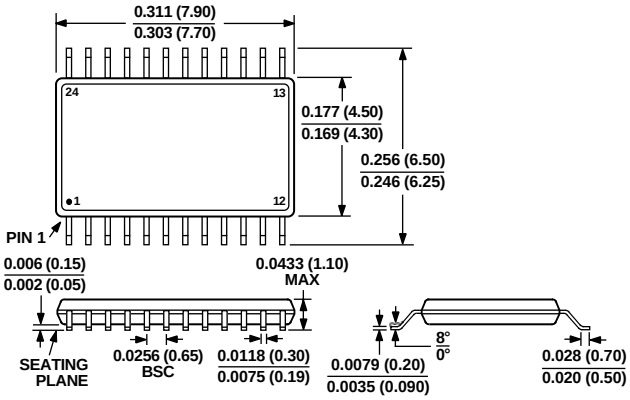


Figure 48. Circuit Side Silkscreen

OUTLINE DIMENSIONS

Dimensions shown in inches and (mm).

24-Lead Plastic TSSOP
(RU-24)



C3689–5–10/99

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