18-Bit Analog-to-Digital Converter for Bridge Sensors

Check for Samples: ADS1131

FEATURES

- **Complete Front-End for Bridge Sensors**
- **Available in an SO Package**
- **Internal Amplifier, Gain of 64**
- **Internal Oscillator**
- **Low-Side Power Switch for Bridge Sensor**
- **18-Bit Noise-Free Resolution**
- **Selectable 10SPS or 80SPS Data Rates**
- **Simultaneous 50Hz and 60Hz Rejection at 10SPS**
- **External Voltage Reference up to 5V for Ratiometric Measurements**
- **Simple, Pin-Driven Control**
- **Two-Wire Serial Digital Interface**
- **Supply Range: 3V to 5.3V**
- **–40°C to +85°C Temperature Range**

APPLICATIONS

- **Weigh Scales**
- **Strain Gauges**
- **Load Cells**
- **Industrial Process Control**

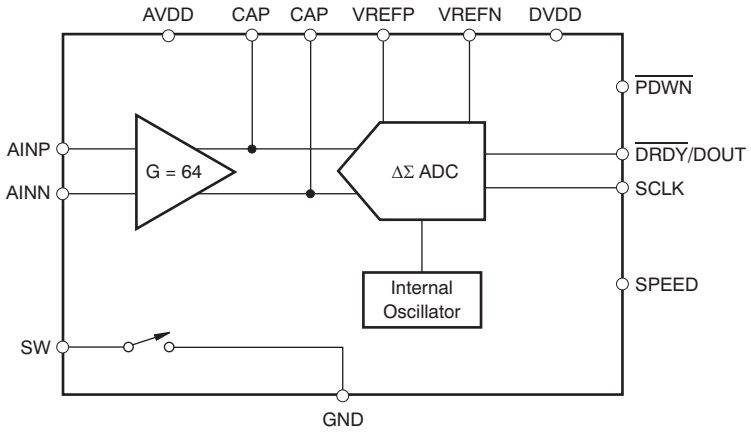
DESCRIPTION

The ADS1131 is a precision, 18-bit analog-to-digital converter (ADC). With an onboard, low-noise amplifier, onboard oscillator, precision 18-bit delta-sigma (ΔΣ) ADC, and bridge power switch, the ADS1131 provides a complete front-end solution for bridge sensor applications including weigh scales, strain gauges, and load cells.

The low-noise amplifier has a gain of 64, supporting a full-scale differential input of ±39mV. The ΔΣ ADC has 18-bit effective resolution and is comprised of a third-order modulator and fourth-order digital filter. Two data rates are supported: 10SPS (with both 50Hz and 60Hz rejection) and 80SPS. The ADS1131 can be put into a low-power standby mode or shut off completely in power-down mode.

The ADS1131 is controlled by dedicated pins; there are no digital registers to program. Data are output over an easily-isolated serial interface that connects directly to the MSP430 and other microcontrollers.

The ADS1131 is available in an SO-16 package and is specified from –40°C to +85°C.



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This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

PACKAGE AND ORDERING INFORMATION(1)

(1) For the most current package and ordering information, see the Package Option Addendum at the end of this document, or visit the device product folder at www.ti.com.

ABSOLUTE MAXIMUM RATINGS(1)

Over operating free-air temperature range, unless otherwise noted.

	ADS1131	UNIT
AVDD to GND	–0.3 to +6	V
DVDD to GND	–0.3 to +6	V
Input current	100, momentary	mA
	10, continuous	mA
Analog input voltage to GND	–0.3 to AVDD + 0.3	V
Digital input voltage to GND	–0.3 to DVDD + 0.3	V
Maximum junction temperature	+150	°C
Operating temperature range	–40 to +85	°C
Storage temperature range	–60 to +150	°C

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

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ELECTRICAL CHARACTERISTICS

Minimum/maximum limit specifications apply from –40°C to +85°C. Typical specifications at +25°C.
All specifications at AVDD = DVDD = VREFP = +5V, and VREFN = GND, unless otherwise noted.

PARAMETER		CONDITIONS	ADS1131 MIN	ADS1131 TYP	ADS1131 MAX	UNIT
ANALOG INPUTS						
Full-scale input voltage (AINP – AINN)				$\pm 0.5V_{REF}/64$		V
		V_{REF} = AVDD = 5V		±39.0		mV
		V_{REF} = AVDD = 3V		±23.4		mV
Common-mode input range			GND + 1.5V		AVDD – 1.5V	V
Differential input current				±2		nA
LOW-SIDE POWER SWITCH						
On-resistance (R_{ON})		AVDD = 5V, I_{SW} = 30mA		3.5	5	Ω
		AVDD = 3V, I_{SW} = 30mA		4	7	Ω
Current through switch					30	mA
SYSTEM PERFORMANCE						
Resolution		No missing codes	18			Bits
Data rate		SPEED = high		80		SPS
		SPEED = low		10		SPS
Digital filter settling time		Full settling		4		Conversions
Integral nonlinearity (INL)		Differential input, end-point fit		±8		ppm
Input offset error				10		µV
Input offset drift				±15		nV/°C
Gain error				1		%
Gain drift				±4		ppm/°C
Normal-mode rejection		f_{IN} = 50Hz or 60Hz ±1Hz, f_{DATA} = 10SPS		90		dB
Common-mode rejection		At dc		110		dB
Noise (peak-to-peak)		f_{DATA} = 10SPS, AVDD = V_{REF} = 5V		1		LSB
		f_{DATA} = 80SPS, AVDD = V_{REF} = 5V		1.7		LSB
		f_{DATA} = 10SPS, AVDD = V_{REF} = 5V		300		nV
		f_{DATA} = 80SPS, AVDD = V_{REF} = 5V		500		nV
Power-supply rejection		At dc		100		dB
VOLTAGE REFERENCE INPUT						
Voltage reference input (V_{REF})		V_{REF} = VREFP – VREFN	1.5	AVDD	AVDD + 0.1V	V
Negative reference input (VREFN)			AGND – 0.1		VREFP – 1.5	V
Positive reference input (VREFP)			VREFN + 1.5		AVDD + 0.1	V
Voltage reference input current				10		nA
DIGITAL INPUT/OUTPUT (DVDD = 2.7V to 5.3V)						
Logic levels	V_{IH}		0.8 DVDD		DVDD + 0.1	V
	V_{IL}		GND		0.2 DVDD	V
	V_{OH}	I_{OH} = 500µA	DVDD – 0.4			V
	V_{OL}	I_{OL} = 500µA			0.2 DVDD	V
Input leakage		$0 < V_{DIGITAL\ INPUT} <$ DVDD			±10	µA
Serial clock input frequency (f_{SCLK})					5	MHz

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ELECTRICAL CHARACTERISTICS (continued)

Minimum/maximum limit specifications apply from –40°C to +85°C. Typical specifications at +25°C.
All specifications at AVDD = DVDD = VREFP = +5V, and VREFN = GND, unless otherwise noted.

PARAMETER	CONDITIONS	ADS1131			UNIT
		MIN	TYP	MAX	
POWER SUPPLY					
Power-supply voltage (AVDD, DVDD)		3		5.3	V
Analog supply current	Normal mode, AVDD = 3V		900		µA
	Normal mode, AVDD = 5V		900		µA
	Standby mode		0.1		µA
	Power-down		0.1		µA
Digital supply current	Normal mode, DVDD = 3V		60		µA
	Normal mode, DVDD = 5V		95		µA
	Standby mode, SCLK = high, DVDD = 3V		45		µA
	Standby mode, SCLK = high, DVDD = 5V		65		µA
	Power-down		0.2		µA
Power dissipation, total	Normal mode, AVDD = DVDD = 3V		2.9		mW
	Normal mode, AVDD = DVDD = 5V		5.0		mW
TEMPERATURE					
Operating temperature range		–40		+85	°C
Specified temperature range		–40		+85	°C

THERMAL INFORMATION

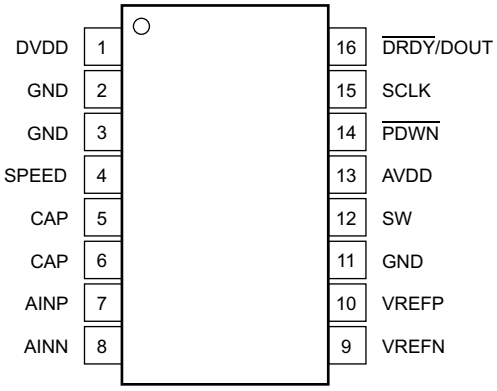
THERMAL METRIC(1)		ADS1131D	UNITS
		D	
		16 PINS	
θ_{JA}	Junction-to-ambient thermal resistance	133.8	°C/W
$\theta_{JC(top)}$	Junction-to-case(top) thermal resistance	71.4	
θ_{JB}	Junction-to-board thermal resistance	60.0	
ψ_{JT}	Junction-to-top characterization parameter	17.4	
ψ_{JB}	Junction-to-board characterization parameter	53.3	
$\theta_{JC(bottom)}$	Junction-to-case(bottom) thermal resistance	n/a	

(1) For more information about traditional and new thermal metrics, see the *IC Package Thermal Metrics* application report, SPRA953.

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PIN CONFIGURATION

D PACKAGE
SO-16
(TOP VIEW)



PIN DESCRIPTIONS

NAME	TERMINAL	ANALOG/DIGITAL INPUT/OUTPUT	DESCRIPTION
DVDD	1	Digital	Digital power supply
GND	2	Supply	Ground for digital and analog supplies
GND	3	Supply	Ground for digital and analog supplies
SPEED	4	Digital input	Data rate select: SPEED = 0: DATA RATE = 10SPS SPEED = 1: DATA RATE = 80SPS
CAP	5	Analog	Gain amplifier bypass capacitor connection
CAP	6	Analog	Gain amplifier bypass capacitor connection
AINP	7	Analog input	Positive analog input
AINN	8	Analog input	Negative analog input
VREFN	9	Analog input	Negative reference input
VREFP	10	Analog input	Positive reference input
GND	11	Supply	Ground for digital and analog supplies
SW	12	Analog	Low-side power switch
AVDD	13	Supply	Analog power supply
$\overline{\text{PDWN}}$	14	Digital input	Power-down: holding this pin low powers down the entire converter and resets the ADC.
SCLK	15	Digital input	Serial clock: clock out data on the rising edge. Also used to initiate Standby mode. See the Standby Mode section for more details.
$\overline{\text{DRDY}}$/DOUT	16	Digital output	Dual-purpose output: Data ready: indicates valid data by going low. Data output: outputs data, MSB first, on the first rising edge of SCLK.

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OVERVIEW

The ADS1131 is a precision, 18-bit ADC that includes a low-noise PGA, internal oscillator, third-order delta-sigma (ΔΣ) modulator, and fourth-order digital filter. The ADS1131 provides a complete front-end solution for bridge sensor applications such as weigh scales, strain gauges, and pressure sensors.

Data can be output at 10SPS for excellent 50Hz and 60Hz rejection, or at 80SPS when higher speeds are needed. The ADS1131 is easy to configure, and all digital control is accomplished through dedicated pins; there are no registers to program. A simple two-wire serial interface retrieves the data.

ANALOG INPUTS (AINP, AINN)

The input signal to be measured is applied to the input pins AINP and AINN. The ADS1131 accepts differential input signals, but can also measure unipolar signals. When measuring unipolar (or single-ended signals) with respect to ground, connect the negative input (AINN) to ground and connect the input signal to the positive input (AINP). Note that when the ADS1131 is configured this way, only half of the converter full-scale range is used, because only positive digital output codes are produced.

LOW-NOISE AMPLIFIER

The ADS1131 features a low-drift, low-noise amplifier that provides a complete front-end solution for bridge sensors. A simplified diagram of the amplifier is shown in Figure 1. It consists of two chopper-stabilized amplifiers (A1 and A2) and three accurately matched resistors (R_1, R_{F1}, and R_{F2}) that construct a differential front-end stage with a gain of 64, followed by gain stage A3 (Gain = 1). The inputs are equipped with an EMI filter, as shown in Figure 1. The cutoff frequency of the EMI filter is 20MHz. By using AVDD as the reference input, the bipolar input ranges from –39mV to +39mV, and the unipolar input ranges from 0mV to +39mV. The inputs of the ADS1131 are protected with internal diodes connected to the power-supply rails. These diodes clamp the applied signal to prevent it from damaging the input circuitry.

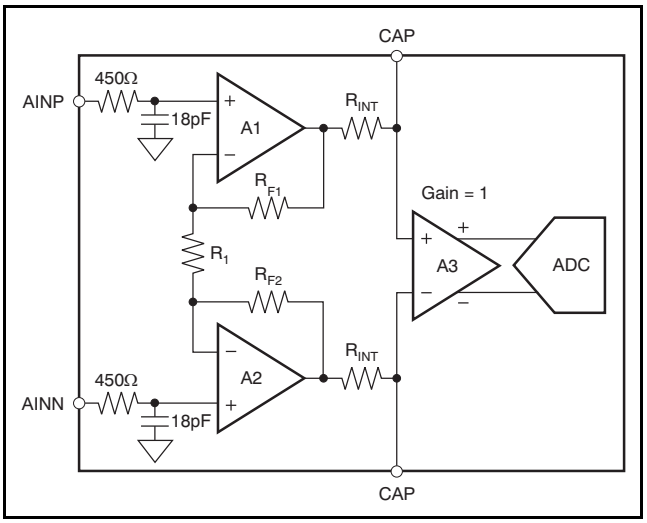


Figure 1. Simplified Diagram of the Amplifier

External Capacitor

An external capacitor (C_{EXT}) across the ADS1131 two CAP pins combines with the internal resistor R_{INT} (on-chip) to create a low-pass filter. The recommended value for C_{EXT} is 0.1μF which provides a corner frequency of 720Hz. This low-pass filter serves two purposes. First, the input signal is bandlimited to prevent aliasing by the ADC and to filter out the high-frequency noise. Second, it attenuates the chopping residue from the amplifier to improve temperature drift performance. NPO or C0G capacitors are recommended. For optimal performance, place the external capacitor very close to the CAP pins.

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VOLTAGE REFERENCE INPUTS (VREFP, VREFN)

The voltage reference used by the modulator is generated from the voltage difference between VREFP and VREFN: V_{REF} = VREFP – VREFN. The reference inputs use a structure similar to that of the analog inputs. In order to increase the reference input impedance, a switching buffer circuitry is used to reduce the input equivalent capacitance. The reference drift and noise impact ADC performance. In order to achieve best results, pay close attention to the reference noise and drift specifications. A simplified diagram of the circuitry on the reference inputs is shown in Figure 2. The switches and capacitors can be modeled approximately using an effective impedance of:

Z_{EFF} = 500MΩ

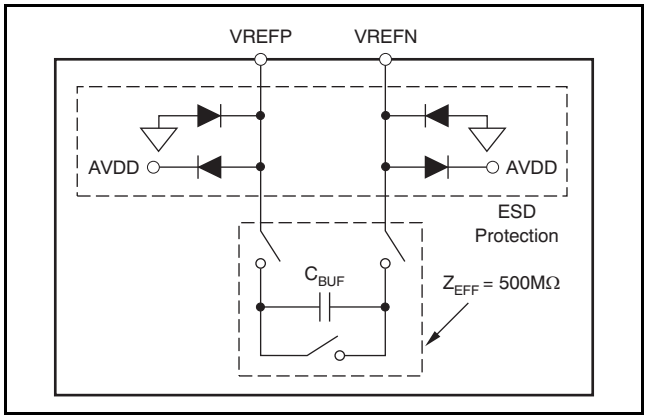


Figure 2. Simplified Reference Input Circuitry

ESD diodes protect the reference inputs. To prevent these diodes from turning on, make sure the voltages on the reference pins do not go below GND by more than 100mV, and likewise, do not exceed AVDD by 100mV:

GND – 100mV < (VREFP or VREFN) < AVDD + 100mV

LOW-SIDE POWER SWITCH (SW)

The ADS1131 incorporates an internal switch for use with an external bridge sensor, as shown in Figure 3. The switch can be used in a return path for the bridge power. By opening the switch, power dissipation in the bridge is eliminated.

The switch is controlled by the ADS1131 conversion status. During normal conversions, the switch is closed (the SW pin is connected to GND). During standby or power-down modes, the switch is opened (the SW pin is high impedance). When using the switch, it is recommended that the negative reference input (VREFN) be connected directly to the bridge ground terminal, as shown in Figure 3 for best performance.

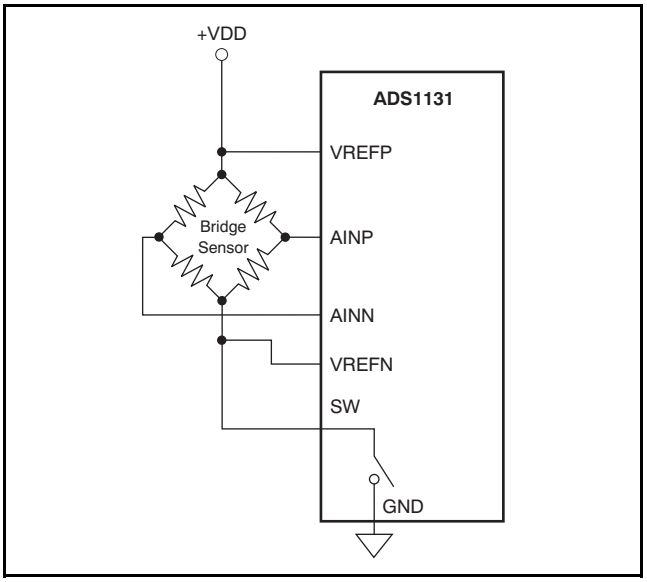


Figure 3. Low-Side Power Switch

CLOCK SOURCE

The ADS1131 uses an internal oscillator. No external clock circuitry is required.

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FREQUENCY RESPONSE

The ADS1131 uses a sinc^4 digital filter with the frequency response. The frequency response repeats at multiples of the modulator sampling frequency of 76.8kHz. The overall response is that of a low-pass filter with a –3dB cutoff frequency of 3.32Hz with the SPEED pin tied low (10SPS data rate) and 11.64Hz with the SPEED pin tied high (80SPS data rate).

To help see the response at lower frequencies, Figure 4(a) illustrates the nominal response out to 100Hz, when the data rate = 10SPS. Notice that signals at multiples of 10Hz are rejected, and therefore simultaneous rejection of 50Hz and 60Hz is achieved.

The benefit of using a sinc^4 filter is that every frequency notch has four zeros on the same location. This response, combined with the low drift internal oscillator, provides an excellent normal-mode rejection of line-cycle interference.

Figure 4(b) zooms in on the 50Hz and 60Hz notches with the SPEED pin tied low (10SPS data rate).

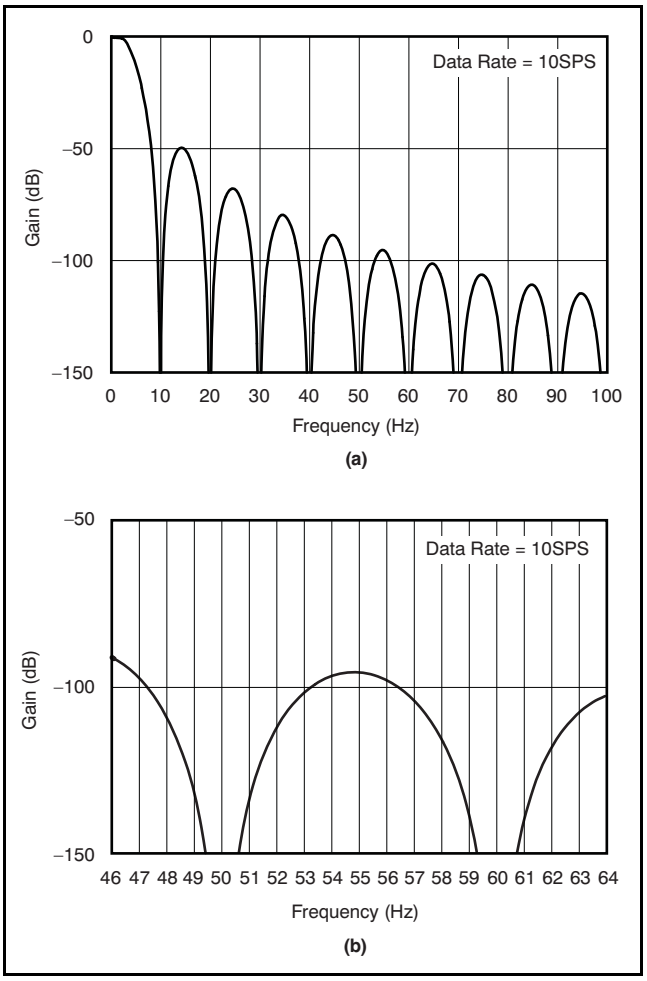


Figure 4. Nominal Frequency Response Out To 100Hz

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SETTLING TIME

Fast changes in the input signal require time to settle. For example, an external multiplexer in front of the ADS1131 can generate abrupt changes in input voltage by simply switching the multiplexer input channels. These sorts of changes in the input require four data conversion cycles to settle. When continuously converting, five readings may be necessary in order to settle the data. If the change in input occurs in the middle of the first conversion, four more full conversions of the fully-settled input are required to obtain fully-settled data. Discard the first four readings because they contain only partially-settled data. Figure 5 illustrates the settling time for the ADS1131.

DATA RATE

The ADS1131 data rate is set by the SPEED pin, as shown in Table 1. When SPEED is low, the data rate is nominally 10SPS. This data rate provides the lowest noise, and also has excellent rejection of both 50Hz and 60Hz line-cycle interference. For applications requiring fast data rates, setting SPEED high selects a data rate of nominally 80SPS.

Table 1. Data Rate Settings

SPEED PIN	DATA RATE
0	10SPS
1	80SPS

DATA FORMAT

The ADS1131 outputs 18 bits of data in binary twos complement format. The least significant bit (LSB) has a weight of $(0.5V_{REF}/64)(2^{17} - 1)$. The positive full-scale input produces an output code of 1FFFFh and the negative full-scale input produces an output code of 20000h. The output clips at these codes for signals exceeding full-scale. Table 2 summarizes the ideal output codes for different input signals.

Table 2. Ideal Output Code vs Input Signal

INPUT SIGNAL V_{IN} (AINP – AINN)	IDEAL OUTPUT
≥ $+0.5V_{REF}/64$	1FFFFh
$(+0.5V_{REF}/64)/(2^{17} - 1)$	00001h
0	00000h
$(-0.5V_{REF}/64)/(2^{17} - 1)$	3FFFFh
≤ $-0.5V_{REF}/64$	20000h

1. Excludes effects of noise, INL, offset, and gain errors.

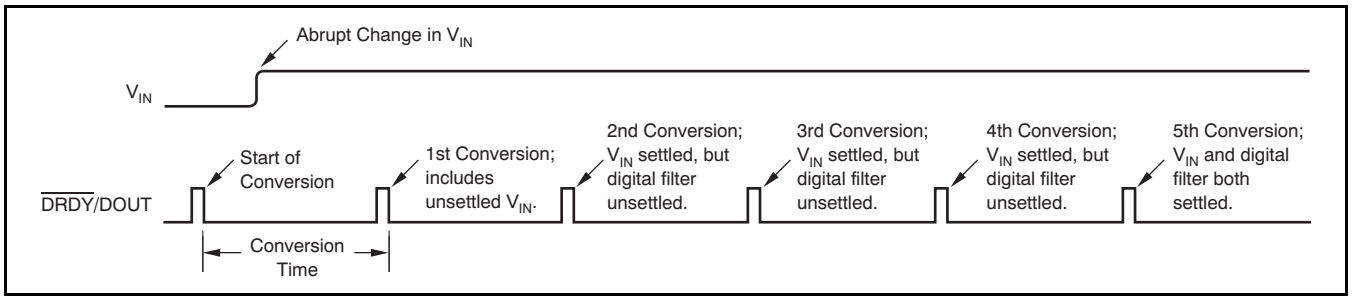


Figure 5. Settling Time in Continuous Conversion Mode

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DATA READY/DATA OUTPUT (DRDY/DOUT)

This digital output pin serves two purposes. First, it indicates when new data are ready by going low. Afterwards, on the first rising edge of SCLK, the DRDY/DOUT pin changes function and begins outputting the conversion data, most significant bit (MSB) first. Data are shifted out on each subsequent SCLK rising edge. After all 18 bits have been retrieved, the pin can be forced high with an additional SCLK. It then stays high until new data are ready. This configuration is useful when polling on the status of DRDY/DOUT to determine when to begin data retrieval.

SERIAL CLOCK INPUT (SCLK)

This digital input shifts serial data out with each rising edge. This input has built-in hysteresis, but care should still be taken to ensure a clean signal. Glitches or slow-rising signals can cause unwanted additional shifting. For this reason, it is best to make sure the rise and fall times of SCLK are both less than 50ns.

DATA RETRIEVAL

The ADS1131 continuously converts the analog input signal. To retrieve data, wait until DRDY/DOUT goes low, as shown in Figure 6. After DRDY/DOUT goes low, begin shifting out the data by applying SCLKs. Data are shifted out MSB first. It is not required to shift out all 18 bits of data, but the data must be retrieved before new data are updated (within t_{CONV}) or else the data will be overwritten. Avoid data retrieval during the update period (t_{UPDATE}). If only 18 SCLKs have been applied, DRDY/DOUT remains at the state of the last bit shifted out until it is taken high (see t_{UPDATE}), indicating that new data are being updated. To avoid having DRDY/DOUT remain in the state of the last bit, the 19th SCLK can be applied to force DRDY/DOUT high, as shown in Figure 7. This technique is useful when a host controlling the device is polling DRDY/DOUT to determine when data are ready.

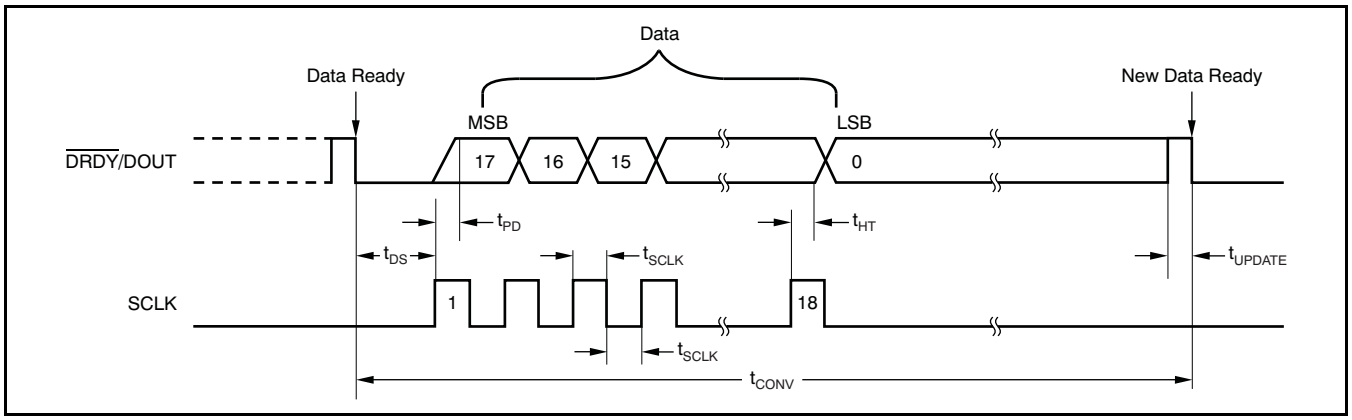


Figure 6. 18-Bit Data Retrieval Timing

SYMBOL	DESCRIPTION		MIN	TYP	MAX	UNITS
t_{DS}	DRDY/DOUT low to first SCLK rising edge		0			ns
t_{SCLK}	SCLK positive or negative pulse width		100			ns
t_{PD} (1)	SCLK rising edge to new data bit valid: propagation delay				50	ns
t_{HT} (1)	SCLK rising edge to old data bit valid: hold time		20			ns
t_{UPDATE}	Data updating: no readback allowed			90		µs
t_{CONV}	Conversion time (1/data rate)	SPEED = 1		12.5		ms
		SPEED = 0		100		ms

(1) Minimum required from simulation.

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STANDBY MODE

Standby mode dramatically reduces power consumption by shutting down most of the circuitry. In Standby mode, the entire analog circuitry is powered down and only the clock source circuitry is awake to reduce the wake-up time from the Standby mode. To enter Standby mode, simply hold SCLK high after DRDY/DOUT goes low; see Figure 8. Standby mode can be initiated at any time during readback; it is not necessary to retrieve all 18 bits of data beforehand.

When $t_{STANDBY}$ has passed with SCLK held high, Standby mode activates. DRDY/DOUT stays high when Standby mode begins. SCLK must remain high to stay in Standby mode. To exit Standby mode (wakeup), set SCLK low. The first data after exiting Standby mode are valid.

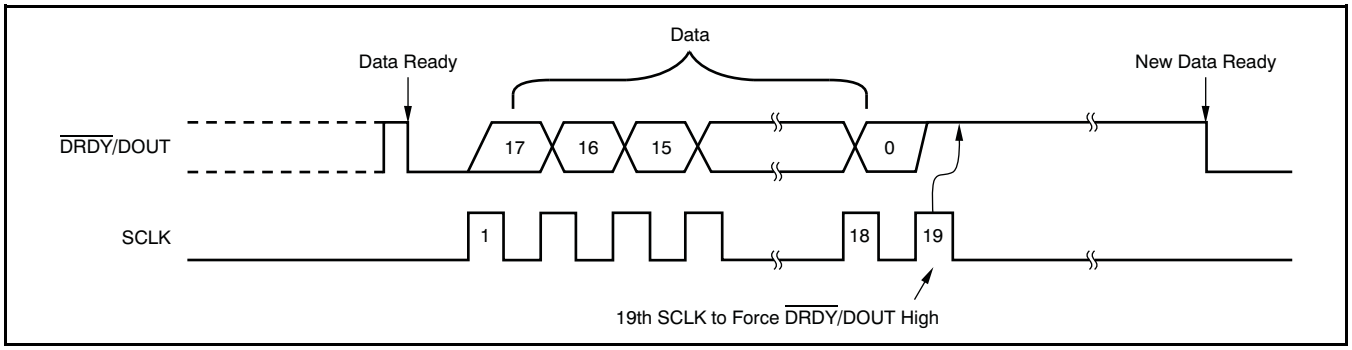


Figure 7. Data Retrieval with DRDY/DOUT Forced High Afterwards

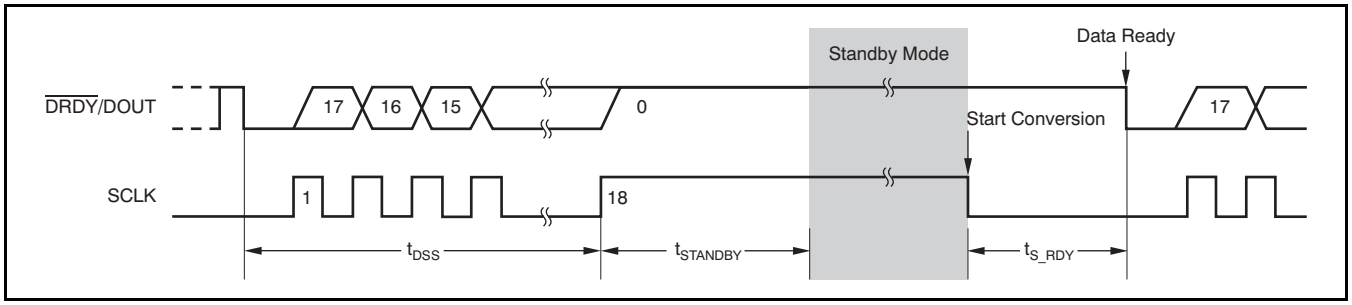


Figure 8. Standby Mode Timing (Can be used for single conversions)

SYMBOL	DESCRIPTION		MIN	TYP	MAX	UNITS
t_{DSS} (1)	SCLK high after DRDY/DOUT goes low to activate Standby mode	SPEED = 1			12.44	ms
		SPEED = 0			99.94	ms
$t_{STANDBY}$	Standby mode activation time	SPEED = 1	0.0125			s
		SPEED = 0	0.1			s
t_{S_RDY} (1)	Data ready after exiting Standby mode	SPEED = 1	No change (typical time required)			ms
		SPEED = 0		401.8		ms

(1) Based on an ideal internal oscillator.

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POWER-DOWN MODE

Power-Down mode shuts down the entire ADC circuitry and reduces the total power consumption close to zero. To enter Power-Down mode, simply hold the $\overline{\text{PDWN}}$ pin low.

Power-Down mode also resets the entire circuitry. Power-Down mode can be initiated at any time during readback; it is not necessary to retrieve all 18 bits of data beforehand. Figure 9 shows the wake-up timing from Power-Down mode.

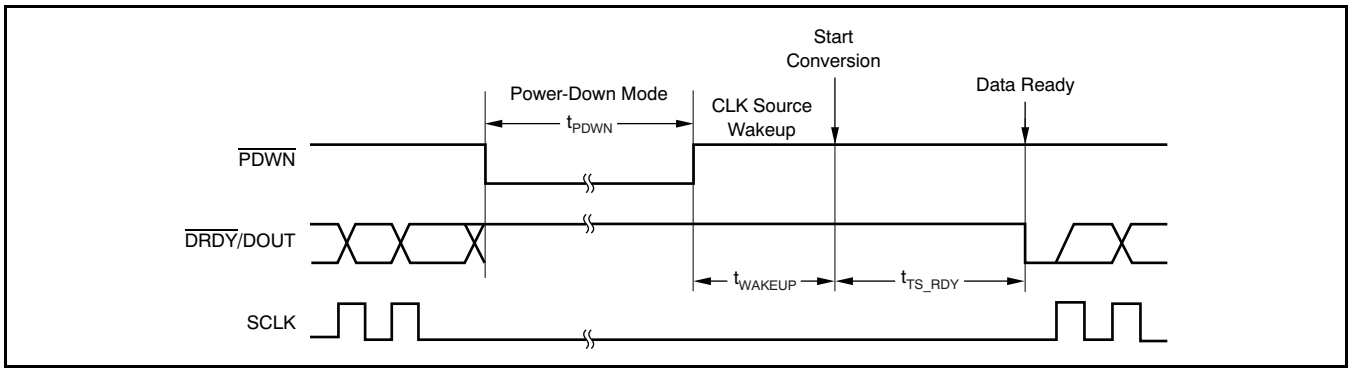


Figure 9. Wake-Up Timing from Power-Down Mode

SYMBOL	DESCRIPTION	MIN	TYP	UNITS
t_{WAKEUP} (1)	Wake-up time after Power-Down mode		7.95	µs
t_{PDWN} (1)	$\overline{\text{PDWN}}$ pulse width	26		µs

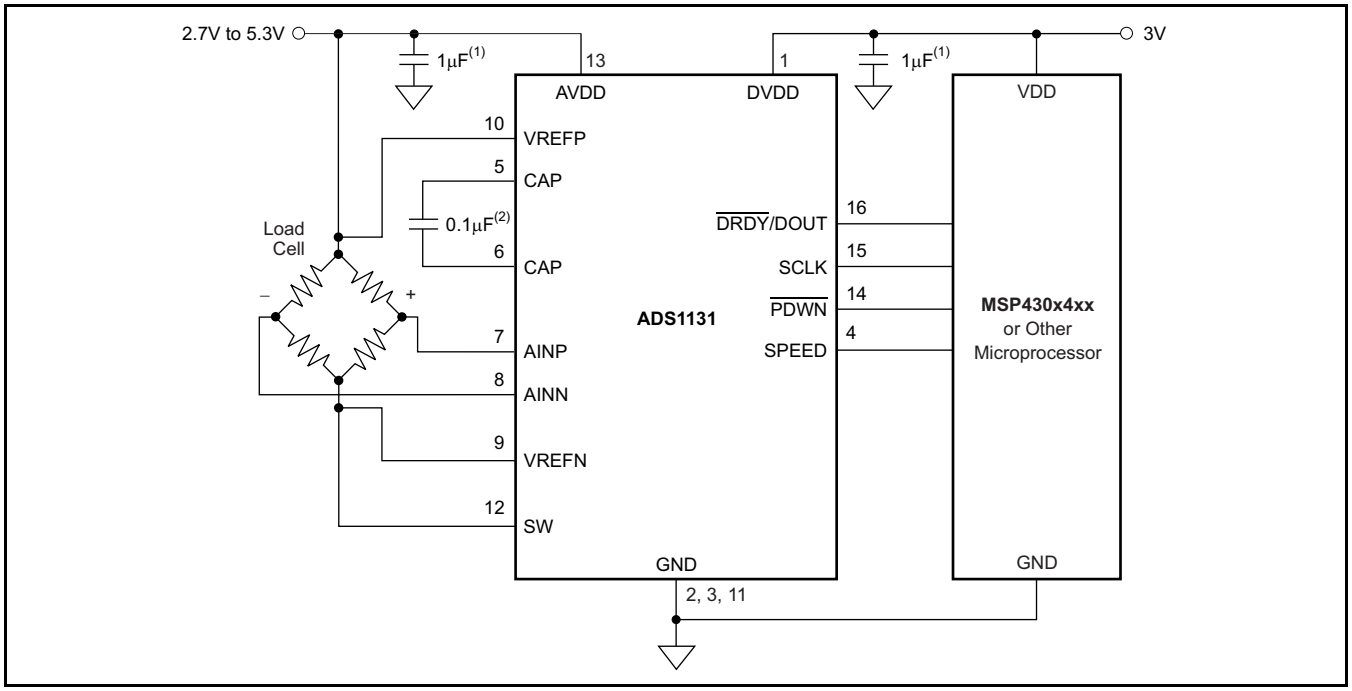
(1) Based on an ideal internal oscillator.

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APPLICATION EXAMPLE

Weigh Scale System

Figure 10 shows a typical ADS1131 application as part of a weigh scale system.



(1) Place a 0.1µF or higher capacitor as close as possible on both AVDD and DVDD.

(2) Place capacitor very close to the ADS1131 CAP pins for optimal performance.

Figure 10. Weigh Scale Example

REVISION HISTORY

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Revision B (September 2011) to Revision C **Page**

- Changed pin 12 name from PSW to SW in pinout drawing 5
- Changed pin 12 name from PSW to SW in Pin Descriptions table 5
- Changed pin numbers in Figure 10 to match the device pinout 13

Changes from Revision A (May 2010) to Revision B **Page**

- Changed *Supply Range* Features bullet 1
- Deleted *ESD Ratings* row and footnote 2 from Absolute Maximum Ratings table 2
- Changed Digital Input/Output, V_{IH} *Logic level* parameter minimum specification in Electrical Characteristics table 3
- Changed Power Supply, *Power-supply voltage* parameter minimum specification in Electrical Characteristics table 4
- Deleted Power Supply, *Analog supply current* parameter maximum specifications in Electrical Characteristics table 4
- Deleted Power Supply, *Digital supply current* parameter maximum specifications in Electrical Characteristics table 4
- Deleted Power Supply, *Power dissipation* parameter maximum specifications in Electrical Characteristics table 4
- Deleted minimum specification and added typical specification to t_{UPDATE} row of table corresponding to Figure 6 10
- Deleted *Power-Up Sequence* section 12

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PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
ADS1131ID	ACTIVE	SOIC	D	16	40	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 85	ADS1131	Samples
ADS1131IDR	ACTIVE	SOIC	D	16	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 85	ADS1131	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

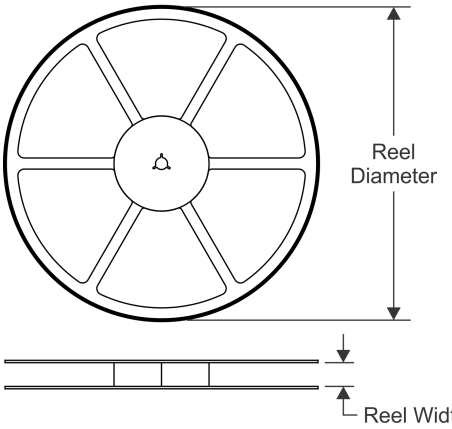
(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

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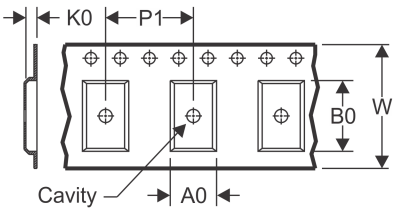
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TAPE AND REEL INFORMATION

REEL DIMENSIONS

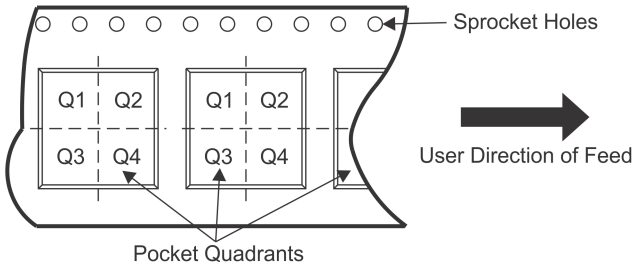


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

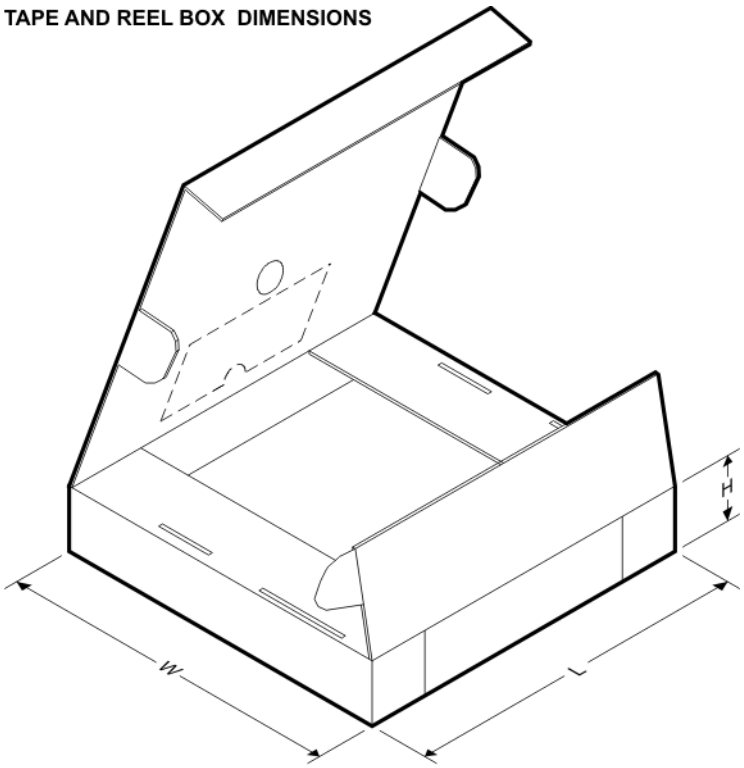
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
ADS1131IDR	SOIC	D	16	2500	330.0	16.4	6.5	10.3	2.1	8.0	16.0	Q1

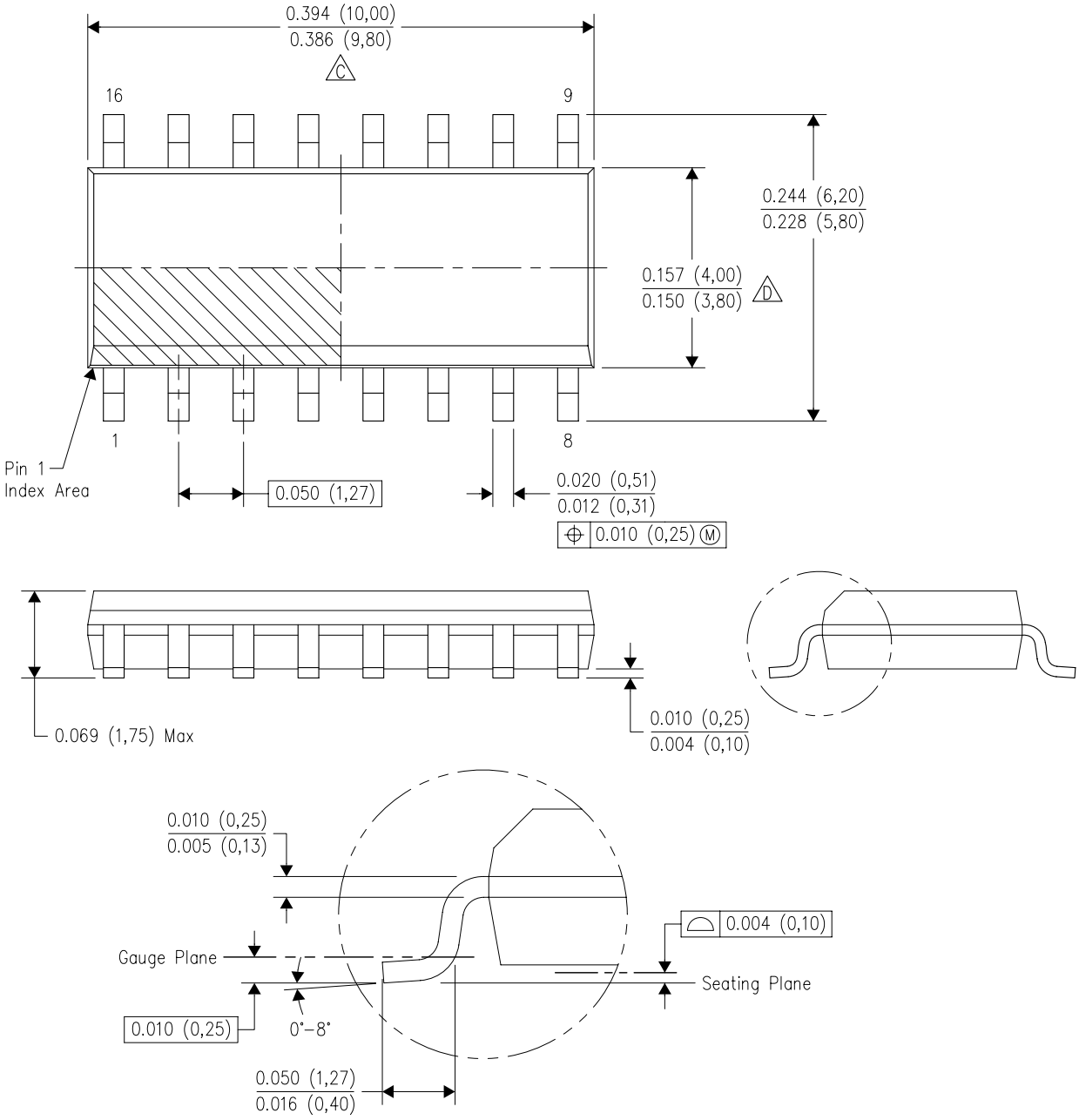
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

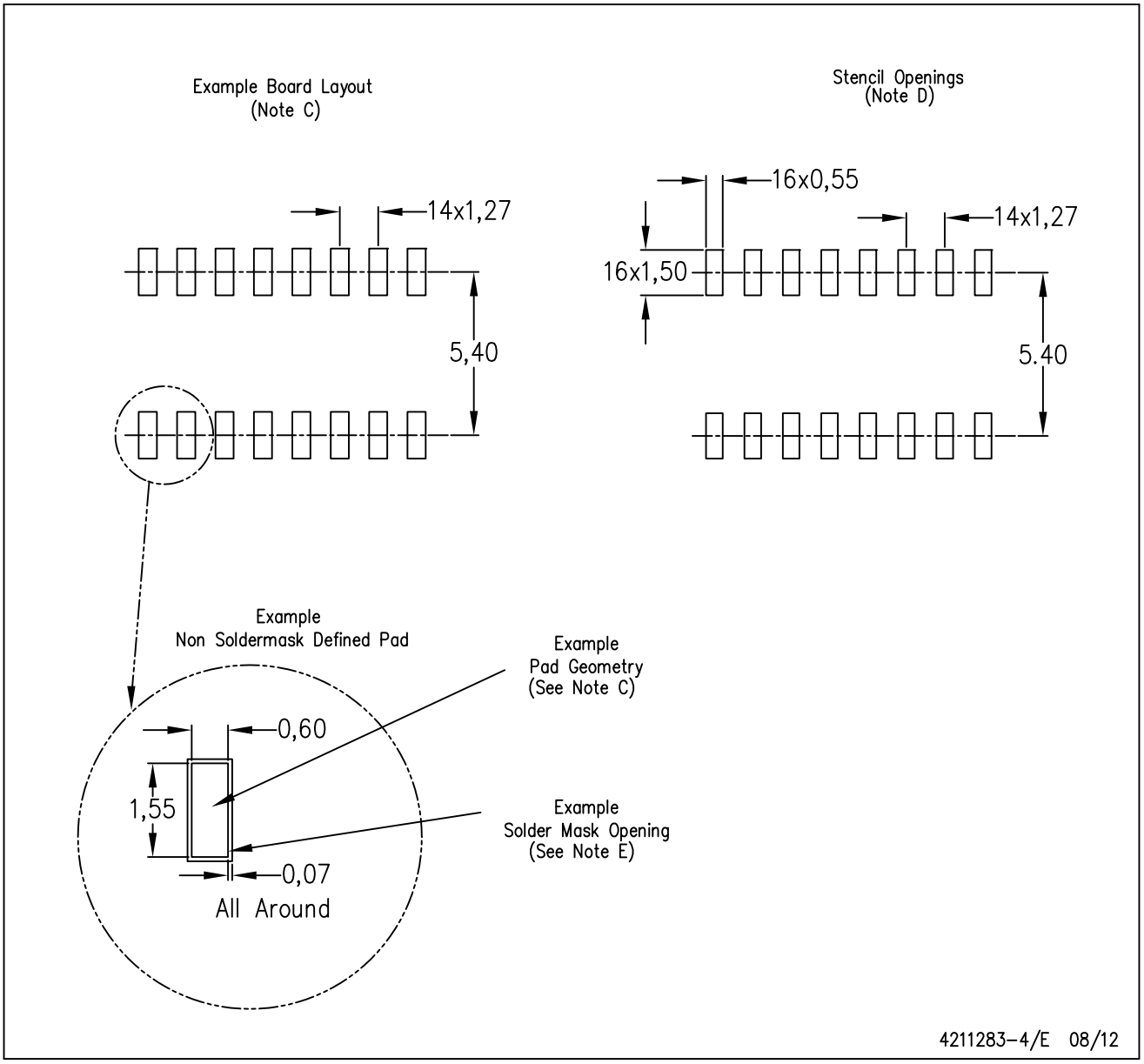
Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
ADS1131IDR	SOIC	D	16	2500	333.2	345.9	28.6

D (R–PDSO–G16) PLASTIC SMALL OUTLINE



NOTES:
A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.006 (0,15) each side.
D. Body width does not include interlead flash. Interlead flash shall not exceed 0.017 (0,43) each side.
E. Reference JEDEC MS–012 variation AC.

D (R–PDSO–G16) PLASTIC SMALL OUTLINE



NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Publication IPC–7351 is recommended for alternate designs.
D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC–7525 for other stencil recommendations.
E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

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