Micropower Single Supply Rail-to-Rail Input-Output Precision Op Amp

The EL8176 is a micropower precision operational amplifier optimized for single supply operation at 5V and can operate down to 2.4V.

The EL8176 draws minimal supply current while meeting excellent DC-accuracy noise and output drive specifications. Competing devices seriously degrade these parameters to achieve micropower supply current.

The EL8176 can be operated from one lithium cell or two Ni-Cd batteries. The input range includes both positive and negative rail. The output swings to both rails.

Ordering Information

PART NUMBER	PART MARKING	TAPE & REEL	PACKAGE	PKG. DWG. #
EL8176FWZ-T7 (Note)	BBVA (Bottom)	7” (3k pcs)	6 Ld SOT-23 (Pb-free)	MDP0038
EL8176FWZ-T7A (Note)	BBVA (Bottom)	7” (250 pcs)	6 Ld SOT-23 (Pb-free)	MDP0038
EL8176FSZ (Note)	8176FSZ	-	8 Ld SO (Pb-free)	MDP0027
EL8176FSZ-T7 (Note)	8176FSZ	7” (1k pcs)	8 Ld SO (Pb-free)	MDP0027

NOTE: Intersil Pb-free plus anneal products employ special Pb-free material sets; molding compounds/die attach materials and 100% matte tin plate termination finish, which are RoHS compliant and compatible with both SnPb and Pb-free soldering operations. Intersil Pb-free products are MSL classified at Pb-free peak reflow temperatures that meet or exceed the Pb-free requirements of IPC/JEDEC J STD-020.

Features

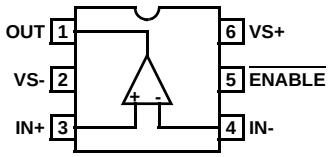
- 55µA supply current
- 100µV max offset voltage (8 Ld SO)
- 2nA input bias current
- 400kHz gain-bandwidth product
- Single supply operation down to 2.4V
- Rail-to-rail input and output
- Output sources 31mA and sinks 26mA load current
- Pb-free plus anneal available (RoHS compliant)

Applications

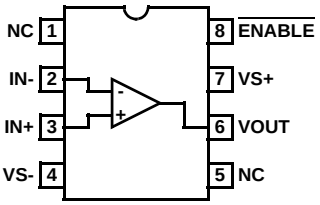
- Battery- or solar-powered systems
- 4mA to 20mA current loops
- Handheld consumer products
- Medical devices
- Thermocouple amplifiers
- Photodiode pre amps
- pH probe amplifiers

Pinouts

EL8176
(6 LD SOT-23)
TOP VIEW



EL8176
(8 LD SO)
TOP VIEW



Absolute Maximum Ratings (T_A = +25°C)

Supply Voltage 5.5V, 1V/µs
Differential Input Voltage 0.5V
Current into I_N+, I_N-, and $\overline{\text{ENABLE}}$ 5mA
Input Voltage . . . . . - 0.5V to V_S+0.5V
Output Short-Circuit Duration . . . . . .Indefinite
Ambient Operating Temperature Range . . . . . .-40°C to +125°C
Storage Temperature Range . . . . . .-65°C to +150°C
Operating Junction Temperature . . . . . .+125°C

CAUTION: Stresses above those listed in "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

IMPORTANT NOTE: All parameters having Min/Max specifications are guaranteed. Typical values are for information purposes only. Unless otherwise noted, all tests are at the specified temperature and are pulsed tests, therefore: $T_J = T_C = T_A$

Electrical Specifications

V_S = 5V, 0V, V_{CM} = 0.1V, V_O = 1.4V, V_{ENH} = 2.0V, V_{ENL} = 0.8V, T_A = +25°C unless otherwise specified. **Boldface limits** apply over the operating temperature range, -40°C to +125°C.

PARAMETER	DESCRIPTION	CONDITIONS	MIN	TYP	MAX	UNIT
V_{OS}	Input Offset Voltage	8 Ld SO	-100	±25	100	µV
			-220		**220**	µV
		6 Ld SOT-23	-350	±80	350	µV
			-350		**350**	µV
$\frac{\Delta V_{OS}}{\Delta Time}$	Long Term Input Offset Voltage Stability			2.4		µV/Mo
$\frac{\Delta V_{OS}}{\Delta T}$	Input Offset Drift vs Temperature			0.7		µV/°C
I_{OS}	Input Offset Current		-1	±0.4	1	nA
			-4		**4**	nA
I_B	Input Bias Current		-2	±0.5	2	nA
			-5		**5**	nA
e_N	Input Noise Voltage Peak-to-Peak	f = 0.1Hz to 10Hz		1		μV_{PP}
	Input Noise Voltage Density	f_O = 1kHz		25		nV/√Hz
i_N	Input Noise Current Density	f_O = 1kHz		0.1		pA/√Hz
CMIR	Input Voltage Range	Guaranteed by CMRR test	0		5	V
CMRR	Common-Mode Rejection Ratio	V_{CM} = 0V to 5V	90	110		dB
			90			dB
PSRR	Power Supply Rejection Ratio	V_S = 2.4V to 5V	90	110		dB
			90			dB
A_{VOL}	Large Signal Voltage Gain	V_O = 0.5V to 4.5V, R_L = 100kΩ	200	500		V/mV
			200			V/mV
		V_O = 0.5V to 4.5V, R_L = 1kΩ		25		V/mV
V_{OUT}	Maximum Output Voltage Swing	VOL; Output low, R_L = 100kΩ		3	8	mV
					10	mV
		VOL; Output low, R_L = 1kΩ		130	200	mV
					300	mV
		VOH; Output high, R_L = 100kΩ	4.994	4.997		V
			4.992			V
		VOH; Output high, R_L = 1kΩ	4.750	4.867		V
			4.7			V

Electrical Specifications V_S = 5V, 0V, V_{CM} = 0.1V, V_O = 1.4V, V_{ENH} = 2.0V, V_{ENL} = 0.8V, T_A = +25°C unless otherwise specified. **Boldface limits** apply over the operating temperature range, -40°C to +125°C. **(Continued)**

PARAMETER	DESCRIPTION	CONDITIONS	MIN	TYP	MAX	UNIT
SR	Slew Rate		**±0.065**	±0.13	**±0.3**	V/µs
GBW	Gain Bandwidth Product	f_O = 100kHz		400		kHz
BW	-3dB Bandwidth	Unity gain, C_{LOAD} = 27pF, R_F = 100Ω		1		MHz
$I_{S,ON}$	Supply Current, Enabled		35	55	75	µA
			30		**90**	µA
$I_{S,OFF}$	Supply Current, Disabled			3	10	µA
					10	µA
I_O+	Short Circuit Output Sourcing Current	R_L = 10Ω	18	31		mA
			18			mA
I_O-	Short Circuit Output Sinking Current	R_L = 10Ω	17	26		mA
			15			mA
V_S	Minimum Supply Voltage	Guaranteed by PSRR test		2.2	2.4	V
					2.4	V
V_{INH}	Enable Pin High Level				2	V
V_{INL}	Enable Pin Low Level		0.8			V
I_{ENH}	Enable Pin Input Current	V_{EN} = 5V	0.25	0.7	2.0	µA
					2.5	µA
I_{ENL}	Enable Pin Input Current	V_{EN} = 0V	-0.5	0	+0.5	µA
			-1		**+1**	µA

Typical Performance Curves

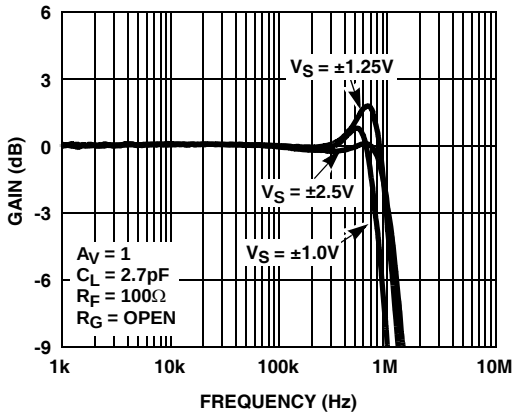


FIGURE 1. UNITY GAIN FREQUENCY RESPONSE vs SUPPLY VOLTAGE

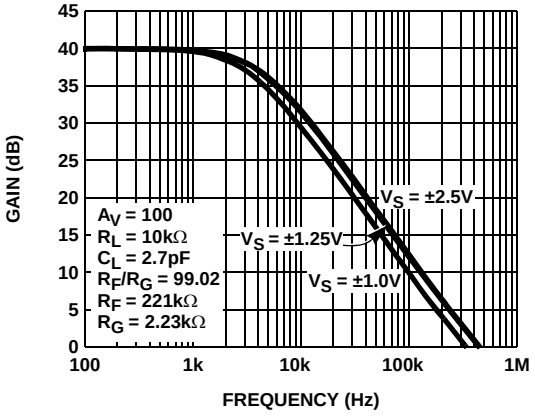


FIGURE 2. FREQUENCY RESPONSE vs SUPPLY VOLTAGE

Typical Performance Curves (Continued)

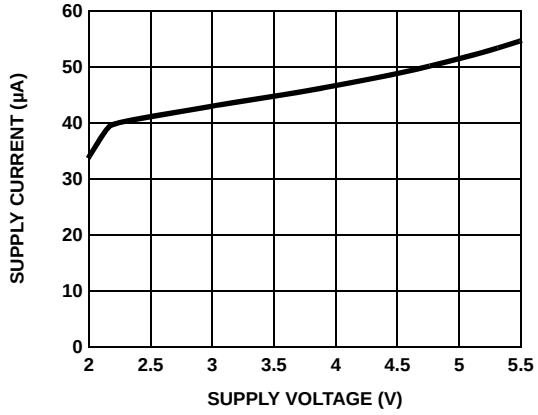


FIGURE 3. SUPPLY CURRENT vs SUPPLY VOLTAGE

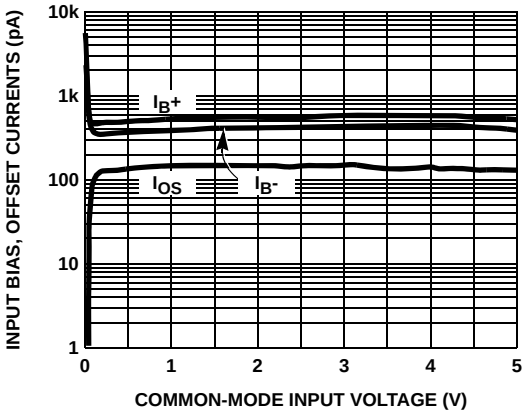


FIGURE 4. INPUT BIAS + OFFSET CURRENTS vs COMMON-MODE INPUT VOLTAGE

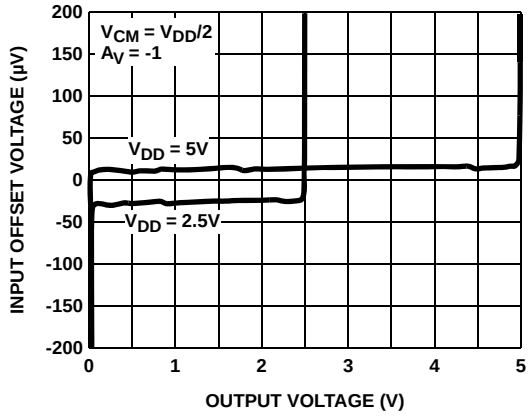


FIGURE 5. INPUT OFFSET VOLTAGE vs OUTPUT VOLTAGE

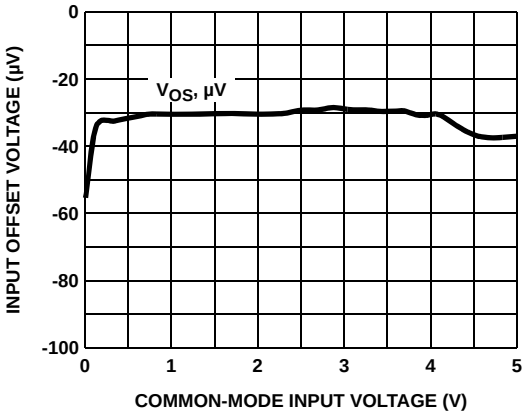


FIGURE 6. INPUT OFFSET VOLTAGE vs COMMON-MODE INPUT VOLTAGE

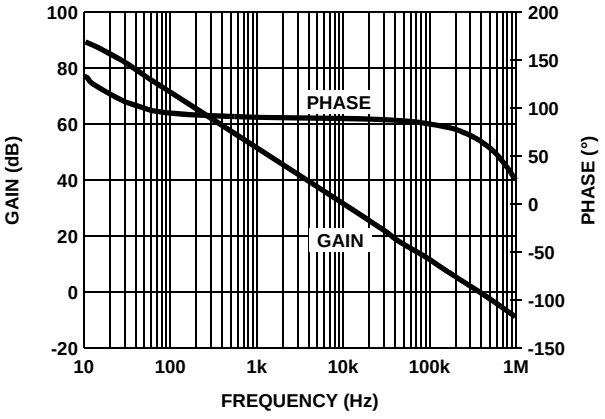


FIGURE 7. A_{VOL} vs FREQUENCY @ 1kΩ LOAD

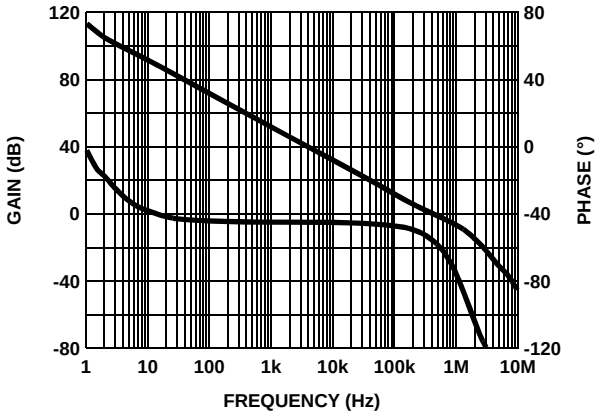


FIGURE 8. A_{VOL} vs FREQUENCY @ 100kΩ LOAD

Typical Performance Curves (Continued)

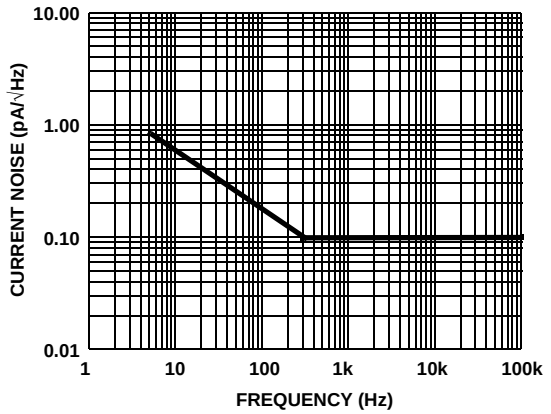


FIGURE 9. CURRENT NOISE vs FREQUENCY

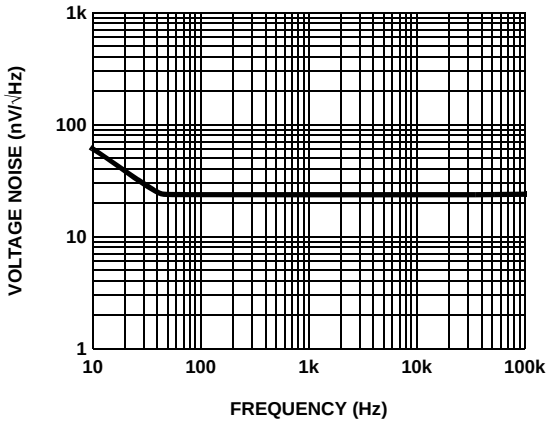


FIGURE 10. VOLTAGE NOISE vs FREQUENCY

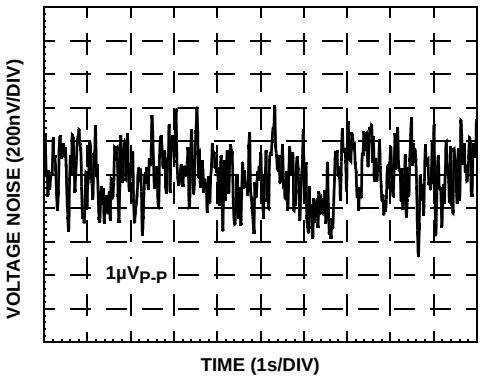


FIGURE 11. 0.1Hz TO 10Hz INPUT VOLTAGE NOISE

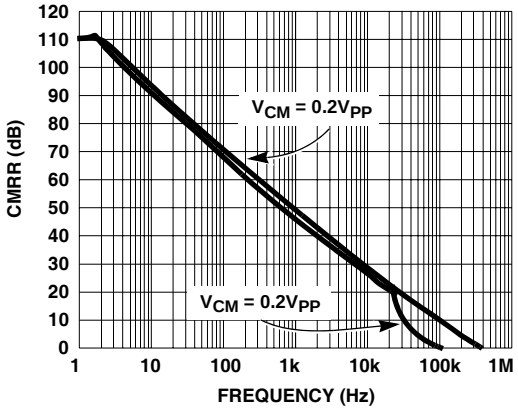


FIGURE 12. CMRR vs FREQUENCY

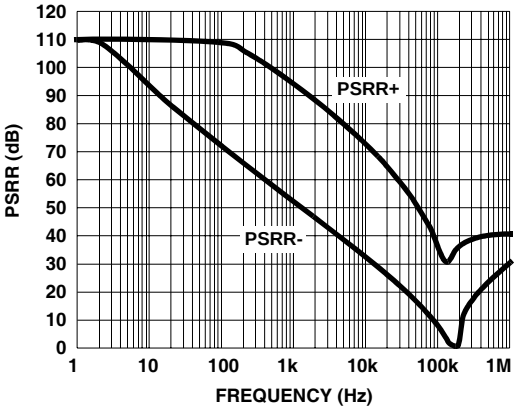


FIGURE 13. PSRR vs FREQUENCY

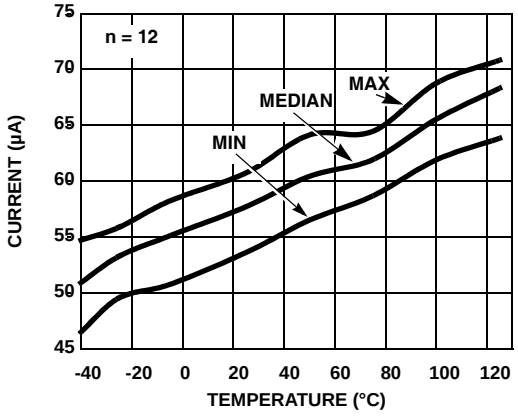


FIGURE 14. SUPPLY CURRENT vs TEMPERATURE
V_S = ±2.5V ENABLED. R_L = INF
FIGURE 15.

Typical Performance Curves (Continued)

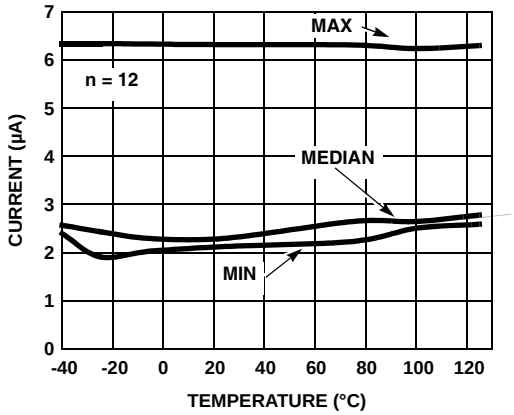


FIGURE 16. SUPPLY CURRENT vs TEMPERATURE V_S = ±2.5V DISABLED. R_L= INF

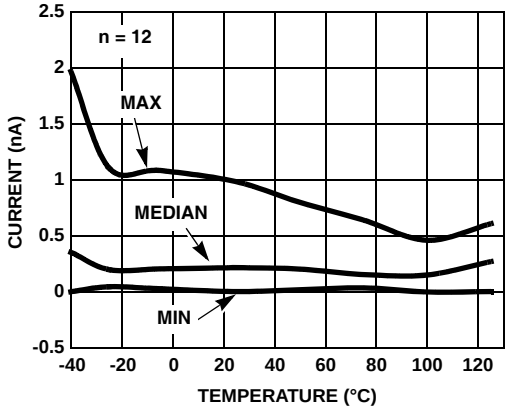


FIGURE 17. I BIAS (+) vs TEMPERATURE V_S = ±2.5V

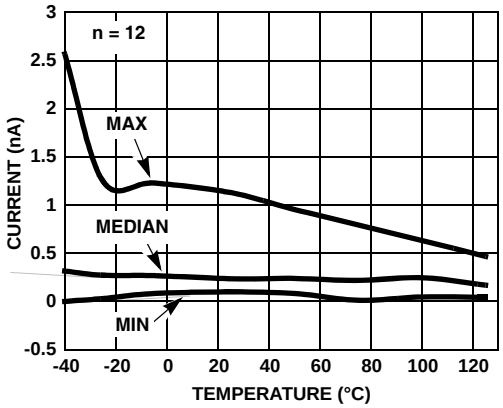


FIGURE 18. I BIAS (+) vs TEMPERATURE V_S = ±1.2V

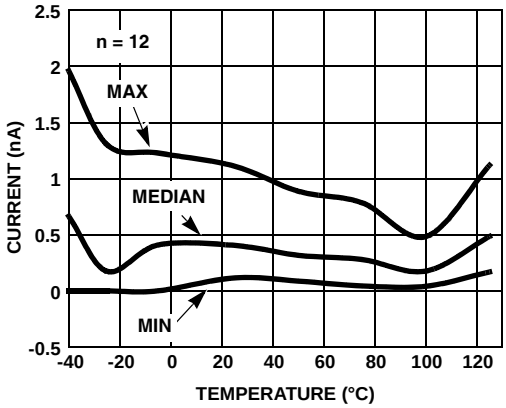


FIGURE 19. I BIAS (-) vs TEMPERATURE V_S = ±2.5V

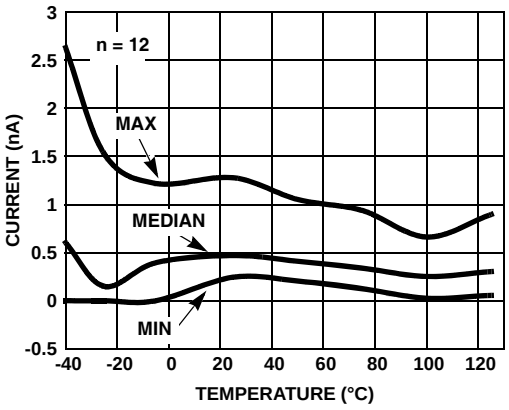


FIGURE 20. I BIAS (-) vs TEMPERATURE V_S = ±1.2V

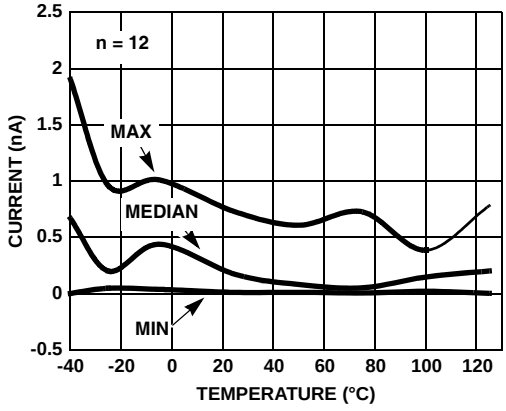


FIGURE 21. INPUT OFFSET CURRENT vs TEMPERATURE V_S = ±2.5V

Typical Performance Curves (Continued)

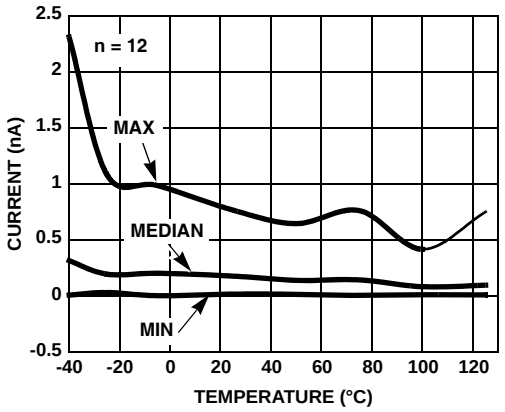


FIGURE 22. INPUT OFFSET CURRENT vs TEMPERATURE
V_S = ±1.2V

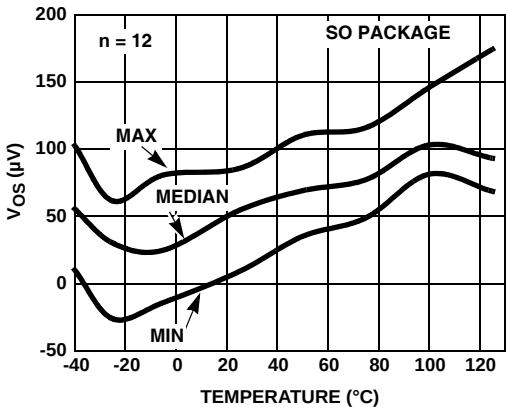


FIGURE 23. INPUT OFFSET VOLTAGE vs TEMPERATURE
V_S = ±2.5V

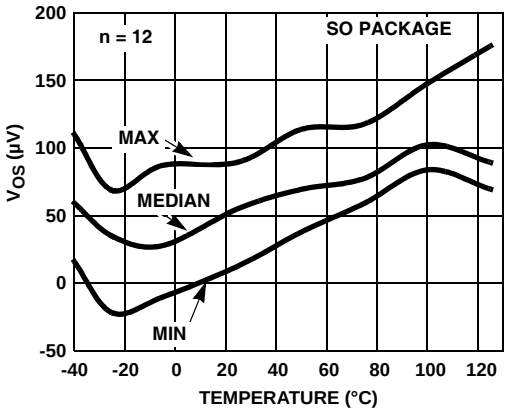


FIGURE 24. INPUT OFFSET VOLTAGE vs TEMPERATURE
V_S = ±1.2V

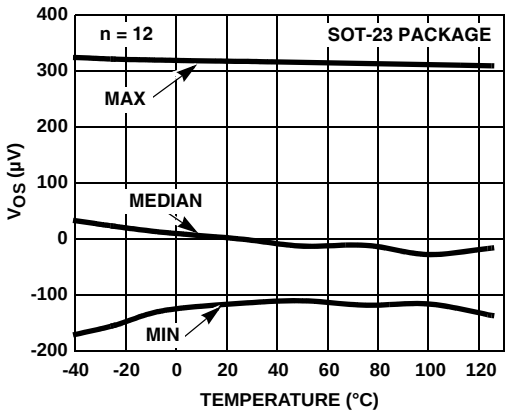


FIGURE 25. INPUT OFFSET VOLTAGE vs TEMPERATURE
V_S = ±2.5V

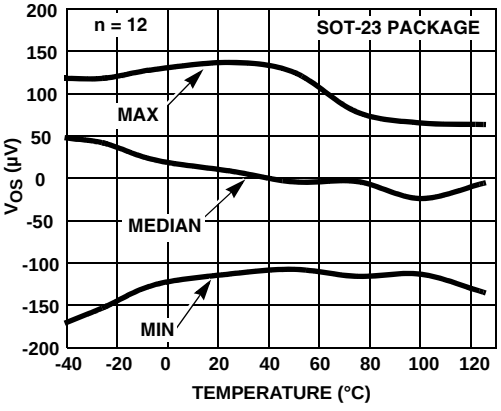


FIGURE 26. INPUT OFFSET VOLTAGE vs TEMPERATURE
V_S = ±1.2V

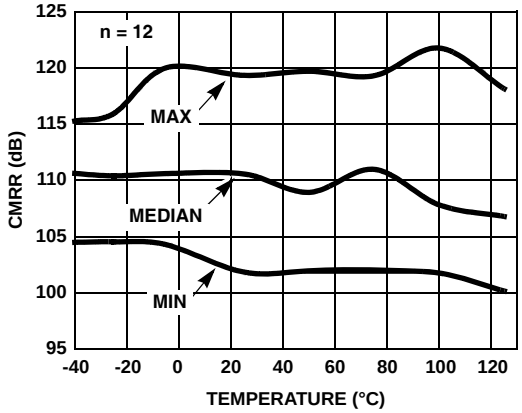


FIGURE 27. CMRR vs TEMPERATURE VCM = +2.5V TO -2.5V

Typical Performance Curves (Continued)

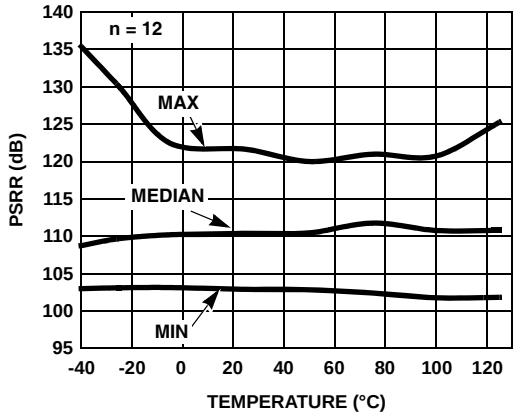


FIGURE 28. PSRR vs TEMPERATURE V_S = ±1.2V TO ±2.5V

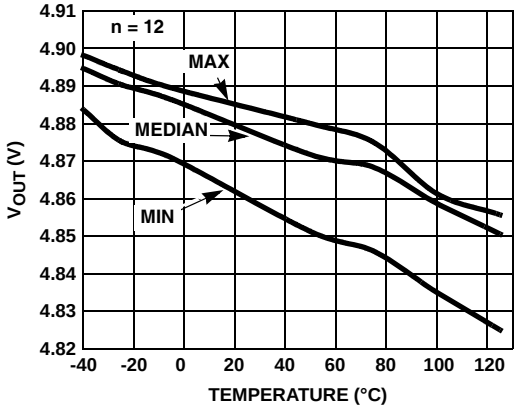


FIGURE 29. POSITIVE V_{OUT} vs TEMPERATURE R_L = 1k V_S = ±2.5V

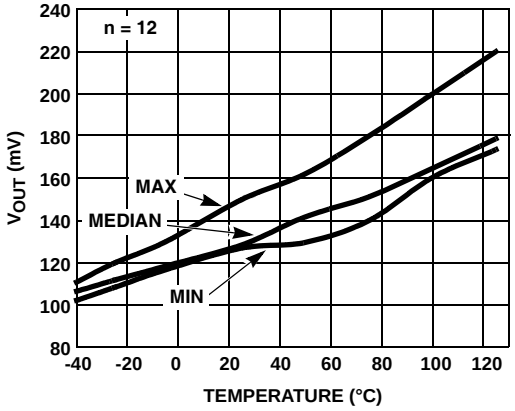


FIGURE 30. NEGATIVE V_{OUT} vs TEMPERATURE R_L = 1k V_S = ±2.5V

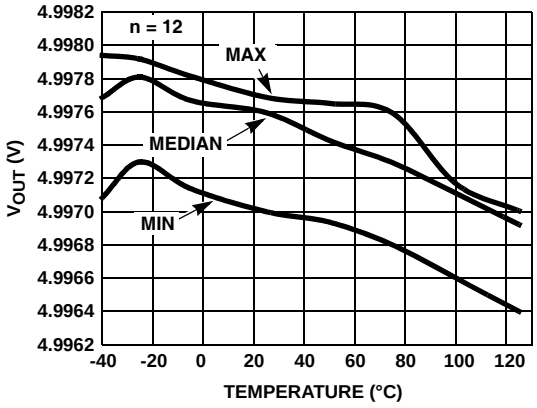


FIGURE 31. POSITIVE V_{OUT} vs TEMPERATURE R_L = 100k V_S = ±2.5V

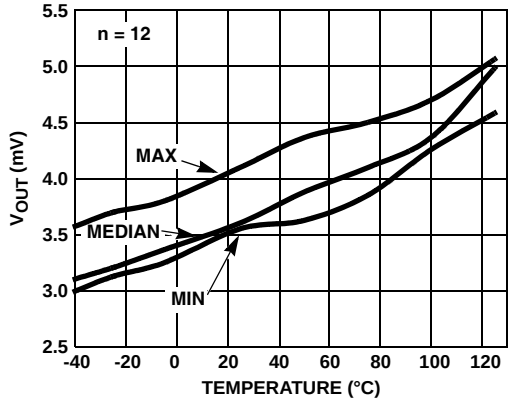


FIGURE 32. NEGATIVE V_{OUT} vs TEMPERATURE R_L = 100k V_S = ±2.5V

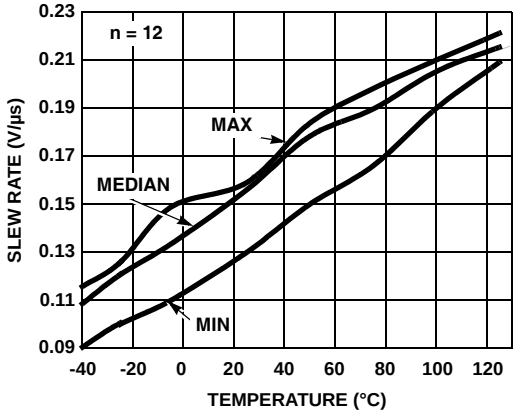


FIGURE 33. +SLEW RATE vs TEMPERATURE V_S = ±2.5V INPUT = ±0.75V, A_V = 2

Typical Performance Curves (Continued)

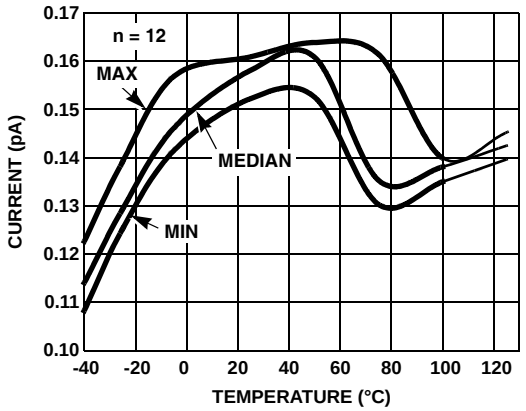


FIGURE 34. -SLEW RATE vs TEMPERATURE V_S = ±2.5V INPUT = ±0.75V, A_V = 2

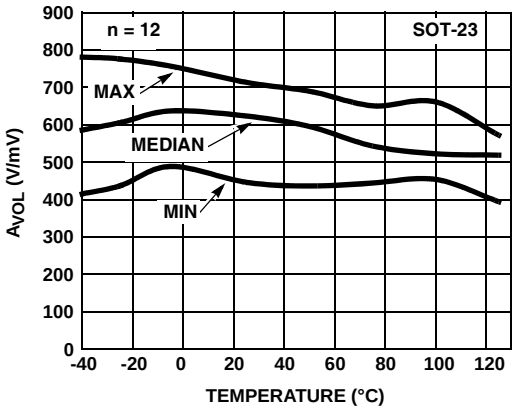


FIGURE 35. A_{VOL}, R_L = 100k V_O @+2V/-2V @V_S ±2.5V

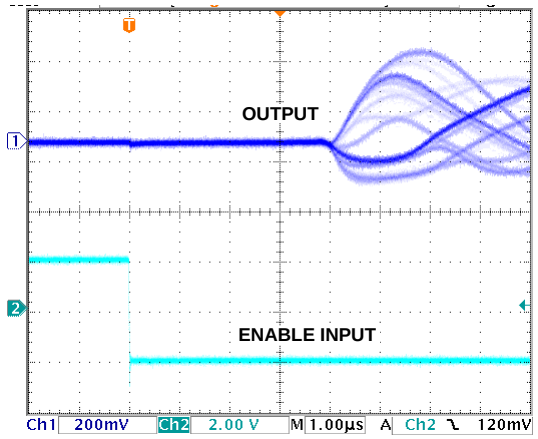


FIGURE 36. ENABLE DELAY TIME

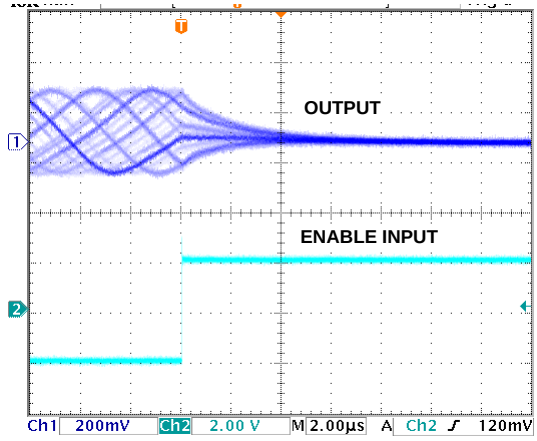


FIGURE 37. DISABLE DELAY TIME

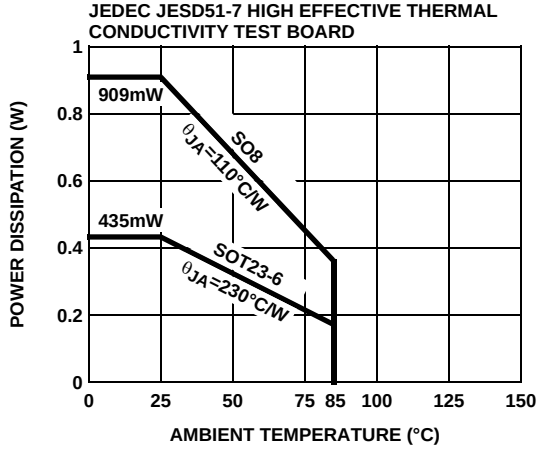


FIGURE 38. PACKAGE POWER DISSIPATION vs AMBIENT TEMPERATURE

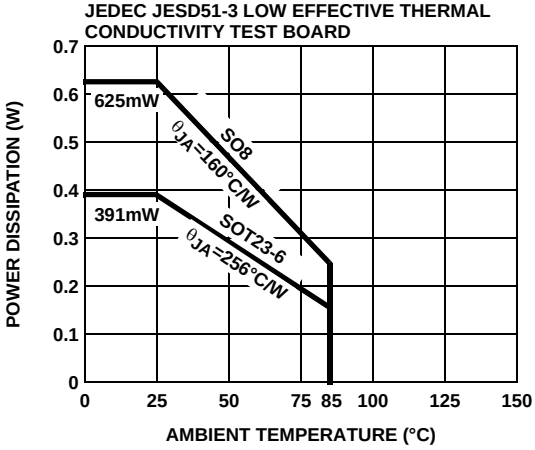


FIGURE 39. PACKAGE POWER DISSIPATION vs AMBIENT TEMPERATURE

Applications Information

Introduction

The EL8176 is a rail-to-rail input and output micro-power precision single supply operational amplifier with an enable feature. The device achieves rail-to-rail input and output operation and eliminates the concerns introduced by a conventional rail-to-rail I/O operational amplifier as discussed below.

Rail-to-Rail Input

The input common-mode voltage range of the EL8176 goes from negative supply to positive supply without introducing offset errors or degrading performance associated with a conventional rail-to-rail input operational amplifier. Many rail-to-rail input stages use two differential input pairs, a long-tail PNP (or PFET) and an NPN (or NFET). Severe penalties have to be paid for this circuit topology. As the input signal moves from one supply rail to another, the operational amplifier switches from one input pair to the other causing drastic changes in input offset voltage and an undesired change in magnitude and polarity of input offset current.

The EL8176 achieves input rail-to-rail without sacrificing important precision specifications and without degrading distortion performance. The EL8176's input offset voltage exhibits a smooth behavior throughout the entire common-mode input range. The input bias current versus the common-mode voltage range for the EL8176 gives us an undistorted behavior from typically 10mV above the negative rail all the way up to the positive rail.

Input Bias Current Compensation

The input bias currents as low as 500pA are achieved while maintaining an excellent bandwidth for a micro-power operational amplifier. Inside the EL8176 is an input bias canceling circuit. The input stage transistors are still biased with an adequate current for speed but the canceling circuit sinks most of the base current, leaving a small fraction as input bias current. The input bias current compensation/cancellation is stable from -40°C to +125°C and operates from typically 10mV to the positive supply rail.

Rail-to-Rail Output

A pair of complementary MOSFET devices achieves rail-to-rail output swing. The NMOS sinks current to swing the output in the negative direction. The PMOS sources current to swing the output in the positive direction. The EL8176 with a 100kΩ load will swing to within 3mV of the supply rails.

Enable/Disable Feature

The EL8176 offers an $\overline{EN}$ pin. The active low $\overline{EN}$ pin disables the device when pulled up to at least 2.0V. When disabled, the output is in a high impedance state and the part consumes typically 3µA. When disabled, the high impedance output allows multiple parts to be MUXed together. When configured as a MUX, the outputs are tied together in parallel and a channel can be selected by pulling the $\overline{EN}$ pin to 0.8V or lower.The $\overline{EN}$ pin has an internal pull-down. If left open or floating, the $\overline{EN}$ pin will internally be pulled low, enabling the part by default.

Proper Layout Maximizes Performance

To achieve the maximum performance of the high input impedance and low offset voltage of the EL8176, care should be taken in the circuit board layout. The PC board surface must remain clean and free of moisture to avoid leakage currents between adjacent traces. Surface coating of the circuit board will reduce surface moisture and provide a humidity barrier, reducing parasitic resistance on the board. The use of guard rings around the amplifier inputs will further reduce leakage currents. Figure 40 shows how the guard ring should be configured and Figure 41 shows the top view of how a surface mount layout can be arranged. The guard ring does not need to be a specific width, but it should form a continuous loop around both inputs. By setting the guard ring voltage equal to the voltage at the non-inverting input, parasitic capacitance is minimized as well. For further reduction of leakage currents, components can be mounted to the PC board using Teflon standoff insulators.

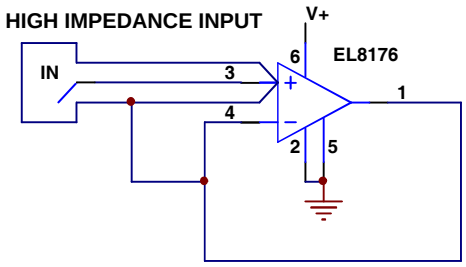


FIGURE 40.

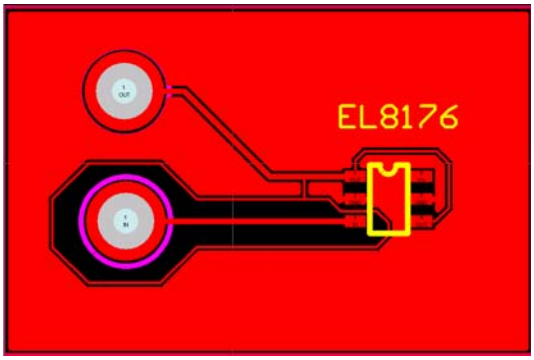


FIGURE 41.

Typical Applications

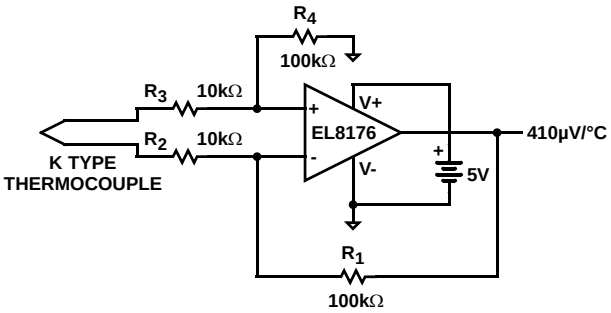
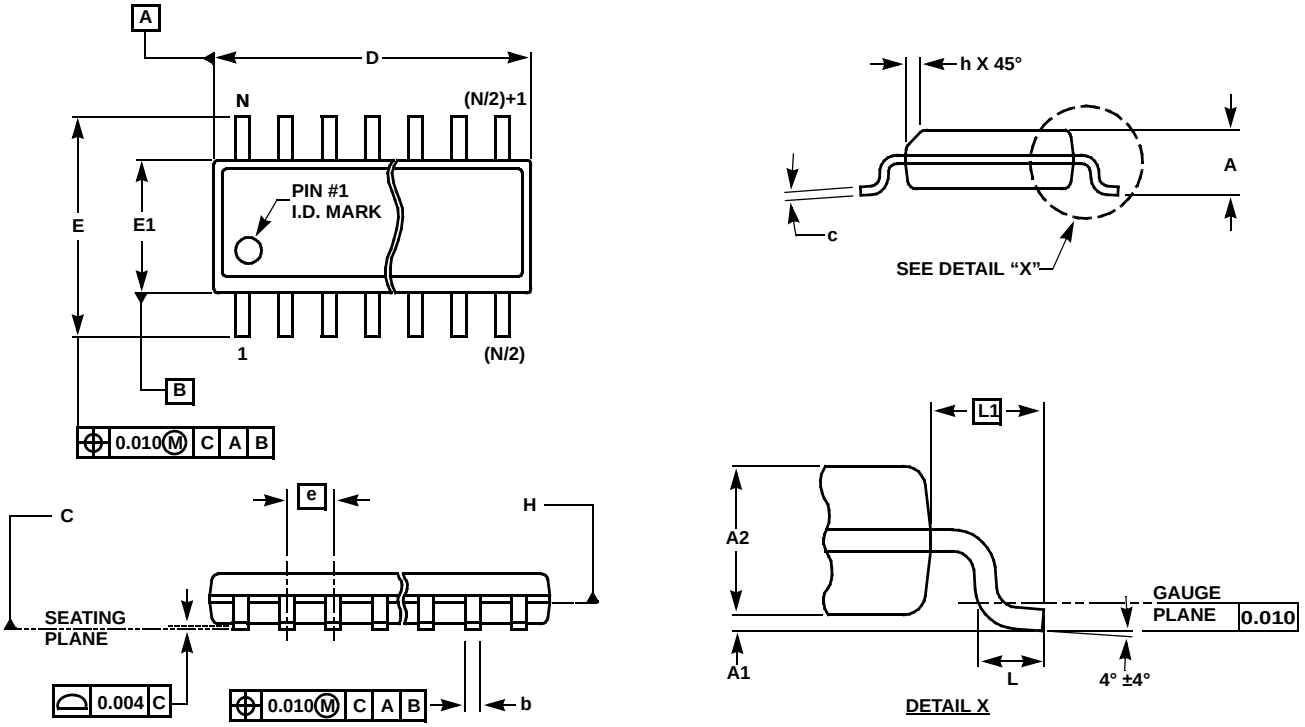


FIGURE 42. THERMOCOUPLE AMPLIFIER

Thermocouples are the most popular temperature-sensing device because of their low cost, interchangeability, and ability to measure a wide range of temperatures. The EL8176 is used to convert the differential thermocouple voltage into single-ended signal with 10X gain. The EL8176's rail-to-rail input characteristic allows the thermocouple to be biased at ground and the converter to run from a single 5V supply.

Small Outline Package Family (SO)



MDP0027

SMALL OUTLINE PACKAGE FAMILY (SO)

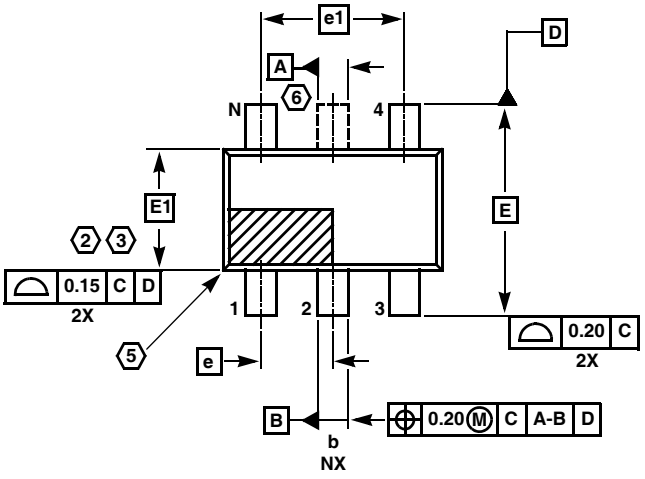
SYMBOL	SO-8	SO-14	SO16 (0.150")	SO16 (0.300") (SOL-16)	SO20 (SOL-20)	SO24 (SOL-24)	SO28 (SOL-28)	TOLERANCE	NOTES
A	0.068	0.068	0.068	0.104	0.104	0.104	0.104	MAX	-
A1	0.006	0.006	0.006	0.007	0.007	0.007	0.007	±0.003	-
A2	0.057	0.057	0.057	0.092	0.092	0.092	0.092	±0.002	-
b	0.017	0.017	0.017	0.017	0.017	0.017	0.017	±0.003	-
c	0.009	0.009	0.009	0.011	0.011	0.011	0.011	±0.001	-
D	0.193	0.341	0.390	0.406	0.504	0.606	0.704	±0.004	1, 3
E	0.236	0.236	0.236	0.406	0.406	0.406	0.406	±0.008	-
E1	0.154	0.154	0.154	0.295	0.295	0.295	0.295	±0.004	2, 3
e	0.050	0.050	0.050	0.050	0.050	0.050	0.050	Basic	-
L	0.025	0.025	0.025	0.030	0.030	0.030	0.030	±0.009	-
L1	0.041	0.041	0.041	0.056	0.056	0.056	0.056	Basic	-
h	0.013	0.013	0.013	0.020	0.020	0.020	0.020	Reference	-
N	8	14	16	16	20	24	28	Reference	-

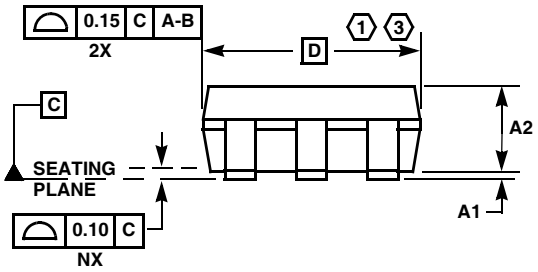
Rev. L 2/01

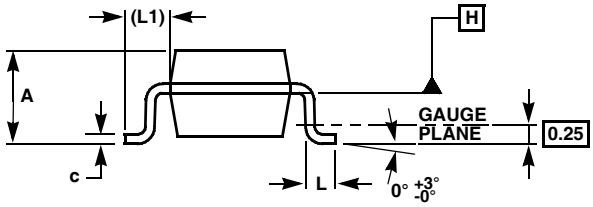
NOTES:

1. Plastic or metal protrusions of 0.006" maximum per side are not included.
2. Plastic interlead protrusions of 0.010" maximum per side are not included.
3. Dimensions "D" and "E1" are measured at Datum Plane "H".
4. Dimensioning and tolerancing per ASME Y14.5M-1994

SOT-23 Package Family







MDP0038

SOT-23 PACKAGE FAMILY

SYMBOL	SOT23-5	SOT23-6	TOLERANCE
A	1.45	1.45	MAX
A1	0.10	0.10	±0.05
A2	1.14	1.14	±0.15
b	0.40	0.40	±0.05
c	0.14	0.14	±0.06
D	2.90	2.90	Basic
E	2.80	2.80	Basic
E1	1.60	1.60	Basic
e	0.95	0.95	Basic
e1	1.90	1.90	Basic
L	0.45	0.45	±0.10
L1	0.60	0.60	Reference
N	5	6	Reference

Rev. E 3/00

NOTES:

1. Plastic or metal protrusions of 0.25mm maximum per side are not included.
2. Plastic interlead protrusions of 0.25mm maximum per side are not included.
3. This dimension is measured at Datum Plane “H”.
4. Dimensioning and tolerancing per ASME Y14.5M-1994.
5. Index area - Pin #1 I.D. will be located within the indicated zone (SOT23-6 only).
6. SOT23-5 version has no center lead (shown as a dashed line).