# M51957A,B/M51958A,B

## Voltage Detecting, System Resetting IC Series

REJ03D0778-0200
Rev.2.00
Aug 20, 2007

## Description

M51957A,B/M51958A,B are semiconductor integrated circuits for resetting of all types of logic circuits such as CPUs, and has the feature of setting the detection voltage by adding external resistance.

They include a built-in delay circuit to provide the desired retardation time simply by adding an external capacitor.

They fined extensive applications, including battery checking circuit, level detecting circuit and waveform shaping circuit.

## Features

- Few external parts
- Large delay time with a capacitor of small capacitance (td ≈ 100 ms, at 0.33 μF) (M51957, M51958)
- Low threshold operating voltage (Supply voltage to keep low-state at low supply voltage): 0.6 V (Typ) at $R_L$ = 22 kΩ
- Wide supply voltage range: 2 V to 17 V
- Wide application range

## Application

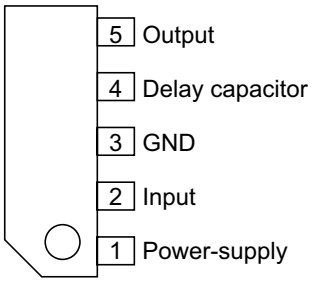
- Reset circuit of Pch, Nch, CMOS, microcomputer, CPU and MCU, Reset of logic circuit, Battery check circuit, switching circuit back-up voltage, level detecting circuit, waveform shaping circuit, delay waveform generating circuit, DC/DC converter, over voltage protection circuit

## Recommended Operating Condition

- Supply voltage range: 2 V to 17 V

## Pin Arrangement

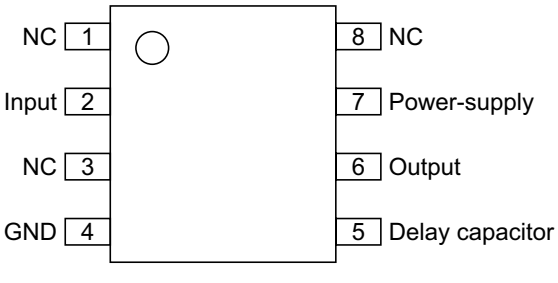
M51957AL/BL
M51958AL/BL




(Top view)

Outline: 5P5T

M51957AFP/BFP
M51958AFP/BFP

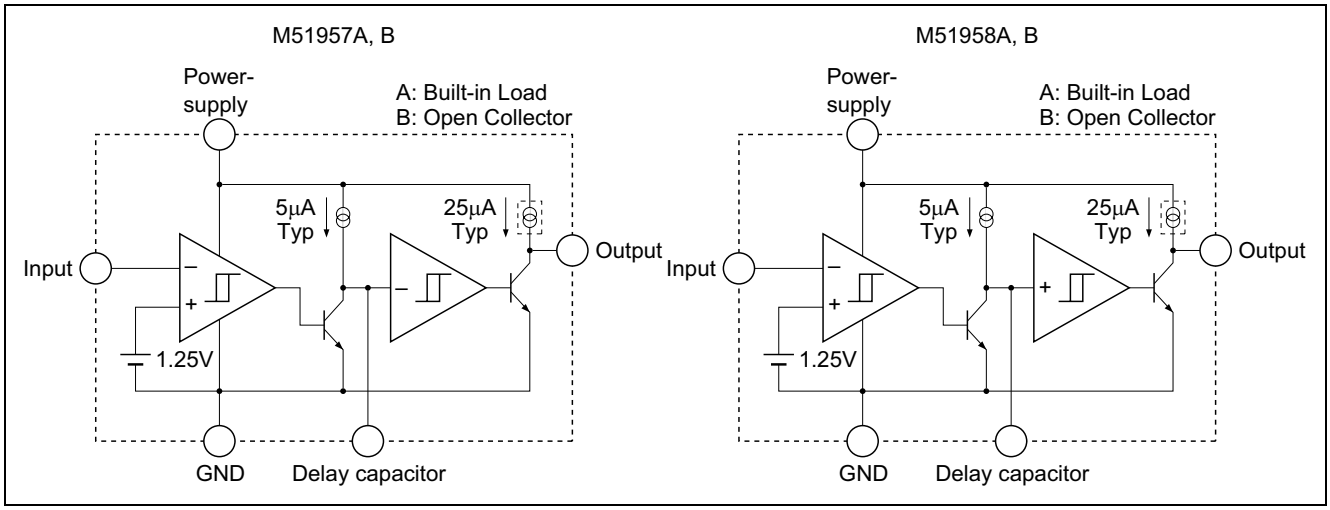



(Top view)

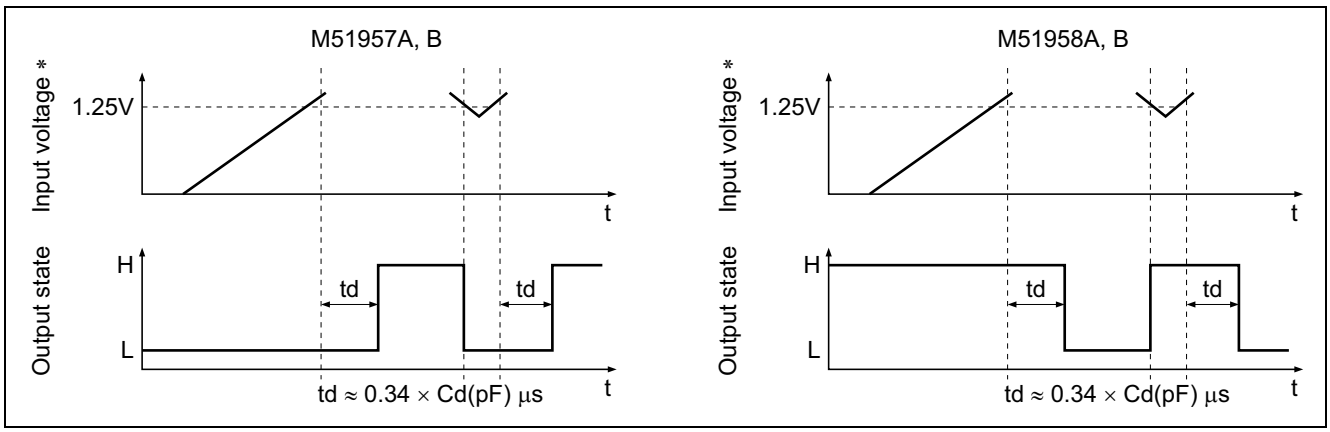
NC: No Connection

Outline: PRSP0008DE-C (recommend)
PRSP0008DA-A (8P2S-A) (not recommend for new design)

## Block Diagram




## Operating Waveform



## Absolute Maximum Ratings

(Ta = 25°C, unless otherwise noted)

| Item | Symbol | Ratings | Unit | Conditions | |
|---|---|---|---|---|---|
| Supply voltage | $V_{CC}$ | 18 | V | | |
| Output sink current | Isink | 6 | mA | | |
| Output voltage | $V_O$ | $V_{CC}$ | V | Type A (output with constant current load) | |
| | | 18 | | Type B (open collector output) | |
| Power dissipation | Pd | 450 | mW | 5-pin SIP | |
| | | 400 | | 8-pin SOP (PRSP0008DE-C): recommend | |
| | | 300 | | 8-pin SOP (PRSP0008DA-A): not recommend | |
| Thermal derating | Kθ | 4.5 | mW/°C | Refer to the thermal derating curve. | 5-pin SIP |
| | | 4.4 | | | 8-pin SOP (PRSP0008DE-C) : recommend |
| | | 3 | | | 8-pin SOP (PRSP0008DA-A) : not recommend |
| Operating temperature | Topr | –30 to +85 | °C | | |
| Storage temperature | Tstg | –40 to +125 | °C | | |
| Input voltage range | $V_{IN}$ | –0.3 to $V_{CC}$ | V | $V_{CC} \leq 7$ V | |
| | | –0.3 to +7 | | $V_{CC} > 7$ V | |

## Electrical Characteristics

(Ta = 25°C, unless otherwise noted)

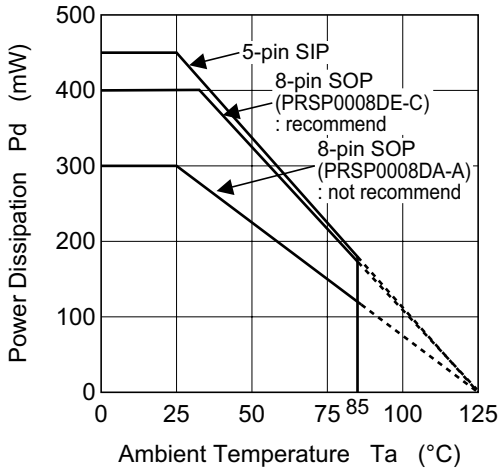
- "L" reset type M51957A, M51957B
- "H" reset type M51958A, M51958B

| Item | Symbol | Min | Typ | Max | Unit | Test Conditions | |
|---|---|---|---|---|---|---|---|
| Detecting voltage | $V_S$ | 1.20 | 1.25 | 1.30 | V | | |
| Hysteresis voltage | $\Delta V_S$ | 9 | 15 | 23 | mV | $V_{CC}$ = 5V | |
| Detecting voltage temperature coefficient | $V_S/\Delta T$ | — | 0.01 | — | %/°C | | |
| Supply voltage range | $V_{CC}$ | 2 | — | 17 | V | | |
| Input current | $I_{IN}$ | — | 100 | 500 | nA | $V_{IN}$ = 1.25V | |
| Circuit current | $I_{CC}$ | — | 390 | 590 | μA | Type A, $V_{CC}$ = 5V | |
| | | — | 360 | 540 | | Type B, $V_{CC}$ = 5V | |
| Delay time | $t_{pd}$ | 1.6 | 3.4 | 7 | ms | Cd = 0.01μF * | |
| Output saturation voltage | Vsat | — | 0.2 | 0.4 | V | L reset type, $V_{CC}$ = 5V, $V_{IN}$ < 1.2V, Isink = 4mA | |
| | | — | 0.2 | 0.4 | | H reset type, $V_{CC}$ = 5V, $V_{IN}$ > 1.35V, Isink = 4mA | |
| Threshold operating voltage | $V_{OPL}$ | — | 0.67 | 0.8 | V | L reset type minimum supply voltage for IC operation | $R_L$ = 2.2kΩ, Vsat ≤ 0.4V |
| | | — | 0.55 | 0.7 | | | $R_L$ = 100kΩ, Vsat ≤ 0.4V |
| Output leakage current | $I_{OH}$ | — | — | 1 | μA | Type B | |
| Output load current | $I_{OC}$ | –40 | –25 | –17 | μA | Type A, $V_{CC}$ = 5V, $V_O$ = 1/2 × $V_{CC}$ | |
| Output high voltage | $V_{OH}$ | $V_{CC}$–0.2 | $V_{CC}$–0.06 | — | V | Type A | |

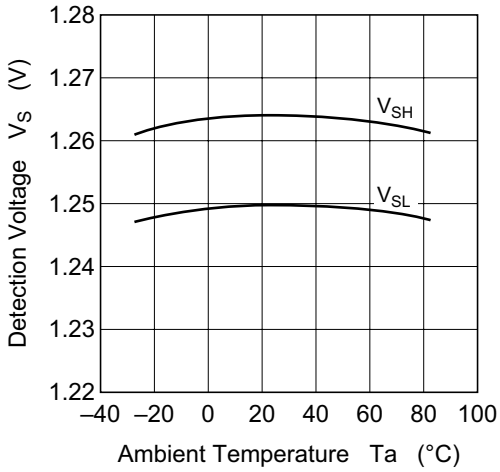
Note: Please set the desired delay time by attaching capacitor of the range between 4700 pF and 10 μF.

## Typical Characteristics

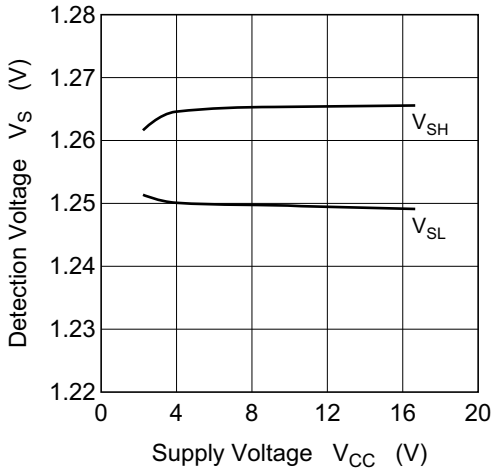
Thermal Derating
(Maximum Rating)



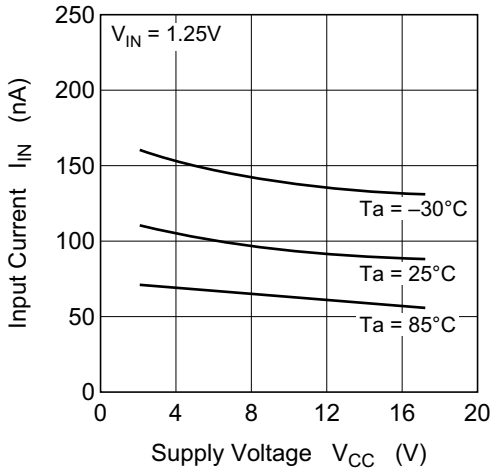

Detection Voltage vs. Ambient Temperature
(Input voltage detection series)



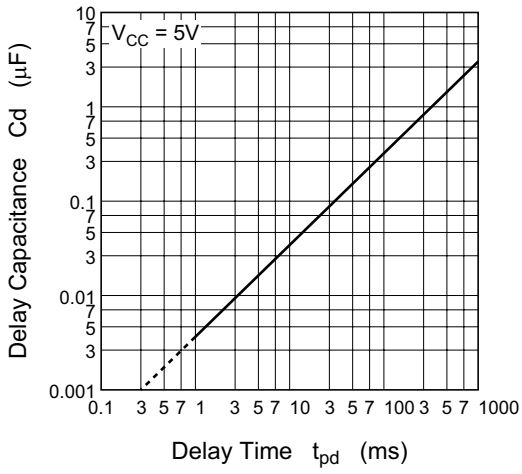

Detection Voltage vs. Supply Voltage
(Input voltage detection series)



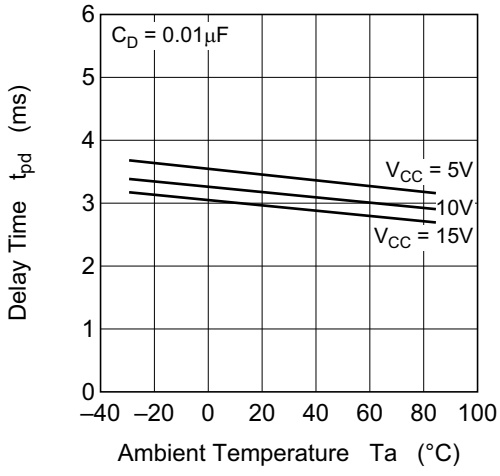

Input Current vs. Supply Voltage
(Input voltage detecting series)



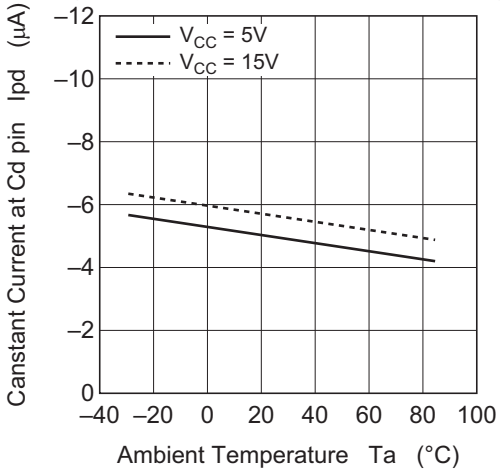

Delay Capacitance vs. Delay Time
(M5195xx, External delay capacitor type)



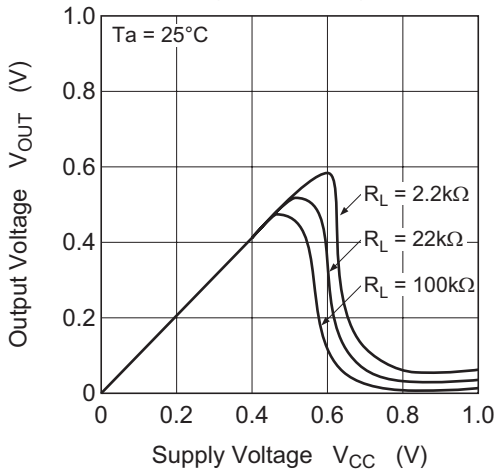

Delay Time vs. Ambient Temperature
(M5195xx, External delay capacitor type)



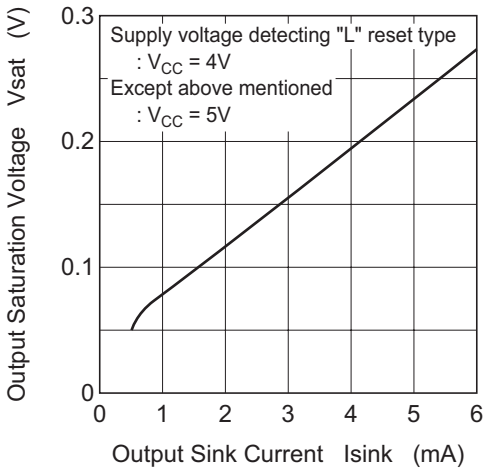
Canstant Current at Cd pin vs. Ambient Temperature
(M5195xx, External delay capacitor type)



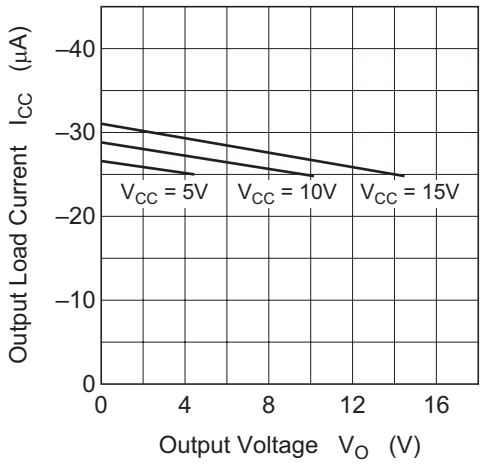

Threshold Operating Voltage
([L] reset type)



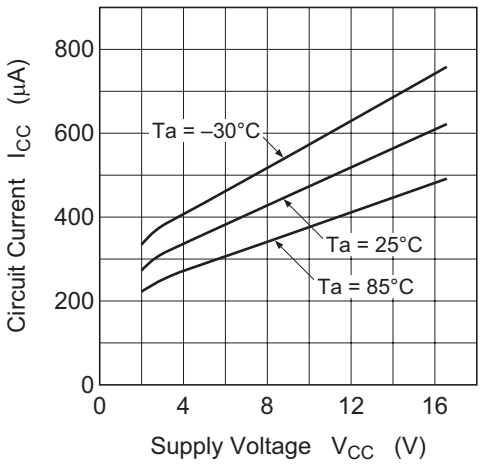

Output Saturation Voltage vs. Output Sink Current




Output Load Current vs. Output Voltage
(M5195xA)




Circuit Current vs. Supply Voltage
(M51957B, M51958B)



## Example of Application Circuit

### Reset Circuit of M5195xx Series

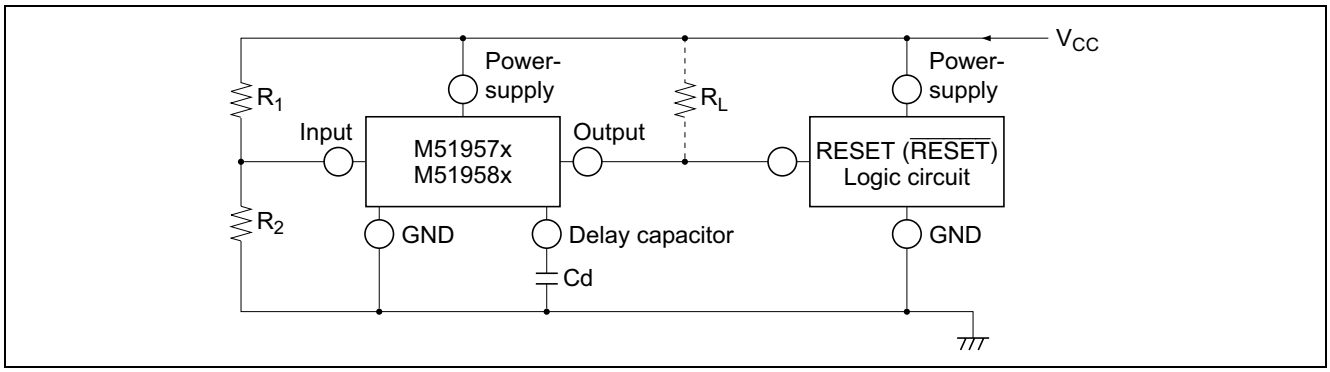



**Figure 1 Reset Circuit of M5195xx Series**

Notes: 1. When the detecting supply voltage is 4.25 V, M51951, M51952, M51953 and M51954 are used. In this case, $R_1$ and $R_2$ are not necessary.
When the voltage is anything except 4.25 V, M51955, M51956, M51957 and M51958 are used. In this case, the detecting supply voltage is $1.25 \times (R_1 + R_2)/R_2$ (V) approximately. The detecting supply voltage can be set between 2 V and 15 V.

2. When the delay time is short, M51951, M51952, M51955 and M51956 are available. These ICs have a delay capacity and the delay time is about 200 µs.
If a longer delay time is necessary, M51953, M51954, M51957 and M51958 are used. In this case, the delay time is about $0.34 \times$ Cd (pF) µs.
3. If the M5195xx and the logic circuit share a common power source, type A (built-in load type) can be used whether a pull-up resistor is included in the logic circuit or not.
4. The logic circuit preferably should not have a pull-down resistor, but if one is present, add load resistor $R_L$ to overcome the pull-down resistor.
5. When the reset terminal in the logic circuit is of the low reset type, M51951, M51953, M51955 and M51957 are used and when the terminal is of the high reset type, M51952, M51954, M51956 and M51958 are used.
6. When a negative supply voltage is used, the supply voltage side of M5195xx and the GND side are connected to negative supply voltage respectively.

### Case of Using Reset Signal except Supply Voltage in the M5195xx Series

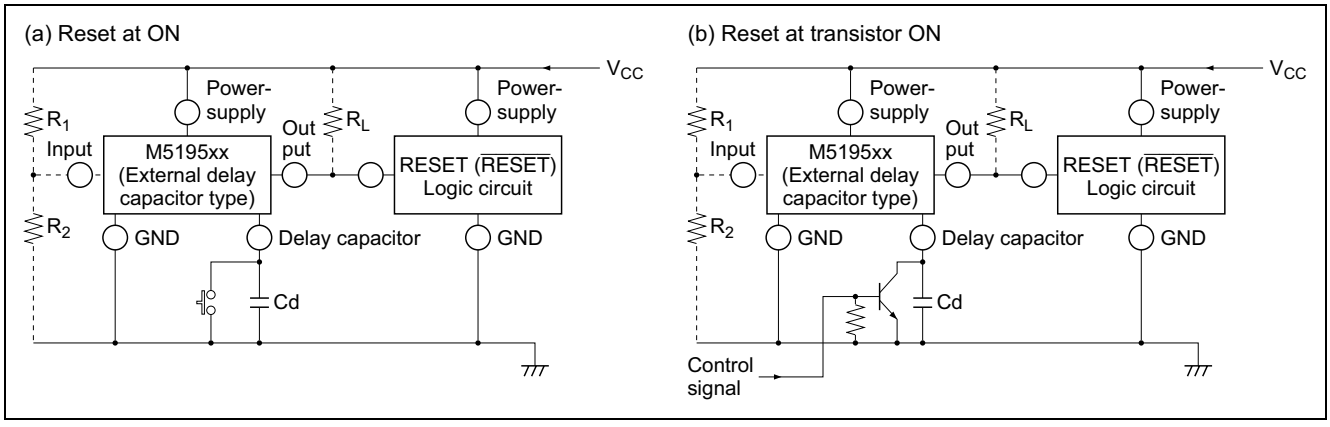



**Figure 2 Case of Using Reset Signal except Supply Voltage in the M5195xx Series**

### Delay Waveform Generating Circuit

When M51957 and M51958 are used, a waveform with a large delay time can generate only by adding a small capacitor.

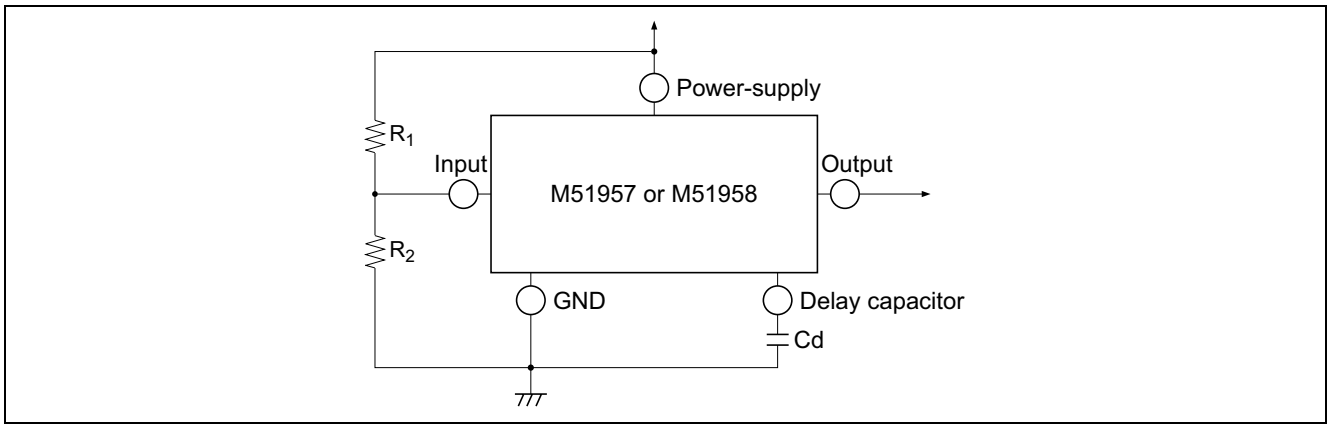



**Figure 3 Delay Waveform Generating Circuit**

### Operating Waveform

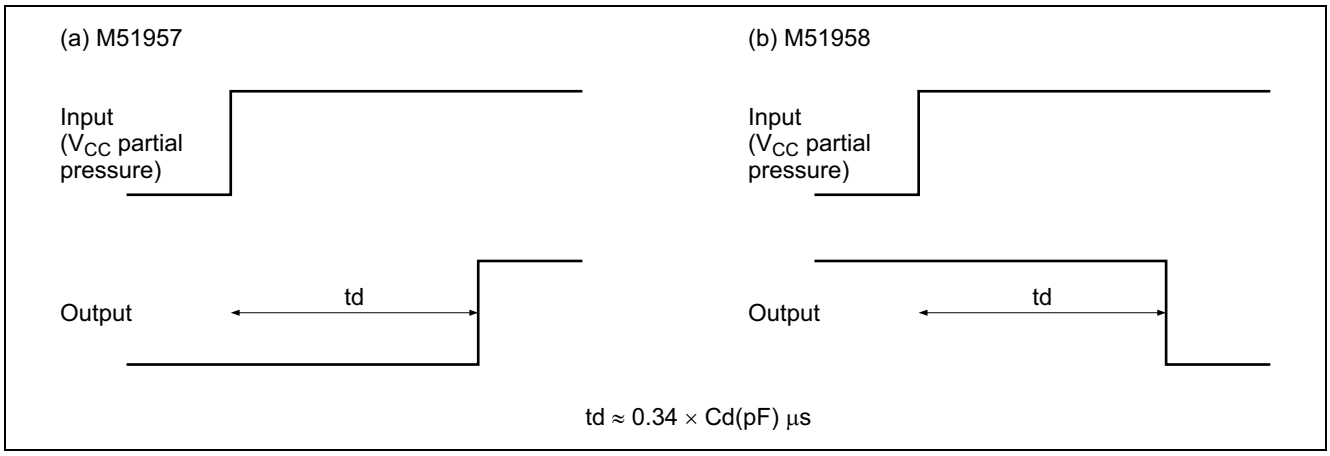



**Figure 4 Operating Waveform**

## Notice for use

### About the Power Supply Line

1. About bypass capacitor
   Because the ripple and the spike of the high frequency noise and the low frequency are superimposed to the power supply line, it is necessary to remove these.
   Therefore, please install $C_1$ and $C_2$ for the low frequency and for the high frequency between the power supply line and the GND line as shown in following figure 5.

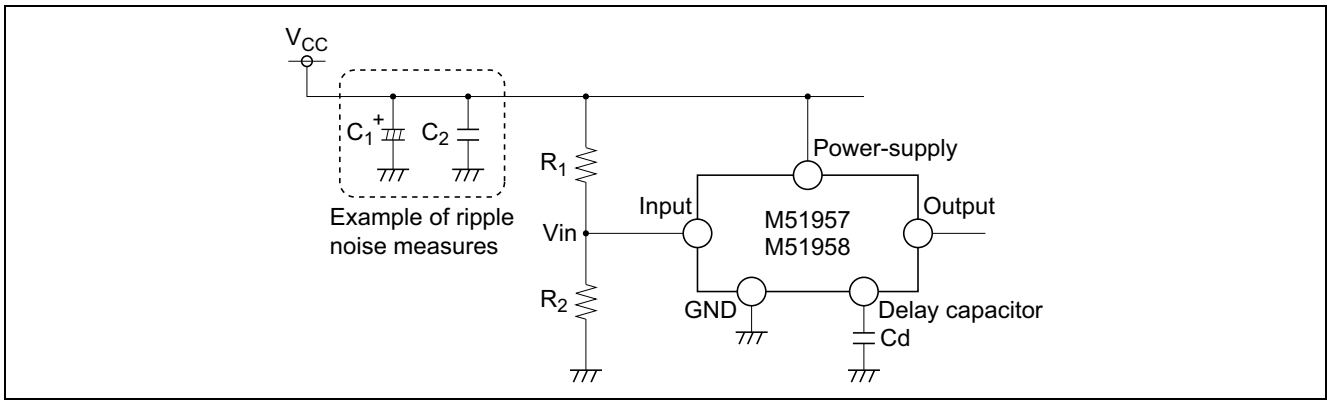



**Figure 5 Example of Ripple Noise Measures**

2. The sequence of voltage impression
   Please do not impress the voltages to the input terminals earlier than the power supply terminal. Moreover, please do not open the power supply terminal with the voltage impressed to the input terminal.
   (The setting of the bias of an internal circuit collapses, and a parasitic element might operate.)

### About the Input Terminal

1. Setting range of input voltage
   The following voltage is recommended to be input to the input terminal (pin 2).

   about 0.8 (V) < Vin < $V_{CC}$ – 0.3 (V) .... at $V_{CC} \leq 7$ V

   about 0.8 (V) < Vin < 6.7 (V) ..... at $V_{CC} > 7$ V

2. About using input terminal
   Please do an enough verification to the transition characteristic etc. of the power supply when using independent power supply to input terminal (pin 2).

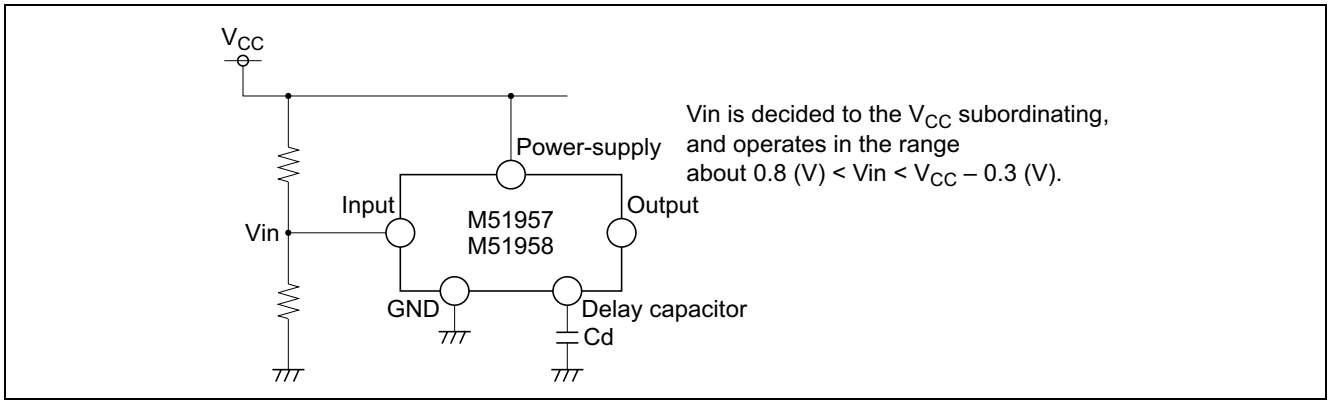
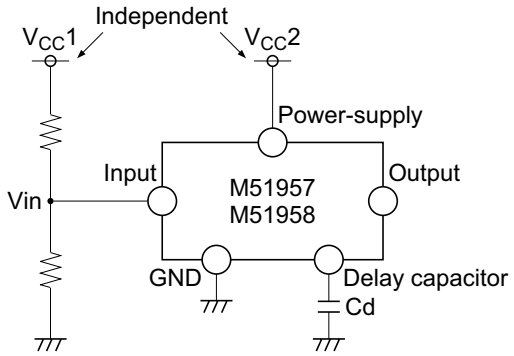
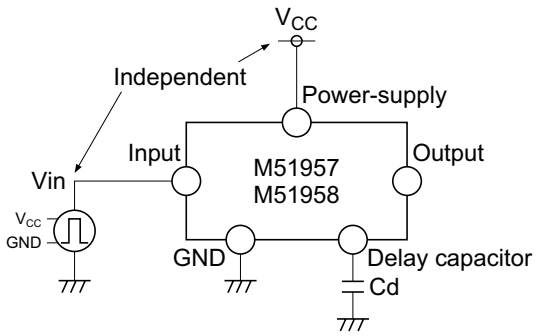



**Figure 6 Recommended Example**




Example 1. Independent power supply system
Please do enough verifying about transition characteristic of $V_{CC}1$ and $V_{CC}2$.




Example 2. Logic pulse input (not recommended)

**Figure 7**

3. Calculation of detecting voltage
   Detecting voltage Vs can be calculated by the following expression.
   However, the error margin is caused in the detecting voltage because input current Iin (standard 100 nA) exists if it sets too big resistance.
   Please set the constant to disregard this error margin.

$$V_S = 1.25 \times \left( \frac{R_1 + R_2}{R_2} \right) + \underline{\text{Iin} \times R_1}$$
$$\text{error margin}$$

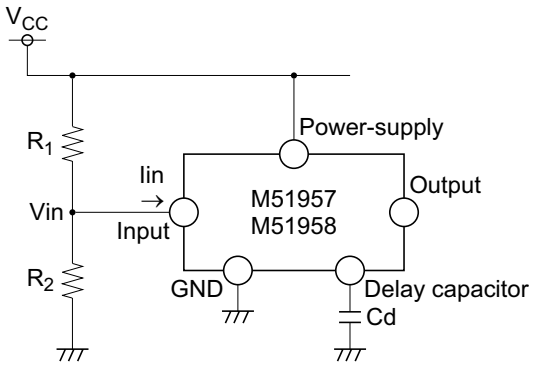



**Figure 8 Influence of Input Current**

4. About the voltage input outside ratings
   Please do not input the voltage outside ratings to the input terminal.
   An internal protection diode becomes order bias, and a large current flows.

### Setting of Delay Capacity

Please use capacitor Cd for the delay within the range of 10 μF or less.

When a value that is bigger than this is set, the problem such as following (1), (2), and (3) becomes remarkable.

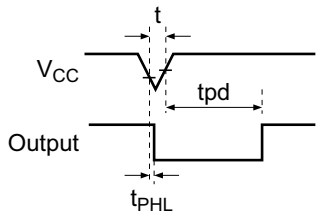



**Figure 9 Time Chart at Momentary Voltage-Decrease**

(1) The difference at delay time becomes remarkable.
A long delay setting of tens of seconds is fundamentally possible. However, when set delay time is lengthened, the range of the difference relatively grows, too. When a set value is assumed to be 'tpd', the difference occurs in the range from 0.47 × tpd to 2.05 × tpd. For instance, 34 seconds can be calculated at 100 μF. However, it is likely to vary within the ranges of 16-70 seconds.

(2) Difficulty to react to a momentary voltage decrease.
For example, the reaction time $t_{PHL}$ is 10 μs when delay capacitor Cd = 0.1 μF.
The momentary voltage-decrease that is longer than such $t_{PHL}$ are occurs, the detection becomes possible. When the delay capacitance is enlarged, $t_{PHL}$ also becomes long. For instance, it becomes about 100 to 200 μs in case of circuit constant C1 = 100 μF.
(Characteristic graph 1 is used and extrapolation in case of Cd = 100 μF.)
Therefore, it doesn't react to momentary voltage-decrease that is shorter than this.

(3) Original delay time is not obtained.
When the momentary voltage-decrease time 't' is equivalent to $t_{PHL}$, the discharge becomes insufficient and the charge starts at that state. This phenomenon occurs at large capacitance. And, original delay time tpd is not obtained.
Please refer to characteristic graph 2. (Delay time versus input pulse width)

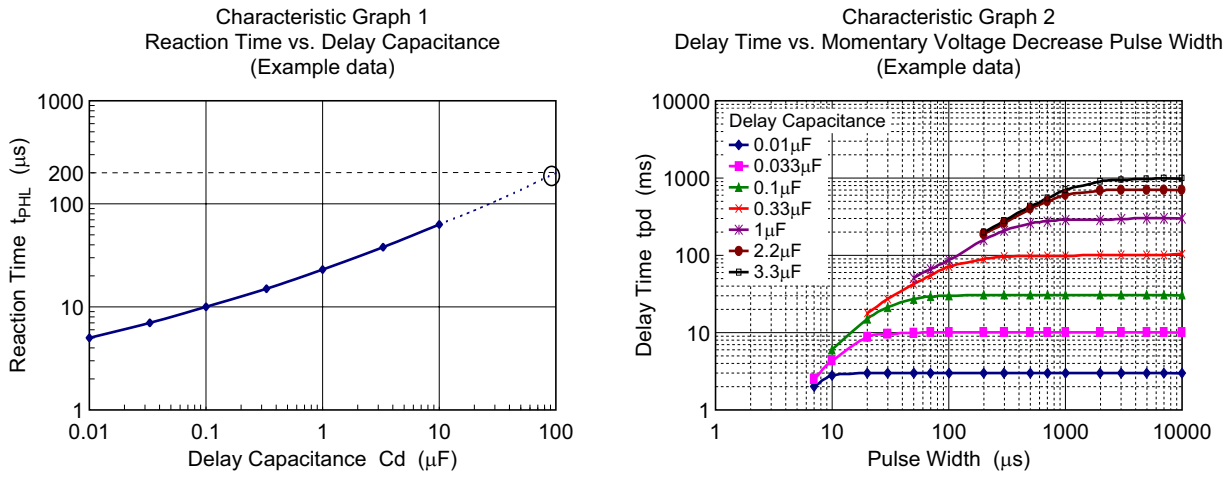



**Figure 10 Characteristic Graph**

### Setting of Output Load Resistance (M51957B/M51958B)

High level output voltage can be set without depending on the power-supply voltage because the output terminal is an open collector type. However, please guard the following notes.

1. Please set it in value (2 V to 17 V) within the range of the power-supply voltage recommendation. Moreover, please never impress the voltage of maximum ratings 18 V or more even momentarily either.
2. Please set output load resistance (pull-up resistance) $R_L$ so that the output current (output inflow current $I_L$) at L level may become 4 mA or less. Moreover, please never exceed absolute maximum rating (6 mA).

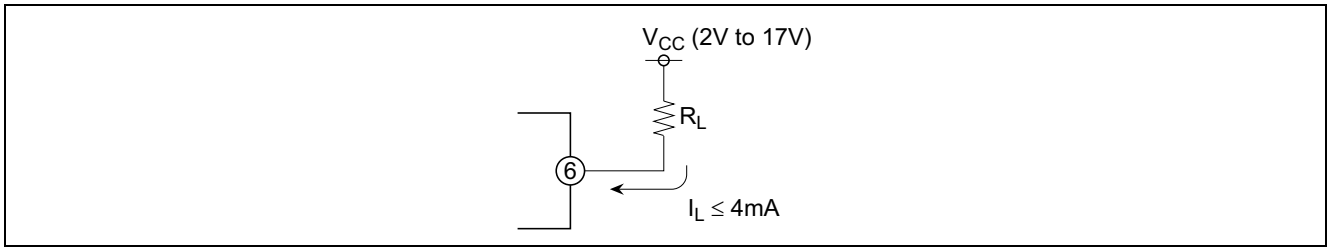



**Figure 11 Output Load Resistance $R_L$**

### Others

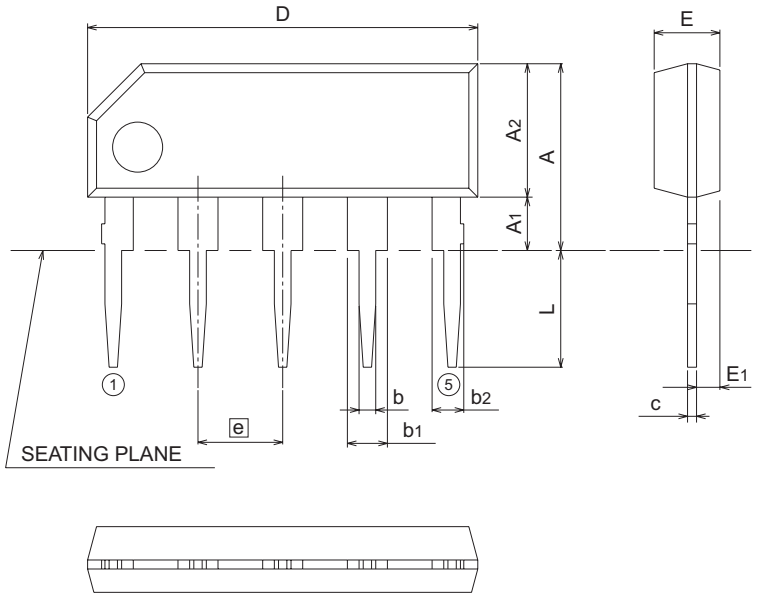
1. Notes when IC is handled are published in our reliability handbook, and please refer it. The reliability handbook can be downloaded from our homepage (following URL). http://www.renesas.com/fmwk.jsp?cnt=reliability_root.jsp&fp=/products/common_info/reliability
2. Additionally, please inquire of our company when there is an uncertain point on use.

## Package Dimensions

### 5P5T

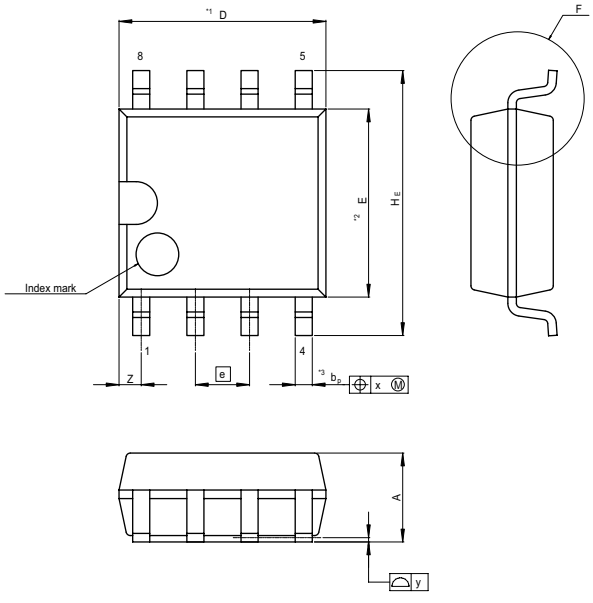
**Plastic 5pin 240mil SIP**

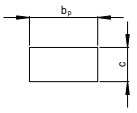
| EIAJ Package Code | JEDEC Code | Weight(g) | Lead Material |
|---|---|---|---|
| SIP5-P-240-2.54 | – | 0.22 | Cu Alloy |



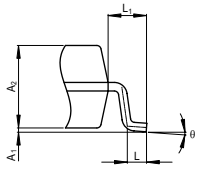

| Symbol | Dimension in Millimeters | | |
|---|---|---|---|
| | Min | Nom | Max |
| A | – | – | 6.1 |
| $A_1$ | 1.4 | – | – |
| $A_2$ | – | 4.0 | – |
| b | 0.4 | 0.5 | 0.6 |
| $b_1$ | 1.1 | 1.2 | 1.5 |
| $b_2$ | 0.75 | 0.85 | 1.15 |
| c | 0.22 | 0.27 | 0.34 |
| D | 11.5 | 11.7 | 11.9 |
| E | 1.77 | 1.97 | 2.17 |
| $E_1$ | 0.6 | 0.7 | 0.8 |
| e | – | 2.54 | – |
| L | 3.0 | – | – |

| JEITA Package Code | RENESAS Code | Previous Code | MASS[Typ.] |
|---|---|---|---|
| P-SOP8-4.4x4.85-1.27 | PRSP0008DE-C | — | 0.1g |




Terminal cross section
( Ni/Pd/Au plating )

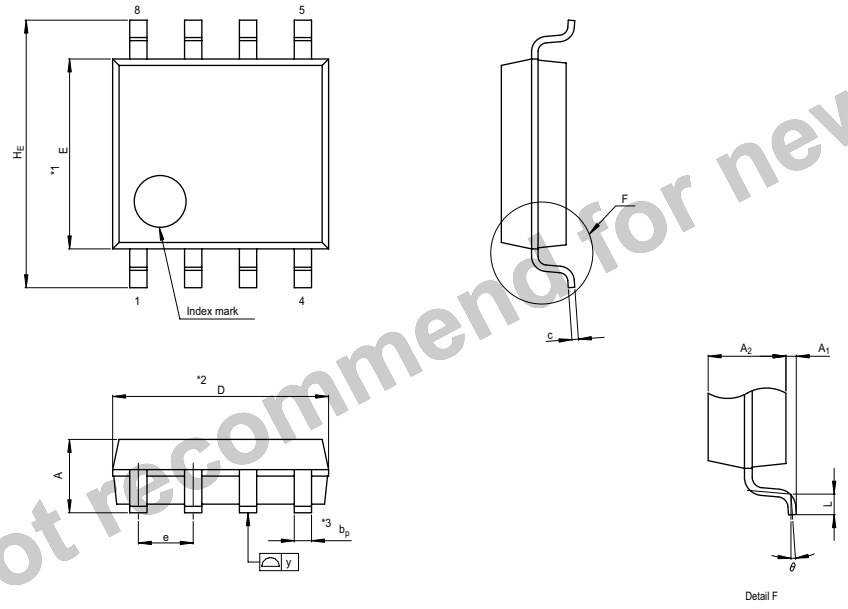



Detail F

NOTE)
1. DIMENSIONS"*1 (Nom)"AND"*2"
DO NOT INCLUDE MOLD FLASH.
2. DIMENSION"*3"DOES NOT
INCLUDE TRIM OFFSET.

| Reference Symbol | Dimension in Millimeters | | |
|---|---|---|---|
| | Min | Nom | Max |
| D | 4.65 | 4.85 | 5.05 |
| E | 4.2 | 4.4 | 4.6 |
| $A_2$ | — | 1.85 | — |
| $A_1$ | 0.00 | 0.1 | 0.20 |
| A | — | — | 2.03 |
| $b_p$ | 0.34 | 0.4 | 0.46 |
| $b_1$ | — | — | — |
| c | 0.15 | 0.20 | 0.25 |
| $c_1$ | — | — | — |
| θ | 0° | — | 8° |
| $H_E$ | 5.7 | 6.2 | 6.5 |
| e | 1.12 | 1.27 | 1.42 |
| x | — | — | 0.12 |
| y | — | — | 0.10 |
| Z | — | — | 0.75 |
| L | 0.25 | 0.45 | 0.65 |
| $L_1$ | — | 0.90 | — |

| JEITA Package Code | RENESAS Code | Previous Code | MASS[Typ.] |
|---|---|---|---|
| P-SOP8-4.4x5-1.27 | PRSP0008DA-A | 8P2S-A | 0.07g |




not recommended for new design

NOTE)
1. DIMENSIONS "*1" AND "*2" DO NOT INCLUDE MOLD FLASH.
2. DIMENSION "*3" DOES NOT INCLUDE TRIM OFFSET.

| Reference Symbol | Dimension in Millimeters | | |
|---|---|---|---|
| | Min | Nom | Max |
| D | 4.8 | 5.0 | 5.2 |
| E | 4.2 | 4.4 | 4.6 |
| $A_2$ | — | 1.5 | — |
| $A_1$ | 0.05 | — | — |
| A | — | — | 1.9 |
| $b_p$ | 0.35 | 0.4 | 0.5 |
| c | 0.13 | 0.15 | 0.2 |
| $\theta$ | 0° | — | 10° |
| $H_E$ | 5.9 | 6.2 | 6.5 |
| e | 1.12 | 1.27 | 1.42 |
| y | — | — | 0.1 |
| L | 0.2 | 0.4 | 0.6 |

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