DECT RF Transceiver

AD6411

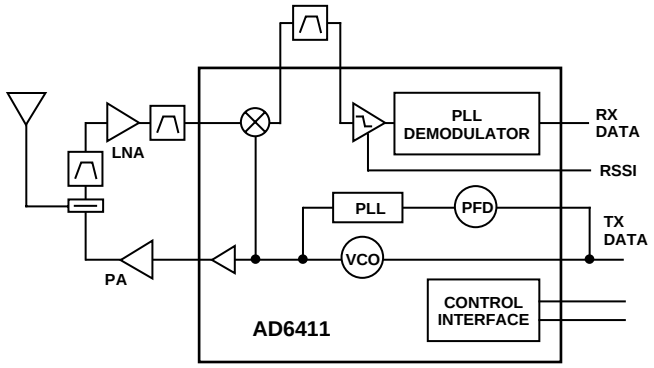
FEATURES

Fully Compliant with DECT Specifications
Single IC DECT Radio
Integrated UHF VCO (External Resonator)
Integrated Synthesizer Supporting Extended Frequency Allocation
Built-In Supply Regulation
Direct VCO Modulation for DECT Transmit Path
PLL-Based Demodulator
Use with Low Cost Plastic Packaged SAW Filters
Ultralow Power Design
Operates from +3.0 V to +5.5 V Battery
User-Selectable Power-Down Modes
Small 48-Lead LQFP Package

APPLICATIONS

DECT Cordless Telephones
DECT-Based Wireless Local Loop Systems
DECT-Based Wireless Data Systems

FUNCTIONAL BLOCK DIAGRAM



DESCRIPTION

The AD6411 provides the complete transmit and receive RF signal processing necessary to implement a digital wireless transceiver based on the Digital Enhanced Cordless Telecommunications (DECT) standard.

The AD6411's receive signal path consists of a mixer, IF amplifiers and PLL demodulator. The low noise, high intercept mixer is a development of the doubly-balanced Gilbert-Cell type. It has a nominal –16 dBm input-referred 1 dB compression point and a –8 dBm input referred third-order intercept. The limiter amplifier provides sufficient gain to drive the PLL demodulator, which provides selectable analog or sliced outputs. The RSSI output provides a voltage proportional to the receive signal strength. It measures nearly 100 dB IF signal strength range with 14 mV/dB gain scaling.

The transmit path accepts baseband data, which is filtered and applied to the VCO directly. The VCO operates at half the RF carrier frequency, and is doubled to avoid pulling due to leakage from the output.

An on-chip PLL frequency synthesizer provides channel selection. Operating modes are selected either through a serial bus or asynchronous control pins. This allows compatibility with most of the available DECT baseband controller ASICs.

The AD6411 is packaged in a 48-lead LQFP.

REV. 0

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AD6411–SPECIFICATIONS (T_A = 25°C, 3.0 V < V_{BAT} < 5.5 V unless otherwise noted)

Parameter	Conditions	Min	Typ	Max	Units
RECEIVE RF MIXER					
RF Input Frequency			1880 to 1930		MHz
Power Gain	Z_{SOURCE} = 50 Ω, Z_{LOAD} = 200 Ω	15	19	21	dB
Input 1 dB Compression Point	Z_{SOURCE} = 50 Ω, Z_{LOAD} = 200 Ω	–21	–16		dBm
Input Third-Order Intercept	Z_{SOURCE} = 50 Ω, Z_{LOAD} = 200 Ω		–8		dBm
SSB Noise Figure	Z_{SOURCE} = 50 Ω, Z_{LOAD} = 200 Ω		11		dB
Output VSWR	100 MHz–120 MHz			1.5:1	
Output Impedance			200		Ω
Input Impedance			50		Ω
RX IF AMPLIFIERS					
Differential Input Impedance			200		Ω
Input VSWR	Input Power < –11 dBm			1.5:1	
IF Noise Figure	Z_{SOURCE} = 200 Ω Differential		6		dB
RSSI					
RSSI Upper Limit	Z_{SOURCE} = 200 Ω Differential	–5	+3		dBm
RSSI Lower Limit	Z_{SOURCE} = 200 Ω Differential		–95		dBm
RSSI High Level Voltage	Input Power = 0 dBm (at IF Input)		1.7		V
RSSI Low Level Voltage	Input Power = –90 dBm (at IF Input)		0.3		V
RSSI Slope	–90 dBm < Input Power < 0 dBm (at IF Input)		14		mV/dB
RSSI Output Impedance	V_{RSSI} = 0.3 V		700		Ω
RSSI Output Response Time	Settling to 95% Value for a 40 dB Input Step, 20 pF External Load			2	µs
PLL DEMODULATOR					
PLL Demodulator Phase Detector Gain	@ 90 Degree Relative Phase	80	115	150	µA/rad
Leakage Current at COFF	Charge Pump Disabled		100		pA
Recommended External VCO Gain			1.152		MHz/V
Demodulator Gain	VCO Gain Set to 1.152 MHz/V		1.736		V/MHz
Demodulator Linearity	THD for FM Tone @ 576 kHz, Peak Deviation 288 kHz		–30		dBc
VOLTAGE REFERENCE					
Output Voltage		1.3	1.37	1.44	V
Output Current				100	µA
TRANSMIT SECTION					
Output Power	Z_L = 50 Ω	–3	+1	+4	dBm
Harmonically Related Spurii	At 0.5 × DECT_Tx: (940 MHz–950 MHz)		–10		dBc
	At 1.5 × DECT_Tx: (2820 MHz–2850 MHz)		–20		dBc
Other Spurii	100 MHz–3000 MHz, Outside DECT Band 1 MHz Measurement Bandwidth		–73		dBc
Output Phase Noise	With UHF Resonator Qu > 30				
1.2 MHz			–120		dBc/Hz
3.0 MHz			–130		dBc/Hz
>4.7 MHz			–135		dBc/Hz
VCO Operating Frequency Range	With Suitable External Resonator	700		1200	MHz
Oscillator Push	Using On-Chip Regulator, 250 mV V_{BAT} Step Change with 5 µs Rise/Fall Time		6		kHz
Oscillator Pull	ΔVSWR = 2:1 Any Phase		55		kHz
SYNTHESIZER					
Reference Input Impedance			>5		kΩ
Reference Input Level		100		1000	mV p-p
Reference Input Frequency		10		20	MHz
VCO Signal Input Range		700		1200	MHz
Charge Pump Current – "Up"	Voltage On Loop Filter (Pin 38) = 1.4 V	–1.30	1.0	–0.77	mA
Charge Pump Current – "Down"	Voltage On Loop Filter (Pin 38) = 1.4 V	0.66	1.0	1.15	mA
Charge Pump Leakage	Output Disabled		<±1		nA
BSW Output "High" Voltage	at I_{LOAD} < = 2 mA	2.5			V

Parameter	Conditions	Min	Typ	Max	Units
VOLTAGE REGULATORS (VS1, VS2)					
Regulated Voltage Output	I_{LOAD} = 60 mA max	2.675	2.725	2.825	V
Dropout Voltage	I_{LOAD} = 60 mA; BCW68F or Equivalent Pass Transistor		150		mV
Load Regulation	VS1: 10 mA < I_{LOAD} < 60 mA				
	VS2: 1 mA < I_{LOAD} < 15 mA			20	mV
Line Transient Response	I_{LOAD} = 10 mA , ΔV_{BAT} = 250 mV, Rise/Fall Time = 2 µs			1.5	mV
Line Rejection	I_{LOAD} = 60 mA, ΔV_{BAT} = 250 mV, Static Change		0.5		mV
Power Supply Rejection	DC-1 MHz		35		dB
POWER CONSUMPTION					
Supply Voltage	V_{BAT}	3.0		5.5	V
All Off Mode			<1		µA
Standby Mode		100	200	400	µA
Prior to TX Slot			52	60	mA
Active TX Slot			52	60	mA
Prior to RX Slot		15	20	25	mA
Active RX Slot	(Synthesizer Dividers On, Charge Pump Off)	45	57	75	mA
OPERATING TEMPERATURE RANGE		–25		+85	°C

ABSOLUTE MAXIMUM RATINGS[1]

Supply Voltage . . . . . +5.5 V
Internal Power Dissipation[2] . . . . . 600 mW
Operating Temperature Range . . . . . –25°C to +85°C
Storage Temperature Range . . . . . –65°C to +150°C
Lead Temperature, Soldering 60 sec . . . . . +300°C

NOTES

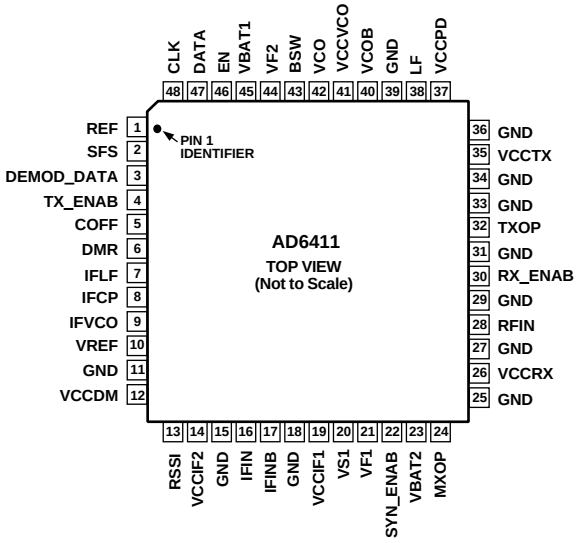
[1]Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only; functional operation of the device at these or any other conditions above those indicated in the operational section of this specification is not implied. Exposure to absolute maximum rating conditions for extended rating conditions for extended periods may affect device reliability.

[2]Thermal Characteristics: 48-lead LQFP package: θ_{JA} = +126°C/W.

ORDERING GUIDE

Model	Temperature Range	Package Description	Package Option
AD6411AST	–25°C to +85°C	48-Lead Plastic LQFP	ST-48

PIN CONFIGURATION
48-Lead LQFP (ST-48)



CAUTION

ESD (electrostatic discharge) sensitive device. Electrostatic charges as high as 4000 V readily accumulate on the human body and test equipment and can discharge without detection. Although the AD6411 features proprietary ESD protection circuitry, permanent damage may occur on devices subjected to high energy electrostatic discharges. Therefore, proper ESD precautions are recommended to avoid performance degradation or loss of functionality.



PIN FUNCTION DESCRIPTIONS

Pin No.	Label	Description	Type	Comments
1	REF	DECT Reference Clock Input	Input	
2	SFS	S-Field Sample	Input	HIGH = Sample; LOW = Hold
3	DEMOD_DATA	Demodulator Output OR Sliced Demodulator Output	Output	Mode Controlled by DSD Bit in Control Register
4	TX_ENAB	Transmit Section Power Control Input	Input	Active-High or Active-Low Set by TSB Bit in Setup Word
5	COFF	Demodulator Offset Capacitor	Output	Connect to External Capacitor
6	DMR	Input for IF PLL Loop Filter Voltage after Data Filter	Input	
7	IFLF	Drive for IF PLL Active Loop Filter	Output	
8	IFCP	Virtual Ground for IF PLL Active Loop Filter	Input	
9	IFVCO	External Resonator for Demodulator VCO	Input	
10	VREF	Voltage Reference Output	Output	1.3 V; Can Be Used for A/D Converter Reference in Soft-Decision Applications
11, 15, 18, 25, 27, 29, 31, 33, 34, 36, 39	GND	Ground	Power	
12	VCCDM	PLL Demodulator Supply	Power	Normally Connected to VS1
13	RSSI	Receive Signal Strength Indicator Output	Output	
14	VCCIF2	IF Supply 2	Power	Normally Connected to VS1
16	IFINB	IF Input	Input	Balanced Input from IF SAW Filter
17	IFIN	IF Input	Input	Balanced Input from IF SAW Filter
19	VCCIF1	IF Supply 1	Power	Normally Connected to VS1
20	VS1	Regulator Sense	Input	Connect to Collector of VS1 Pass Device
21	VF1	Regulator Force	Output	Connect to Base of VS1 Pass Device
22	SYN_ENAB	Synthesizer Section Power Control Input	Input	Active-High or Active-Low Set by SSB Bit in Setup Word
23	VBAT2	Connect to Battery	Power	
24	MXOP	Receive Mixer Output	Output	
26	VCCRX	Receive RF Supply	Power	Normally Connected to VS1
28	RFIN	Receive Mixer Input	Input	
30	RX_ENAB	Receive Section Power Control Input	Input	Active-High or Active-Low Set by RSB Bit in Setup Word
32	TXOP	Transmit Output	Output	Open Collector Output
35	VCCTX	Transmit Supply	Power	Normally Connected to VS1
37	VCCPD	Phase Detector and Charge Pump Supply	Power	Normally Connected to VS1
38	LF	Loop Filter (from Charge Pump Output)	Output	
40	VCOB	UHF Oscillator	Input	VCO Tank Circuit
41	VCCVCO	Supply for Second Regulator Sense	Power	Connect to Collector of VS2 Pass Device
42	VCO	UHF Oscillator	Input	VCO Tank Circuit
43	BSW	Resonator Band Switch Output	Output	Controls Tank Circuit Band Segment
44	VF2	Regulator Force	Output	Connect to Base of VS2 Pass Device
45	VBAT1	Connect to Battery	Power	
46	EN	3-Wire Bus Enable	Input	
47	DATA	3-Wire Bus Data	Input	
48	CLK	3-Wire Bus Clock	Input	

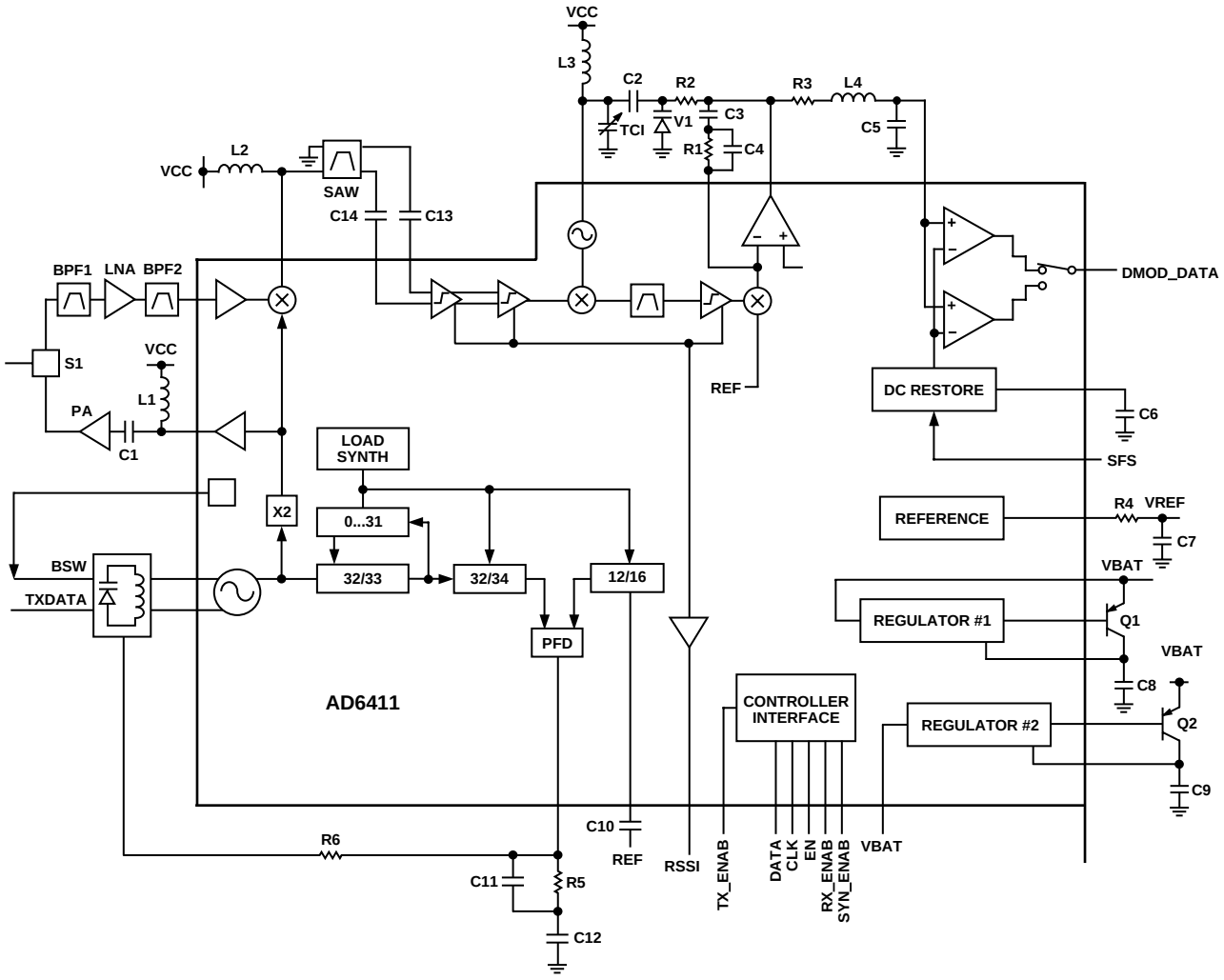


Figure 1. Functional Block Diagram

PRODUCT OVERVIEW

The AD6411 provides most of the active circuitry required to realize a complete low power DECT transceiver.

Figure 1 shows the main sections of the AD6411. It consists, in the receive path, of a UHF mixer and two-stage IF strip with integrated demodulator and data slicer. The transmit path consists of a VCO, frequency doubler and buffer amplifier.

Channel selection is performed by an on-chip PLL synthesizer. All AD6411 operating modes can be controlled by parallel control inputs or the serial interface.

Receive Mixer

The UHF mixer is an improved Gilbert-cell design. The dynamic range at the input of the mixer is determined, at the upper end, by the maximum input signal level of –16 dBm in 50 Ω at RFIN up to which the mixer remains linear and a valid RSSI signal is provided and, at the lower end, by the noise level.

The local oscillator input of the receive mixer is internally provided by the LO, which is obtained by doubling the on-chip VCO frequency.

The output of the mixer is single-ended. The nominal conversion gain is specified for operation into a 110.592 MHz or 112.32 MHz SAW IF DECT bandpass filter. The power gain of 17 dB is measured between the mixer input and the input of this filter.

IF Circuits and Demodulator

Demodulation is achieved via a PLL. This is shown in detail in Figure 2. An external manufacturing trim is required to achieve the required level of frequency accuracy. The approach is to adjust the capacitor TC1 (with the presence of an unmodulated carrier) such that the dc level at Pin 3 (DEMOD_DATA) is equal to the voltage on the external reference pin VREF.

Two demodulation modes are supported. In one mode any frequency offset due to reference drift or frequency offsets on the incoming carrier are propagated to the output (referred to as "Normal" demodulation). The other method is to use a feature of the DECT system that enables a secondary compensation circuit to track out frequency offsets ("S-field sampling," which is enabled by the pin SFS—active high together with the configuration bit SFM set over the serial interface).

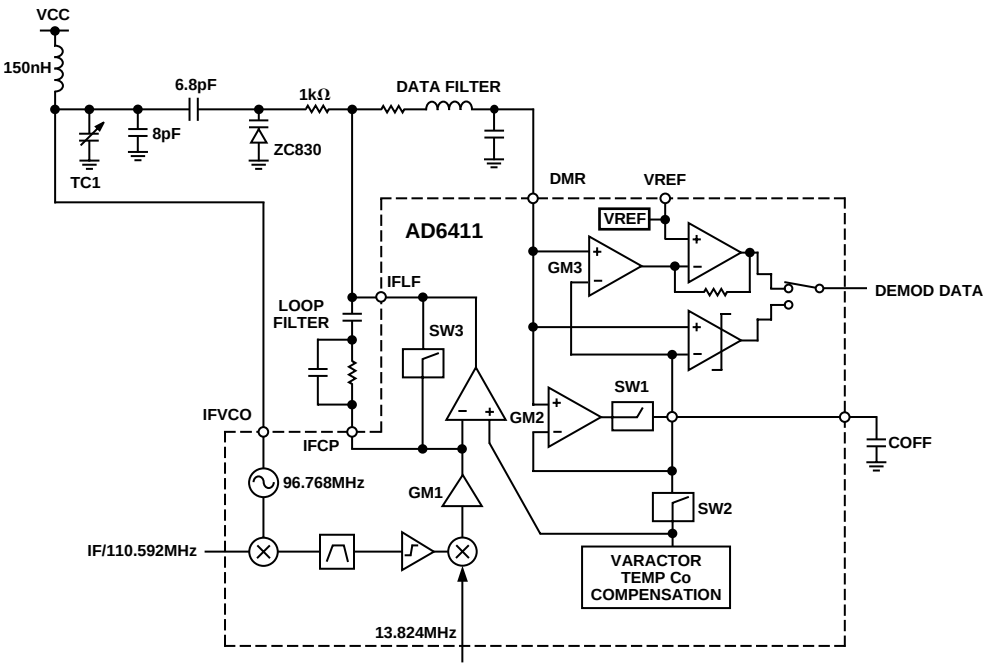


Figure 2. PLL Demodulator Block Diagram

The block diagram shows the principle of operation of these two modes together with the internal switch settings as shown in Figure 2.

Table I. Supported Demodulation Modes

Mode	SW1	SW2	SW3	Comment
Prior to RX SFS = Don't Care SFM = 0	Open	Closed	Closed	Precharge Loop Filter and C Offset Capacitor
Normal Demod – Active RX SFS = Don't Care SFM = 0	Open	Closed	Open	Use Temperature Compensated Reference Voltage
S-Field Sample SFS = 1 SFM = 1	Closed	Open	Open	
S-Field Hold SFS = 0 SFM = 1	Open	Open	Open	

An important consideration in normal demodulation mode is any drift after the initial setup of the VCO. One mechanism is the Capacitance vs. Temperature coefficient of the external varactor. This has a known characteristic which is compensated by an internal reference voltage generation circuit.

UHF VCO

A single UHF VCO oscillator is provided operating at one-half the required frequency. Therefore, in transmit mode the oscillator operates from (approximately) 940 MHz to 950 MHz, and in receive mode the oscillator operates from (approximately) 884 MHz–895 MHz. This requires a switched resonator design, and band switch control is provided by the AD6411.

A balanced oscillator configuration is used which has the advantages of rejection of common-mode interference and noise, and less coupling to and from other parts of the IC and radio.

Transmit Functions

The DECT transmit function is achieved by direct modulation of the UHF VCO operating at half the final transmit output frequency. An on-chip doubler converts this to the final carrier frequency. In this mode the synthesizer is set to a high impedance mode i.e., "fly-wheeled." The drift is sufficiently low for both single-slot and double-slot transmit operation.

Synthesizer and LO Functions

A complete synthesizer is implemented on the IC that is capable of generating all the required DECT channel allocations (including the extended DECT bands). This synthesizer can use reference frequencies of either 13.824 MHz or 10.368 MHz, controlled by the RD bit in the control register.

Synthesizer Programming

The required channels are programmed by setting the RD bit in the control register to the correct value, then programming the A and M Counters as shown below through the serial interface.

Transmit

DECT Channel	A Counter	M Counter	Frequency/MHz
9	1	34	1881.792
8	2	34	1883.520
7	3	34	1885.248
6	4	34	1886.976
5	5	34	1888.704
4	6	34	1890.432
3	7	34	1892.160
2	8	34	1893.888
1	9	34	1893.888
0	10	34	1897.344

The A Counter range is 0–31, allowing the AD6411 to be used in the extended DECT bands, up to the following maximum frequency:

A Counter	M Counter	Frequency/MHz
31	34	1933.632

Receive (Local Oscillator Frequency)
Main values are shown for a 110.592 MHz IF frequency. Values in parentheses are for the 112.32 MHz.

DECT Channel	A Counter	M Counter	Frequency/MHz
9	1 (0)	32	1771.200 (1769.472)
8	2 (1)	32	1772.928 (1771.200)
7	3 (2)	32	1774.656 (1772.928)
6	4 (3)	32	1776.384 (1774.656)
5	5 (4)	32	1778.112 (1776.384)
4	6 (5)	32	1779.840 (1778.112)
3	7 (6)	32	1781.568 (1779.840)
2	8 (7)	32	1783.296 (1781.568)
1	9 (8)	32	1785.024 (1783.296)
0	10 (9)	32	1786.752 (1785.024)

Serial Interface
The IC operating modes can be controlled via the 3-wire serial interface or via the three external control lines provided (TX_ENAB, RX_ENAB, SYN_ENAB). The three external control lines allow mode control of the IC if the baseband controller cannot access the serial interface between slots. In either case the 3-wire serial interface is used to program the channel number. Detailed below is the register setup and the serial interface operation.

The serial interface consists of a 16-bit shift register and two registers for configuration of the IC and mode control. This allows mode control of the IC with a single 16-bit write. DATA is the serial data input (data MSB first), CLK is the shift register clock (positive edge trigger), EN (positive edge trigger) is the serial interface enable. All internal register values are retained when sections of the IC are powered down. Figure 3 shows the timing diagram for the serial interface.

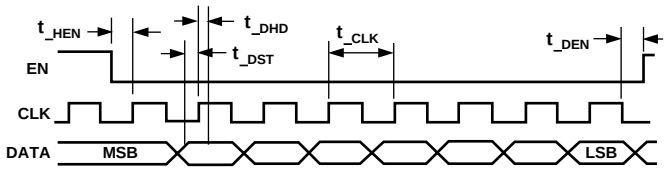


Figure 3. Serial Interface Timing Diagram

Parameter	Symbol	Typ	Unit
Maximum Serial Clock Frequency	f_clk	13.824	MHz
Serial Data Set Up Time	t_dst	8	ns
Serial Data Hold Time	t_dhd	8	ns
Enable Set Up to Clock High	t_hen	10	ns
Clock Low to Enable Low	t_den	5	ns

The Least Significant Bit of the serial control word selects either the "one-time setup" register or the operating mode register, with the remaining 15 bits as data. Table II below details the internal IC register mapping.

Table II. Register Mapping

Address (D0)	Function	Comments
0	One-Time IC Setup	See Table III
1	IC Operating Mode	See Table IV

AD6411 INITIAL SETUP
On power-up the state of the IC is *not* defined. A one-time setup register must be loaded through the serial interface port, and is selected when the LSB of the serial word is 0. After this one-time setup, a single serial word controls operation of the IC.

Table III. One-Time IC Setup Register

D15	D14	D13	D12	D11	D10	D9	D8
X	RSB	TSB	SSB	RXM1	RXM0	TXM	BSWS

D7	D6	D5	D4	D3	D2	D1	D0
CF0	CT1	CT0	DSD	SFM	PDS	RD	0

One-Time Setup Register Bit Definitions

RSB: Receive Control Line Sense Bit

RSB	Function
0	Receive Section POWER UP Active HIGH
1	Receive Section POWER UP Active LOW

TSB: Transmit Control Line Sense Bit

TSB	Function
0	Transmit Section POWER UP Active HIGH
1	Transmit Section POWER UP Active LOW

SSB: Synthesizer Control Line Sense Bit

SSB	Function
0	Synthesizer POWER UP Active LOW
1	Synthesizer POWER UP Active HIGH

RXM1, RXM0: Divider Power Mode In Active Receive Slot

RXM1	RXM0	Function
0	0	Dividers Powered Down, VCO Flywheeled in Active Receive Mode
0	1	Dividers Powered Up, VCO Flywheeled in Active Receive Mode
1	0	Dividers Powered Up, VCO Locked to Synthesizer in Active Receive Mode
1	1	Dividers Powered Up, VCO Locked to Synthesizer in Active Receive Mode

TXM: Divider Power Mode In Active Transmit Slot

TXM	Function
0	Dividers Powered Down, VCO Flywheeled in Active Mode
1	Dividers Powered Up, VCO Flywheeled in Active Mode

BSWS: Band Switch Sense (Control with External Lines)

BSWS	Function
0	Band Switch Output High in Receive Slot, PIN Diode ON
1	Band Switch Output Low in Receive Slot, PIN Diode ON

CF0: Configuration Bit 0

CF0	Function
0	Use Serial Interface for Mode Control
1	Use External Control Lines for Mode Control

CT1, CT0: Charge Pump Test Bits

CT1	CT0	Function
0	0	Three-State Output
0	1	Force Pump UP Current (Nom 1 mA)
1	0	Force Pump DOWN Current (Nom 1 mA)
1	1	Normal Operation (Driven from PFD)

DSD: Disable Data Slicer

DSD	Function
0	Disable On-Chip Data Slicer. Analog Output at Pin DEMOD_DATA
1	Enable On-Chip Data Slicer. Digital Output at Pin DEMOD_DATA

DSD bit is configured at power-up depending on whether an external data slicer is being used in the system. Data slicer is disabled when the IF strip is powered down irrespective of the status of bit DSD.

SFM: S-Field Mode

SFM	Function
0	Normal Demodulation Mode
1	S-Field Sampling Mode

PDS: Phase Detector Sense

PDS	Function
0	PFD Pumps UP when Fvco > Fref
1	PFD Pumps UP when Fref > Fvco

RD: Reference Divide Ratio

RD	Function
0	Reference Frequency = 10.368 MHz
1	Reference Frequency = 13.824 MHz

CONTROLLING THE AD6411 OPERATING MODE

Table IV. Operating Mode Control Register

D15	D14	D13	D12	D11	D10	D9	D8
M0	A4	A3	A2	A1	A0	IF/RSSI	RXMixer

D7	D6	D5	D4	D3	D2	D1	D0
DMOD	DIV	CP	TX BUF	UHF VCO	BSW	REGS	1

The operating mode register, loaded through the serial port when the LSB is "1," allows any circuit block to be independently powered on or off. This can be bypassed to enable mode control of the IC via the three external control lines. Transitions between major DECT modes can be made with a single word program (including channel change) when using the serial interface only. Table V defines the bit status for the various IC operating modes when used with the serial interface only.

Table V. Bit Status for the Different Operating Modes

Data Bits (D9 . . . D0) Operating Mode Register	Function	Comments
00 0000 0101	All Off Mode	All Circuits Off
00 0000 0111	Stand-By Mode	Regulators On
00 0111 1111	Prior to TX Slot	VCO, TX Buffer, Dividers, Charge Pump, Regulators Active, VREF (1.4 V) Active
00 0101 1111	Active TX Slot	VCO, TX Buffer, Dividers, Regulator Circuits Active, VREF (1.4 V) Active[1]
00 1110 1011	Prior to RX Slot	VCO[2], Dividers, Charge Pump, Regulators, Demodulator Precharge Circuits Active, VREF (1.4 V) Active
11 1100 1011	Active RX Slot	RX Mixer, VCO[2], Dividers, Regulators, Demodulator, Receive Strip Circuits Active, VREF (1.4 V) Active

NOTES
[1]Alternatively it may be possible to power-down the dividers in an active transmit slot depending on the effect of thermal transients on VCO pulling. In this mode the dividers are biased but inactive. This can also be implemented when external control lines are used with bits TXM, RXM1, RXM0.
[2]Band switch output is determined by the status of BSW. Band switch output is Low when BSW is high, high when BSW is low. In Table V, band switch output is high for AcRx and PrRx slots, otherwise it is low.

CHANNEL SELECTION/FREQUENCY CONTROL

The M0 and A4–A0 bits in the operating mode register control the channel selection for the AD6411 synthesizer. The M0 bit selects the M Counter division ratio.

M0: M Counter Divide Ratio

M0	Function
0	M Divide Ratio 32
1	M Divide Ratio 34

The A4 through A0 bits control the A counter division ratio, and control the channel selection. Refer to the section of this data sheet on Synthesizer Programming for a mapping of channel frequency to synthesizer divider words.

A4–A0: A Counter Division Ratio

"A"	A4	A3	A2	A1	A0
0	0	0	0	0	0
1	0	0	0	0	1
2	0	0	0	1	0
3	0	0	0	1	1
–	–	–	–	–	–
30	1	1	1	1	0
31	1	1	1	1	1

ANALOG/RF INTERFACE DETAILS

The AD6411 is an advanced 1.9 GHz radio transceiver circuit and requires careful attention to the selection of external components. The AD6411 is readily capable of performance that meets the ETS-300-176-1 (formerly TBR06) DECT radio specifications. This section of the data sheet will describe suggestions for external componentry that will allow the design of a complete DECT RF transceiver.

Low Noise Amplifier

An external LNA is required to meet the RF leakage specifications in ETS-300-176-1. The following circuit, based on a Siemens BFP405 discrete transistor, is representative of a suitable LNA. The SC1.89 SAW filter removes images prior to the down converter. The filter is matched to the AD6411 input with a printed inductor and fixed capacitor. Complete details of the circuit, with transmission-line dimensions, can be found in Siemens Application Note No. 020.

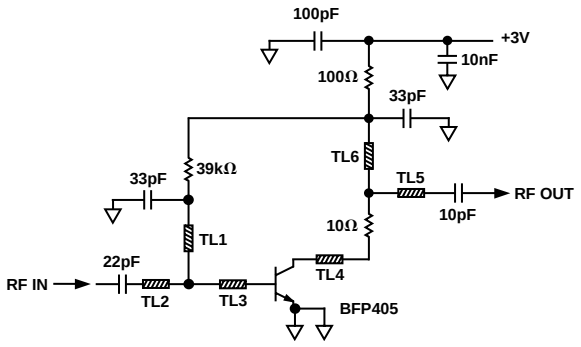


Figure 4. LNA circuit

UHF VCO Tank Circuit

The UHF VCO is probably the most critical part of an AD6411-based DECT radio. The design shown in Figure 5 uses a printed inductor, a BBY53 (or equivalent) common-cathode dual varactor, and a PIN-diode (BAR63-03W or equivalent) band switch to cover the DECT band. The capacitance added to the tank circuit by the PIN-diode is needed to switch the VCO to the DECT receive band. It is switched out of the circuit in the transmit mode, in which the VCO is directly modulated by baseband transmit data. With this scheme, no manufacturing trim is needed to tune the VCO to the DECT band. Tank component values will need slight modification to cover the "extended DECT" frequency bands. The dimensions of tank inductor L1 will depend on the circuit board material and thickness used. Contact Analog Devices for assistance on UHF tank inductor layout.

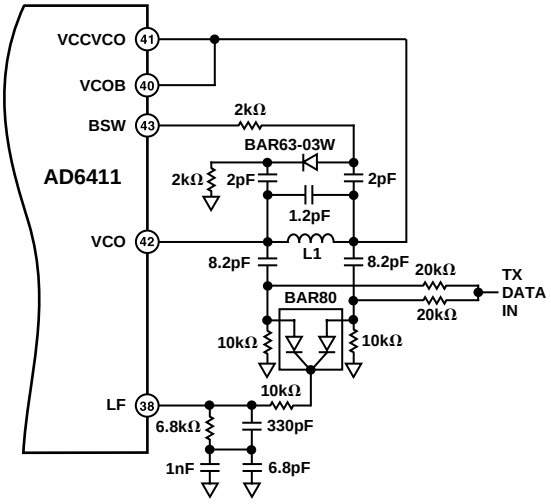


Figure 5. UHF VCO Circuit

Power Management

The AD6411 reduces the external components needed for power management in a DECT radio by integrating voltage regulators on-chip. The circuit can therefore operate directly from a 3.0 V to 5.5 V unregulated battery supply.

There are two regulators. The first, VS1 (Pins 20, 21 and 23), uses an external BCW68F (or similar) PNP pass transistor to provide a regulated 2.75 V nominal supply voltage to most of the AD6411 circuitry. The second regulator, VS2 (Pins 41, 44, and 45), is intended to provide the regulated voltage to the UHF VCO section and should not be used for other circuitry.

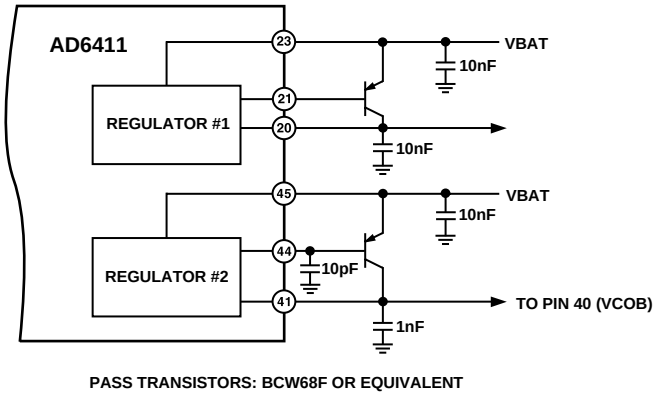


Figure 6. Voltage Regulator Circuitry

Transmit/Receive Switching

Since the same antenna is used for both transmit and receive, a switch consisting of PIN diodes and printed transmission lines is used to disconnect the receive path from the antenna during transmit periods. A suggested circuit is shown in Figure 7. Complete details can be found in Siemens Application Note No. 007.

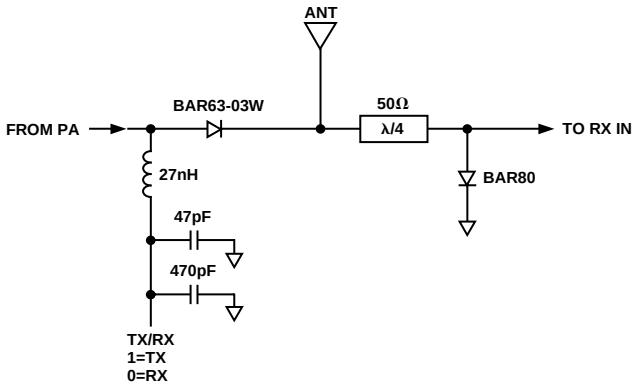
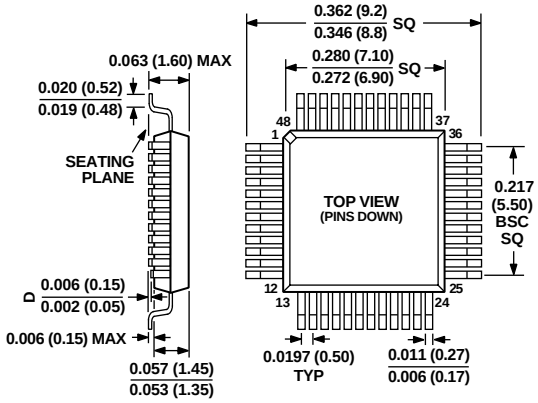


Figure 7. T/R Switch

OUTLINE DIMENSIONS

Dimensions shown in inches and (mm).

48-Lead Plastic LQFP
(ST-48)



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