VI BRICK® PFM®
PF175B480C033FP-00

Actual Size:
1.92 x 1.91 x 0.37 in
48,7 x 48,6 x 9,5 mm

Isolated AC-DC Converter with PFC

Features

- Isolated AC-to-DC converter with PFC
- Low profile
- Power Density: 243 W/in³
  330 W in 3.67 in² footprint
- High efficiency (~93%) over world-wide AC mains
  - Rectified 85 – 264 VAC
- Secondary-side energy storage
- Simplified mounting and thermal management
- SELV 48 V Output
  - Efficient power distribution to POL converters
  - 3,000 VAC / 4,242 VDC isolation
- PFC (THD) exceeds EN61000-3-2 requirements
- ZVS high frequency (MHz) switching
- Low profile, high density filtering
- 100°C baseplate operation

Typical Applications

- Telecom (WiMAX, Power Amplifiers, Optical Switches)
- Automatic Test Equipment (ATE)
- LED lighting
- High Efficiency Server Power
- Office equipment (Printers, Copiers, Projectors)
- Industrial Equipment (Process Controllers, Material Handling, Factory Automation)
- Switch Mode Power Supplies (SMPS)

Product Overview

The VI BRICK® PFM® Isolated AC-DC Converter with PFC is an AC-to-DC converter, operating from a rectified universal AC input to generate an isolated 48 Vdc output bus with power factor correction. With its ZVS high frequency Adaptive Cell™ topology, the VI BRICK PFM converter consistently delivers high efficiency across worldwide AC mains. Modular PFM converters and downstream DC-DC VI BRICK products support secondary-side energy storage and efficient power distribution at 48 V, providing superior power system performance and connectivity from the wall plug to the point-of-load.

Major Specifications

V_{IN}	85 – 264 V_{AC} (rectified)
V_{OUT}	48 V_{DC} (isolated)
P_{OUT}	330 W

Nomenclature

Function		Input Voltage Designator			Package Size	Output Voltage Vout (V) (x10)			Temperature Grade	Output Power Pout (W) (÷10)			Baseplate	Pin Style		Revision	
P	F	1	7	5	B	4	8	0	C	0	3	3	F	P	–	0	0

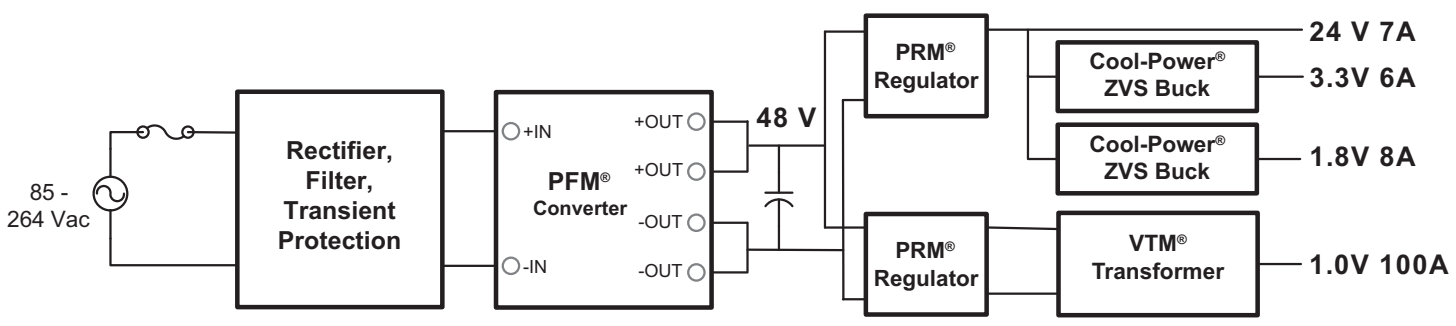
Universal (85-264 Vac)

Grade	Operating	Storage
C =	-20 to 100°C	-40 to 125°C
T =	-40 to 100°C	-40 to 125°C
M =	-55 to 100°C	-65 to 125°C

F = Slotted Flange

P = Through hole

Typical Application: Universal AC Input, Quad Output, 300W Power Supply



1.0 ABSOLUTE MAXIMUM RATINGS

The Absolute Maximum Ratings below are stress ratings only.
Operation at or beyond these maximum ratings can cause permanent damage to device. Electrical specifications do not apply when operating beyond rated operating conditions. Positive pin current represents current flowing out of the pin.

1.0 Absolute Maximum Ratings

PARAMETER	MIN	MAX	UNIT	NOTES
Input voltage (+In to -In)	0	600	Vpk	1 ms max
Input voltage (+In to -In)	0	385	Vpk	Continuous
Input voltage slew rate	-25	25	V/µs	Common Mode and Differential Mode
RSV1 to –IN	-0.3	5.3	V_{DC}	Do not connect to this pin
EN to –IN	-0.3	5.3	V_{DC}	5 V tolerant 3.3 V logic
RSV3 to –IN	-0.3	5.3	V_{DC}	Do not connect to this pin
Output voltage (+Out to -Out)	-0.5	57.0	V_{DC}	
Output current	0.0	10.2	A	
TEMPERATURE				
Operating junction	-55	125	°C	Worst case semiconductor
Operating temperature	-20	100	°C	C-Grade; baseplate
	-40	100	°C	T-Grade; baseplate
	-55	100	°C	M-Grade; baseplate
Storage temperature	-40	125	°C	C-Grade
	-40	125	°C	T-Grade
	-65	125	°C	M-Grade
DIELECTRIC WITHSTAND				
Dielectric Withstand Input – Output	3000		V_{RMS}	
Dielectric Withstand Input – Base	1500		V_{RMS}	
Dielectric Withstand Output – Base	1500		V_{RMS}	

2.0 ELECTRICAL CHARACTERISTICS

Specifications apply over all line and load conditions, 50 Hz and 60 Hz line frequencies, T_C= 25°C, unless otherwise noted.
***Boldface** specifications apply over the temperature range of the specified product grade. C_{OUT} is 6800 µF +/- 20% unless otherwise specified.*

2.0 Electrical Characteristics

ATTRIBUTE	SYMBOL	CONDITIONS / NOTES	MIN	TYP	MAX	UNIT
POWER INPUT SPECIFICATION						
Input voltage range, continuous operation	V_{IN}		**85**		**264**	V_{RMS}
Input voltage range, transient, non-operational (peak)	V_{IN}	1 ms			600	V
Input voltage cell reconfiguration low-to-high threshold	V_{IN-CR+}			145	**148**	V_{RMS}
Input voltage cell reconfiguration high-to-low threshold	V_{IN-CR-}		**132**	135		V_{RMS}
Input voltage slew rate	dV_{IN}/dt	Common Mode and Differential Mode	-25		25	V/µs
Input current (peak)	I_{INRP}				12	A
Source line frequency range	f_{line}		47		63	Hz
Power factor	PF	Input power >100 W		0.9		-
Input inductance, maximum	L_{IN}	Differential mode inductance, common mode inductance may be higher			1	mH
Input capacitance, maximum	C_{IN}	After bridge rectifier, between +IN and - IN			1.5	µF
NO LOAD SPECIFICATION						
Input power – no load, maximum	P_{NL}	EN floating, see Figure 6		1.1	1.5	W
Input power – disabled, maximum	P_Q	EN pulled low, see Figure 7			1.6	W
POWER OUTPUT SPECIFICATION						
Output voltage set point	V_{OUT}	Vin = 230 Vrms, 10% Load	47.5	49	50.5	V
Output voltage, no load	V_{OUT-NL}	Over all operating steady state line conditions	**46**	51.5	**55**	V
Output voltage range (transient)	V_{OUT}	Non-faulting abnormal line and load transient conditions	**30**		**55**	V
Output power	P_{OUT}	See Figure 1, SOA			**330**	W
Efficiency	η	V_{IN} = 230 V, full load, exclusive of input rectifier losses	92	93.5		%
		85 V < V_{IN} < 264 V, full load, exclusive of input rectifier losses	**91**			%
		85 V < V_{IN} < 264 V, 75% load, exclusive of input rectifier losses	92			%
Output voltage ripple, switching frequency	$V_{OUT-PP-HF}$	Over all operating steady-state line and load conditions, 20 MHz BW, measured at C3, Figure 29		100	**300**	mV
Output voltage ripple line frequency	$V_{OUT-PP-LF}$	Over all operating steady-state line and load conditions, 20 MHz BW		3.8	5	V
Output capacitance (external)	$C_{OUT-EXT}$		**6000**		**12000**	µF
Output turn-on delay	T_{ON}	From V_{IN} applied, EN floating		400	**1000**	ms
		From EN pin release, V_{IN} applied				
Start-up setpoint aquisition time	T_{SS}	Full load		400	500	ms
Cell reconfiguration response time	T_{CR}	Full load		5.5	11	ms
Voltage deviation (transient)	$\%V_{OUT-TRANS}$				8	%
Recovery time	T_{TRANS}			250	500	ms
Line regulation	$\%V_{OUT-LINE}$	Full load		0.5	1	%
Load regulation	$\%V_{OUT-LOAD}$	10% to 100% load		0.5	1	%
Output current (continuous)	I_{OUT}	See Figure 1, SOA			**6.9**	A

2.0 ELECTRICAL CHARACTERISTICS (CONT.)

2.0 Electrical Characteristics (Continued)

ATTRIBUTE	SYMBOL	CONDITIONS / NOTES	MIN	TYP	MAX	UNIT
POWER OUTPUT SPECIFICATION (CONTINUED)						
Output current (transient)	I_{OUT-PK}	20 ms duration, average power ≤P_{OUT}, max			**10.2**	A
Output switching cycle charge	Q_{TOT}				**13.5**	µC
Output inductance (parasitic)	$L_{OUT-PAR}$	Frequency @ 1 MHz, simulated J-lead model		1		nH
Output capacitance (internal)	$C_{OUT-INT}$	Effective value at nominal output voltage		7		µF
Output capacitance (internal ESR)	R_{COUT}			0.5		mΩ
POWERTRAIN PROTECTIONS						
Input undervoltage turn-on	$V_{IN-UVLO+}$	See Timing Diagram		74	**83**	V_{RMS}
Input undervoltage turn-off	$V_{IN-UVLO-}$		**65**	71		V_{RMS}
Input overvoltage turn-on	$V_{IN-OVLO-}$	See Timing Diagram	**265**	270		V_{RMS}
Input overvoltage turn-off	$V_{IN-OVLO+}$			273	**283**	V_{RMS}
Output overvoltage threshold	$V_{OUT-OVLO+}$	Instantaneous, latched shutdown	**55.3**	56.6	**59.0**	V
Upper start/restart temperature threshold (case)	$T_{CASE-OTP-}$		**100**			°C
Overtemperature shutdown threshold (internal)	T_{J-OTP+}		**130**			°C
Overtemperature shutdown threshold (case)	$T_{CASE-OTP+}$			**110**		°C
Undertemperature shutdown threshold (case)	$T_{CASE-UTP-}$	T, C Grades		-61		°C
		M Grade		-73		
Lower start / restart temperature threshold (case)	$T_{CASE-UTP+}$	T, C Grades		-52		°C
		M Grade		-65		
Overcurrent blanking time	T_{OC}	Based on line frequency	**400**	460	**550**	ms
Input overvoltage response time	T_{POVP}				**6**	µs
Input undervoltage response time	T_{UVLO}	Based on line frequency	**27**	39	**51**	ms
Output overvoltage response time	T_{SOVP}	Powertrain on	**60**	120	**180**	µs
Short circuit response time	T_{SC}	Powertrain on, operational state		60	**120**	µs
Fault retry delay time	T_{OFF}	See Timing Diagram		10		s
Output power limit	P_{PROT}		**330**			W

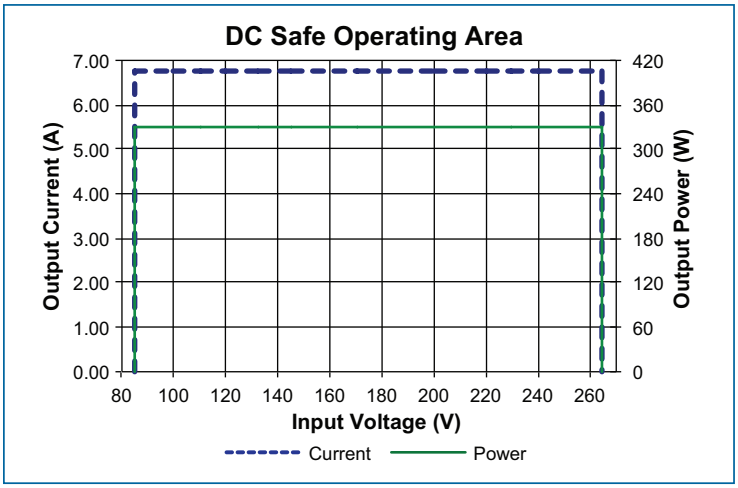


Figure 1 — DC output safe operating area

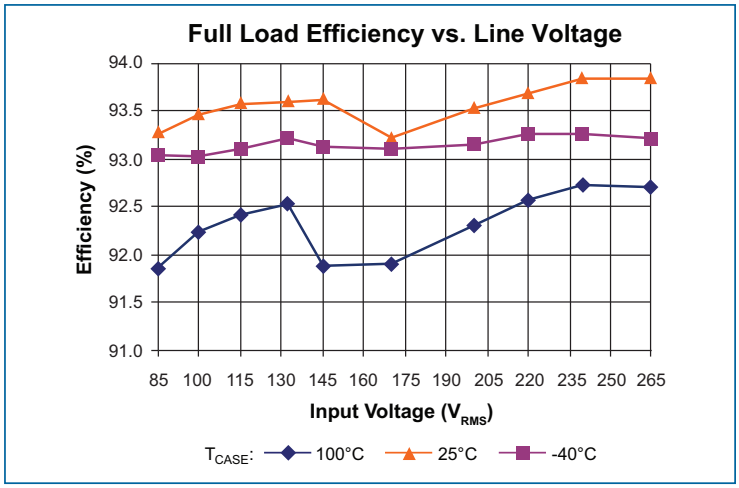


Figure 2 — Full load efficiency vs. line voltage

3.0 SIGNAL CHARACTERISTICS

Specifications apply over all line and load conditions, 50 Hz and 60 Hz line frequencies, T_C= 25°C, unless otherwise noted.
Boldface *specifications apply over the temperature range of the specified product grade. C_{OUT} is 6800 µF +/- 20% unless otherwise specified.*

3.0 Signal Characteristics

ENABLE : EN

- The EN pin enables and disables the PFM® converter; when held below 0.8 V the unit will be disabled.
- The EN pin can reset the PFM converter after a latching OVP event.
- The EN pin voltage is 3.3 V during normal operation.
- The EN pin is referenced to the –IN pin of the converter.

SIGNAL TYPE	STATE	ATTRIBUTE	SYMBOL	CONDITIONS / NOTES	MIN	TYP	MAX	UNIT
DIGITAL INPUT	Startup	EN enable threshold	V_{EN_EN}		2.31			V
	Standby	EN disable time	t_{EN_DIS}	From any point in line cycle		9	**16**	ms
		EN disable threshold	V_{EN_DIS}				0.99	V
		EN resistance to disable	R_{EN_EXT}	Max allowable resistance to -IN required to disable the module			**4.28**	kΩ

RESERVED : RSV1, RSV3

No connections are required to these pins. In noisy enviornments, it is beneficial to add a 0.1 µF capacitor between each reserved pin and -IN.

4.0 FUNCTIONAL BLOCK DIAGRAM

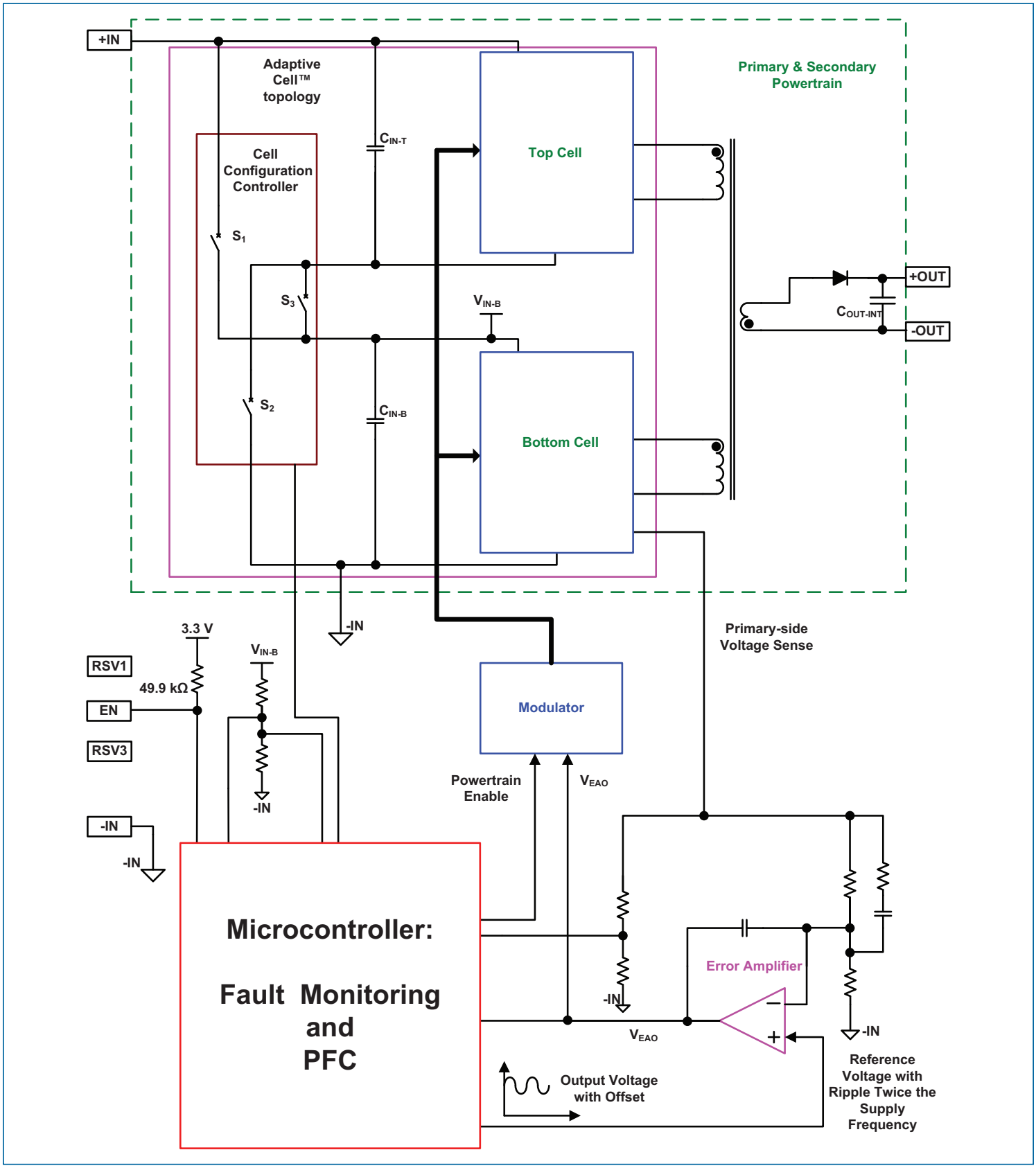


Figure 3 — Functional block diagram

5.0 HIGH LEVEL FUNCTIONAL STATE DIAGRAM

Conditions that cause state transitions are shown along arrows. Sub-sequence activities are listed inside the state bubbles.

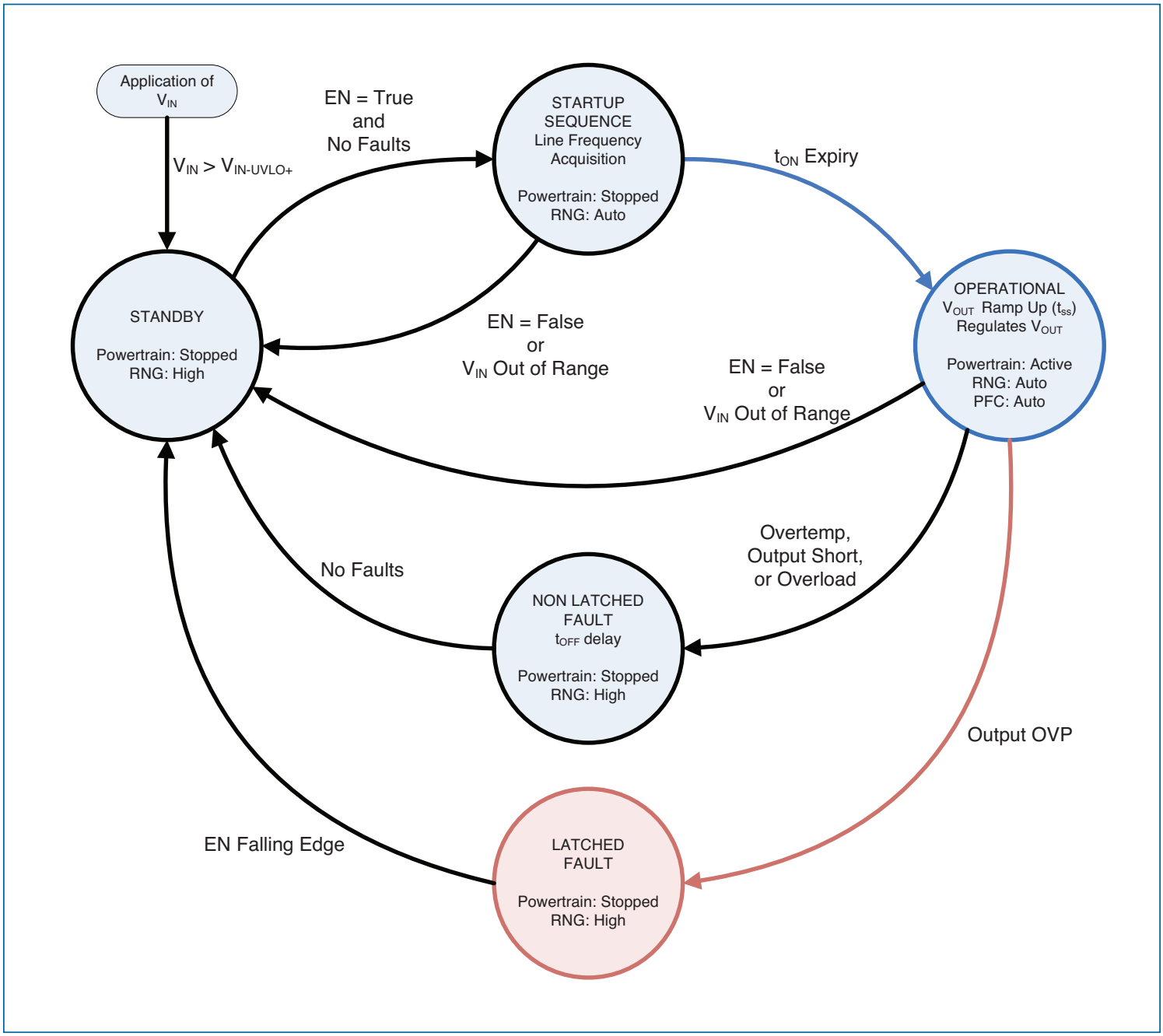


Figure 4 *— State diagram*

6.0 TIMING DIAGRAMS

Module inputs are shown in blue; Module outputs are shown in brown;
Timing diagram assumes resistive load, adjusted as shown in the diagram, except in the case of output OVP.

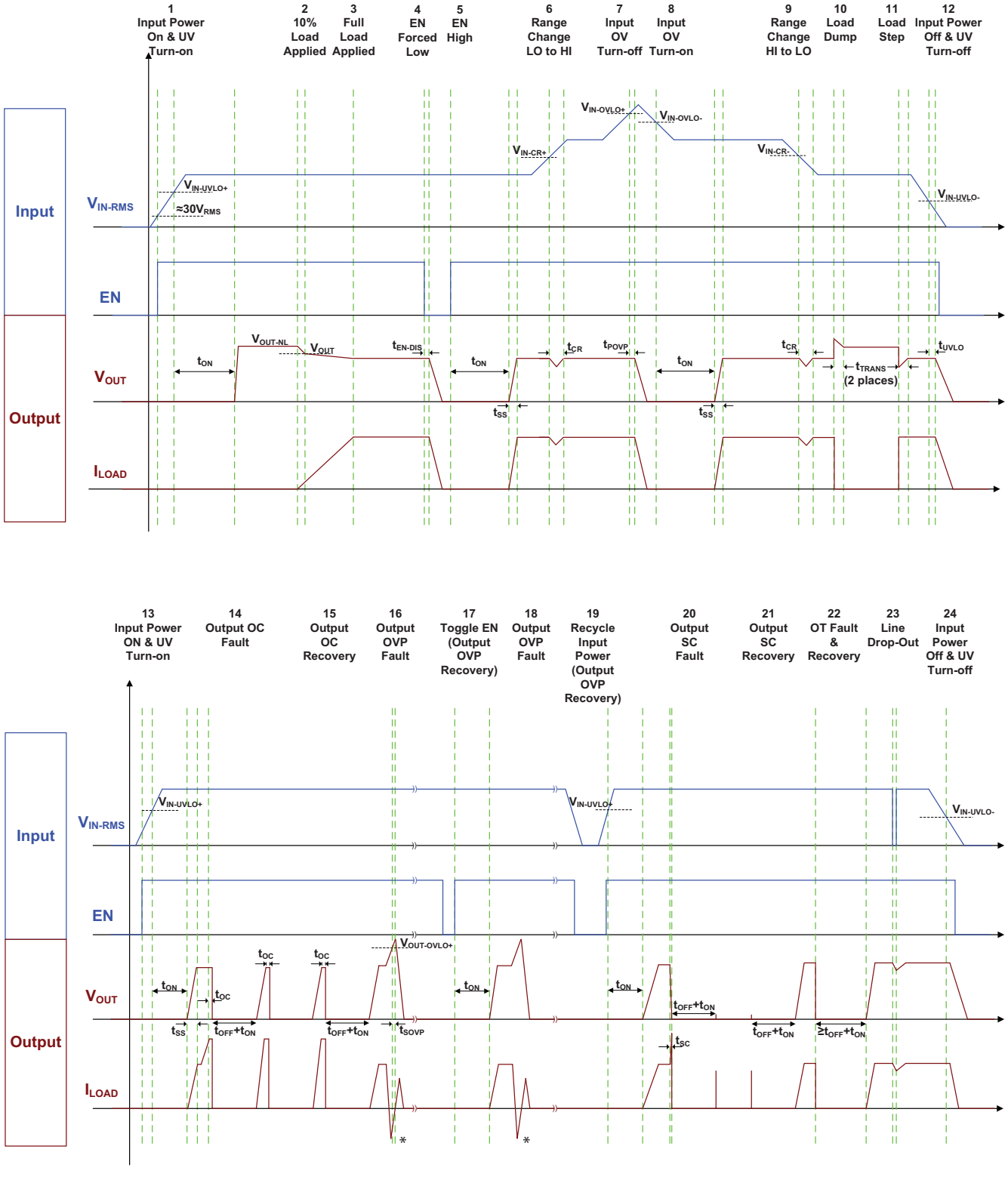


*Figure 5 — Timing diagram - * Negative current is externally forced and shown for the purpose of OVP protection scenario.*

7.0 APPLICATION CHARACTERISTICS

The following figures present typical performance at T_C = 25ºC, unless otherwise noted. See associated figures for general trend data.

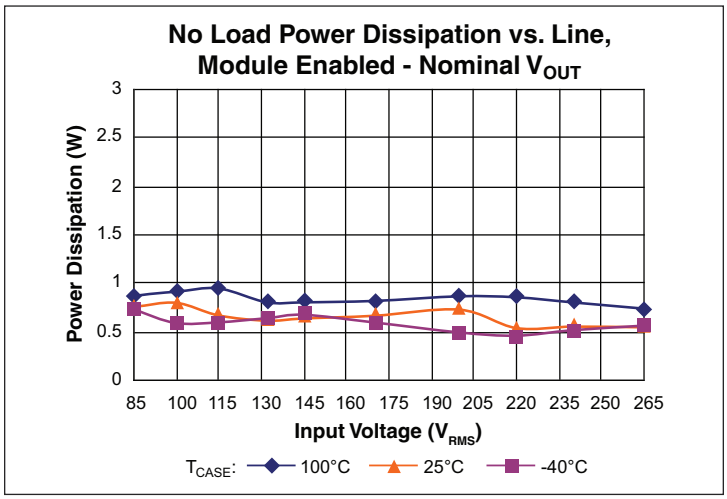


Figure 6 – *Typical no load power dissipation vs. V_{IN}, module enabled.*

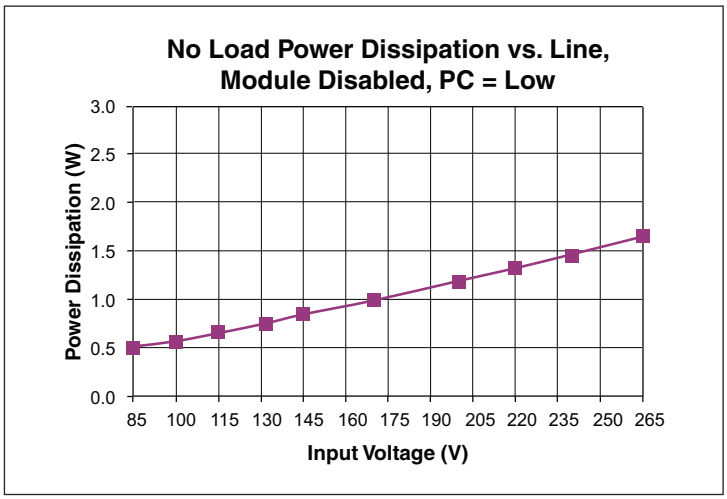


Figure 7 – *No load power dissipation trend vs. V_{IN}, module disabled.*

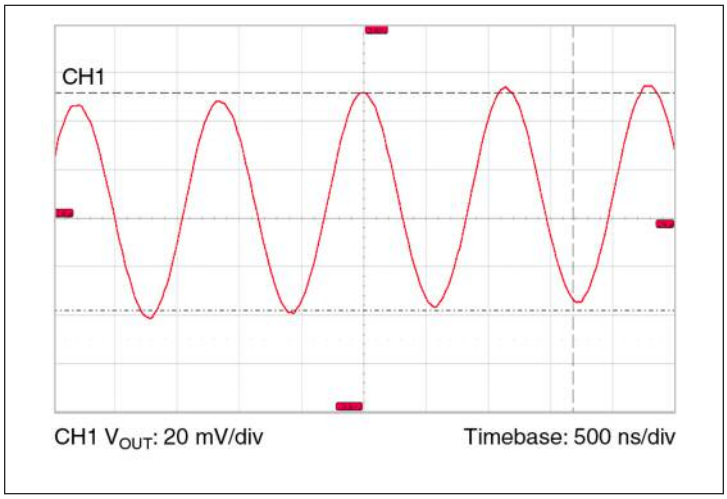


Figure 8 – *Typical switching frequency output voltage ripple waveform, T_{CASE} = 30ºC, V_{IN} = 230 V, I_{OUT} = 6.9 A, no external ceramic capacitance.*

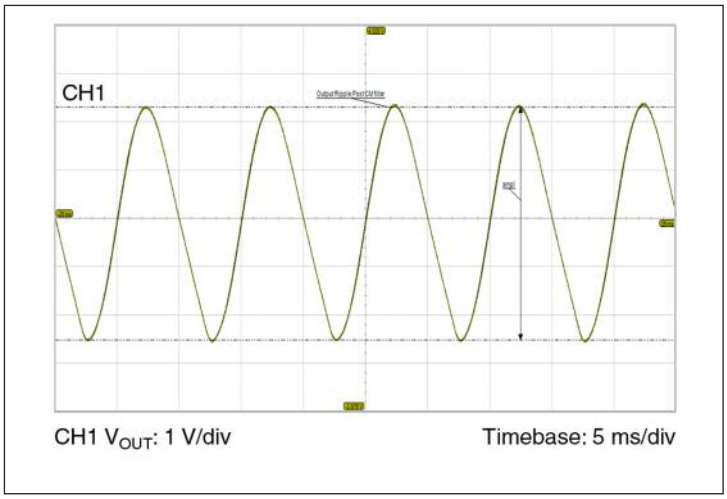


Figure 9 – *Typical line frequency output voltage ripple waveform, T_{CASE} = 30ºC, V_{IN} = 230 V, I_{OUT} = 6.9 A, C_{OUT} = 6,800 µF. Measured at C3, Fig 29.*

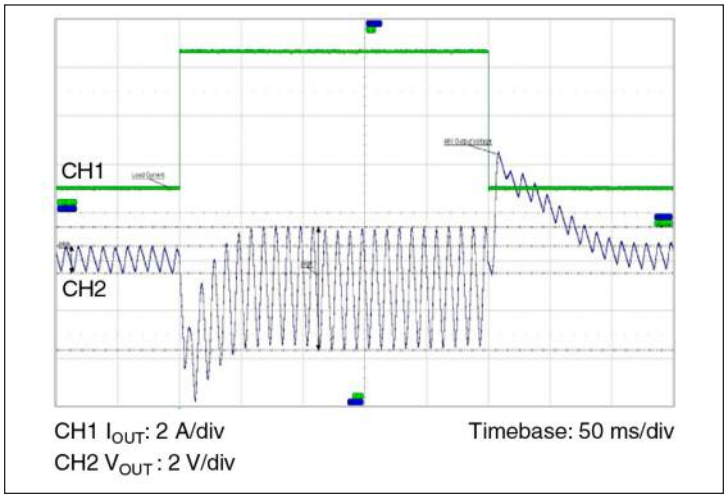


Figure 10 – *Typical output voltage transient response, T_{CASE} = 30ºC, V_{IN} = 230 V, I_{OUT} = 1.0 A to 6.7 A, C_{OUT} = 6,800 µF.*

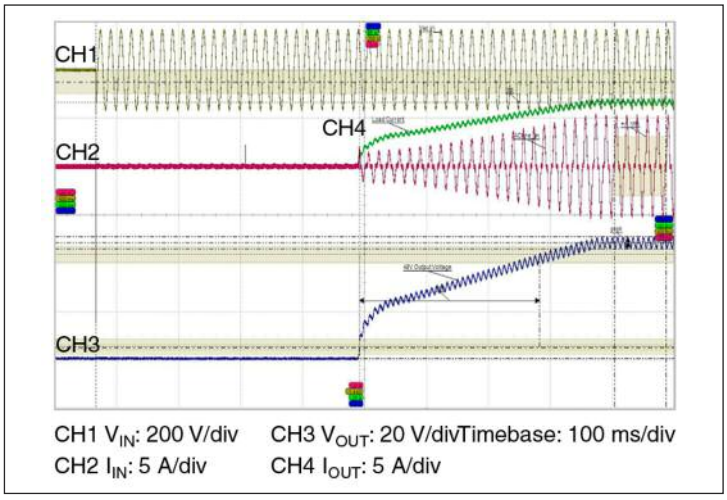


Figure 11 – *Typical startup waveform, application of V_{IN}, R_{LOAD} = 7.1 Ω, C_{OUT} = 6,800 µF.*

7.0 APPLICATION CHARACTERISTICS (CONTINUED)

The following figures present typical performance at T_C = 25°C, unless otherwise noted. See associated figures for general trend data.

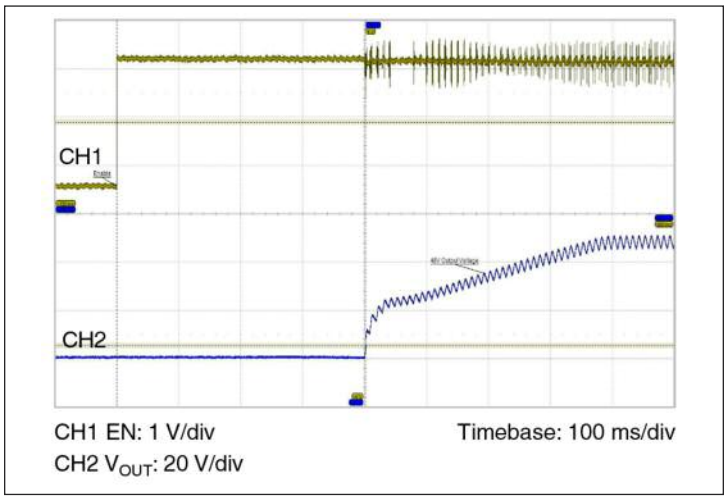


Figure 12 – *Typical startup waveform, EN pin release, V_{IN} = 240 V, R_{LOAD} = 7.1 Ω, C_{OUT} = 6,800 µF.*

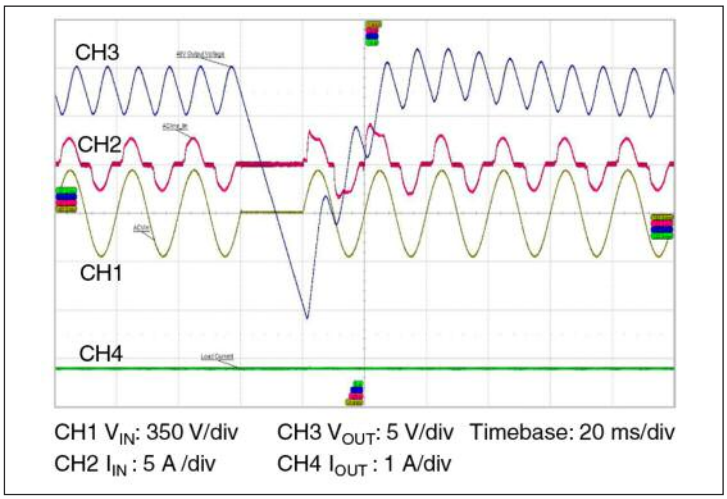


Figure 13 – *Line drop out, 50 Hz, 0° phase, V_{IN} = 230 V, I_{LOAD} = 6.8A, C_{OUT} = 6,800 µF.*

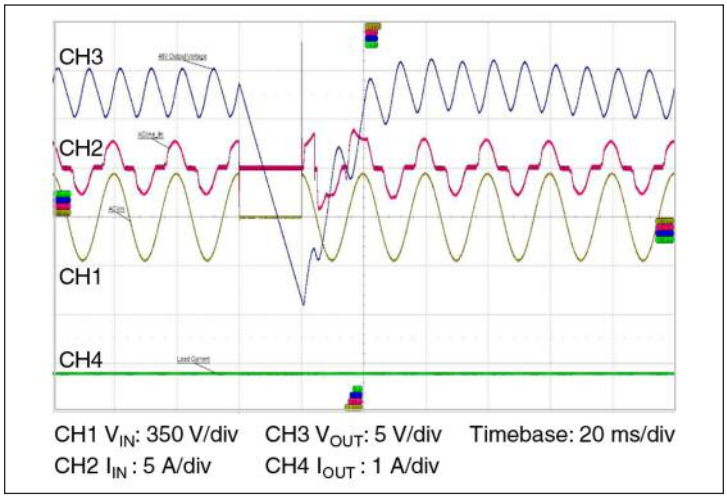


Figure 14 – *Line drop out, 50 Hz, 90° phase, V_{IN} = 230 V, I_{LOAD} = 6.8A, C_{OUT} = 6,800 µF.*

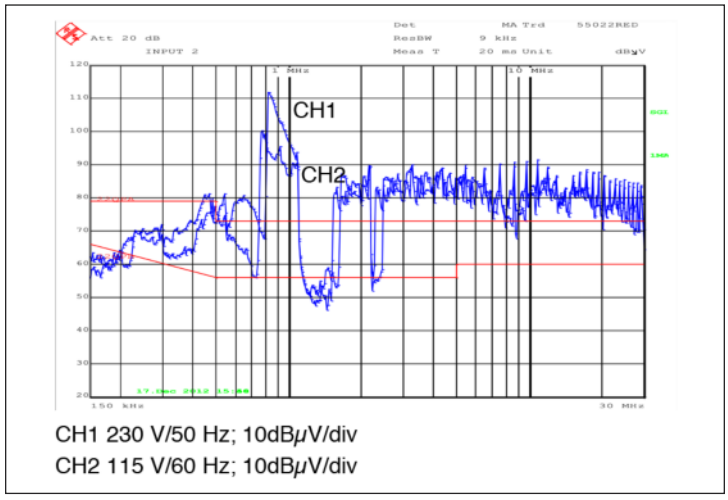


Figure 15 – *Typical conducted emissions, full load, 3x0.47uF X caps +IN to -IN, no CM filter. C_{OUT} = 6,800 µF, -Out grounded.*

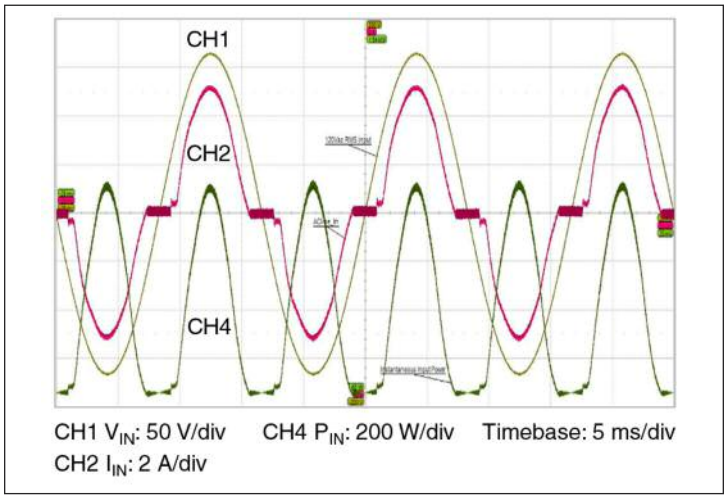


Figure 16 – *Typical line current waveform, V_{IN} = 120 V, P_{LOAD} = 330 W.*

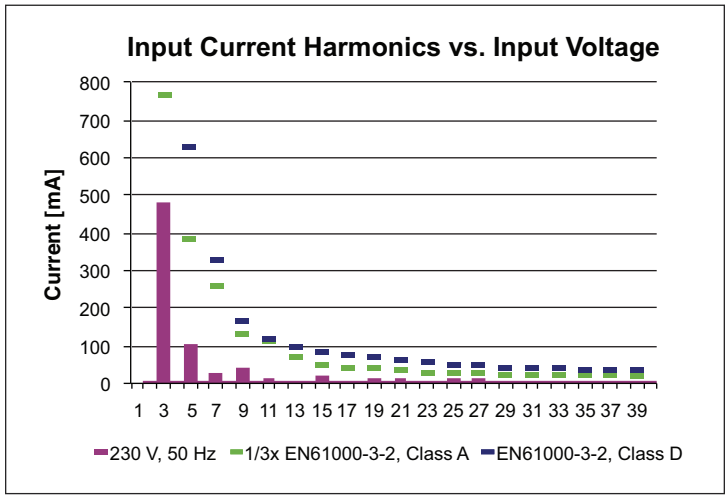


Figure 17 – *Typical input current harmonics, full load vs. V_{IN}.*

7.0 APPLICATION CHARACTERISTICS (CONTINUED)

The following figures present typical performance at T_C = 25ºC, unless otherwise noted. See associated figures for general trend data.

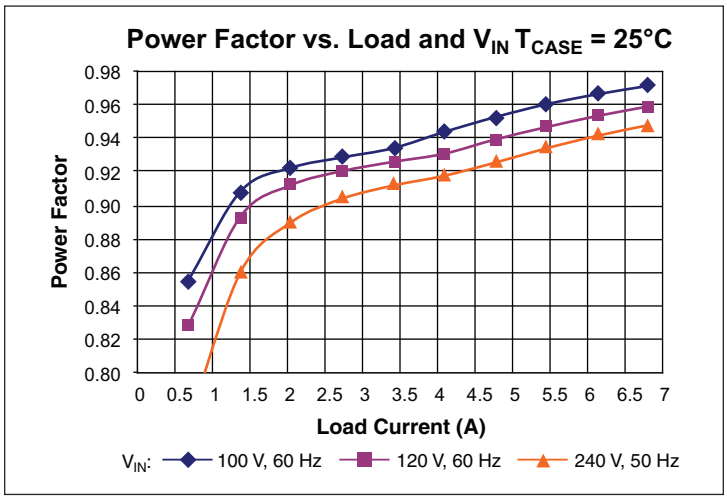


Figure 18 – *Typical power factor vs. V_{IN} and I_{OUT}.*

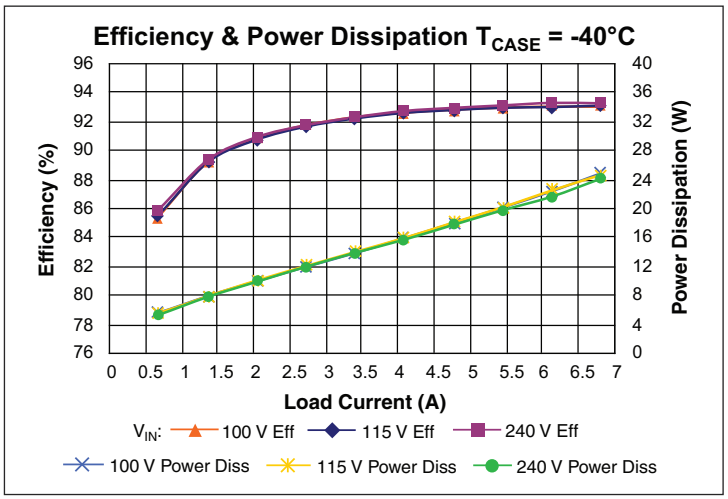


Figure 19 – *V_{IN} to V_{OUT} efficiency and power dissipation vs. V_{IN} and I_{OUT}, T_{CASE} = -40ºC.*

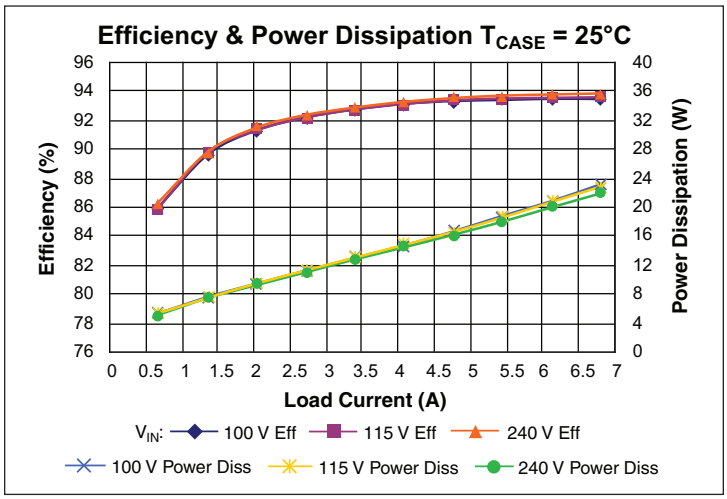


Figure 20 – *V_{IN} to V_{OUT} efficiency and power dissipation vs. V_{IN} and I_{OUT}, T_{CASE} = 25ºC.*

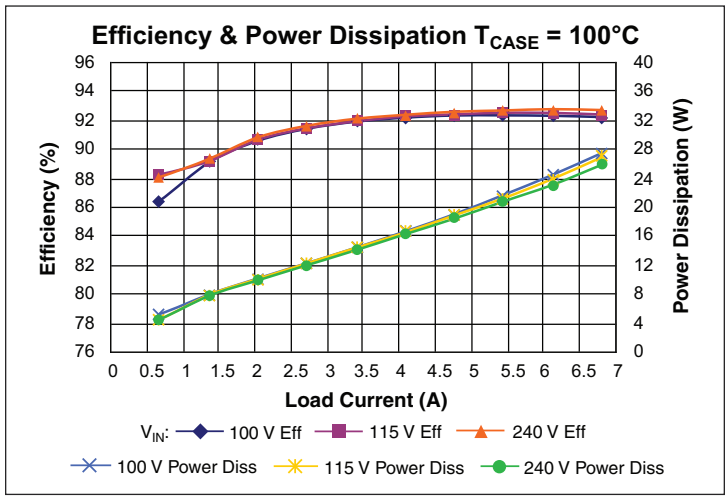


Figure 21 – *V_{IN} to V_{OUT} efficiency and power dissipation vs. V_{IN} and I_{OUT}, T_{CASE} = 100ºC.*

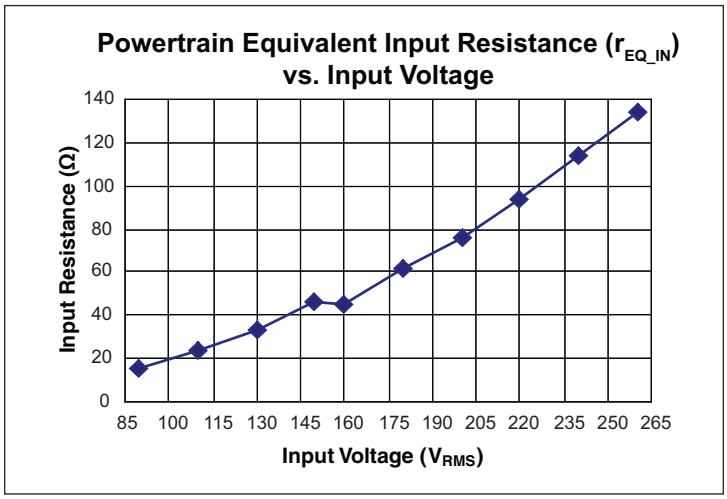


Figure 22 – *Dynamic input resistance vs. V_{IN}, I_{OUT} = 6.9 A.*

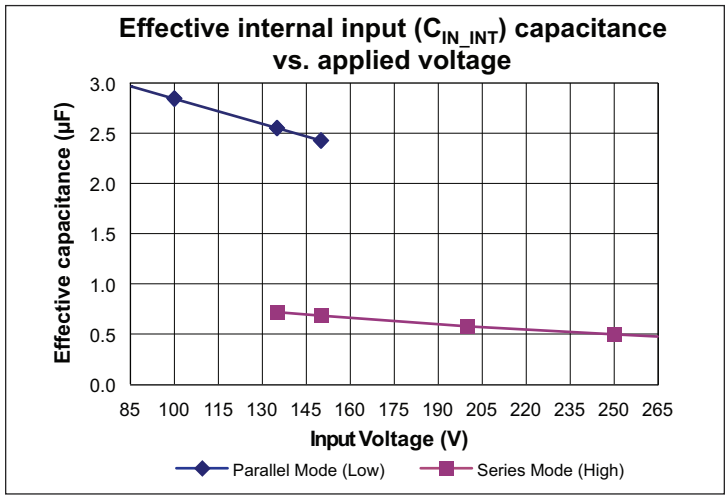


Figure 23 – *Effective input capacitance vs. V_{IN}.*

8.0 GENERAL CHARACTERISTICS

Specifications apply over all line and load conditions, T_C = 25°C, unless otherwise noted.

8.0 General Characteristics

ATTRIBUTE	SYMBOL	CONDITIONS / NOTES		MIN	TYP	MAX	UNIT
MECHANICAL							
Length	L				48.6/[1.91]		mm/[in]
Width	W				48.7/[1.92]		mm/[in]
Height	H				9.50/[0.37]		mm/[in]
Volume	Vol				22.5/[1.37]		cm^3/[in^3]
Weight	W				57.5/[2.03]		g/[oz]
Pin material		C10200 copper, full hard					µin
Underplate		Nickel		100		150	
Pin finish		Pure matte tin, whisker resistant chemistry		200		300	
THERMAL							
Operating baseplate (case) temperature	T_C	Any operating condition	C Grade	-20		100	°C
			T Grade	-40			
			M Grade	-55			
Thermal resistance, baseplate to sink, flat greased surface					0.22		°C/W
Thermal resistance, baseplate to sink, thermal pad (36964)					0.19		°C/W
Thermal capacity					44.5		Ws/°C
Thermal design		See Section 10.9					
ASSEMBLY							
ESD rating	ESD_{HBM}	Human Body Model, "JEDEC JESD 22-A114C.01"		1000			V
	ESD_{MM}	Machine Model, "JEDEC JESD 22-A115B"		N/A			
	ESD_{CDM}	Charged Device Model, "JEDEC JESD 22-C101D"		400			
SOLDERING							
See application note		Soldering Methods and Procedure for Vicor Power Modules »					
SAFETY & RELIABILITY							
MTBF		Telecordia Issue 2 - Method I Case 1; Ground Benign, Controlled			2.51		MHrs
		MIL-HDBK-217 Plus Parts Count - 25°C ground Benign, Stationary			4.93		MHrs
Agency approvals/standards		cTUVus, UL/cUL, EN, IEC 60950-1					
		CE, Low Voltage Directive; 2006/95/EC					
		CE Marked for Low Voltage Directive and RoHS Recast Directive, as applicable					
EMI/EMC COMPLIANCE							
Harmonics		EN61000-3-2: 2009, Harmonic Current Emisions – Class A					

9.0 PRODUCT OUTLINE DRAWING AND RECOMMENDED PCB FOOTPRINT

9.1 Module Outline

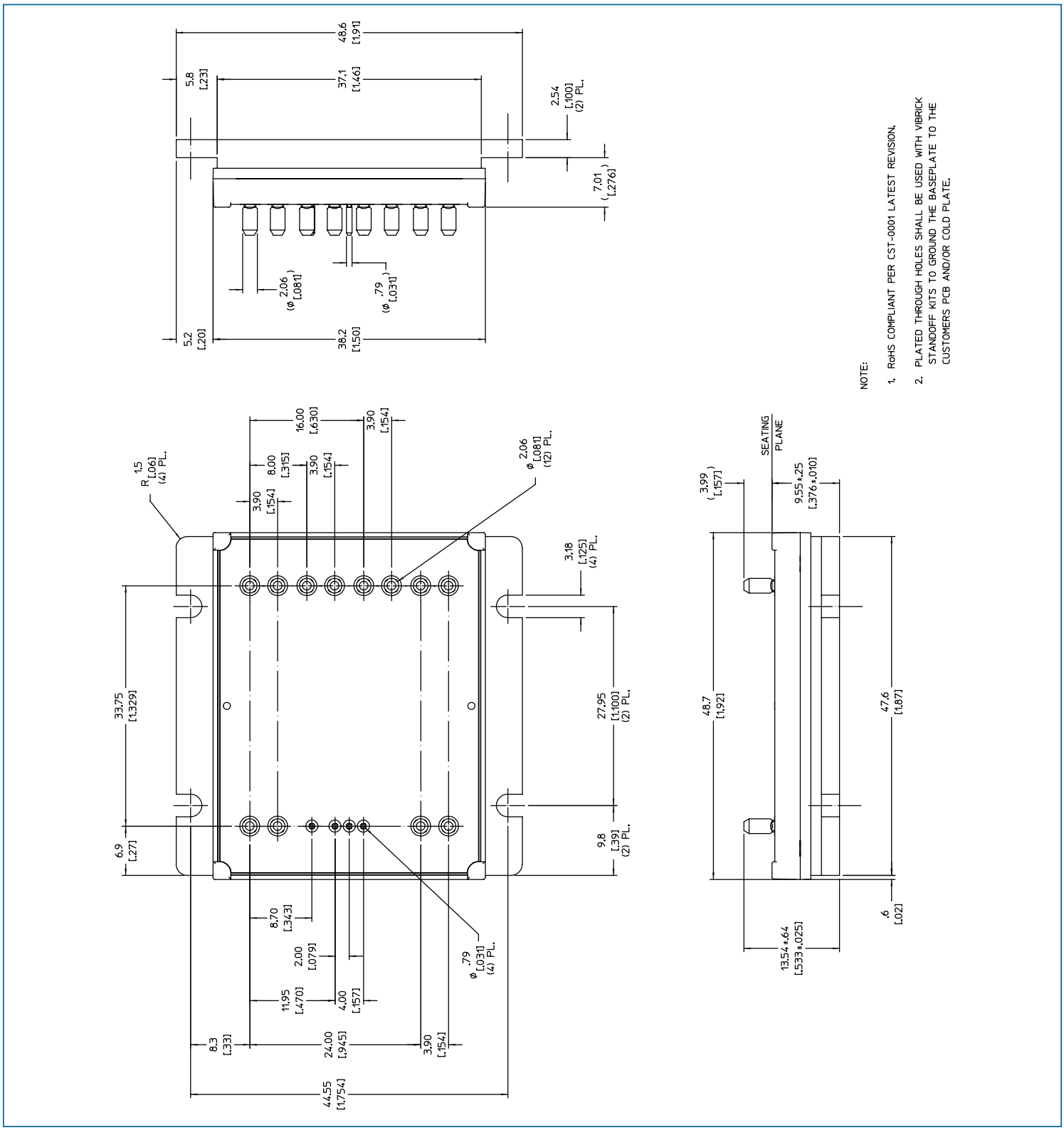


Figure 24 — Product outline drawing;
Product outline drawings are available in .pdf and .dxf formats.
3D mechanical models are available in .pdf and .step formats.
See http://www.vicorpower.com/cms/home/technical_resources/Mechanical_Drawings/Modules for more details.

9.0 PRODUCT OUTLINE DRAWING AND RECOMMENDED PCB FOOTPRINT (CONT.)

9.2 PCB Mounting Specifications

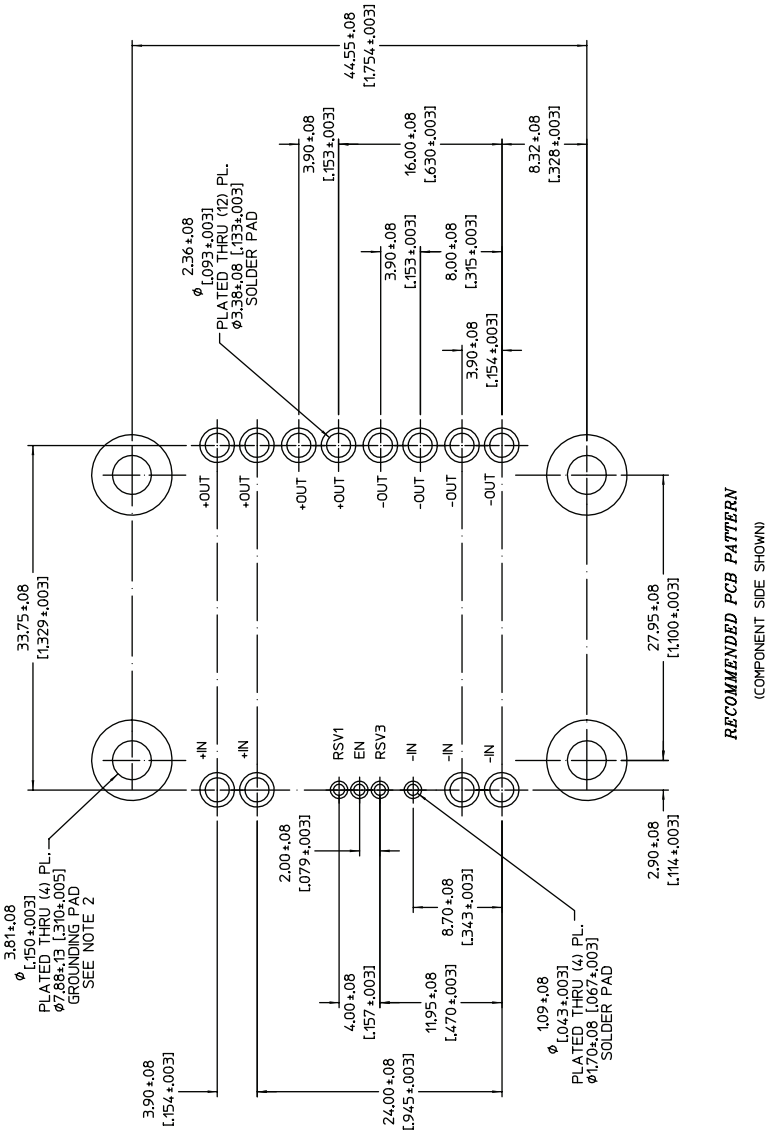


Figure 25 — Recommended PCB pattern;
Product outline drawings are available in .pdf and .dxf formats.
3D mechanical models are available in .pdf and .step formats.
See http://www.vicorpower.com/cms/home/technical_resources/Mechanical_Drawings/Modules for more details.

10.0 PRODUCT DETAILS AND DESIGN GUIDELINES

10.1 Building Blocks and System Designs

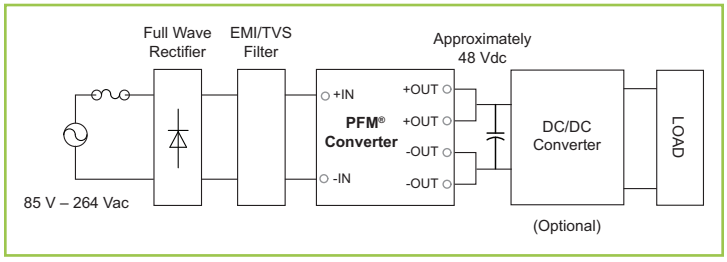


Figure 26 – *300 W Universal AC to DC Supply*

The VI BRICK® PFM® Isolated AC-DC Converter with PFC is a high efficiency AC-to-DC converter, operating from a rectified universal AC input to generate an isolated SELV 48 VDC output bus with power factor correction. It is a component of an AC to DC power supply system such as the one shown in Figure 26 above.

The input to the PFM converter is a rectified, sinusoidal AC source with a power factor maintained by the converter with harmonics conforming to IEC 61000-3-2. Upstream filtering enables compliance with the standards relevant to the application (Surge, EMI, etc.).

The PFM converter uses secondary-side energy storage (at the SELV 48 V bus) and optional PRM™ regulators to maintain output hold up through line dropouts and brownouts. Downstream regulators also provide tighter voltage regulation, if required.

The PF175B480C033FP-00 is designed for standalone operation; however, it may be part of a system that is paralleled by downstream DC/DC converters. Please contact Vicor Sales or refer to our website, www.vicorpower.com, for higher power applications.

10.1.1 Traditional PFC Topology

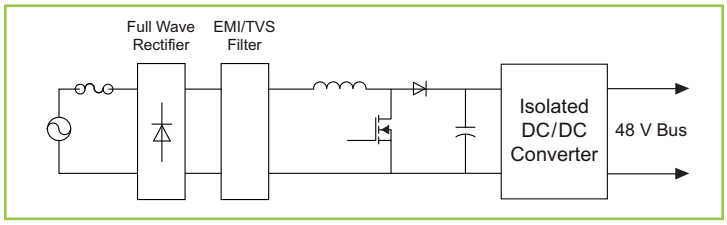


Figure 27 – *Traditional PFC AC to DC supply*

To cope with input voltages across worldwide AC mains (85-264 Vac), traditional AC-DC power supplies (Figure 27) use 2 power conversion stages: 1) a PFC boost stage to step up from a rectified input as low as 85 Vac to ~380 Vdc; and 2) a DC-DC down converter from 380 Vdc to a 48 V bus. The efficiency of the boost stage and of traditional power supplies is significantly compromised operating from worldwide AC lines as low as 85 Vac.

10.1.2 Adaptive Cell™ Topology

With its single stage Adaptive Cell™ topology, the PFM converter enables consistently high efficiency conversion from worldwide AC mains to a 48 V bus and efficient secondary-side power distribution.

10.2 Power Factor Correction

The converter provides power factor correction over worldwide AC mains. Power factor correction is disabled in low power mode to improve efficiency. It is disabled in transient mode to allow quicker recovery upon input transients. Load transients that approach the line frequency should be filtered or avoided as these may reduce PFC.

10.3 Small Signal Characteristics

Figure 28 shows the small signal model of the converter. Because of its internal feedback loop and PFC modulation, within its regulation bandwidth (dynamic response shown in figure 10) the converter's output can be effectively modeled with two sources in series and a passive filter:

- A constant, 49 Vdc voltage generator.
- A dependent voltage source, V_{RIPPLE}, which outputs a variable amplitude sinewave at a frequency twice the input line.
- A first order filter, R_{OUT} C_{OUT_INT}.

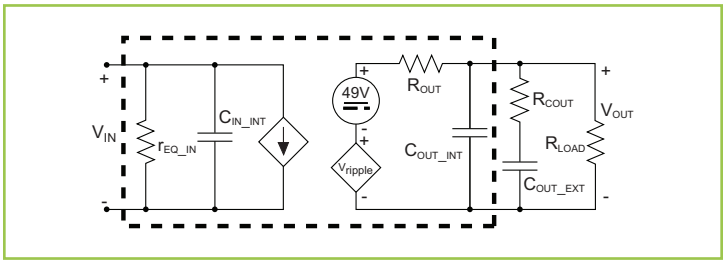


Figure 28 – *PF175B480C033FP-00 AC small signal model*

Output voltage stability is guaranteed as long as hold up capacitance C_{OUT} and load fall within the specified ranges. Input line stability needs to be verified at system design level. Magnitude of the dynamic input impedance r_{EQ_IN} is provided in Figure 22. The input line impedance can be modeled as a series $R_{LINE}L_{LINE}$ circuit. Ceramic decoupling capacitors will not significantly damp the network because of their low ESR; therefore in order to guarantee stability the following conditions must be verified:

$$R_{LINE} > \frac{L_{LINE}}{(C_{IN\_INT} + C_{IN\_EXT}) \cdot |r_{EQ\_IN}|} \quad (1)$$

$$R_{LINE} << |r_{EQ\_IN}| \quad (2)$$

It is critical that the line source resistance be at least an octave lower than the converter's dynamic input impedance, (2). However, R_{LINE} cannot be made arbitrarily low otherwise equation (1) is violated and the system will show instability, due to under-damped RLC input network.

10.0 PRODUCT DETAILS AND DESIGN GUIDELINES (CONT.)

10.4 Input Fuse Selection

VI BRICK® products are not internally fused in order to provide flexibility in configuring power systems. Input line fusing is recommended at system level, in order to provide thermal protection in case of catastrophic failure. The fuse shall be selected by closely matching system requirements with the following characteristics:

- Current rating
  (usually greater than the VI BRICK® PFM® converter's maximum current)
- Maximum voltage rating
  (usually greater than the maximum possible input voltage)
- Ambient temperature
- Breaking capacity per application requirements
- Nominal melting I^2t
- Recommended fuse: ≤ 5 A, 216 Series Littelfuse

10.5 Fault Handling

10.5.1 Input Undervoltage (UV) Fault Protection

The converter's input voltage (proportional to V_{IN-B} as shown in Figure 3) is monitored by the micro-controller to detect an input under voltage condition. When the input voltage is less than the $V_{IN-UVLO-}$, a fault is detected, the fault latch and reset logic disables the modulator, the modulator stops powertrain switching, and the output voltage of the unit falls. After a time t_{UVLO}, the unit shuts down. Faults lasting less than t_{UVLO} may not be detected. Such a fault does not go through an auto-restart cycle. Once the input voltage rises above $V_{IN-UVLO+}$, the unit recovers from the input UV fault, the powertrain resumes normal switching after a time t_{ON} and the output voltage of the unit reaches the set point voltage within a time t_{SS}.

10.5.2 Input Overvoltage (OV) Fault Protection

The input voltage (proportional to V_{IN-B}, as shown in Figure 3) is monitored by the micro-controller to detect an input over voltage condition. When the input voltage is more than the $V_{IN-OVLO-}$, a fault is detected, the reset logic disables the modulator, the modulator stops powertrain switching, and the output voltage of the converter falls. After a time t_{POVP}, the converter shuts down. Faults lasting less than t_{POVP} may not be detected. Such a fault does not go through an auto-restart cycle. Once the input voltage falls below $V_{IN-OVLO-}$, the unit recovers from the input OV fault, the powertrain resumes normal switching after a time t_{ON} and the output voltage reaches the set point voltage within a time t_{SS}.

10.5.3 Overcurrent (OC) Fault Protection

The unit's output current, determined by V_{EAO}, V_{IN-B} and the primary-side sensed output voltage, (as shown in Figure 3) is monitored by the microcontroller to detect an output OC condition. If the output current exceeds its current limit, a fault is detected, the reset logic disables the modulator, the modulator stops powertrain switching, and the output voltage of the converter falls after a time t_{OC}. As long as the fault persists, the converter goes through an auto-restart cycle with off time equal to t_{OFF} + t_{ON} and on time equal to t_{OC}. Faults shorter than a time t_{OC} may not be detected. Once the fault is cleared, the converter follows its normal start up sequence after a time t_{OFF}.

10.5.4 Short Circuit (SC) Fault Protection

The microcontroller determines a short circuit on the output of the unit by measuring its primary sensed output voltage and V_{EAO} (shown in Figure 3). Most commonly, a drop in the primary-sensed output voltage triggers a short circuit event. The converter responds to a short circuit event within a time t_{SC}. The converter then goes through an auto restart cycle, with an off time equal to t_{OFF} + t_{ON} and an on time equal to t_{SC}, for as long as the short circuit fault condition persists. Once the fault is cleared, the unit follows its normal start up sequence after a time t_{OFF}. Faults shorter than a time t_{SC} may not be detected.

10.5.5 Temperature Fault Protection

The microcontroller monitors the temperature within the converter. If this temperature exceeds T_{J-OTP+}, an over temperature fault is detected, the reset logic block disables the modulator, the modulator stops the powertrain switching and the output voltage of the PFM converter falls. Once the case temperature falls below $T_{CASE-OTP-}$, after a time greater than or equal to t_{OFF}, the converter recovers and undergoes a normal restart. Faults shorter than a time t_{OTP} may not be detected. If the temperature falls below $T_{CASE-UTP-}$, an under temperature fault is detected, the reset logic disables the modulator, the modulator stops powertrain switching and the output voltage of the unit falls. Once the case temperature rises above $T_{CASE-UTP}$, after a time greater than or equal to t_{OFF}, the unit recovers and undergoes a normal restart.

10.5.6 Output Overvoltage Protection (OVP)

The microcontroller monitors the primary sensed output voltage (as shown in Figure 3) to detect output OVP. If the primary sensed output voltage exceeds $V_{OUT-OVLO+}$, a fault is latched, the logic disables the modulator, the modulator stops powertrain switching, and the output voltage of the converter falls after a time t_{SOVP}.Faults shorter than a time t_{SOVP} may not be detected. This type of fault is a latched fault and requires that 1) the EN pin be toggled or 2) the input power be recycled in to recover from the fault.

10.0 PRODUCT DETAILS AND DESIGN GUIDELINES (CONT.)

10.6 Hold up Capacitance

The VI BRICK® PFM® converter uses secondary-side energy storage (at the SELV 48 V bus) and optional PRM® regulators to maintain output hold up through line dropouts and brownouts. The PFM converter's output bulk capacitance can be sized to achieve the required hold up functionality.

Hold up time depends upon the output power drawn from the PFM converter based AC-to-DC front-end and the input voltage range of downstream DC-to-DC converters.

The following formula can be used to calculate hold up capacitance for a system comprised of PFM converter based AC front-end and a PRM regulator:

$$C = 2*P_{OUT}*(0.005+t_d)/(V_2^2 - V_1^2) \quad (3)$$

where:

C	PFM converter's output bulk capacitance in farads
t_d	Hold up time in seconds
P_{OUT}	PFM converter's output power in watts
V_2	Output voltage of PFM™ converter in volts
V_1	PRM regulator undervoltage turn off (volts)
	–OR–
	$P_{OUT}/I_{OUT\text{-}PK}$, whichever is greater.

10.7 Output Filtering

The converter requires an output bulk capacitor in the range of 6000 µF to 12000 µF for proper operation of the PFC front-end.

The output voltage has the following two components of voltage ripple:

1) Line frequency voltage ripple: $2*f_{LINE}$ Hz component

2) Switching frequency voltage ripple: 1 MHz converter switching frequency component

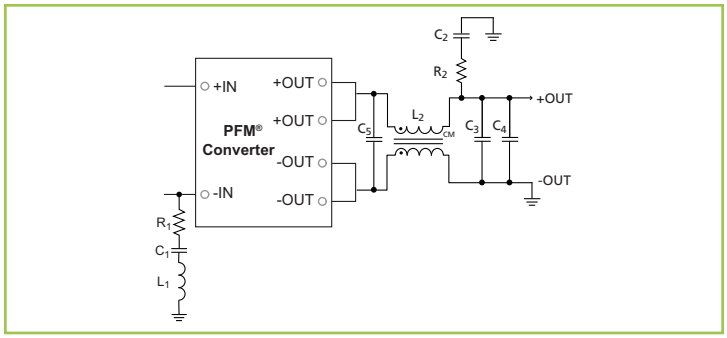


Figure 29 – *Typical filter schematic (positive output)*

Where, in the schematic:

C1	2.2nF (Murata GA355DR7GF222KW01L)
C2	4.7nF (Murata GA355DR7GF472KW01L)
C3	3.3µF (TDK C4532X7R1H335MT)
C4	6800uF 63V (Panasonic UVR1J682MRD)
C5	100uF 63V (Nichicon UVY1J101MPD)
F1	5A, 216 Series Littlefuse
L1	15µH (TDK MLF2012C150KT, Vicor PN 37052-601)
L2	600µH (Vicor 37052-601)
R1	6.8Ω
R2	2.2Ω

10.7.1 Line Frequency Filtering

Output line frequency ripple depends upon output bulk capacitance. Output bulk capacitor values should be calculated based on line frequency voltage ripple. High-grade electrolytic capacitors with adequate ripple current ratings, low ESR and a minimum voltage rating of 63 V are recommended.

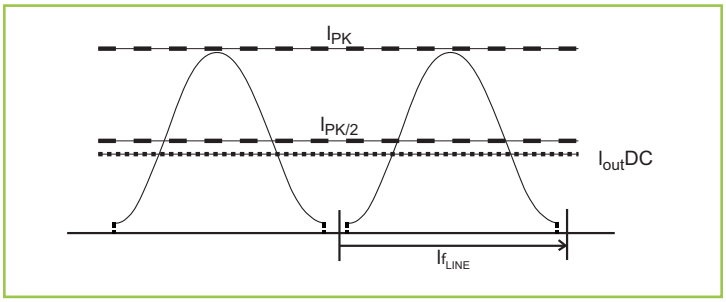


Figure 30 – *Output current waveform*

Based on the output current waveform, as seen in Figure 30, the following formula can be used to determine peak-to-peak line frequency output voltage ripple:

$$V_{PP1} \cong 0.2 * P_{OUT}/(V_{OUT} * f_{LINE} * C) \quad (4)$$

where:

V_{PP1}	Output voltage ripple Peak-to-peak line frequency
P_{OUT}	Average output power
V_{OUT}	Output voltage set point, nominally 48 V
f_{LINE}	Frequency of line voltage
C	Output bulk capacitance
I_{DC}	Maximum average output current
I_{PK}	Peak-to-peak line frequency output current ripple

10.0 PRODUCT DETAILS AND DESIGN GUIDELINES (CONT.)

In certain applications, the choice of bulk capacitance may be determined by hold up requirements and low frequency output voltage filtering requirements. Such applications may use the greater capacitance value determined from these requirements. The ripple current rating for the bulk capacitors can be determined from the following equation:

$$I_{ripple} \cong 0.8 * P_{OUT}/V_{OUT} \quad (5)$$

10.7.2 Switching Frequency Filtering

Output switching frequency voltage ripple is the function of the output bypass ceramic capacitor. Output bypass ceramic capacitor values should be calculated based on switching frequency voltage ripple. Normally bypass capacitors with low ESR are used with a sufficient voltage rating.

Output bypass ceramic capacitor value for allowable peak-to-peak switching frequency voltage ripple can be determined by:

$$C_3 = Q_{TOT} / V_{OUT\text{-}PP\text{-}HF} - C_{OUT\text{-}INT} \quad (6)$$

where:

$V_{OUT\text{-}PP\text{-}HF}$	Allowable peak to peak output switching frequency voltage ripple in volts
Q_{TOT}	The total output charge per switching cycle at full load, maximum 13.5 µC
C_{OUT_INT}	The module internal effective capacitance
C_3	Required output bypass ceramic capacitor

10.8 EMI Filtering and Transient Voltage Suppression

10.8.1 EMI Filtering

The PFM® Isolated AC-DC Converter with PFC is designed such that it will comply with EN 55022 Class B with moderate upstream filtering and output to earth Y-capacitance. If one of the outputs is connected to earth ground, an additional small output common mode choke is also required.

In such a situation, the output switching ripple shown in figure 8 should be expected at the output of the filter. In cases where other means are used to control radiated emissions, and more ripple can be tolerated, the output filter can be simplified by removal of the common mode inductor, and C5, which is used to reduce the Q of the LC resonant tank.

The emissions spectrum without input filtering is shown in Figure 15 in Section 7.0.

10.8.2 Transient Voltage Suppression

In order to comply with line transient specifications such as those for surge (i.e. EN 61000-4-5) and fast transient (i.e. EN 61000-4-4 fast transient/"burst"), an upstream transient voltage suppression circuit is needed. Consult factory for more information.

10.9 Thermal Design

Thermal management of internally dissipated heat should maximize heat removed from the baseplate surface, since the baseplate represents the lowest aggregate thermal impedance to internal components. The baseplate temperature should be maintained below 100°C. Cooling of the system PCB should be provided to keep the leads below 100°C, and to control maximum PCB temperatures in the area of the converter.

10.10 Powering a Constant Power Load

When the output voltage of the PFM converter is applied to the input of the PRM® regulator, the regulator turns on and acts as a constant-power load. When the PFM converter's output voltage reaches the input undervoltage turn on of the regulator, the regulator will attempt to start. However, the current demand of the PRM regulator at the undervoltage turn on point and the hold up capacitor charging current may force the PFM converter into current limit. In this case, the unit may shut down and restart repeatedly. In order to prevent this multiple restart scenario, it is necessary to delay enabling a constant-power load when powered up by the PFM converter based upstream AC to 48 V frontend until after the output set point of the PFM converter is reached.

This can be achieved by

1) keeping the downstream constant-power load off during power up sequence

and

2) turning the downstream constant-power load on after the output voltage of the converter reaches 48 V steady state.

After the initial startup, the output of the PFM converter can be allowed to fall to 30 V during a line dropout at full load. In this case, the circuit should not disable the PRM regulator if the input voltage falls after it is turned on; therefore, some form of hysteresis or latching is needed on the enable signal for the constant power load. The output capacitance of the PFM converter should also be sized appropriately for a constant power load to prevent collapse of the output voltage of the PFM converter during line dropout (see Section 10.6, Hold up Capacitance). A constant-power load can be turned off after completion of the required hold up time during the power-down sequence or can be allowed to turn off when it reaches its own undervoltage shutdown point.

The timing diagram in Figure 31 shows the output voltage of the PFM converter and the PC pin voltage and output voltage of the PRM regulator for the power up and power down sequence. It is recommended to keep the time delay approximately 10 to 20 ms.

10.0 PRODUCT DETAILS AND DESIGN GUIDELINES (CONT.)

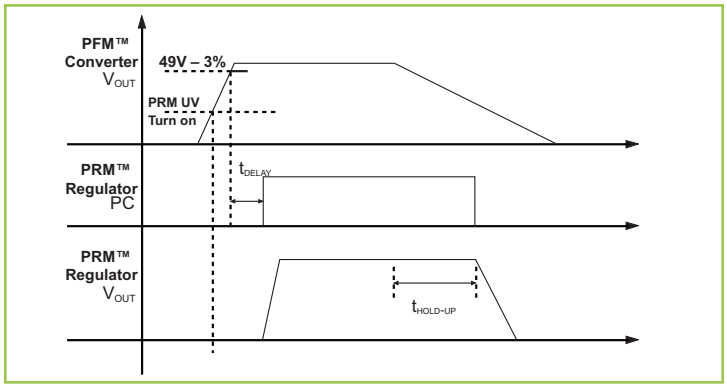


Figure 31 – *PRM® Enable Hold off Waveforms*

Special care should be taken when enabling the constant-power load near the auto-ranger threshold, especially with an inductive source upstream of the PFM® converter. A load current spike may cause a large input voltage transient, resulting in a range change which could temporarily reduce the available power (see Section 10.11, Adaptive Cell™ Topology).

10.11 Adaptive Cell™ Topology

The Adaptive Cell topology utilizes magnetically coupled "top" and "bottom" primary cells that are adaptively configured in series or parallel by a configuration controller comprised of an array of switches. A microcontroller monitors operating conditions and defines the configuration of the top and bottom cells through a range control signal.

A comparator inside the microcontroller monitors the line voltage and compares it to an internal voltage reference. If the input voltage of the PFM converter crosses above the positive going cell reconfiguration threshold voltage, the output of the comparator transitions, causing switches S_1 and S_2 to open and switch S_3 to close (see Figure 3). With the top cell and bottom cell configured in series, the unit operates in "high" range and input capacitances C_{IN-T} and C_{IN-B} are in series.

If the peak of input voltage of the unit falls below the negative-going range threshold voltage for two line cycles, the cell configuration controller opens switch S_3 and closes switches S_1 and S_2. With the top cell and bottom cells configured in parallel, the unit operates in "low" range and input capacitances C_{IN-T} and C_{IN-B} are in parallel.

Power processing is held off while transitioning between ranges and the output voltage of the unit may temporarily droop. External output hold up capacitance should be sized to support power delivery to the load during cell reconfiguration. The minimum specified external output capacitance of 6000 µF is sufficient to provide adequate ride-through during cell reconfiguration for typical applications.

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