- **Drive Capability and Output Counts**
  - **80 mA (Current Sink) x 16 Bits**
  - **120 mA (Current Sink) x 8 Bits**
- **Constant Current Output Range**
  - **5 to 80 mA/10 to 120mA (Selectable by MODE Terminal) (Current Value Setting for All Output Terminals Using External Resistor and Internal Brightness Control Register)**
- **Constant Current Accuracy**
  - **±4% (Maximum Error Between Bits)**
- **Voltage Applied to Constant Current Output Terminals**
  - **Minimum 0.4 V (Output Current 5 mA to 40 mA)**
  - **Minimum 0.7 V (Output Current 40 to 80 mA)**
- **256 Gray Scale Display**
  - **Pulse Width Control 256 Steps**
- **Brightness Adjustment**
  - **Output Current Adjustment for 32 Steps (Adjustment for Brightness Deviation Between LED Modules)**
  - **8 Steps Brightness Control by 8 Times Speed Gray Scale Control Clock (Brightness Adjustment for Panel)**
- **Error Output Signal Check**
  - **Check Error Output Signal Line Such as Protection Circuit When Operating**
- **Data Output Timing Selectable**
  - **Select Data Output Timing for Shift Register Relative to Clock**
- **OVM (Output Voltage Monitor)**
  - **Monitor Voltage on Constant Current Output Terminals (Detect LED Disconnection and Short Circuit)**
- **WDT (Watchdog Timer)**
  - **Turn Output Off When Scan Signal Stopped**
- **TSD (Thermal ShutDown)**
  - **Turn Output Off When Junction Temperature Exceeds Limit**
- **Data Input**
  - **Clock Synchronized 8 Bit Parallel Input (Schmitt-Triggered Input)**
- **Data Output**
  - **Clock Synchronized 8 Bit Parallel Output (3-State Output)**
- **Input Signal Level . . . CMOS Level**
- **Power Supply Voltage . . . 4.5 V to 5.5 V**
- **Maximum Output Voltage . . . 17 V (Max)**
- **Data Transfer Rate . . . 15 MHz (Max)**
- **Gray Scale Clock Frequency 8 MHz (Max)**
- **Operating Free-Air Temperature Range –20°C to 85°C**
- **100-Pin HTQFP Package (P_D=4.7 W, T_A = 25°C)**

description

The TLC5904 is a constant current driver incorporating shift register, data latch, and constant current circuitry with current value adjustable and a 256 gray scale display using pulse width control. The output current can be selected as maximum 80 mA with 16 bits or 120 mA with 8 bits, and the current value of constant current output can be set by one external resistor. After this device is mounted on a PCB, the brightness deviation between LED modules (ICs) can be adjusted by external data input, and the brightness control for the panel can be accomplished by the brightness adjustment circuitry. Also, the device incorporates the output voltage monitor (OVM) used for LED open detection (LOD) by monitoring the constant current output. Moreover, the device incorporates watchdog time (WDT) circuitry, which turns the constant current output off when a scan signal is stopped at the dynamic scanning operation, and thermal shutdown (TSD) circuitry, which turns the constant current output off when the junction temperature exceeds the limit.

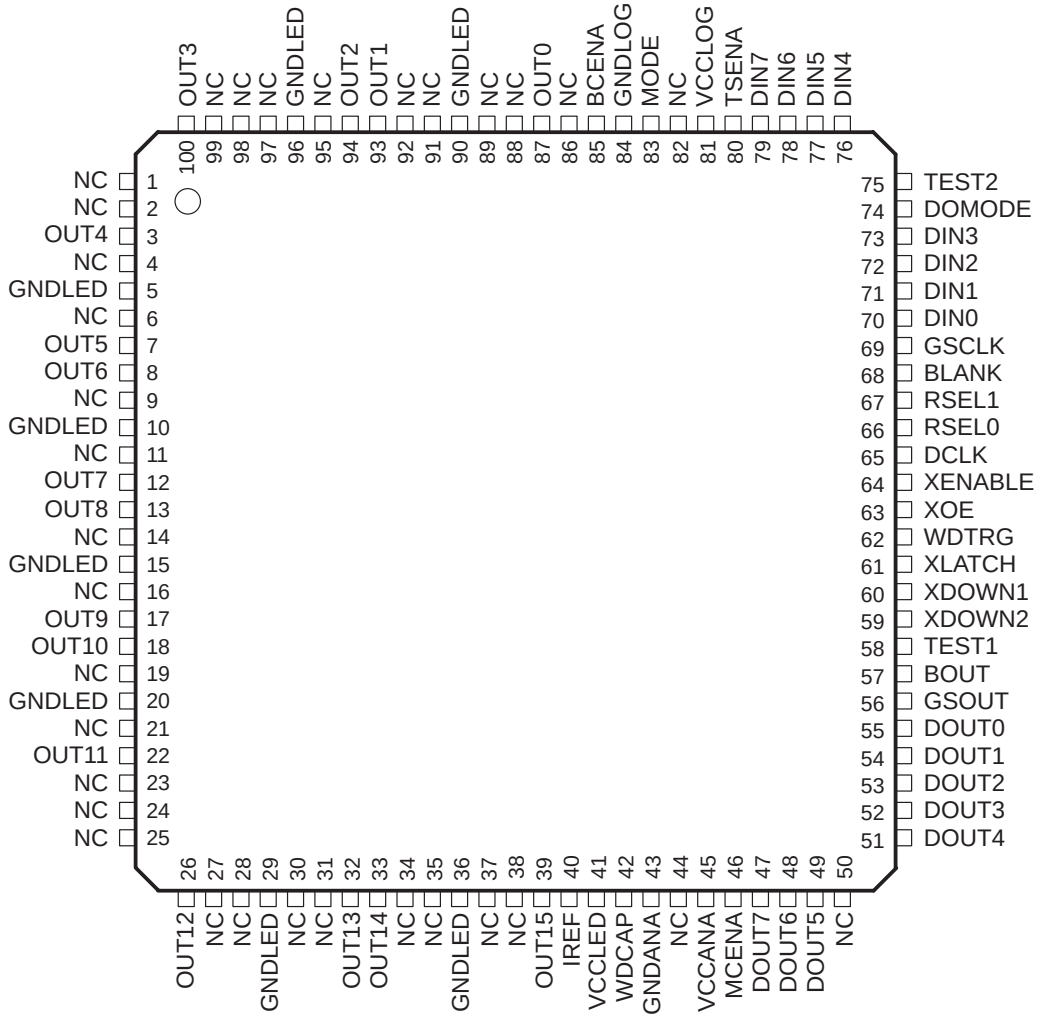


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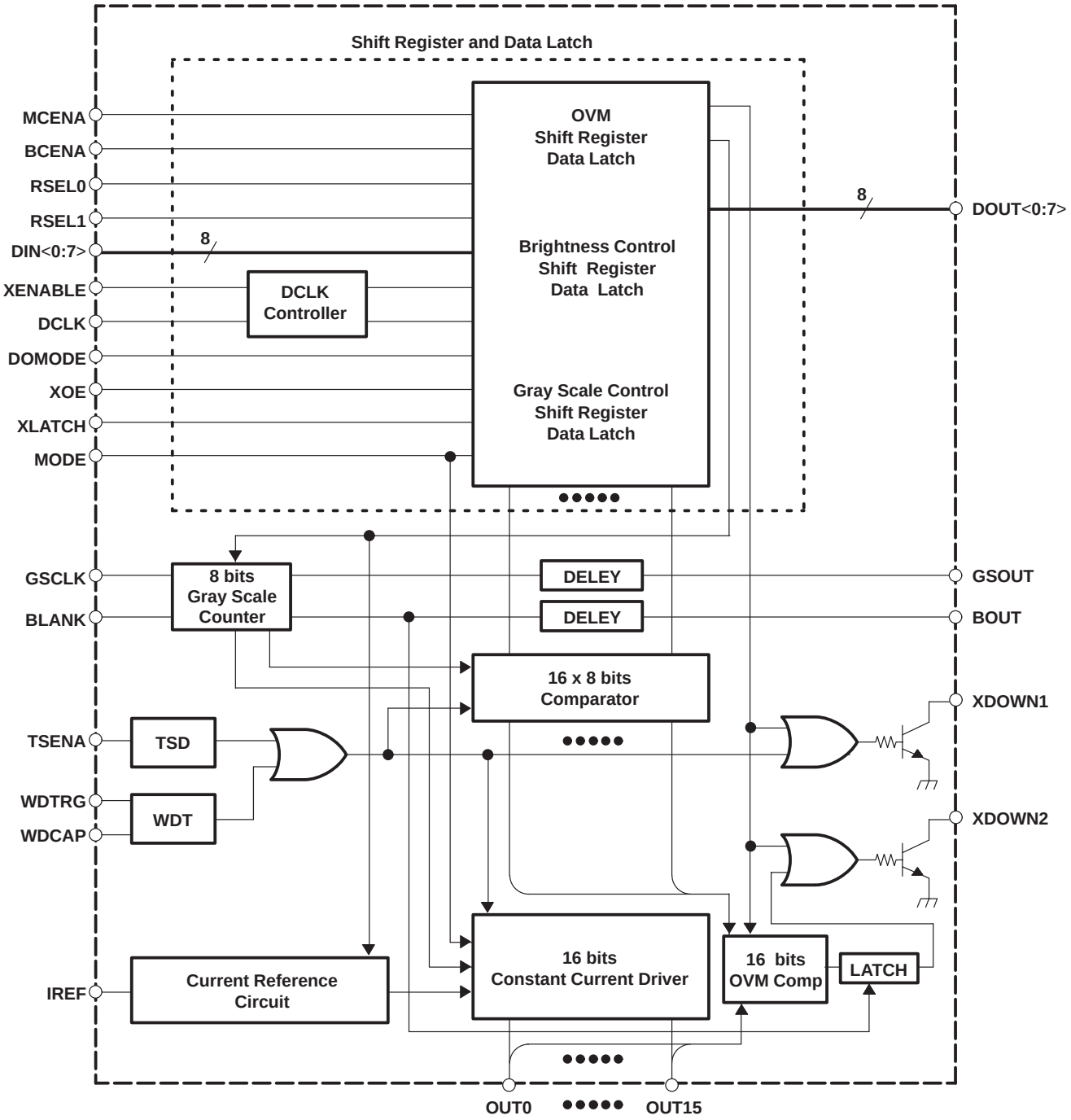
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PZP PACKAGE
(TOP VIEW)

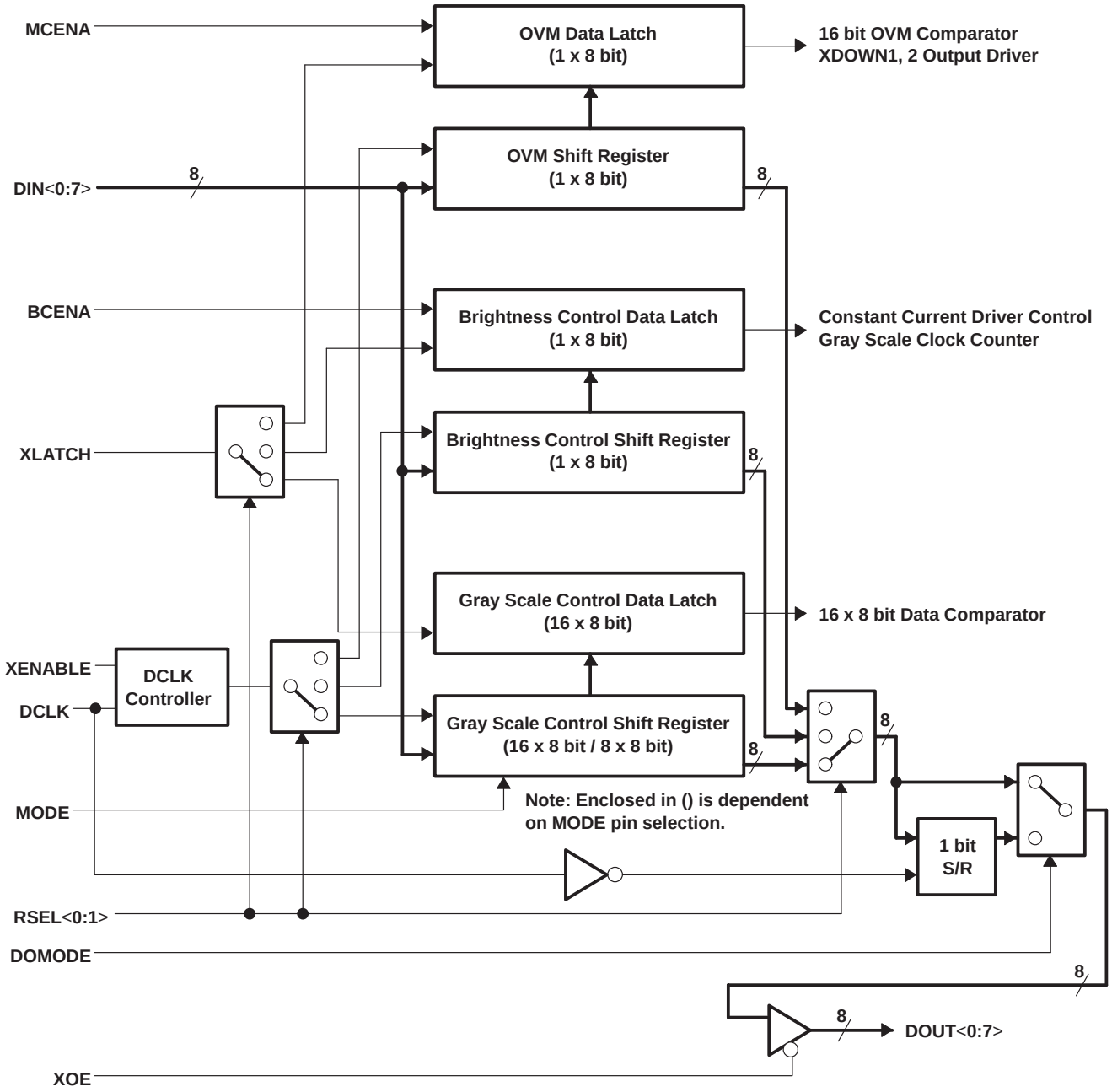


functional block diagram



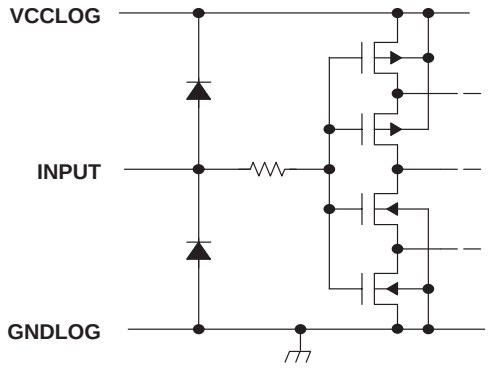
NOTE: All the input terminals are with Schmitt-triggered inverter except IREF and WDCAP.

functional block diagram for shift register and data latch

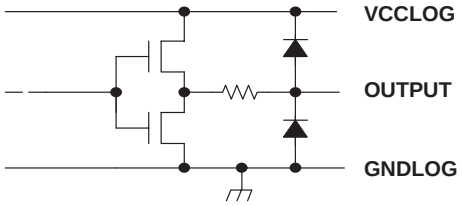


equivalent input and output schematic diagrams

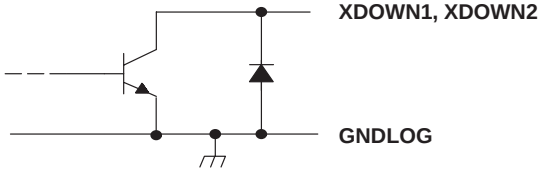
Input



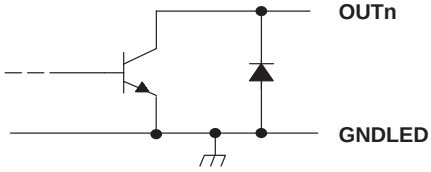
DOUT0–7, GSOUT, BOUT



XDOWN1, XDOWN2



OUTn



Terminal Functions

TERMINAL NAME	TERMINAL NO.	I/O	DESCRIPTION
BCENA	85	I	Brightness control enable. When BCENA is low, the brightness control latch is set to the default value. The output current value in this status is 100% of the setting value by an external resistor. The frequency division ratio of GSCLK is1/1. When BCENA is high, writing to brightness control latch is enabled.
BLANK	68	I	Blank(light off). When BLANK is high, all the output of the constant current driver is turned off. The constant current output, which the gray scale data is not zero, is turned on (LED on) synchronizing to the falling edge of GSCLK after the next rising edge of GSCLK when BLANK goes from high to low.
BOUT	57	O	Blank signal delay. BOUT is the output with addition of delay time to BLANK.
DCLK	65	I	Clock input for data transfer. The input data is from DIN. All data on the shift register is selected by RSEL0 and RSEL1, and output data at DOUT is shifted by 1 bit synchronizing to DCLK. The data except for DOUT is synchronized to the rising edge, and the edge for data from DOUT is determined by the level of DOMODE.
DIN0 – DIN7	70,71,72,73, 76,77,78,79	I	Input for 8 bit parallel data. These terminals are inputs to the shift register for gray scale data, brightness control, and OVM. The register selected is determined by RSEL0, 1.
DOMODE	74	I	Timing select for data output. When DOMODE is low, DOUT0–7 is changed synchronizing to the rising edge of DCLK. When DOMODE is high, DOUT0–7 is changed synchronizing to the falling edge of DCLK.
DOUT0 – DOUT7	55,54,53,52, 51,49,48,47	O	Output for 8 bit parallel data with 3-state. These terminals are outputs to the shift register for gray scale data, brightness control, and OVM. The register selected is determined by RSEL0, 1.
GNDANA	43		Analog ground (internally connected to GNDLOG and GNDLED)
GNDLOG	84		Logic ground (internally connected to GNDANA and GNDLED)
GNDLED	5,10,15,20, 29,36,90,96		LED driver ground (internally connected to GNDANA and GNDLOG)
GSCLK	69	I	Clock input for gray scale. The gray scale display is accomplished by lighting LEDs until the number of GSCLK counted is equal to data latched.
GSOUT	56	O	Clock delay for gray scale. GSOUT is the output with the addition of delay time to GSCLK.
IREF	40	I/O	Constant current value setting. LED current is set to the desired value by connecting an external resistor between IREF and GND. The 37 times current compares current across the external resistor sink on the output terminal.
MCENA	46	I	OVM enable. When MCENA is low, the OVM latch is set to the default value. The comparison voltage in this status is 0.3V. When MCENA is high, writing to the OVM latch is enabled.
MODE	83	I	8/16 bits select. When MODE is high, 16 bits output is selected. When MODE is low, 8 bits output is selected.
NC	1,2,4,6,9,11,14,16, 19,21,23,24,25,27, 28,30,31,34,35,37, 38,44,50,82,86,88, 89,91,92,95,97,98, 99		No internal connection
OUT0 – OUT15	87,93,94,100, 3,7,8,12,13, 17,18,22,26, 32,33,39	O	Constant current output
RSEL0 RSEL1	66 67	I	Shift register data latch switching. When RSEL1 is low, gray scale data shift register latch is selected at RSEL0 low, and the brightness control register latch is selected at RSEL0 high. When RSEL1 is high, the OVM register latch is selected at RSEL0 low, and no register latch is selected at RSEL0 high.

Terminal Functions (Continued)

TERMINAL NAME	TERMINAL NO.	I/O	DESCRIPTION
TSENA	80	I	TSD(thermal shutdown) enable. When TSENA is high, TSD is enabled. When TSENA is low, TSD is disabled.
TEST1 TEST2	58 75	I	TEST. Factory test terminal. TEST1 and TEST2 should be connected to GND for normal operation.
THERMAL PAD	package bottom		Heat sink pad. This pad is connected to the lowest potential IC or thermal layer.
VCCANA	45		Analog power supply voltage
VCCLOG	81		Logic power supply voltage
VCCLED	41		LED driver power supply voltage
WDTRG	62	I	WDT (watchdog timer) trigger input. By applying a scan signal to this terminal, the scan signal can be monitored by turning the constant current output off to protect the LED from damage if the scan signal stops during the constant period designed.
WDCAP	42	I	WDT (watchdog timer) detection time adjustment. WDT detection time is adjusted by connecting a capacitor between WDCAP and GND. When WDCAP is directly connected to GND, WDT function is disabled. In this case, WDTRG should be tied to a high or a low level.
XDOWN1	60	O	Shutdown. XDOWN1 is configured as open collector. It goes low when constant current output is shut down by WDT or TSD function.
XDOWN2	59	O	OVM comparator output. XDOWN2 is configured as an open collector. It monitors terminal voltage when constant current output is turned on. XDOWN2 goes low when this voltage is lower than the level selected by OVM latch. When BLANK is set high, the previous level is held.
XENABLE	64	I	DCLK enable. When XENABLE is low, data transfer is enabled. Data transfer starts on the rising edge of DCLK after XENABLE goes low. During XENABLE high, no data is transferred.
XLATCH	61	I	Latch. When XLATCH is high, data on the shift register goes through latch. When XLATCH is low, data is latched. Accordingly, if data on the shift register is changed during XLATCH high, this new value is latched (level latch).
XOE	63	I	Data output enable. When XOE is low, DOUT0–7 terminals are drived. When XOE is high, DOUT0–7 terminals go to a high-impedance state.

absolute maximum ratings (see Note 1)†

Logic supply voltage, VCC(LOG) . . . . . – 0.3 V to 7 V
Supply voltage for constant current circuit, VCC(LED) . . . . . – 0.3 V to 7 V
Analog supply voltage, VCCANA . . . . . – 0.3 V to 7 V
Output current (dc), $I_{O(LC)}$ . . . . . 90 mA
Input voltage range . . . . . – 0.3 V to VCCLOG + 0.3 V
Output voltage range, $V_{O(DOUTn)}$, $V_{O(BOUT)}$ and $V_{O(GSOUT)}$ . . . . . – 0.3 V to VCCLOG + 0.3 V
Output voltage range, $V_{O(OUTn)}$ and $V_{O(DOWNn)}$ . . . . . – 0.3 V to 18 V
Storage temperature range, T_{stg} . . . . . –55°C to 150°C
Continuous total power dissipation at (or below) T_A = 25°C . . . . . 4.7 W
Power dissipation rating at (or above) T_A = 25°C . . . . . 38.2m W/°C

† Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTE 1: All voltage values are with respect to the GNDLOG terminal.

recommended operating conditions

dc characteristics

PARAMETER	TEST CONDITIONS	MIN	NOM	MAX	UNIT
Logic supply voltage, VCCLOG		4.5	5	5.5	V
Supply voltage for constant current circuit, VCCLED		4.5	5	5.5	V
Analog power supply, VCCANA		4.5	5	5.5	V
Voltage between VCC, V_{DIFF1}	V_{DIFF1} = VCCLOG – VCCANA VCCLOG – VCCLED, VCCANA – VCCLED	– 0.3	0	0.3	V
Voltage between GND, V_{DIFF2}	V_{DIFF2} = GNDLOG – GNDANA GNDLOG – GNDLED, GNDANA – GNDLED	– 0.3	0	0.3	V
Voltage applied to constant current output, V_{OUTn}	OUT0 to OUT15 off			17	V
High-level input voltage, V_{IH}		0.8 VCCLOG		VCCLOG	V
Low-level input voltage, V_{IL}		GNDLOG		0.2 VCCLOG	V
High-level output current, I_{OH}	VCCLOG = 4.5V, DOUT0 to DOUT7, BOUT, GSOUT			– 1	mA
Low-level output current, I_{OL}	VCCLOG = 4.5V, DOUT0 to DOUT7, BOUT, GSOUT			1	mA
	VCCLOG = 4.5V, XDOWN1, XDOWN2			5	mA
Constant output current, $I_{O(LC)}$	OUT0 to OUT15	5		80	mA
Operating free-air temperature range, T_A		– 20		85	°C

ac characteristics, VCCLOG = VCCANA = VCCLED = 4.5 V to 5.5 V, T_A = – 20 to 85°C (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
f_{DCLK}	DCLK clock frequency	At single operation			15	MHz
		At cascade operation (DOMODE = L)			10	
t_{wh}/t_{wl}	DCLK pulse duration (high or low level)		20			ns
f_{GSCLK}	GSCLK clock frequency	Frequency division ratio 1/1			8	MHz
t_{wh}/t_{wl}	GSCLK pulse duration (high or low level)		40			ns
f_{WDT}	WDTRG clock frequency				8	MHz
t_{wh}/t_{wl}	WDTRG pulse duration (high or low level)		40			ns
t_{wh}	XLATCH pulse duration (high)		50			ns
t_r/t_f	Rise/fall time				100	ns
t_{su}	Setup time	DINn – DCLK	10			ns
		BLANK – GSCLK	20			
		XENABLE – DCLK	15			
		XLATCH – DCLK	15			
		XLATCH – GSCLK	15			
		RSEL – DCLK↑	10			
		RSEL – XLATCH	20			
t_h	Hold time	DINn – DCLK	15			ns
		XENABLE – DCLK	20			
		XLATCH – DCLK	30			
		RSEL – DCLK↓	20			
		RSEL – XLATCH	20			

electrical characteristics,
MIN/MAX: VCCLOG= VCCANA = VCCLED = 4.5 V to 5.5 V, T_A = – 20 to 85°C
TYP: VCCLOG = VCCANA = VCCLED = 5 V, T_A = 25°C (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
V_{OH}	High-level output voltage	DOUTn, GSOUT, BOUT, I_{OH} = – 1.0mA	VCCLOG – 0.5			V
V_{OL}	Low-level output voltage	DOUTn, GSOUT, BOUT, I_{OL} = 1.0mA,			0.5	V
		XDOWN1, XDOWN2, I_{OL} = 5 mA			0.5	
I_I	Input current	V_{IN} = VCCLOG or GNDLOG			±1	µA
I_{LOG}	Supply current (logic)	Input signal is static,T SENA = H, WDCAP = OPEN			1	mA
		Data transfer,D CLK = 15 MHz, GSCLK = 8 MHz		18	30	mA
I_{ANA}	Supply current (analog)	LED turnon, R_{IREF} = 590 Ω		3	5	mA
		LED turnoff R_{IREF} = 590 Ω		3	5	
I_{LED}	Supply current (constant current driver)	LED turnoff, R_{IREF} = 1180 Ω		15	20	mA
		LED turnoff, R_{IREF} =590 Ω		30	40	
		V_{OUT} = 1 V. R_{IREF} = 1180 Ω All output bits turn on		25	35	
		V_{OUT} = 1, R_{IREF} = 590 Ω All output bits turn on		50	70	
I_{OLC1}	Constant output current (includes error between bits)	V_{OUT} = 1 V, R_{IREF} = 1180 Ω	35	40	45	mA
I_{OLC2}	Constant output current (includes error between bits)	V_{OUT} = 1 V, R_{IREF} = 590 Ω	70	80	90	mA
I_{OLK}	Constant output leakage current	OUT0 to OUT15 (V_{OUTn} = 15 V)			0.1	µA
		XDOWN1,2 (V_{XDOWNn} = 15 V)			1	µA
		DOUTn, (V_{OUTn} = VCCLOG or GND)			1	µA
ΔI_{OLC}	Constant output current error between bit	VCCLOG=VCCANA=VCCLED=5 V, V_{OUT} = 1 V, R_{IREF} = 590 Ω All output bits turn on		±1%	±4%	
$I\Delta_{OLC1}$	Changes in constant output current depend on supply voltage	V_{OUT} = 1 V, R_{IREF} = 1180 Ω, V_{IREF} = 1.24 V, 1 bit output turn on		±1	±4	%/V
$I\Delta_{OLC2}$	Changes in constant output current depend on output voltage	V_{OUT} = 1 V to 3 V, R_{IREF} = 1180 Ω, V_{IREF} = 1.24 V, 1 bit output turn on		±1	±2	%/V
T_{tsd}	TSD detection temperature	Junction temperature	150	160	170	°C
T_{wdt}	WDT detection temperature	No external capacitor	5	10	15	ms
V_{IREF}	Voltage reference	BCENA = L, R_{IREF} = 590 Ω		1.24		V

switching characteristics, C_L = 15pF, MIN/MAX: VCCLOG= VCCANA = VCCLED = 4.5 V to 5.5, T_A = –20 to 85°C TYP: VCCLOG = VCCANA = VCCLED = 5 V, T_A = 25°C (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_r	Rise time	DOUTn		12	30	ns
		GSOUT, BOUT		13	30	
		OUTn (see Figure 1)		250		
t_f	Fall time	DOUTn		8	20	ns
		GSOUT, BOUT		10	25	
		OUTn (see Figure 1)		200		
t_d	Propagation delay time	OUTn+1 – OUTn		35	60	ns
		BLANK↑ – OUT0		350	500	
		BLANK – BOUT	20	40	70	
		GSCLK↓ – OUT0		350	500	
		GSCLK – GSOUT	20	40	70	
		DCLK – DOUTn	15	30	50	
		XOE↓ – DOUTn (see Note 2)	10	20	35	
		XOE↑ – DOUTn (see Note 2)	10	15	25	
		GSCLK – XDOWN2 (Δ0.1 V)			5000	

NOTE 2: Until DOUT will be turned on (drive) or turned off (Hi-Z).

PARAMETER MEASUREMENT INFORMATION

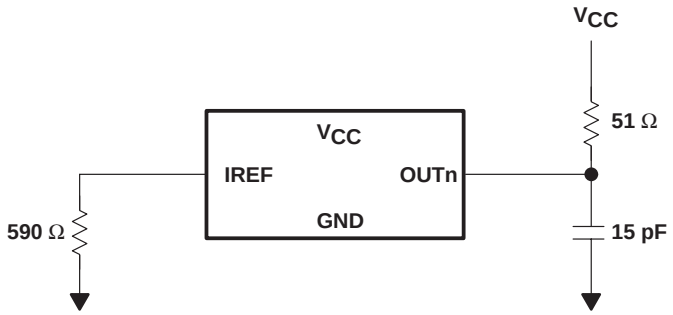


Figure 1. Rise Time and Fall Time Test Circuit for OUTn

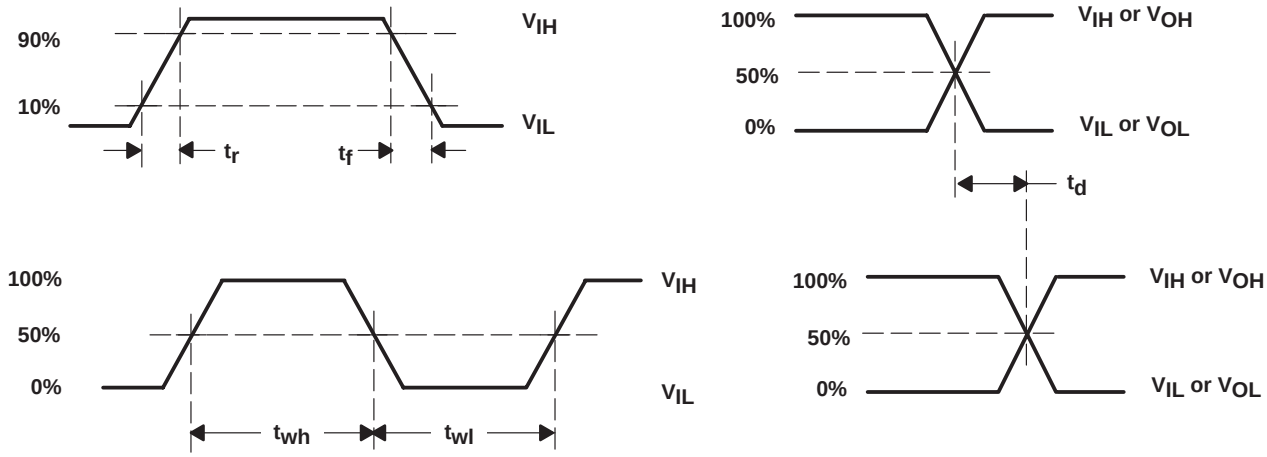


Figure 2. Timing Requirements

PRINCIPLES OF OPERATION

constant current output selection by user (80 mA × 16 bits or 120 mA × 8 bits)

When the MODE terminal is set to high, output is selected as 80 mA × 16 bits. When the MODE terminal is set to low, output is selected as 120 mA × 8 bits. By this setting, the shift register latch for gray scale data is changed to the configuration corresponding to the bit selected. Note that two constant output terminals should be tied to an LED such as OUT0-to-OUT1 and OUT2-to-OUT3 because they operate in a pair when the 8 bits output mode is selected. Also, in this case, the current value of the constant current output is the same as the 16 bits output mode. Therefore, when an output current of 120 mA is desired, the resister connected to the IREF terminal should be selected to the same value as the output current of 60 mA.

Table 1. Operation Mode Selection

MODE	OUTPUT
H	80 mA × 16 bits
L	120 mA × 8 bits

On the constant current output terminals (OUT0–15), approximately 37 times the current which flows through external resistor, R_{IREF} (connected between IREF and GND), can flow. The external resistor value is calculated using the following equation:

$R_{IREF}\ (\Omega) \cong 37 \times 1.24\ (V)/I_{O(LC)}(A)$ where BCENA is low.

Note that more current flows if IREF is connect to GND directly.

constant output current operation

The constant current output turns on the sink constant current if all the gray scale data in the gray scale latch is not zero on the falling edge of the gray scale clock after the next rising edge of the gray scale clock when BLANK goes from high to low. After that, the number of the falling edge is counted by the 8-bit gray scale counter. Then, the output counted corresponding to gray scale data is turned off (stop to sink constant current). If the shift register for gray scale is updated during XLATCH high, data on the gray scale data latch is also updated affecting the constant current output number of the gray scale. Accordingly, during the on-state of constant current output, the XLATCH should be kept to a low level and the gray scale data latch should be held. If there are constant current output terminals unconnected (includes LED disconnection), the LED should be turned on after writing zero to the gray scale data latch corresponding to output unconnected. Unless this action is taken, the supply current on the constant current driver will increase resulting in the influence of the current value for the constant current output light on.

shift register latch

The device provides three kinds of shift register latchs including the gray scale data, brightness control, and OVM. To write data into a shift register, DCLK and DIN are utilized. The selection of a shift register will be done by RSEL0 and RSEL1 as shown in below table. Note that RSEL0 and RSEL1 should be changed when both DCLK and XLATCH are low.

Table 2. Shift Register Latch Selection

RSEL0	RSEL1	SHIFT REGISTER LATCH SELECTED
L	L	Shift register latch for gray scale data
L	H	Shift register latch for brightness control
H	L	Shift register latch for OVM
H	H	N/A (DOUTn is tied to low level)

PRINCIPLES OF OPERATION

shift register latch for gray scale data

The shift register latch for the gray scale data is set as an 8 × 1 byte configuration at the 8 bit mode, and as a 16 × 1 byte configuration at the 16 bit mode. The gray scale data, configured as 8 bits, represents the time when constant current output is being turned on, and the data range is 0 to 255 (00h to FFh). When the gray scale data is 0, the time is shortest, and the output is not turned on(light off). On the other hand, when the gray scale data is 255, the time is longest, and it turns on during the time of the 255 clocks from GSCLK. The configuration of the shift register and latch for gray scale data is shown below.

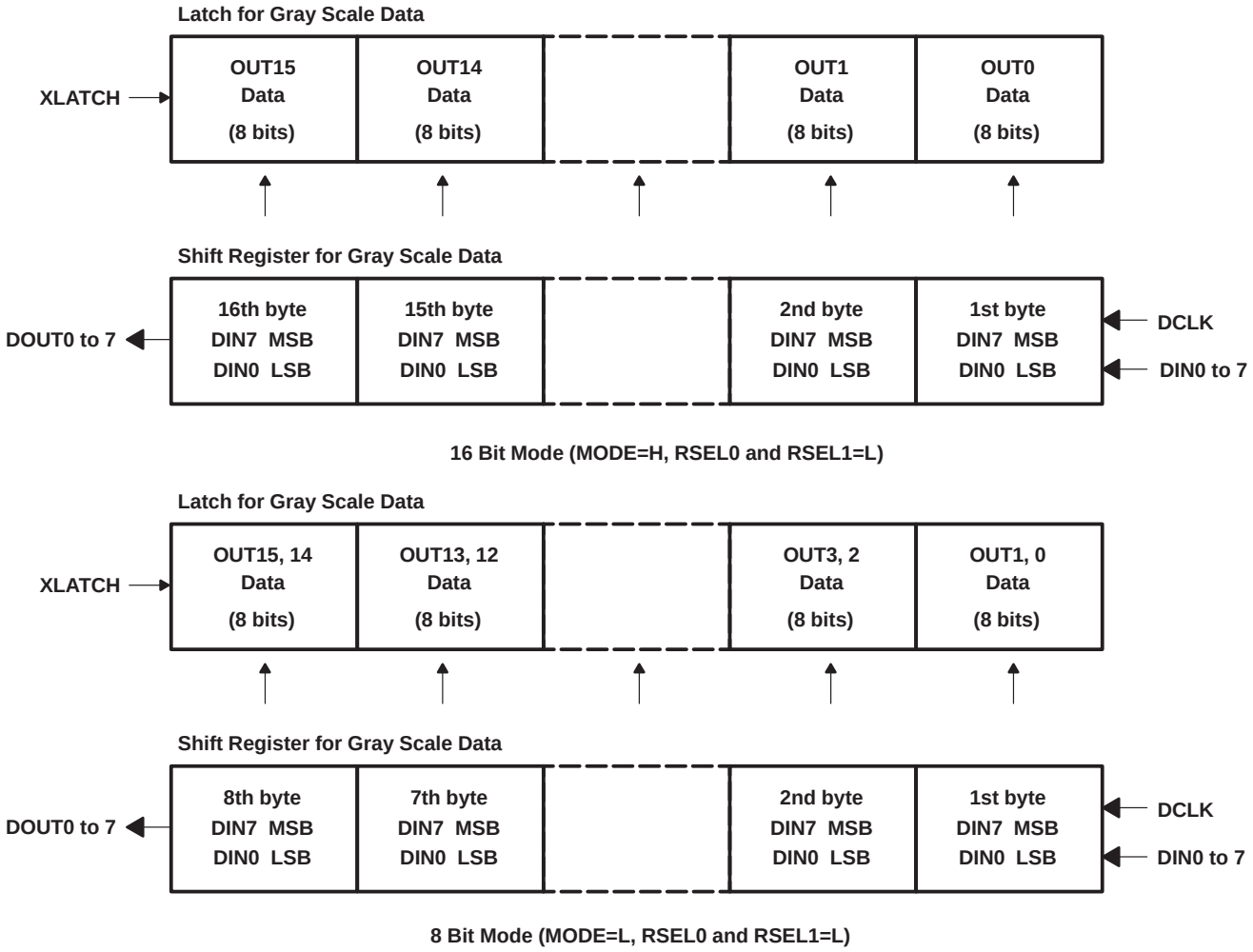
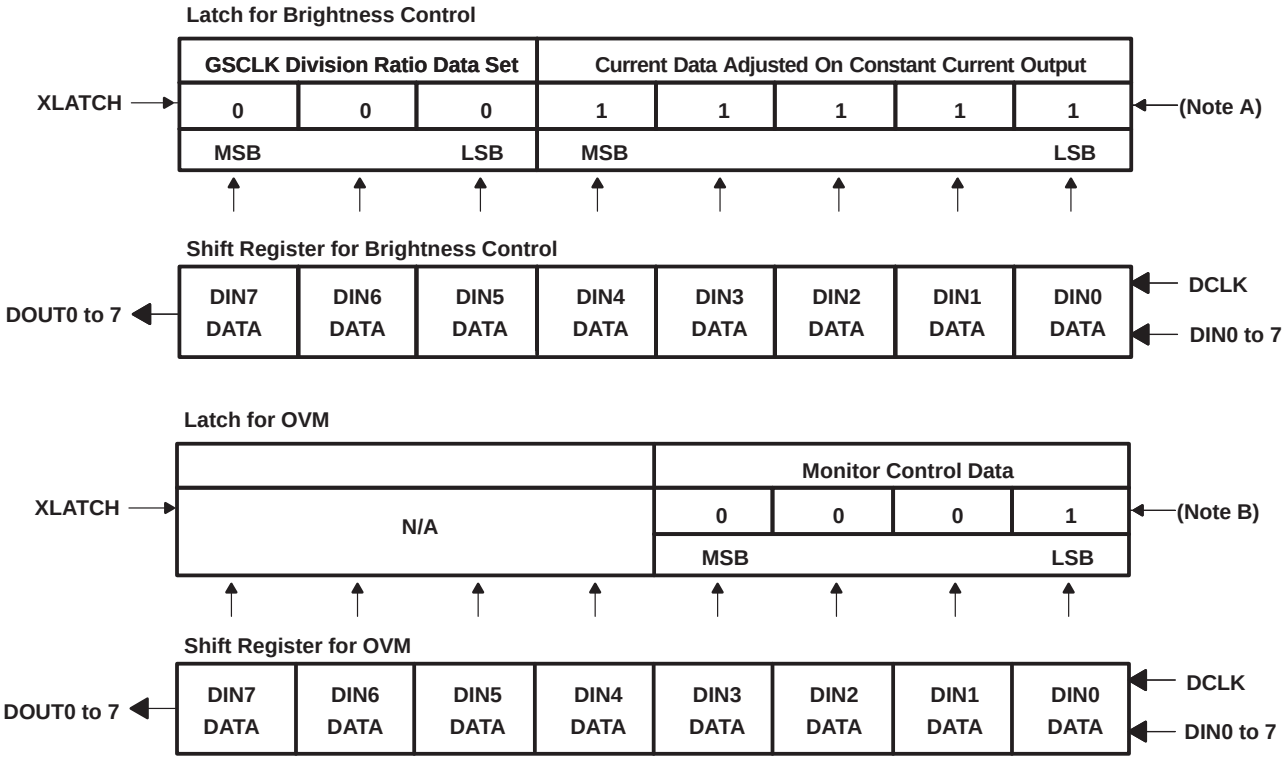


Figure 3. Relationship Between Shift Register and Latch for Gray Scale Data

PRINCIPLES OF OPERATION

shift register latch for brightness control and OVM

The shift register latch for both brightness control and OVM (Output Voltage Monitor) is configured with a 1 x 1 byte. In the shift register latch for brightness control, the division ratio of GSCLK can be set and the output current value on the constant current output can be adjusted. In the shift register latch for OVM, the comparison voltage at OVM comparator on the constant current output terminals (OUT0 to OUT15) can be set and the output signal for both XDOWN1 and XDOWN2 can be forced to low level. When power up, the latch data is indeterminate and the shift register is not initialized. Data should be written to the shift register latch prior to turning the constant current output on (BLANK=L) when these functions are used. Also, it is inhibited to rewrite the latch value for brightness control when the constant current output is turned on. When these functions are not used, the latch value can be set to the default value setting BCENA or MCENA to low level (tied to GND). The configuration of the shift register and the latch for brightness control and monitor control is shown in below.



Note A: Indicates default value at the BCENA terminal = 0 if the brightness control latch = 1
Note B: Indicates default value at the MCENA terminal = 0 if the OVM latch =1

Figure 4. Relationship Between Shift Register and Latch for Brightness Control and OVM

write data to shift register latch

The shift register latch written to is selected using the RSEL0 and RSEL1 terminals. The data is applied to the DIN data input terminal and is clocked into the shift register synchronizing to the rising edge of DCLK after XENABLE is pulled low. The shift register for the gray scale data is 8 bits length at 8 bit mode resulting in eight times DCLK, and 16 bit length at 16 bit mode resulting in sixteen times DCLK, and as for the brigtness control and monitor control resulting one times DCLK input. At the number of DCLK input for each case, data can be written into the shift register. In this condition, when XLATCH is pulled high, data in the shift register is clocked into the latch (data through), and when XLATCH is pulled low, the data is held (latch).

PRINCIPLES OF OPERATION

brightness control function

By writting data into the brightness control latch, the current on all constant current outputs can be adjusted to control the variation of brightness between ICs and the division ratio for the gray scale clock can be set to control the variation of brigtness for the total panel system.

output current adjustment on all constant current outputs – brightness adjustment between ICs

By using the lower 5 bits of the brightness control latch, the output current can be adjusted to 32 steps. 1 step is 1.6% of the current ratio between 100% and 51.6% when the set output current is 100% by an external resistor. By using this function, the brightness control between modules (ICs) can be adjusted sending desired data externally even if ICs are mounted on print-circuit board. When BCENA is pulled low, output current is set to 100%.

Table 3. Relative Current Ratio For Total Constant Current Output

CODE	CURRENT RATIO (%)	20 (mA)	80 (mA)	V_{IREF} (TYP)
MSB 00000 LSB	51.6	10.3	41.3	0.63
. . . .	. . . .	. . . .	. . . .	. . . .
11110	98.4	19.7	78.7	1.22
11111†	100	20.0	80.0	1.24

† BCENA is low.

frequency division ratio setting for gray scale clock – panel brightness adjustment

By using the upper 3 bits of the brightness control latch, the gray scale clock can be divided into a frequency division ratio of 1/1 to 1/8. If the gray scale clock is set to 8 times the speed (256x8=2048) of frequency during horizontal scanning time, the brightness can be adjusted to 8 steps selecting the frequency division ratio. By using this function, the total panel brightness can be adjusted at once, and it applies to the brightness of day or night circumstances. When BCENA is pulled low, the gray scale clock is not divided. When BCENA is pulled high, the brightness can be adjusted (see Table 4).

Table 4. Relative Brightness Ratio For Total Constant Current Output

CODE	FREQUENCY DIVISION RATIO	RELATIVE BRIGHTNESS RATIO (%)
MSB 000 LSB†	1/1	12.5
. . . .	. . . .	. . . .
110	1/7	87.5
111	1/8	100

† BCENA is low.

OVM (output voltage monitor) function

By writing data into the OVM latch, the comparison voltage for the voltage comparator of OUT0 to OUT15 can be set, and the output signal for XDOWN1 and XDOWN2 can be checked.

PRINCIPLES OF OPERATION

OVM comparator

The OVM comparator compares the voltage on the constant current output terminal during turnon with comparison voltage set by the OVM latch. When the voltage on the constant current output terminal is lower, XDOWN2 goes low. As shown in Figure 5, the comparator is provided in every output portion, and the comparison result corresponding to the output to be turned on appears in the XDOWN2 terminal. Since the XDOWN2 terminal is an open-collector output, outputs of multiple ICs are brought together.

The output terminal for comparison result is only XDOWN2. The voltage on all the constant current output can be checked to monitor XDOWN2 turning output on in turn. The voltage on the constant current output, when turned on, can be also measured changing the comparison voltage set by the OVM latch. Using this function, sensing (LOD function) an LED disconnection (output voltage is below 0.3 V) and short circuit (output voltage is extremely high) can be detected and specifies which LED encountered this failure. Also, by monitoring the output voltage and controlling the voltage across anode of the LED to minimize the voltage on the constant current output (approximately 0.7 V at I_O = 80 mA), the temperature rising of the chip can be minimized. Furthermore, by setting BLANK to low during LED on, the comparison result immediately before can be held. Thus, synchronizing timing to check XDOWN2 from the system to the LED lighting timing is not required. Note that the gray scale data being turned on should be a minimum of 5 μs since XDOWN2 output is required approximately 5 μs after the constant current output is turned on. The comparison result is also required approximately 5 μs after the changed latch data.

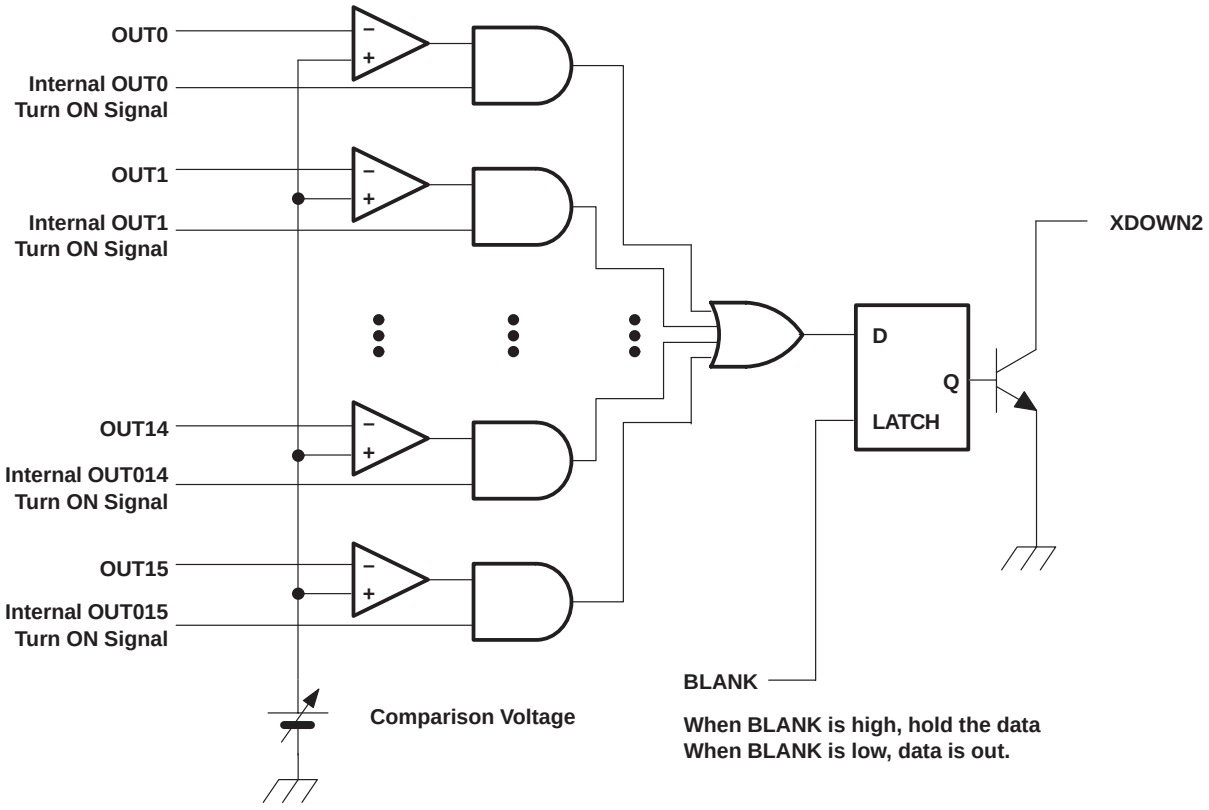


Figure 5. OVM functional diagram

PRINCIPLES OF OPERATION

output signal check for XDOWN1, XDOWN2

XDOWN1 or XDOWN2 can be forced to low level by setting the appropriate latch value for OVM. This allows the investigation of the correct connection of XDOWN1 or XDOWN2 to the external system.

OVM comparator setting

Setting the OVM latch is shown in Table 5. Note that the comparison voltage is set to the default value of 0.3 V when MCENA is tied to the low level.

Table 5. OVM Setting

MONITOR CONTROL DATA MSB LSB	COMPARISON VOLTAGE	XDOWN1	XDOWN2
0000	NO COMPARISON	DEPEND ON TSD/WDT	HI–Z
0001†	0.3 V	DEPEND ON TSD/WDT	DEPEND ON OVM COMPARATOR
0010	0.4 V	DEPEND ON TSD/WDT	DEPEND ON OVM COMPARATOR
0011	0.5 V	DEPEND ON TSD/WDT	DEPEND ON OVM COMPARATOR
0100	0.6 V	DEPEND ON TSD/WDT	DEPEND ON OVM COMPARATOR
0101	0.7 V	DEPEND ON TSD/WDT	DEPEND ON OVM COMPARATOR
0110	0.8 V	DEPEND ON TSD/WDT	DEPEND ON OVM COMPARATOR
0111	0.9 V	DEPEND ON TSD/WDT	DEPEND ON OVM COMPARATOR
1000	1.0 V	DEPEND ON TSD/WDT	DEPEND ON OVM COMPARATOR
1001	1.1 V	DEPEND ON TSD/WDT	DEPEND ON OVM COMPARATOR
1010	1.2 V	DEPEND ON TSD/WDT	DEPEND ON OVM COMPARATOR
1011	1/3 × VCCANA	DEPEND ON TSD/WDT	DEPEND ON OVM COMPARATOR
1100	1/2 × VCCANA	DEPEND ON TSD/WDT	DEPEND ON OVM COMPARATOR
1101	2/3 × VCCANA	DEPEND ON TSD/WDT	DEPEND ON OVM COMPARATOR
1110	0.3 V	L	DEPEND ON OVM COMPARATOR
1111	0.3 V	DEPEND ON TSD/WDT	L

† MCENA is low.

DOUT output timing selection

The timing for the DOUT output change can be switched by selecting the DOMODE level. When DOMODE is low, the DOUT is changed synchronizing to the rising edge of DCLK. When DOMODE is high, the DOUT is changed synchronizing to the falling edge of DCLK. When the shift operation with DOMODE is high, data can be protected from a shift error even if the DCLK signal is buffered externally in serial. In this case, when ICs are connected in cascade, the maximum data transfer speed at will be slower than the case of DOMODE low.

PRINCIPLES OF OPERATION

protection

This device incorporates WDT and TSD functions. If WDT or TSD functions, constant current output is stopped and XDOWN1 goes low. Therefore, by monitoring the XDOWN1 terminal, these failures can be detected immediately. Since the XDOWN1 output is configured as an open collector, outputs of multiple ICs are brought together.

WDT (watchdog timer)

The constant current output is forced to turn off and XDOWN1 goes low when the fixed period elapsed after the signal applied to WDTRG has not been changed. Therefore, by connecting a scan signal (signal to control line displayed) to WDTRG, the stop of the scan signal can be detected and the constant current output is turned off. This prevents the LED from burning and damage caused by continuous LED turnon at the dynamic scanning operation. The detection time can be set using an external capacitor, Cext. The typical value is approximately 10 ms without a capacitor, 160 ms with a 1000 pF capacitor and 1500 ms with a 0.01 μF capacitor. During static operation, the WDT function is disabled connecting WDCAP to GND (high or low level should be applied to WDTRG). Note that normal operations will resume changing the WDTRG level when WDT functions.

WDT operational time: $T\ (ms) \cong 10 + 0.15 \times Cext\ (pF)$

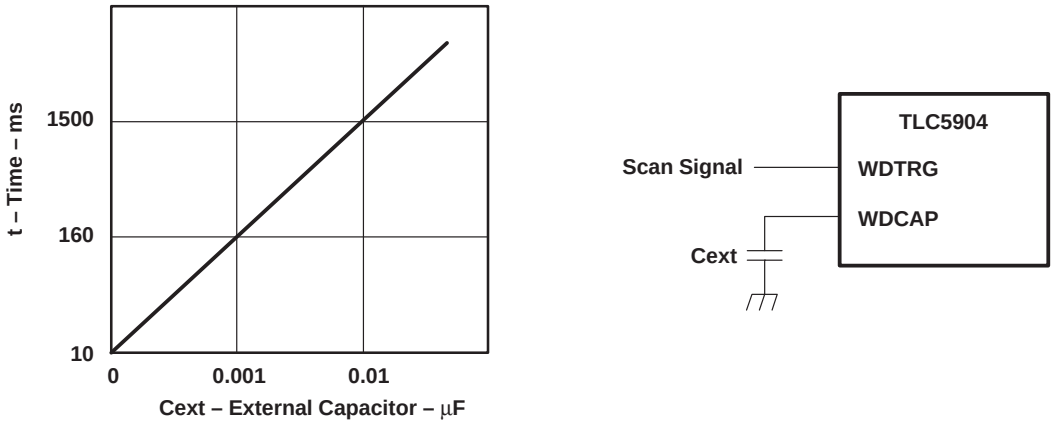


Figure 6. WDT Operational Time and Usage Example

TSD (thermal shutdown)

When the junction temperature exceeds the limit, TSD starts to function and turns the constant current output off, and XDOWN1 goes low. When TSD is used, TSENA should be pulled high. When TSD is not used, TSENA should be pulled low. To recover from the constant current output off-state to normal operations, the power supply should be turned off or TSENA should be pulled low once.

PRINCIPLES OF OPERATION

noise reduction

concurrent switching noise reduction

The concurrent switching noise has a potential to occur when multiple outputs turn on or off at the same time. To prevent this noise, the device has delay output terminals such as XGSOUT and BOUT for GSCLK (gray scale clock) and BLANK (blanking signal) respectively. By connecting these outputs to the GSCLK and BLANK terminals of next stage IC, it allows differences in the switching time between ICs. When GSCLK is output to GSOUT through the device, duty will be changed between input and output, and the number of stages to be connected will be limited depending on frequency.

output slope

When the output current is 80 mA, the time to change constant current output to turnon and turnoff is approximately 150 ns and 250 ns respectively. This allows reduced concurrent switching noise when multiple outputs turn on or off at the same time.

delay between constant current output

The constant current output has a delay time of approximately 30 ns between outputs. This means approximately 450 ns delay time exists between OUT0 and OUT15. This time differences by delay allows reduced concurrent switching noise as well as the output slope previously described. This delay time has the same value at the 8 bits or 16 bits operation mode.

power supply

The followings should be taken into consideration:

1) VCCLOG, VCCANA, and VCCLED should be supplied by a single power supply to minimize voltage differences between these terminals.

2) The bypass capacitor should be located between the power supply and GND to eliminate the variation of power supply voltage.

GND

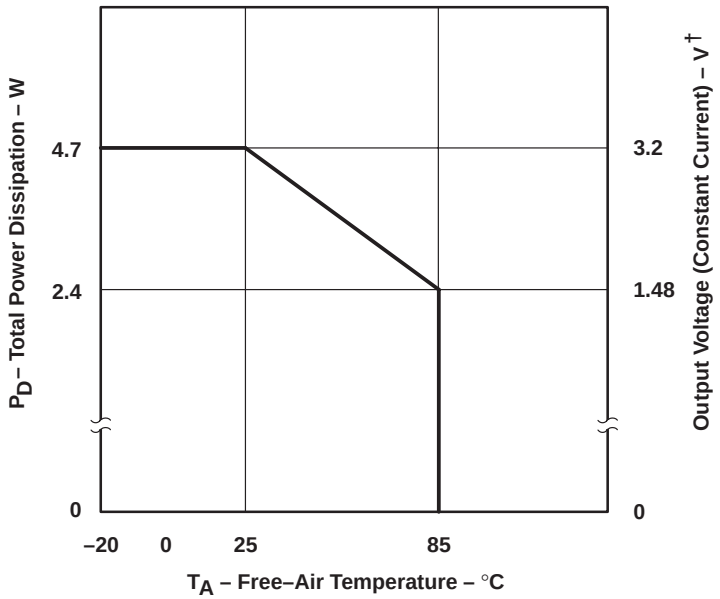
Although GNDLOG, GNDANA, and GNDLED are internally tied together, these terminals should be externally connected to reduce noise influence.

thermal pad

The thermal pad should be connected to GND to eliminate the noise influence when it is connected to the bottom side of IC chip. Also, the desired thermal effect will be obtained by connecting this pad to the PCB pattern with better thermal conductivity.

PRINCIPLES OF OPERATION

power rating – free-air temperature



† VCCLOG=VCCANA=VCCLED=5.0V, I_{OLC} = 80 mA, I_{CC} is typical value.

NOTES: A. IC is mounted on PCB. PCB size: 102 x 76 × 1.6 [mm^3], four layers with the internal two layer being plane. The thermal pad is soldered to the PCB pattern of 10 × 10 [mm^2]. For operation above 25°C free-air temperature, derate linearly at the rate of 38.2 mW/°C.

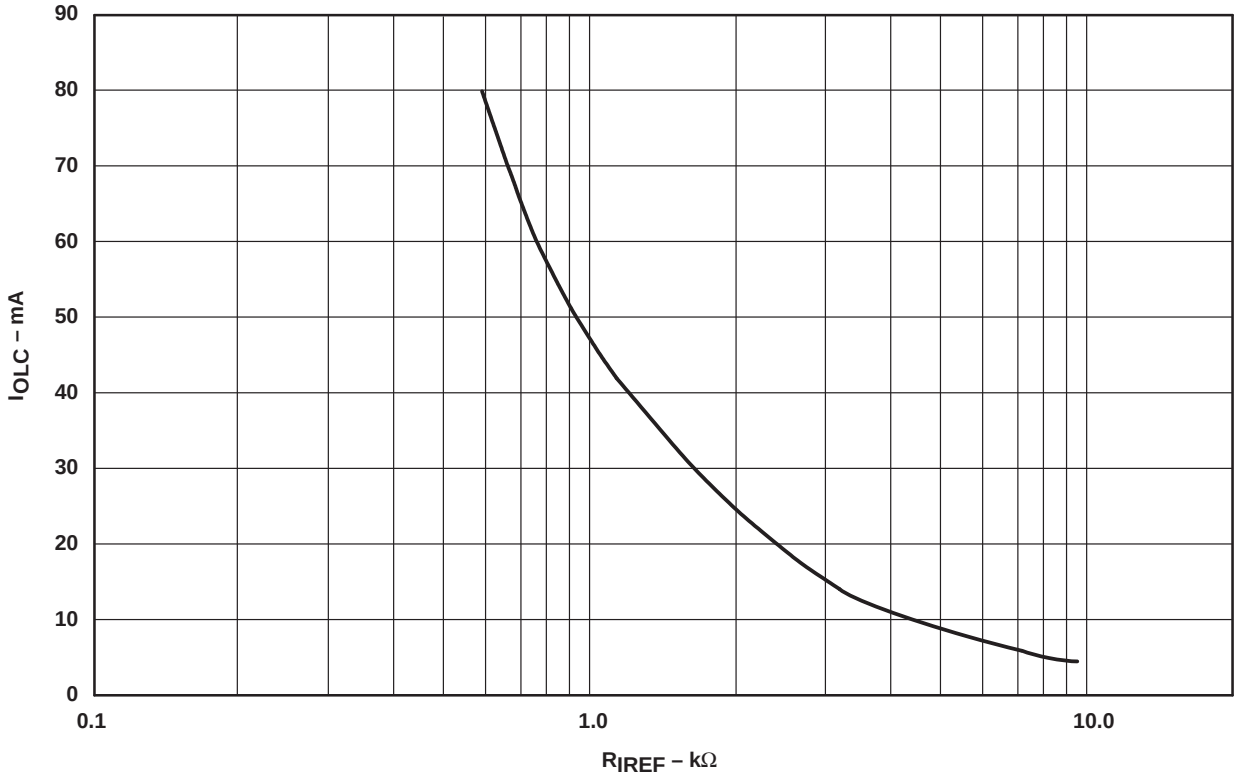
B. The thermal impedance will be varied depending on mounting conditions. Since the PZP package established low thermal impedance by radiating heat from the thermal pad, the thermal pad should be soldered to the pattern with low a thermal impedance.

C. Consider thermal characteristics when selecting the material for the PCB, since the temperature will rise around the thermal pad.

Figure 7. Power Rating

PRINCIPLES OF OPERATION

constant output current



NOTE: Conditions: V_{OUT} = 1.0V, V_{IREF} = 1.24V

$$I_{OLC}(mA) \cong \frac{V_{IREF}(V)}{R_{IREF}(k\Omega)} \times 37$$

$$R_{IREF}\ (k\Omega) \cong \frac{47}{I_{OLC}(mA)}$$

NOTE: Shows the output current at the 16 bit mode. and at the 8 bit mode (MODE=L). Output current is the sum of both outputs. This sum current should be set from 10 mA to 120 mA. The resistor, R_{IREF}, should be located as close to the IREF terminal as possible to avoid the noise influence.

Figure 8. Current on Constant Current Output vs External Resistor

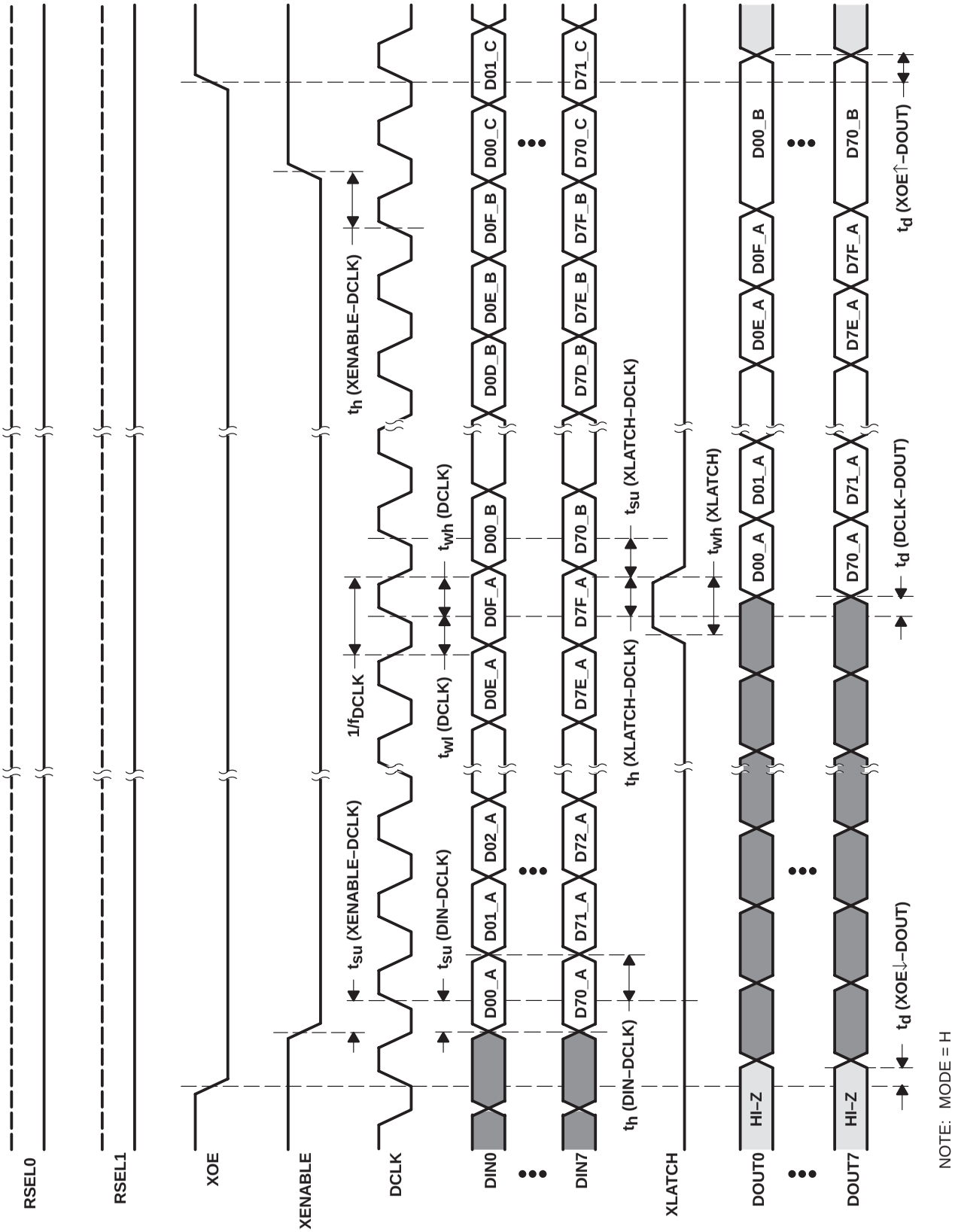


Figure 9. Timing Diagram (Shift Register for Gray Scale Data)

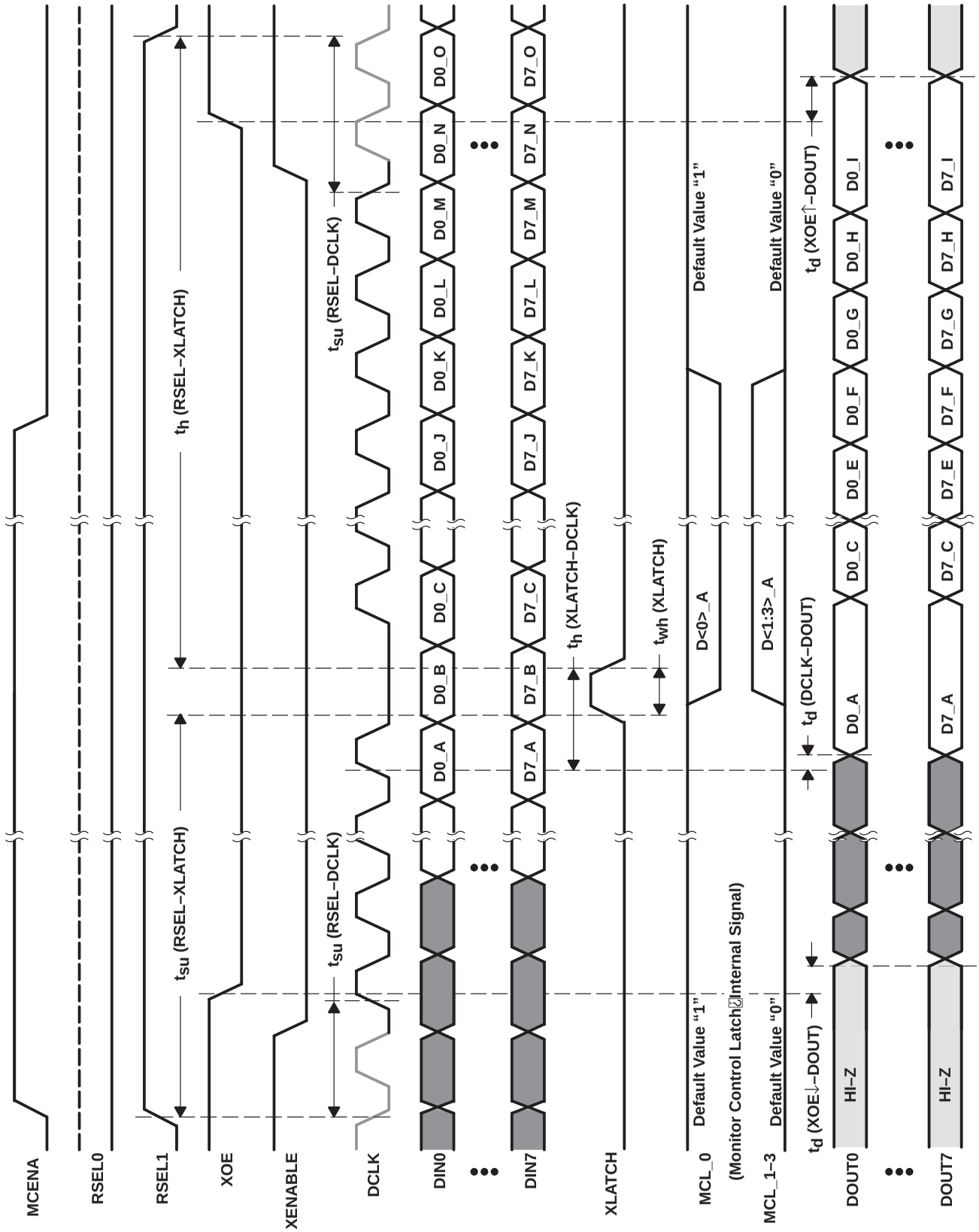


Figure 10. Timing Diagram (Shift Register for Monitor Control)

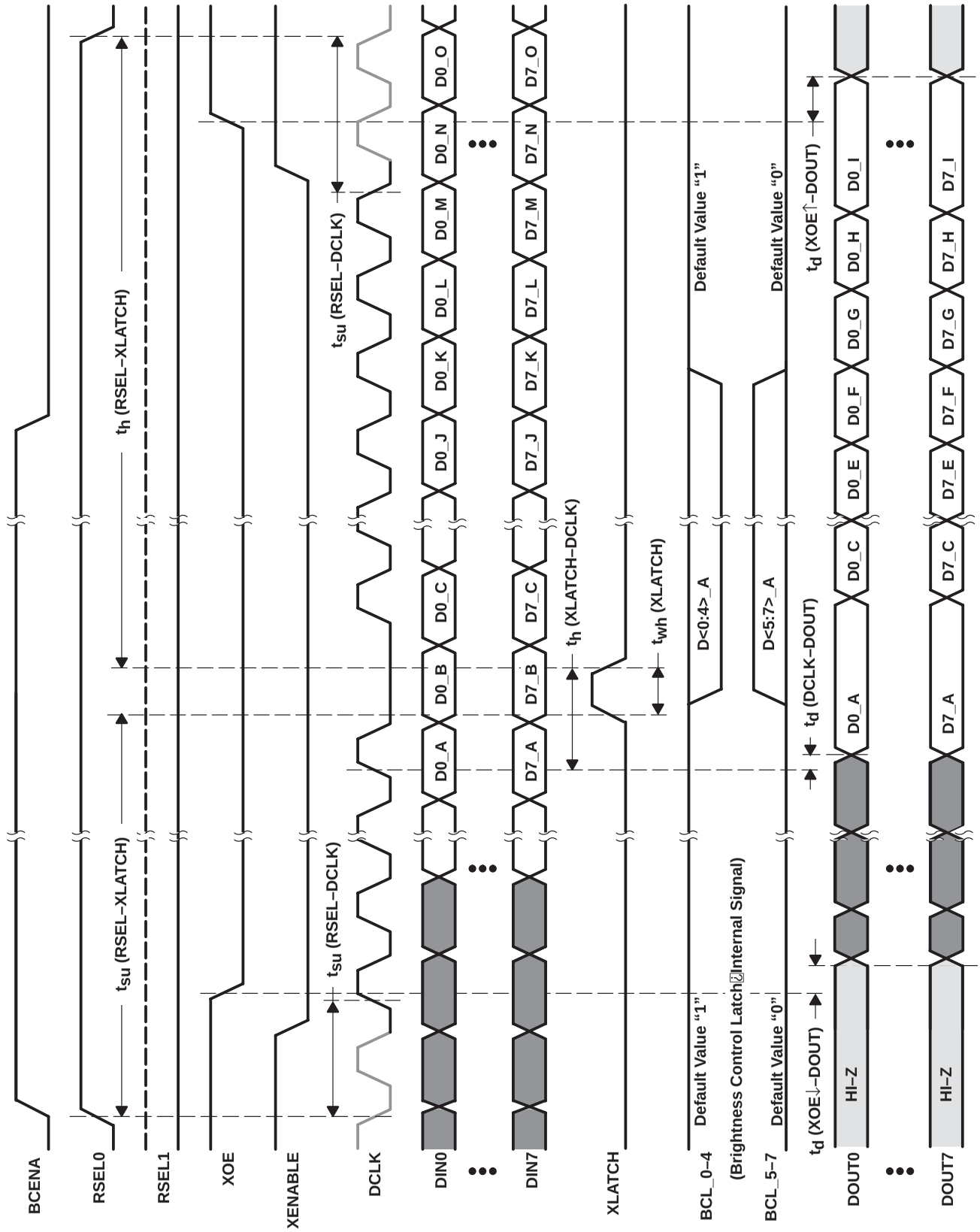


Figure 11. Timing Diagram (Shift Register for Brightness Control)

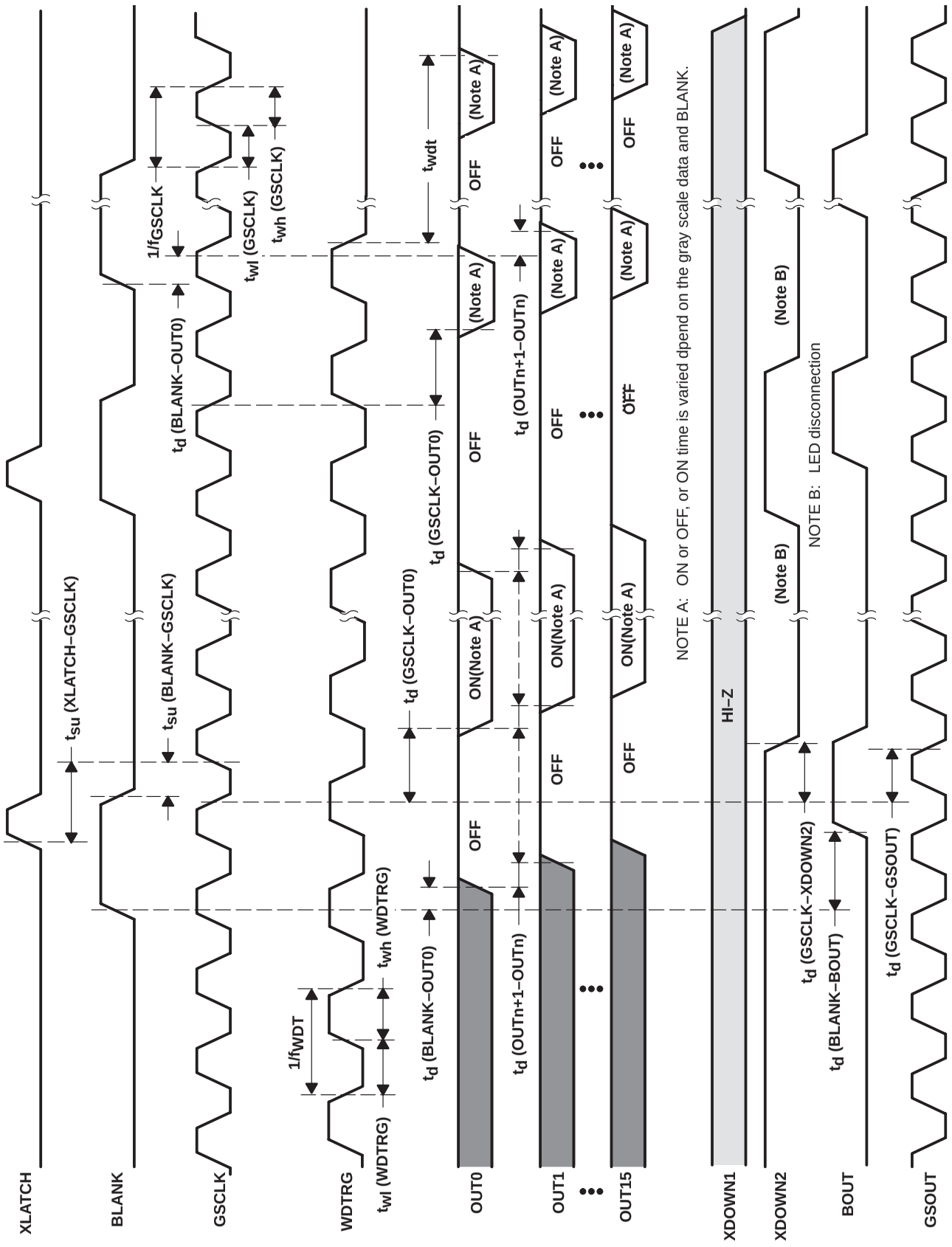
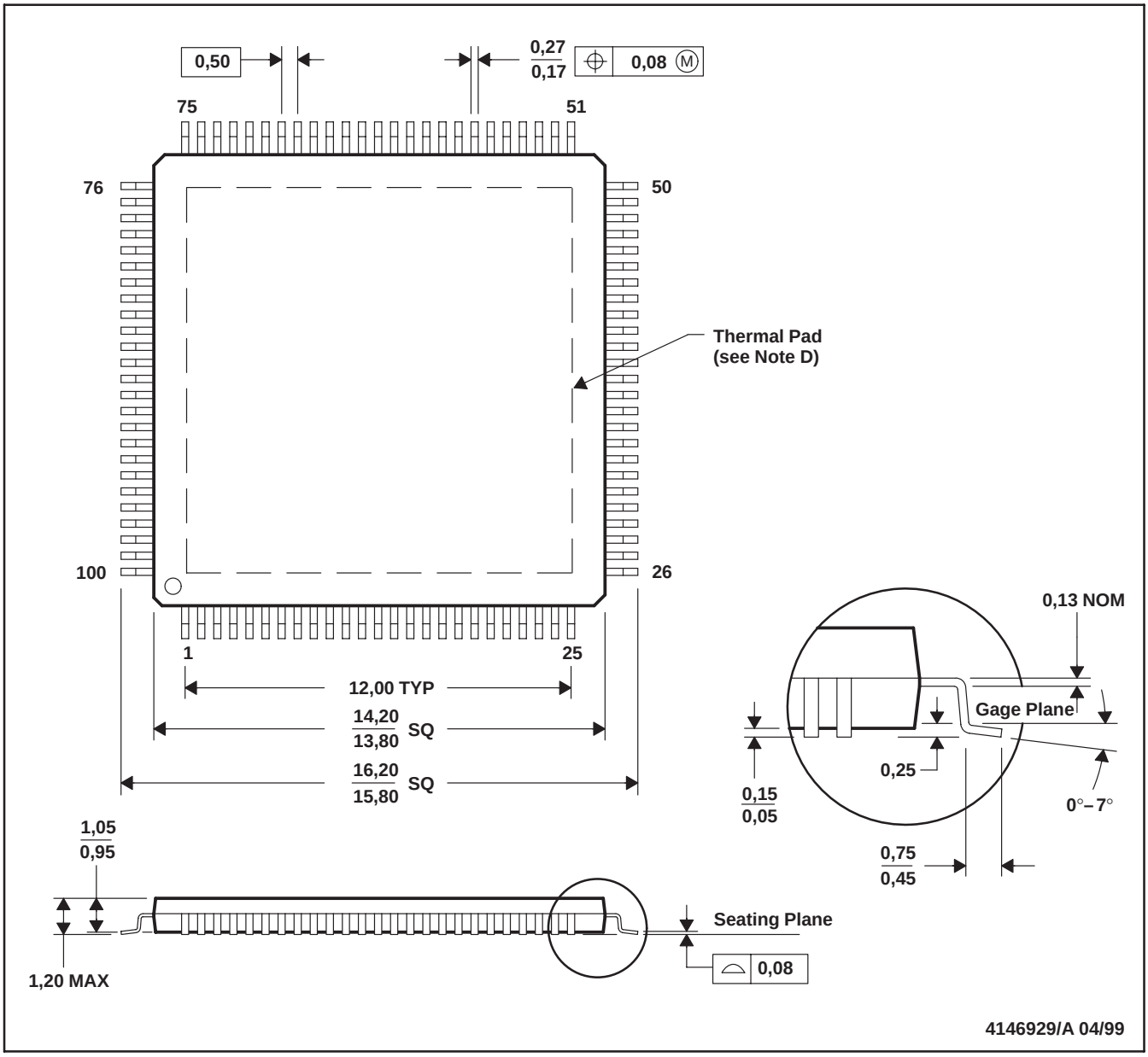


Figure 12. Timing Diagram (Constant Current Output)

MECHANICAL DATA

PZP (S-PQFP-G100) **PowerPAD™ PLASTIC QUAD FLATPACK**



NOTES: A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusion.
D. The package thermal performance may be enhanced by bonding the thermal pad to an external thermal plane.
This pad is electrically and thermally connected to the backside of the die and possibly selected leads. The demensions of the thermal pad are 5 mm x 5 mm. The pad is centered on the bottom of the package.
E. Falls within JEDEC MS-026

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