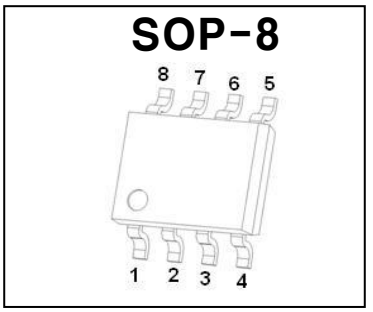
P Channel MOS FET

$V_{(BR)DSS}$	$R_{DS(on)}$MAX	I_D
-20V	8.5mΩ@-4.5V	-14A
	10.5mΩ@-2.5V	
	14mΩ@-1.8V	



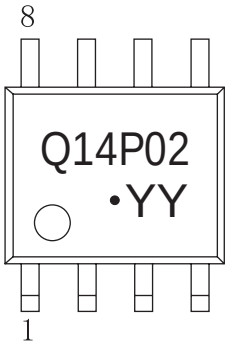
FEATURE

- High Density Cell Design for Ultra Low Rdson
- Fully Characterized Avalanche Voltage and Current
- Good Stablility and Uniformity With High E_{AS}
- Excellent Package for Good Heat Dissipation

APPLICATION

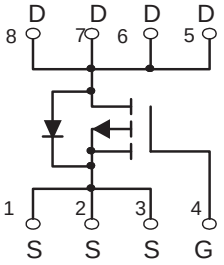
- Load Switch
- Battery Protection

MARKING



Q14P02 = Device code
Solid dot=Pin1 indicator
Solid dot = Green molding compound device, if none, the normal device
YY=Date Code

Equivalent Circuit



ABSOLUTE MAXIMUM RATINGS (T_a=25℃ unless otherwise noted)

Parameter	Symbol	Value	Unit
Drain-Source Voltage	V_{DS}	- 20	V
Gate-Source Voltage	V_{GS}	±12	V
Continuous Drain Current	I_D	-14	A
Pulsed Drain Current (note 1)	I_{DM}	-56	A
Power Dissipation	P_D	1.4	W
Thermal Resistance,Junction-to-ambient(note 2)	$R_{\theta JA}$	89.29	℃/W
Operating Junction and Storage Temperature Range	T_J,T_{STG}	-55~+150	℃

MOSFET ELECTRICAL CHARACTERISTICS

T_a=25℃ unless otherwise specified

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
STATIC CHARACTERISTICS						
Drain-source breakdown voltage	$V_{(BR)DSS}$	V_{GS} = 0V, I_D =-250μA	-20			V
Zero gate voltage drain current	I_{DSS}	V_{DS} =-18V,V_{GS} = 0V			-1	μA
Gate-body leakage current	I_{GSS}	V_{GS} =±12V, V_{DS} = 0V			±100	nA
Gate threshold voltage (note3)	$V_{GS(th)}$	V_{DS} =V_{GS}, I_D =-250μA	-0.4	-0.7	-1.2	V
Drain-source on-resistance(note 3)	$R_{DS(on)}$	V_{GS} =-4.5V, I_D =-14A		5.0	8.5	mΩ
		V_{GS} =-2.5V, I_D =-12A		7.0	10.5	mΩ
		V_{GS} =-1.8V, I_D =-5A		10.5	14	mΩ
Forward tranconductance(note 3)	g_{FS}	V_{DS} =-5V, I_D =-14A		45		S
Diode forward voltage (note 3)	V_{SD}	I_S=-14A, V_{GS} = 0V			-1.2	V
DYNAMIC CHARAC TERISTICS (note 4)						
Input Capacitance	C_{iss}	V_{DS} =-10V,V_{GS} =0V,f =1MHz		3500		pF
Output Capacitance	C_{oss}			577		pF
Reverse Transfer Capacitance	C_{rss}			445		pF
SWITCHING CHARACTERISTICS (note 4)						
Turn-on delay time	$t_{d(on)}$	V_{GS}=-4.5V,V_{DD}=-10V,R_L=0.5Ω R_{GEN}=3Ω		18		ns
Turn-on rise time	t_r			42		ns
Turn-off delay time	$t_{d(off)}$			85		ns
Turn-off fall time	t_f			23		ns
Total Gate Charge	Q_g	V_{DS}=-10V,I_D=-20A, V_{GS}=-4.5V		55		nC
Gate-Source Charge	Q_{gs}			10		nC
Gate-Drain Charge	Q_{gd}			15		nC

Notes :

1.Repetitive Rating:Pulse width limited by maximum junction temperature.

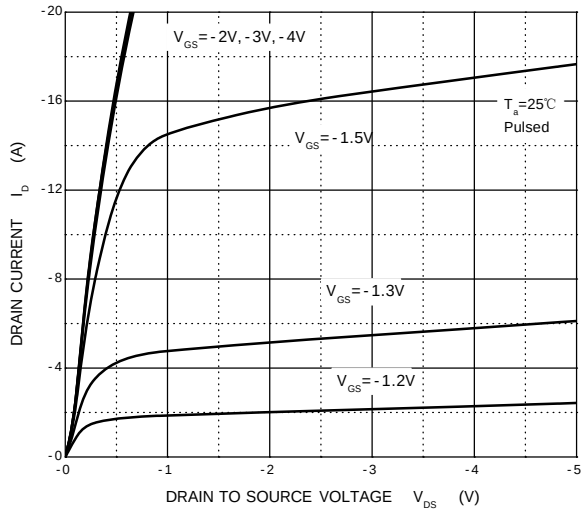
2.Surface mounted on FR4 board ,t≤10 sec.

3. Pulse Test : Pulse width≤300μs, duty cycle≤2%.

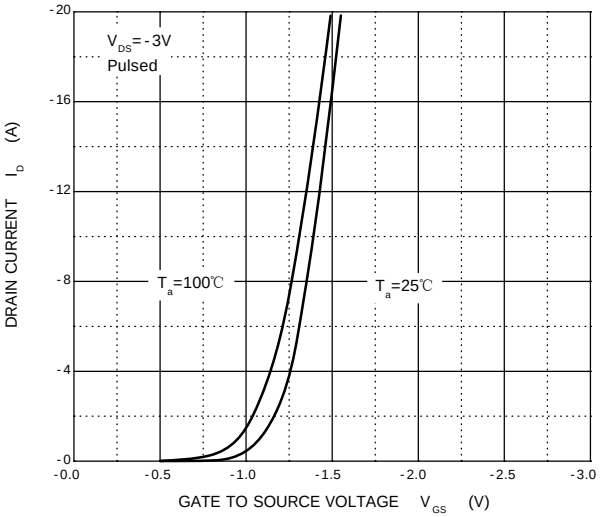
4. Graranted by design，not subject to production.

TYPICAL ELECTRICAL AND THERMAL CHARACTERISTICS

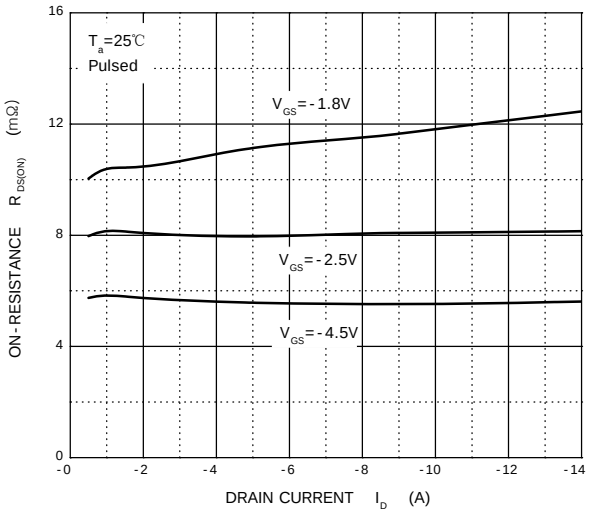
Output Characteristics



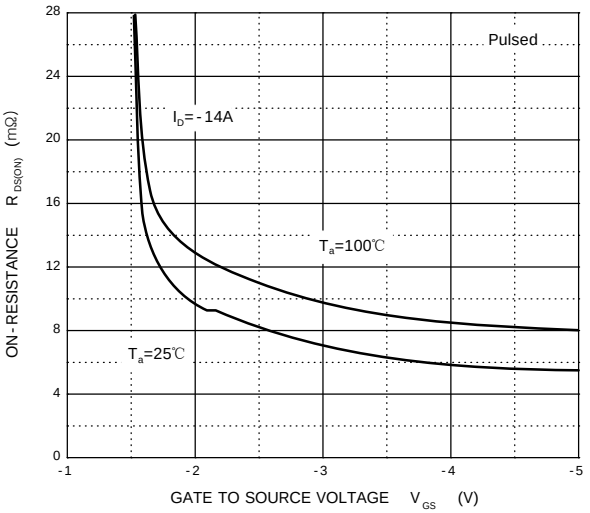
Transfer Characteristics



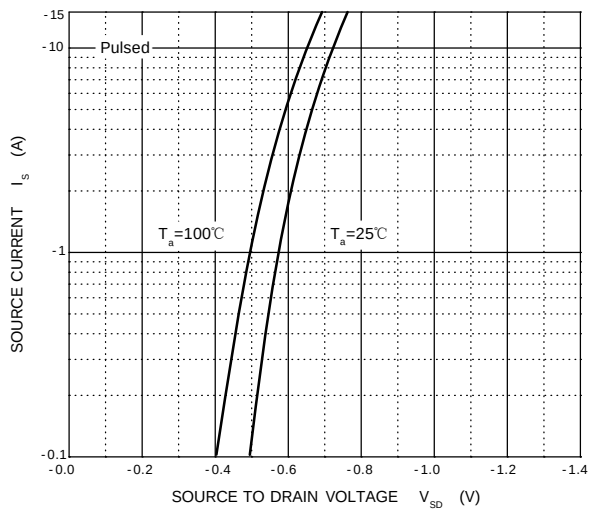
$R_{DS(ON)}$ —— I_D



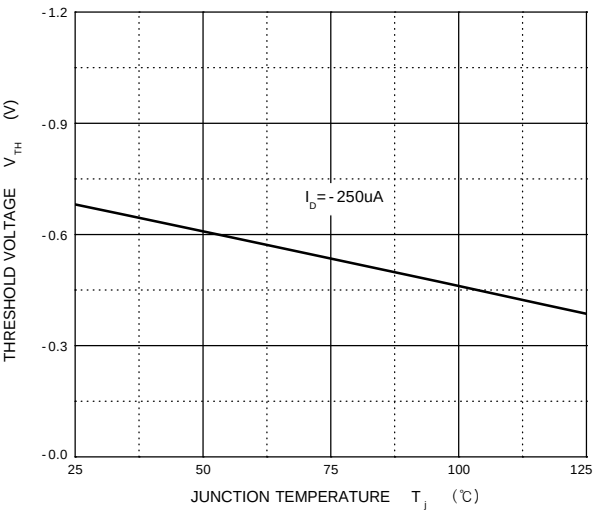
$R_{DS(ON)}$ —— V_{GS}



I_S —— V_{SD}

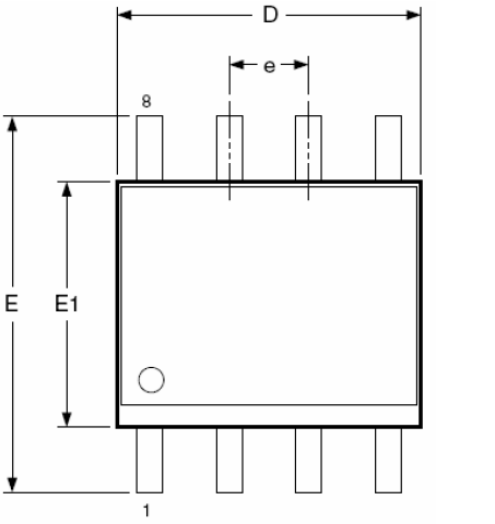


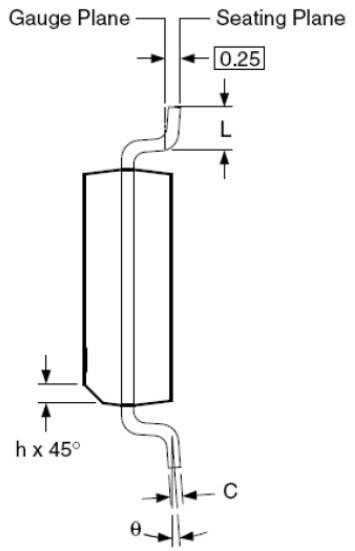
Threshold Vol tage

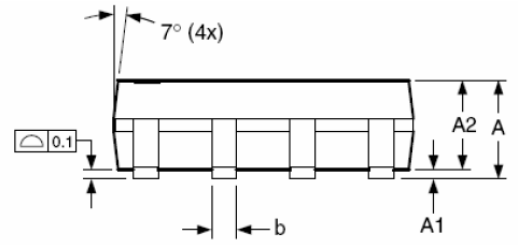


SOP-8 PACKAGE INFORMATION

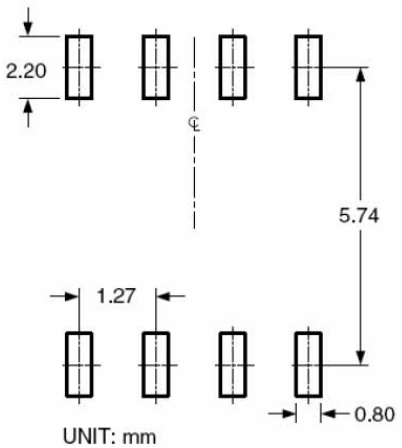
Dimensions in Millimeters (UNIT:mm)







RECOMMENDED LAND PATTERN



Dimensions in millimeters

Symbols	Min.	Nom.	Max.
A	1.35	1.65	1.75
A1	0.10	—	0.25
A2	1.25	1.50	1.65
b	0.31	—	0.51
c	0.17	—	0.25
D	4.80	4.90	5.00
E1	3.80	3.90	4.00
e	1.27 BSC		
E	5.80	6.00	6.20
h	0.25	—	0.50
L	0.40	—	1.27
θ	0°	—	8°

Dimensions in inches

Symbols	Min.	Nom.	Max.
A	0.053	0.065	0.069
A1	0.004	—	0.010
A2	0.049	0.059	0.065
b	0.012	—	0.020
c	0.007	—	0.010
D	0.189	0.193	0.197
E1	0.150	0.154	0.157
e	0.050 BSC		
E	0.228	0.236	0.244
h	0.010	—	0.020
L	0.016	—	0.050
θ	0°	—	8°

NOTES:

1. All dimensions are in millimeters.
2. Dimensions are inclusive of plating
3. Package body sizes exclude mold flash and gate burrs. Mold flash at the non-lead sides should be less than 6 mils.
4. Dimension L is measured in gauge plane.
5. Controlling dimension is millimeter, converted inch dimensions are not necessarily exact.