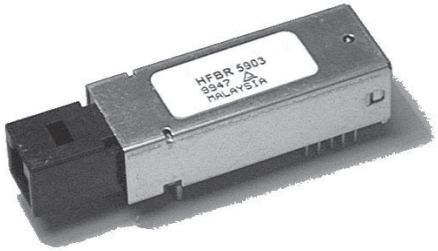
HFBR-5903, HFBR- 5903E, HFBR- 5903A

FDDI, Fast Ethernet Transceivers in 2 x 5 Package Style

Data Sheet



Description

The HFBR-5900 family of transceivers from Avago Technologies provide the system designer with products to implement a range of FDDI and ATM (Asynchronous Transfer Mode) designs at the 100 Mb/ s-125 MBd rate.

The transceivers are all supplied in the new industry standard 2 x 5 DIP style with a MT-RJ fiber connector interface.

FDDI PMD, ATM and Fast Ethernet 2 km Backbone Links

The HFBR-5903 is a 1300 nm product with optical performance compliant with the FDDI PMD standard. The FDDI PMD standard is ISO/IEC 9314-3: 1990 and ANSI X3.166 - 1990.

These transceivers for 2 km multimode fiber backbones are supplied in the small 2 x 5 MT-RJ package style for those designers who want to avoid the larger MIC/R (Media Interface Connector/Receptacle) defined in the FDDI PMD standard.

Avago Technologies also provides several other FDDI products compliant with the PMD and SM-PMD standards. These products are available with MIC/R, ST©, SC and FC connector styles. They are available in the 1 x 9, 1 x 13 and 2 x 11 transceiver and 16 pin transmitter/receiver package styles for those designs that require these alternate configurations.

Features

- Multisourced 2 x 5 package style with MT-RJ receptacle
- Single +3.3 V power supply
- Wave solder and aqueous wash process compatible
- Manufactured in an ISO 9002 certified facility
- Full compliance with the optical performance requirements of the FDDI PMD standard
- Full compliance with the FDDI LCF-PMD standard
- Full compliance with the optical performance requirements of the ATM 100 Mb/s physical layer
- Full compliance with the optical performance requirements of 100 Base-FX version of IEEE 802.3u

Applications

- Multimode fiber backbone links
- Multimode fiber wiring closet to desktop links

Ordering Information

The HFBR-5903 1300 nm product is available for production orders through the Avago Technologies Component Field Sales Offices and Authorized Distributors world wide.

HFBR-5903 = 0°C to +70°C No Shield

HFBR-5903E = 0°C to +70°C Extended Shield

HFBR-5903A = -40°C to +85°C No Shield.

The HFBR-5903 is also useful for both ATM 100 Mb/s inter faces and Fast Ethernet 100 Base-FX interfaces. The ATM Forum User-Network Interface (UNI) Standard, Version 3.0, defines the Physical Layer for 100 Mb/s Multimode Fiber Interface for ATM in Section 2.3 to be the FDDI PMD Standard. Likewise, the Fast Ethernet Alliance defines the Physical Layer for 100 Base-FX for Fast Ethernet to be the FDDI PMD Standard.

ATM applications for physical layers other than 100 Mb/s Multimode Fiber Interface are supported by Avago Technologies. Products are available for both the single-mode and the multimode fiber SONET OC-3c (STS-3c), SDH (STM-1) ATM interfaces and the 155 Mb/s-194 logic output and the Signal Detect function. The Data output is differential. The Signal Detect output is single-ended. Both Data and Signal Detect outputs are PECL compatible, ECL referenced (shifted) to a +3.3 V power supply. The receiver outputs, Data Out and Data Out Bar, are squelched at Signal Detect Deassert. That is, when the light input power decreases to a typical -38 dBm or less, the Signal Detect Deasserts, i.e. the Signal Detect output goes to a PECL low state. This forces the receiver outputs, Data Out and Data Out Bar to go to steady PECL levels High and Low respectively.

Package

The overall package concept for the Avago Technologies transceiver consists of the following basic elements; two optical subassemblies, an electrical subassembly and the housing as illustrated in Figure 1.

The package outline drawing and pin out are shown in Figures 2 and 3. The details of this package outline and pin out are compliant with the multisource definition of the 2 x 5 DIP. The low profile of the Avago Technologies transceiver design complies with the maximum height allowed for the MT-RJ connector over the entire length of the package.

The optical subassemblies utilize a high-volume assembly process together with low-cost lens elements which result in a cost-effective building block.

The electrical subassembly consists of a high volume multilayer printed circuit board on which the IC and various surface-mounted passive circuit elements are attached.

The receiver section includes an internal shield for the electrical and optical subassemblies to ensure high immunity to external EMI fields.

The outer housing is electrically conductive. The MT-RJ port is molded of filled nonconductive plastic to provide mechanical strength and electrical isolation. The solder posts of the Avago Technologies design are isolated from the internal circuit of the transceiver.

The transceiver is attached to a printed circuit board with the ten signal pins and the two solder posts which exit the bottom of the housing. The two solder posts provide the primary mechanical strength to withstand the loads imposed on the transceiver by mating with the MT-RJ connectored fiber cables.

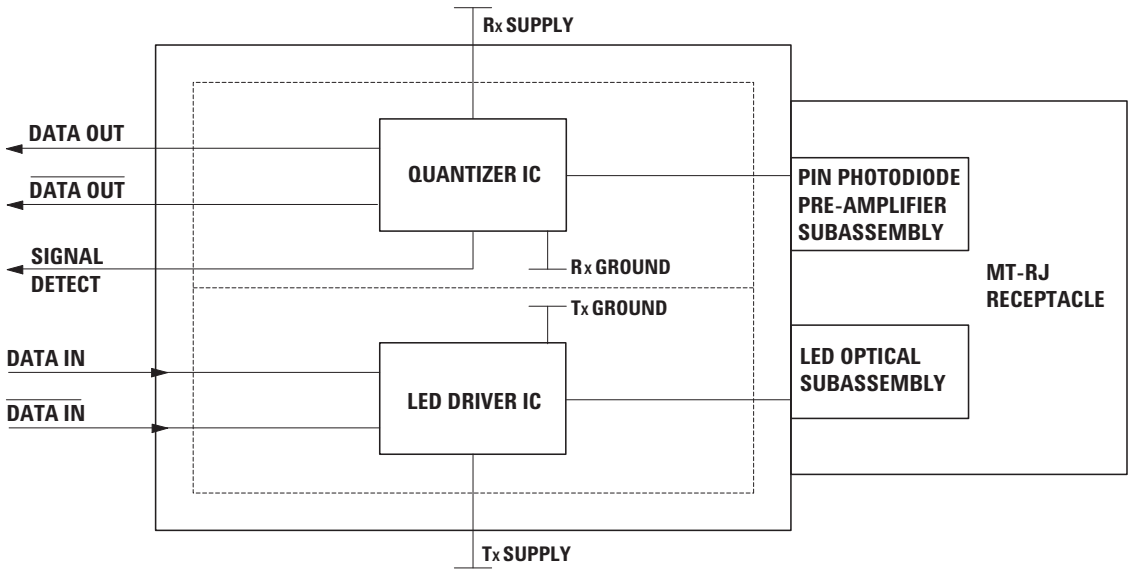
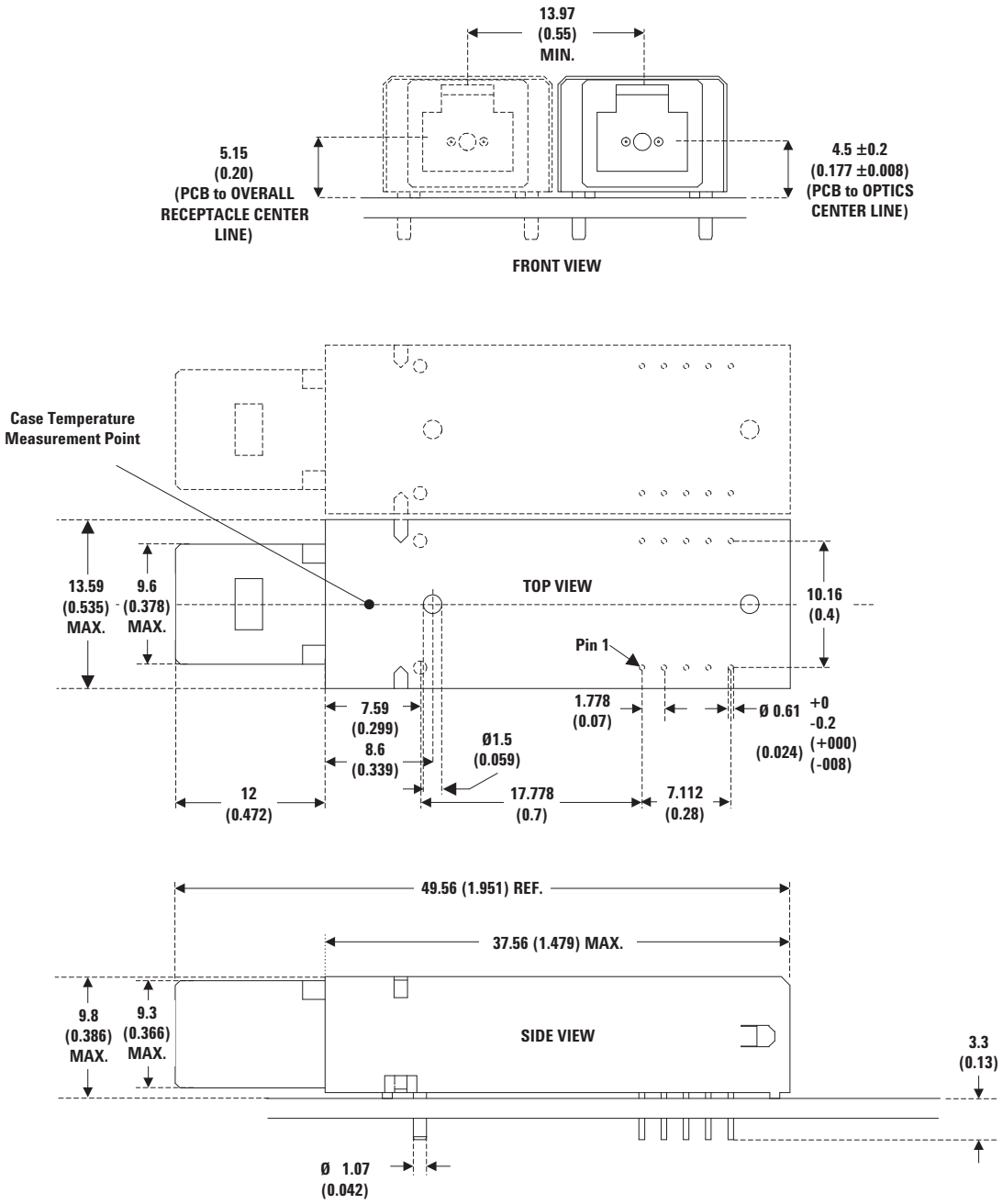


Figure 1. Block Diagram.



DIMENSIONS IN MILLIMETERS (INCHES)

NOTES:
1. THIS PAGE DESCRIBES THE MAXIMUM PACKAGE OUTLINE, MOUNTING STUDS, PINS AND THEIR RELATIONSHIPS TO EACH OTHER.
2. TOLERANCED TO ACCOMMODATE ROUND OR RECTANGULAR LEADS.
3. ALL 12 PINS AND POSTS ARE TO BE TREATED AS A SINGLE PATTERN.
4. THE MT-RJ HAS A 750 µm FIBER SPACING.
5. THE MT-RJ ALIGNMENT PINS ARE IN THE MODULE.
6. FOR SM MODULES, THE FERRULE WILL BE PC POLISHED (NOT ANGLED).
7. SEE MT-RJ TRANSCEIVER PIN OUT DIAGRAM FOR DETAILS.

Figure 2. Package Outline Drawing

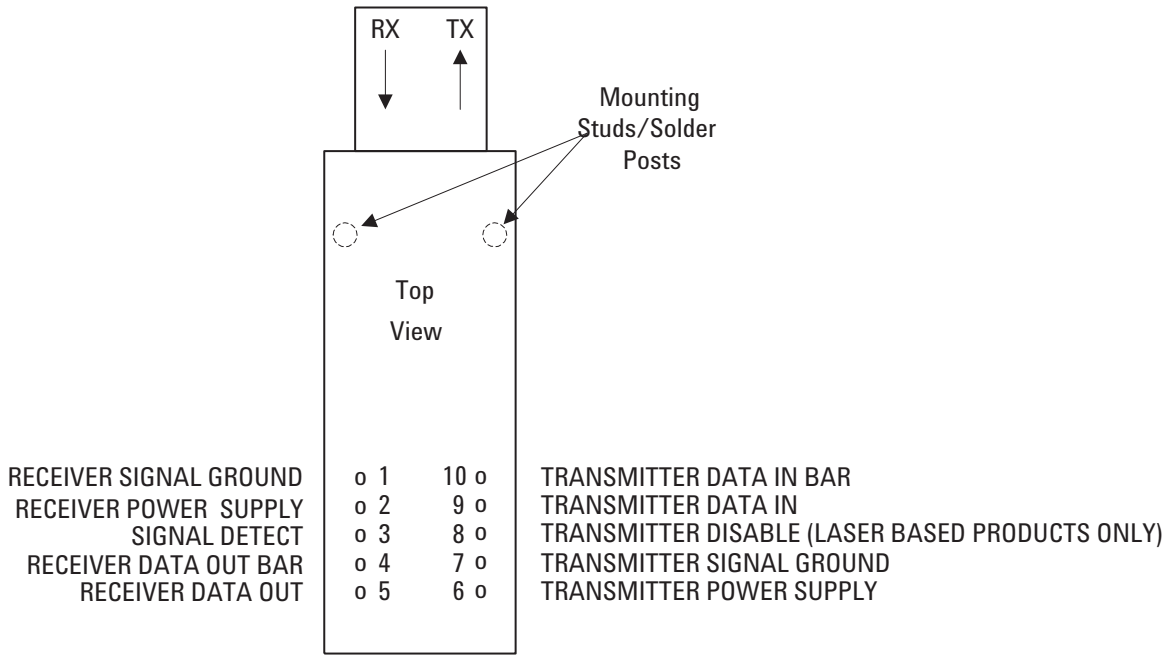


Figure 3. Pin Out Diagram.

Pin Descriptions:

Pin 1 Receiver Signal Ground V_{EE} RX:

Directly connect this pin to the receiver ground plane.

Pin 2 Receiver Power Supply V_{CC} RX:

Provide +3.3 V dc via the recommended receiver power supply filter circuit. Locate the power supply filter circuit as close as possible to the V_{CC} RX pin.

Pin 3 Signal Detect SD:

Normal optical input levels to the receiver result in a logic "1" output.

Low optical input levels to the receiver result in a fault condition indicated by a logic "0" output.

This Signal Detect output can be used to drive a PECL input on an upstream circuit, such as Signal Detect input or Loss of Signal-bar.

Pin 4 Receiver Data Out Bar RD-:

No internal terminations are provided. See recommended circuit schematic.

Pin 5 Receiver Data Out RD+:

No internal terminations are provided. See recommended circuit schematic.

Pin 6 Transmitter Power Supply V_{CC} TX:

Provide +3.3 V dc via the recommended transmitter power supply filter circuit. Locate the power supply filter circuit as close as possible to the V_{CC} TX pin.

Pin 7 Transmitter Signal Ground V_{EE} TX:

Directly connect this pin to the transmitter ground plane.

Pin 8 Transmitter Disable T_{DIS}:

No internal connection. Optional feature for laser based products only. For laser based products connect this pin to +3.3 V TTL logic high "1" to disable module. To enable module connect to TTL logic low "0".

Pin 9 Transmitter Data In TD+:

No internal terminations are provided. See recommended circuit schematic.

Pin 10 Transmitter Data In Bar TD-:

No internal terminations are provided. See recommended circuit schematic.

Mounting Studs/Solder Posts

The mounting studs are provided for transceiver mechanical attachment to the circuit board. It is recommended that the holes in the circuit board be connected to chassis ground.

Application Information

The Applications Engineering group is available to assist you with the technical understanding and design trade-offs associated with these transceivers. You can contact them through your Avago Technologies sales representative.

The following information is provided to answer some of the most common questions about the use of these parts.

Transceiver Optical Power Budget versus Link Length

Optical Power Budget (OPB) is the available optical power for a fiber optic link to accommodate fiber cable losses plus losses due to in-line connectors, splices, optical switches, and to provide margin for link aging and unplanned losses due to cable plant reconfiguration or repair.

Figure 4 illustrates the predicted OPB associated with the transceiver specified in this data sheet at the Beginning of Life (BOL). These curves represent the attenuation and chromatic plus modal dispersion losses associated with the 62.5/125 µm and 50/125 µm fiber cables only. The area under the curves represents the remaining OPB at any link length, which is available for overcoming non-fiber cable related losses.

Avago Technologies LED technology has produced 1300 nm LED devices with lower aging characteristics than normally associated with these technologies in the industry. The industry convention is 1.5 dB aging for 1300 nm LEDs. The Avago Technologies 1300 nm LEDs will experience less than 1 dB of aging over normal commercial equipment mission life periods. Contact your Avago Technologies sales representative for additional details.

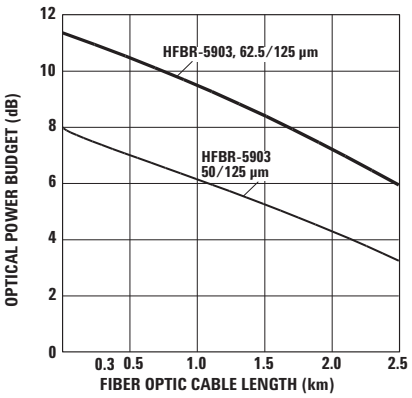


Figure 4. Typical Optical Power Budget at BOL versus Fiber Optic Cable Length.

Figure 4 was generated with a Avago Technologies fiber optic link model containing the current industry conventions for fiber cable specifications and the FDDI PMD and LCF-PMD optical parameters. These parameters are reflected in the guaranteed performance of the transceiver specifications in this data sheet. This same model has been used extensively in the ANSI and IEEE committees, including the ANSI X3T9.5 committee, to establish the optical performance requirements for various fiber optic interface standards. The cable parameters used come from the ISO/IEC JTC1/SC 25/WG3 Generic Cabling for Customer Premises per DIS 11801 document and the EIA/TIA-568-A Commercial Building Telecommunications Cabling Standard per SP-2840.

Transceiver Signaling Operating Rate Range and BER Performance

For purposes of definition, the symbol (Baud) rate, also called signaling rate, is the reciprocal of the shortest symbol time. Data rate (bits/sec) is the symbol rate divided by the encoding factor used to encode the data (symbols/bit).

When used in FDDI and ATM 100 Mb/s applications the performance of the 1300 nm transceivers is guaranteed over the signaling rate of 10 MBd to 125 MBd to the full conditions listed in individual product specification tables.

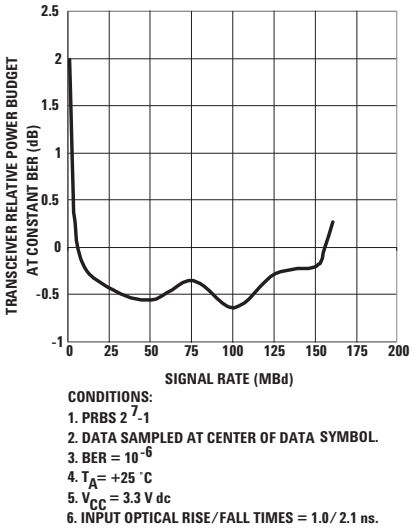


Figure 5. Transceiver Relative Optical Power Budget at Constant BER vs. Signaling Rate.

The transceivers may be used for other applications at signaling rates outside of the 10 MBd to 125 MBd range with some penalty in the link optical power budget primarily caused by a reduction of receiver sensitivity. Figure 5 gives an indication of the typical performance of these 1300 nm products at different rates.

These transceivers can also be used for applications which require different Bit Error Rate (BER) performance. Figure 6 illustrates the typical trade-off between link BER and the receivers input optical power level.

Transceiver Jitter Performance

The Avago Technologies 1300 nm transceivers are designed to operate per the system jitter allocations stated in Table E1 of Annex E of the FDDI PMD and LCF-PMD standards.

The Avago Technologies 1300 nm transmitters will tolerate the worst case input electrical jitter allowed in these tables without violating the worst case output jitter requirements of Sections 8.1 Active Output Interface of the FDDI PMD and LCF-PMD standards.

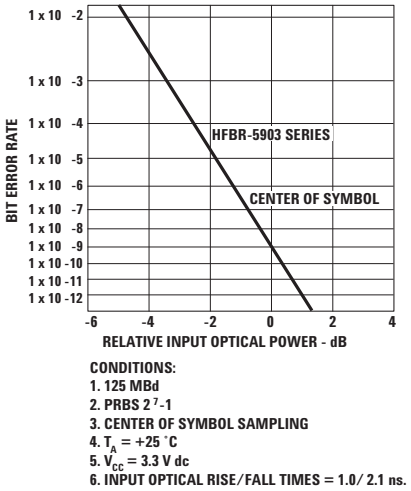
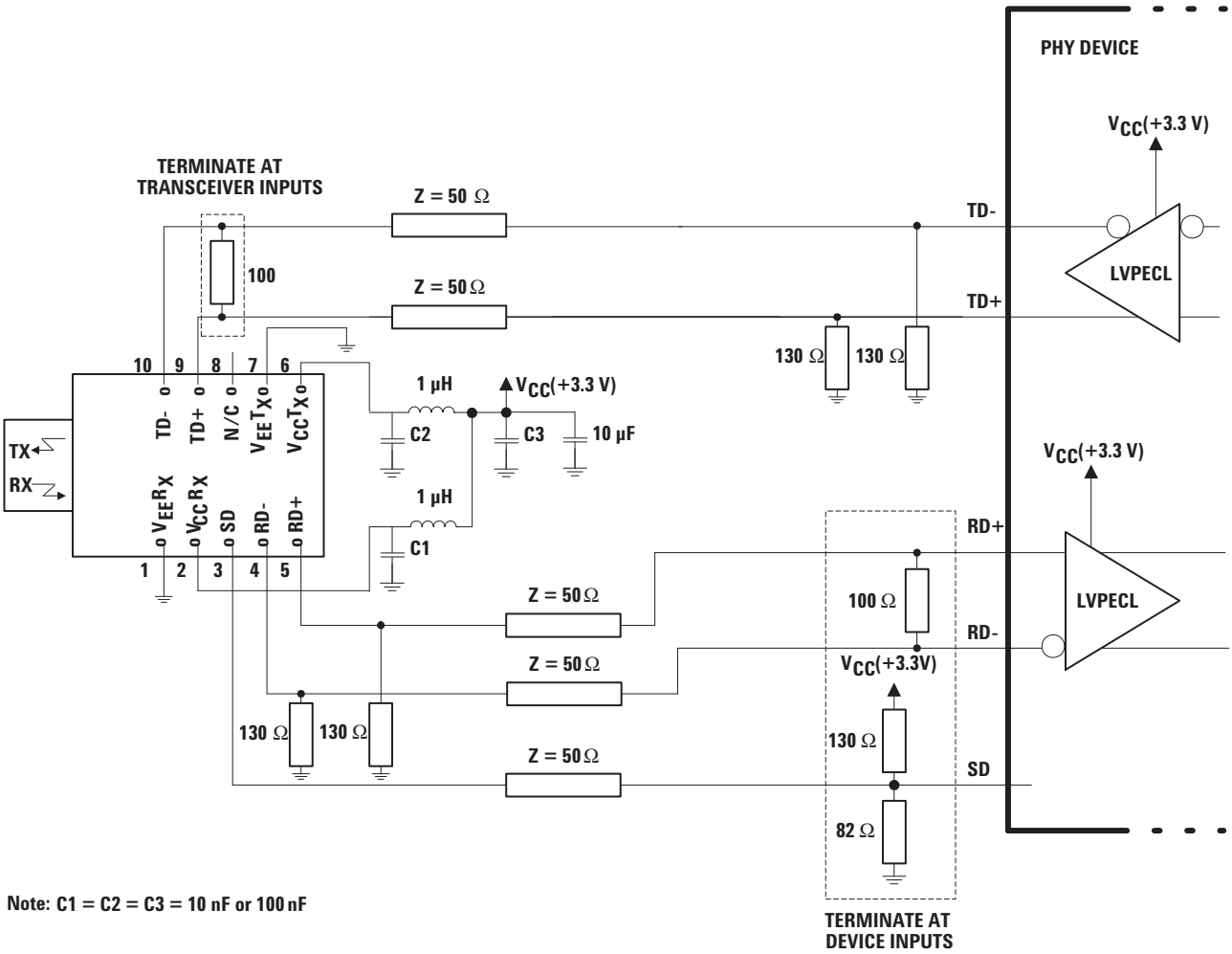


Figure 6. Bit Error Rate vs. Relative Receiver Input Optical Power.



Note: C1 = C2 = C3 = 10 nF or 100 nF

Figure 7. Recommended Decoupling and Termination Circuits

The Avago Technologies 1300 nm receivers will tolerate the worst case input optical jitter allowed in Sections 8.2 Active Input Interface of the FDDI PMD and LCF-PMD standards without violating the worst case output electrical jitter allowed in Table E1 of Annex E.

The jitter specifications stated in the following 1300 nm transceiver specification tables are derived from the values in Table E1 of Annex E. They represent the worst case jitter contribution that the transceivers are allowed to make to the overall system jitter without violating the Annex E allocation example. In practice the typical contribution of the Avago Technologies transceivers is well below these maximum allowed amounts.

Recommended Handling Precautions

Avago Technologies recommends that normal static precautions be taken in the handling and assembly of these transceivers to prevent damage which may be induced by electrostatic discharge (ESD). The HFBR-5900 series of transceivers meet MIL-STD-883C Method 3015.4 Class 2 products.

Care should be used to avoid shorting the receiver data or signal detect outputs directly to ground without proper current limiting impedance.

Solder and Wash Process Compatibility

The transceivers are delivered with protective process plugs inserted into the MT-RJ connector receptacle. This process plug protects the optical subassemblies during wave solder and aqueous wash processing and acts as a dust cover during shipping.

These transceivers are compatible with either industry standard wave or hand solder processes.

Shipping Container

The transceiver is packaged in a shipping container designed to protect it from mechanical and ESD damage during shipment or storage.

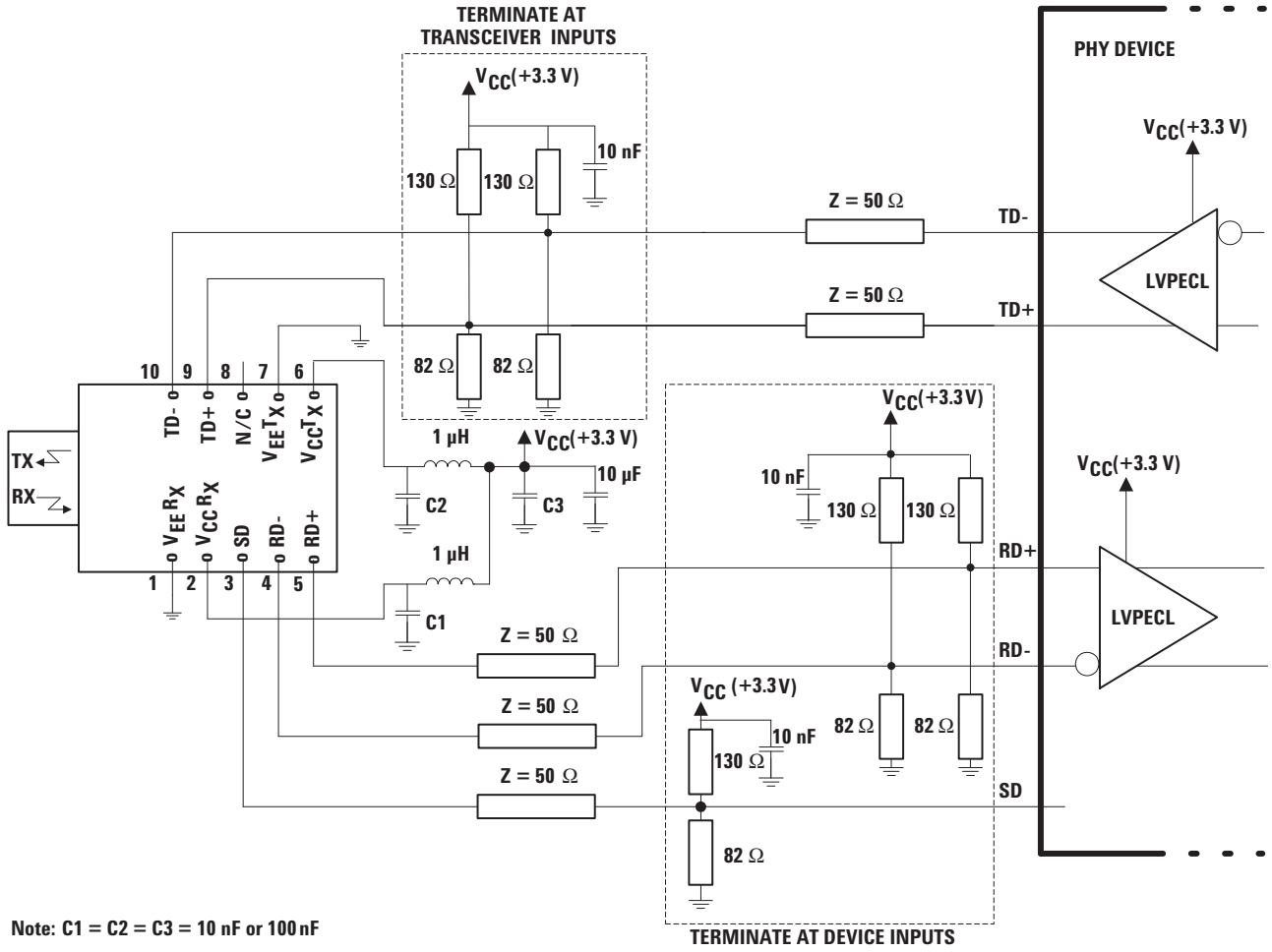


Figure 8. Alternative Termination Circuits

Board Layout - Decoupling Circuit, Ground Planes and Termination Circuits

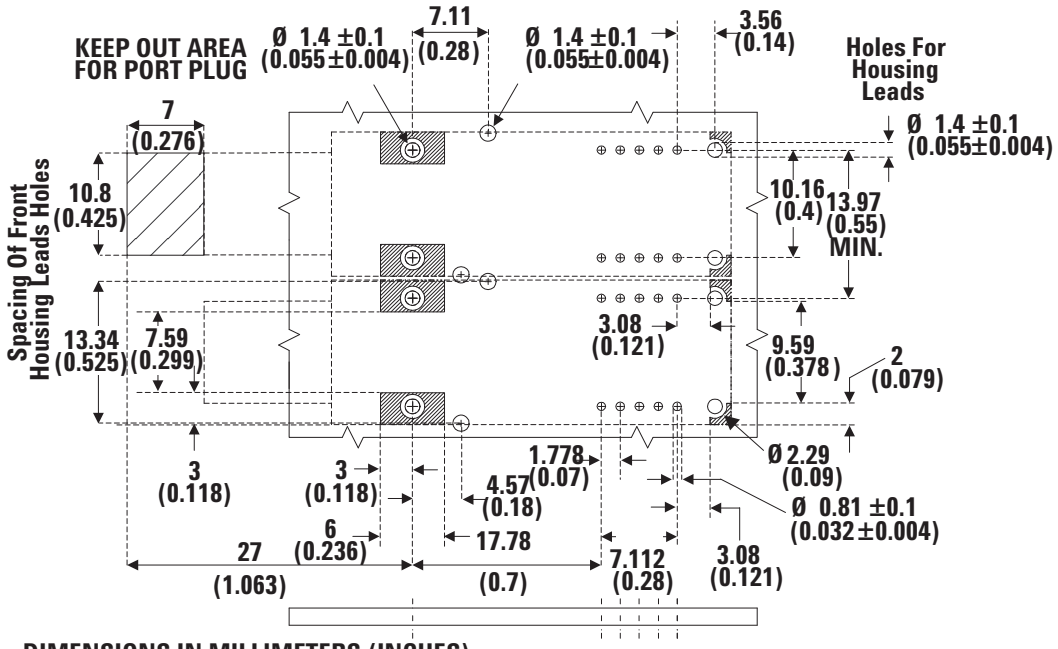
It is important to take care in the layout of your circuit board to achieve optimum performance from these transceivers. Figure 7 provides a good example of a schematic for a power supply decoupling circuit that works well with these parts. It is further recommended that a continuous ground plane be provided in the circuit board directly under the transceiver to provide a low inductance ground for signal return current. This recommendation is in keeping with good high frequency board layout practices. Figures 7 and 8 show two recommended termination schemes.

Board Layout - Hole Pattern

The Avago Technologies transceiver complies with the circuit board "Common Transceiver Footprint" hole pattern defined in the original multisource announcement which defined the 2 x 5 package style. This drawing is reproduced in Figure 9 with the addition of ANSI Y14.5M compliant dimensioning to be used as a guide in the mechanical layout of your circuit board.

Regulatory Compliance

These transceiver products are intended to enable commercial system designers to develop equipment that complies with the various international regulations governing certification of Information Technology Equipment. See the Regulatory Compliance Table for details. Additional information is available from your Avago Technologies sales representative.



DIMENSIONS IN MILLIMETERS (INCHES)

NOTES:

1. **THIS FIGURE DESCRIBES THE RECOMMENDED CIRCUIT BOARD LAYOUT FOR THE MT-RJ TRANSCEIVER PLACED AT .550 SPACING.**
2. **THE HATCHED AREAS ARE KEEP-OUT AREAS RESERVED FOR HOUSING STANDOFFS. NO METAL TRACES OR GROUND CONNECTION IN KEEP-OUT AREAS.**
3. **10 PIN MODULE REQUIRES ONLY 16 PCB HOLES, INCLUDING 4 PACKAGE GROUNDING TAB HOLES CONNECTED TO SIGNAL GROUND.**
4. **THE SOLDER POSTS SHOULD BE SOLDERED TO CHASSIS GROUND FOR MECHANICAL INTEGRITY AND TO ENSURE FOOTPRINT COMPATIBILITY WITH OTHER SFF TRANSCEIVERS.**

Figure 9. Recommended Board Layout Hole Pattern

Regulatory Compliance Table

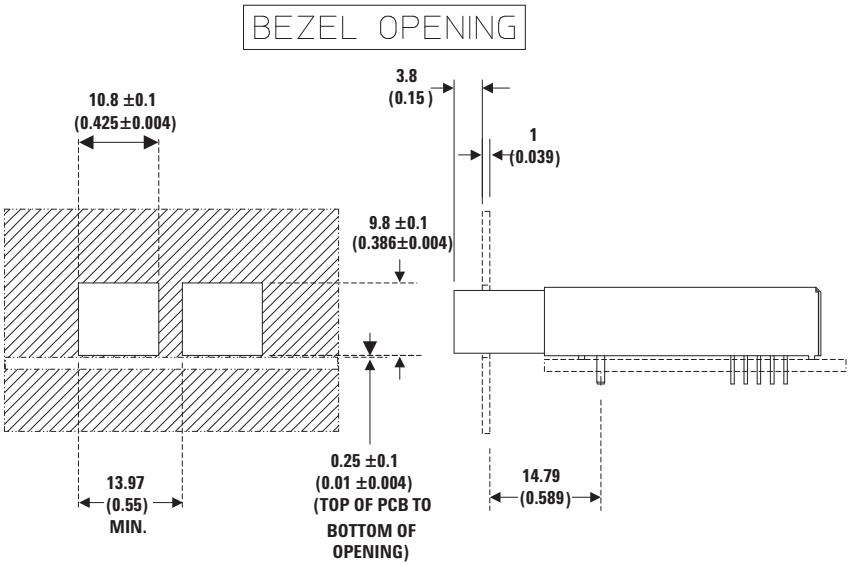
Feature	Test Method	Performance
Electrostatic Discharge (ESD) to the Electrical Pins	MIL-STD-883C Method 3015.4	Meets Class 2 (2000 to 3999 Volts). Withstand up to 2200 V applied between electrical pins.
Electrostatic Discharge ESD) to the MT-RJ Receptacle	Variation of IEC 801-2	Typically withstand at least 25 kV without damage when the MT-RJ Connector Receptacle is contacted by a Human Body Model probe.
Electromagnetic Interference (EMI)	FCC Class B CENELEC CEN55022 VCCI Class 2	Transceivers typically provide a 10 dB margin to the noted standard limits when tested at a certified test range with the transceiver mounted to a circuit card without a chassis enclosure.
Immunity	Variation of IEC 801-3	Typically show no measurable effect from a 10 V/m field swept from 10 to 450 MHz applied to the transceiver when mounted to a circuit card without a chassis enclosure.
Eye Safety	IEC 825 Issue 1 1993:11 Class 1 CENELEC EN60825 Class 1	Compliant per Avago Technologies testing under single fault conditions. TUV Certification: LED Class 1

Electrostatic Discharge (ESD)

There are two design cases in which immunity to ESD damage is important.

The first case is during handling of the transceiver prior to mounting it on the circuit board. It is important to use normal ESD handling precautions for ESD sensitive devices. These precautions include using grounded wrist straps, work benches, and floor mats in ESD controlled areas.

The second case to consider is static discharges to the exterior of the equipment chassis containing the transceiver parts. To the extent that the MT-RJ connector is exposed to the outside of the equipment chassis it may be subject to whatever ESD system level test criteria that the equipment is intended to meet.



DIMENSIONS IN MILLIMETERS (INCHES)

Figure 10. Recommended Panel Mounting

Electromagnetic Interference (EMI)

Most equipment designs utilizing this high speed transceiver from Avago Technologies will be required to meet the requirements of FCC in the United States, CENELEC EN55022 (CISPR 22) in Europe and VCCI in Japan.

Applications Support Materials

Contact your local Avago Technologies Component Field Sales Office for information on how to obtain PCB layouts and evaluation boards for the 2 x 5 transceivers.

Immunity

Equipment utilizing these transceivers will be subject to radio-frequency electromagnetic fields in some environments. These transceivers have a high immunity to such fields.

For additional information regarding EMI, susceptibility, ESD and conducted noise testing

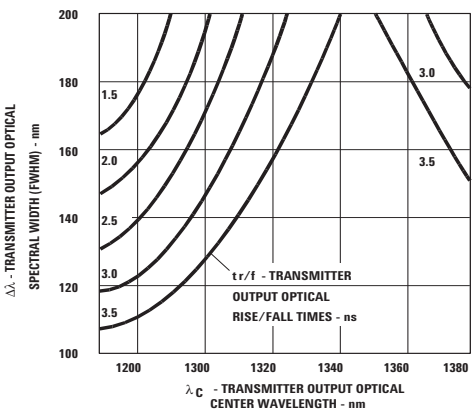
Board Layout- Art Work

The Applications Engineering group has developed Gerber file artwork for a multilayer printed circuit board layout incorporat-ing the recommendations above. Contact your local Avago Technologies sales representative for details.procedures and results on the 1 x 9 Transceiver family, please refer to Applications Note 1075, *Testing and Measuring Electromagnetic Compatibility Performance of the HFBR-510X/-520X Fiber Optic Transceivers.*

Transceiver Reliability and Performance Qualification Data

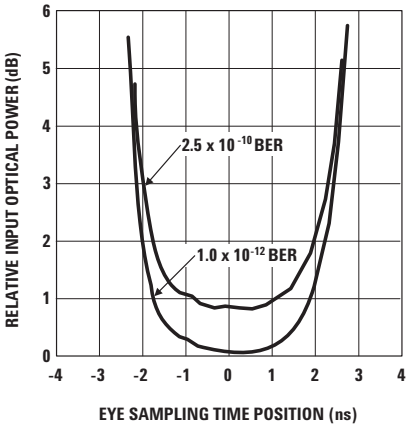
The 2 x 5 transceivers have passed Avago Technologies reliability and performance qualification testing and are undergoing ongoing quality and reliability monitoring. Details are available from your Avago Technologies sales representative.

These transceivers are manufactured at the Avago Technologies Singapore location which is an ISO 9002 certified facility.



HFBR-5903 FDDI TRANSMITTER TEST RESULTS OF λC, Δλ AND tr/f ARE CORRELATED AND COMPLY WITH THE ALLOWED SPECTRAL WIDTH AS A FUNCTION OF CENTER WAVELENGTH FOR VARIOUS RISE AND FALL TIMES.

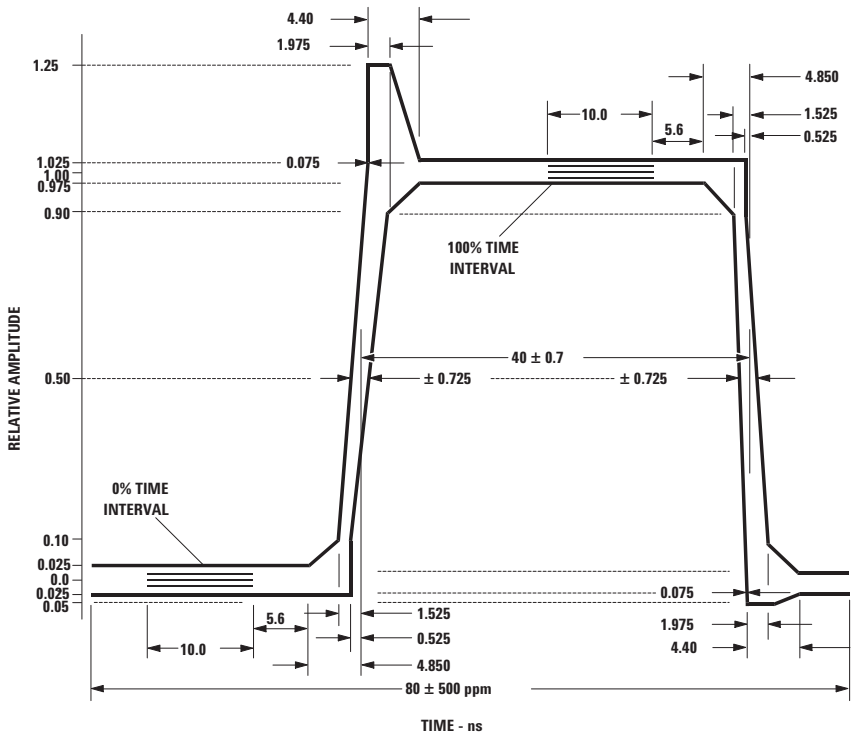
Figure 11. Transmitter Output Optical Spectral Width (FWHM) vs. Transmitter Output Optical Center Wavelength and Rise/Fall Times.



CONDITIONS:

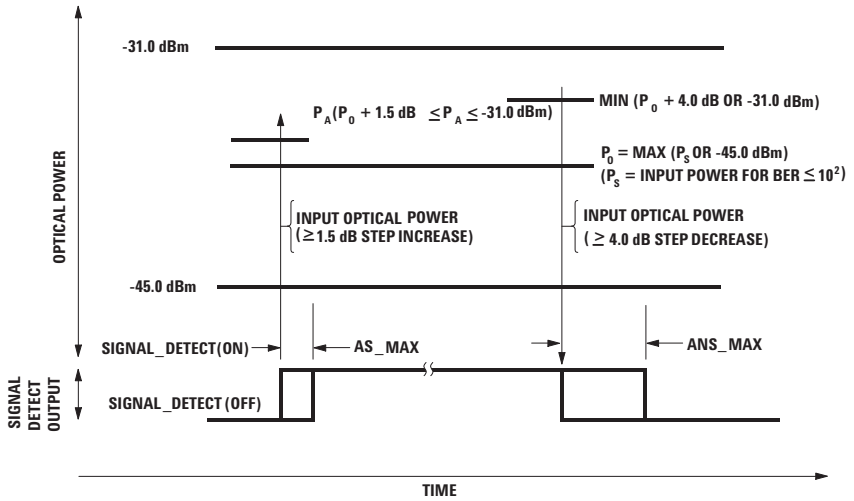
1. T_A = +25 °C
2. V_{CC} = 3.3 V dc
3. INPUT OPTICAL RISE/FALL TIMES = 1.0/2.1 ns.
4. INPUT OPTICAL POWER IS NORMALIZED TO CENTER OF DATA SYMBOL.
5. NOTE 19 AND 20 APPLY.

Figure 13. Relative Input Optical Power vs. Eye Sampling Time Position.



THE HFBR-5903 OUTPUT OPTICAL PULSE SHAPE SHALL FIT WITHIN THE BOUNDARIES OF THE PULSE ENVELOPE FOR RISE AND FALL TIME MEASUREMENTS.

Figure 12. Output Optical Pulse Envelope.



AS _ MAX - MAXIMUM ACQUISITION TIME (SIGNAL).
AS _ MAX IS THE MAXIMUM SIGNAL _ DETECT ASSERTION TIME FOR THE STATION.
AS _ MAX SHALL NOT EXCEED 100.0 µs. THE DEFAULT VALUE OF AS _ MAX IS 100.0 µs.

ANS _ MAX - MAXIMUM ACQUISITION TIME (NO SIGNAL).
ANS _ MAX IS THE MAXIMUM SIGNAL _ DETECT DEASSERTION TIME FOR THE STATION.
ANS _ MAX SHALL NOT EXCEED 350 µs. THE DEFAULT VALUE OF AS _ MAX IS 350 µs.

Figure 14. Signal Detect Thresholds and Timing.

Absolute Maximum Ratings

Stresses in excess of the absolute maximum ratings can cause catastrophic damage to the device. Limits apply to each parameter in isolation, all other parameters having values within the recommended operating conditions. It should not be assumed that limiting values of more than one parameter can be applied to the product at the same time. Exposure to the absolute maximum ratings for extended periods can adversely affect device reliability.

Parameter	Symbol	Min.	Typ.	Max.	Unit	Notes
Storage Temperature	T_S	-40		+100	°C	
Lead Soldering Temperature	T_{SOLD}			+260	°C	
Lead Soldering Time	t_{SOLD}			10	sec.	
Supply Voltage	V_{CC}	-0.5		3.6	V	
Data Input Voltage	V_I	-0.5		V_{CC}	V	
Differential Input Voltage (p-p)	V_D			2.0	V	1
Output Current	I_O			50	mA	

Recommended Operating Conditions

Parameter	Symbol	Min.	Typ.	Max.	Unit	Notes
Ambient Operating Temperature						
HFBR-5903/5903E	T_A	0		+70	°C	A
HFBR-5903A	T_A	-40		+85	°C	B
Supply Voltage	V_{CC}	3.135		3.465	V	
Data Input Voltage - Low	V_{IL} - V_{CC}	-1.810		-1.475	V	
Data Input Voltage - High	V_{IH} - V_{CC}	-1.165		-0.880	V	
Data and Signal Detect Output Load	R_L		50		W	2
Differential Input Voltage (p-p)	V_D		0.800		V	

Notes:

A. Ambient Operating Temperature corresponds to transceiver case temperature of 0°C mininum to +85 °C maximum with necessary airflow applied. Recommended case temperature measurement point can be found in Figure 2.

B. Ambient Operating Temperature corresponds to transceiver case temperature of -40 °C mininum to +100 °C maximum with necessary airflow applied. Recommended case temperature measurement point can be found in Figure 2.

Transmitter Electrical Characteristics

HFBR-5903/5903E (T_A = 0°C to +70°C, V_{CC} = 3.135 V to 3.465 V)
HFBR-5903A (T_A = -40°C to +85°C, V_{CC} = 3.135 V to 3.465 V)

Parameter	Symbol	Min.	Typ.	Max.	Unit	Notes
Supply Current	I_{CC}		133	175	mA	3
Power Dissipation	P_{DISS}		0.45	0.60	W	5a
Data Input Current - Low	I_{IL}	-350	-2		µA	
Data Input Current -High	I_{IH}		18	350	µA	

Receiver Electrical Characteristics

HFBR-5903/5903E (T_A = 0°C to +70°C, V_{CC} = 3.135 V to 3.465 V)
HFBR-5903A (T_A = -40°C to +85°C, V_{CC} = 3.135 V to 3.465 V)

Parameter	Symbol	Min.	Typ.	Max.	Unit	Notes
Supply Current	I_{CC}		65	120	mA	4
Power Dissipation	P_{DISS}		0.225	0.415	W	5b
Data Output Voltage - Low	V_{OL} - V_{CC}	-1.840		-1.620	V	6
Data Output Voltage - High	V_{OH} - V_{CC}	-1.045		-0.880	V	6
Data Output Rise Time	t_r	0.35		2.2	ns	7
Data Output Fall Time	t_f	0.35		2.2	ns	7
Signal Detect Output Voltage - Low	V_{OL} - V_{CC}	-1.840		-1.620	V	6
Signal Detect Output Voltage - High	V_{OH} - V_{CC}	-1.045		-0.880	V	6
Signal Detect Output Rise Time	t_r	0.35		2.2	ns	7
Signal Detect Output Fall Time	t_f	0.35		2.2	ns	7
Power Supply Noise Rejection	PSNR		50		mV	

Transmitter Optical Characteristics

HFBR-5903/5903E (T_A = 0°C to +70°C, V_{CC} = 3.135 V to 3.465 V)
HFBR-5903A (T_A = -40°C to +85°C, V_{CC} = 3.135 V to 3.465 V)

Parameter		Symbol	Min.	Typ.	Max.	Unit	Notes
Output Optical Power 62.5/125 µm. NA = 0.275 fiber	BOL EOL	P_O	-19 -20	-15.7	-14	dBm avg.	11
Output Optical Power 50/125 µm. NA = 0.20 fiber	BOL EOL	P_O	-22.5 -23.5	-20.3	-14	dBm avg.	11
Optical Extinction Ratio				0.05 -33	0.2 -27	% dB	12
Output Optical Power at Logic Low "0" State		P_O ("0")			-45	dBm avg	13
Center Wavelength		l_c	1270	1308	1380	nm	14 Fig 11
Spectral Width - FWHM - RMS		DI		147 63		nm	14 Fig 11
Optical Rise Time		t_r	0.6	1.9	3.0	ns	14/15 Fig 11, 12
Optical Fall Time		t_f	0.6	1.6	3.0	ns	14/15 Fig 11, 12
Duty Cycle Distortion Contributed by the Transmitter		DCD		0.02	0.6	ns p-p	16
Data Dependent Jitter Contributed by the Transmitter		DDJ		0.02	0.6	ns p-p	17
Random Jitter Contributed by the Transmitter		RJ		0	0.69	ns p-p	18

Receiver Optical and Electrical Characteristics

HFBR-5903/5903E (T_A = 0°C to +70°C, V_{CC} = 3.135 V to 3.465 V)
HFBR-5903A (T_A = -40°C to +85°C, V_{CC} = 3.135 V to 3.465 V)

Parameter	Symbol	Min.	Typ.	Max.	Unit	Notes
Input Optical Power Minimum at window edge	$P_{IN\ MIN}$ (W)		-33.5	-31	dBm avg.	19 Fig 13
Minimum Input Optical Power at eye center	$P_{IN\ MIN}$ (C)		-34.5	-31.8	dBm avg.	20 Fig 13
Input Optical Power Maximum	$P_{IN\ MAX}$	-14	-11.8		dBm avg.	19
Operating Wavelength	l	1270		1380	nm	
Duty Cycle Distortion Contributed by the Receiver	DCD		0.02	0.4	ns p-p	8
Data Dependent Jitter Contributed by the Receiver	DDJ		0.35	1.0	ns p-p	9
Random Jitter Contributed by the Receiver	RJ		1.0	2.14	ns p-p	10
Signal Detect - Asserted	P_A	P_D + 1.5 dB		-33	dBm avg	21, 22 Fig 14
Signal Detect - Deasserted	P_D	-45			dBm avg	23, 24 Fig 14
Signal Detect - Hysteresis	P_A - P_D	1.5	2.4		dB	Fig 14
Signal Detect Assert Time (off to on)	AS_Max	0	2	100	µs	21, 22 Fig 14
Signal Detect Deassert Time (on to off)	ANS_Max	0	5	350	µs	23, 24 Fig 14

Notes:

1. This is the maximum voltage that can be applied across the Differential Transmitter Data Inputs to prevent damage to the input ESD protection circuit.
2. The outputs are terminated with 50 Ω connected to V_{CC} -2 V.
3. The power supply current needed to operate the transmitter is provided to differential ECL circuitry. This circuitry maintains a nearly constant current flow from the power supply. Constant current operation helps to prevent unwanted electrical noise from being generated and conducted or emitted to neighboring circuitry.
4. This value is measured with the outputs terminated into 50 Ω connected to V_{CC} - 2 V and an Input Optical Power level of -14 dBm average.

5a. The power dissipation of the transmitter is calculated as the sum of the products of supply voltage and current.

5b. The power dissipation of the receiver is calculated as the sum of the products of supply voltage and currents, minus the sum of the products of the output voltages and currents.

6. This value is measured with respect to V_{CC} with the output terminated into 50 Ω connected to V_{CC} - 2 V.
7. The output rise and fall times are measured between 20% and 80% levels with the output connected to V_{CC} -2 V through 50 Ω.
8. Duty Cycle Distortion contributed by the receiver is measured at the 50% threshold using an IDLE Line State, 125 MBd (62.5 MHz square-wave), input signal. The input optical power level is -20 dBm average. See Application Information - Transceiver Jitter Section for further information.
9. Data Dependent Jitter contributed by the receiver is specified with the FDDI DDJ test pattern described in the FDDI PMD Annex A.5. The input optical power level is -20 dBm average. See Application Information - Transceiver Jitter Section for further information.
10. Random Jitter contributed by the receiver is specified with an IDLE Line State, 125 MBd (62.5 MHz square-wave), input signal. The input optical power level is at maximum "PIN Min. (W)". See Application Information - Transceiver Jitter Section for further information.
11. These optical power values are measured with the following conditions:
    - The Beginning of Life (BOL) to the End of Life (EOL) optical power degradation is typically 1.5 dB per the industry convention for long wavelength LEDs. The actual degradation observed in Avago Technologies' 1300 nm LED products is < 1 dB, as specified in this data sheet.
    - Over the specified operating voltage and temperature ranges.
    - With HALT Line State, (12.5 MHz square-wave), input signal.
    - At the end of one meter of noted optical fiber with cladding modes removed.

    The average power value can be converted to a peak power value by adding 3 dB. Higher output optical power transmitters are available on special request. Please consult with your local Avago Technologies sales representative for further details.
12. The Extinction Ratio is a measure of the modulation depth of the optical signal. The data "0" output optical power is compared to the data "1" peak output optical power and expressed as a percentage. With the transmitter driven by a HALT Line State (12.5 MHz square-wave) signal, the average optical power is measured. The data "1" peak power is then calculated by adding 3 dB to the measured average optical power. The data "0" output optical power is found by measuring the optical power when the transmitter is driven by a logic "0" input. The extinction ratio is the ratio of the optical power at the "0" level compared to the optical power at the "1" level expressed as a percentage or in decibels.
13. The transmitter provides compliance with the need for Transmit_ Disable commands from the FDDI SMT layer by providing an Output Optical Power level of < -45 dBm average in response to a logic "0" input. This specification applies to either 62.5/125 µm or 50/125 µm fiber cables.
14. This parameter complies with the FDDI PMD requirements for the trade-offs between center wavelength, spectral width, and rise/fall times shown in Figure 11.
15. This parameter complies with the optical pulse envelope from the FDDI PMD shown in Figure 12. The optical rise and fall times are measured from 10% to 90% when the transmitter is driven by the FDDI HALT Line State (12.5 MHz square-wave) input signal.
16. Duty Cycle Distortion contributed by the transmitter is measured at a 50% threshold using an IDLE Line State, 125 MBd (62.5 MHz square-wave), input signal. See Application Information - Transceiver Jitter Performance Section of this data sheet for further details.
17. Data Dependent Jitter contributed by the transmitter is specified with the FDDI test pattern described in FDDI PMD Annex A.5. See Application Information - Transceiver Jitter Performance Section of this data sheet for further details.
18. Random Jitter contributed by the transmitter is specified with an IDLE Line State, 125 MBd (62.5 MHz square-wave), input signal. See Application Information - Transceiver Jitter Performance Section of this data sheet for further details.
19. This specification is intended to indicate the performance of the receiver section of the transceiver when Input Optical Power signal characteristics are present per the following definitions. The Input Optical Power dynamic range from the minimum level (with a window time-width) to the maximum level is the range over which the receiver is guaranteed to provide output data with a Bit Error Rate (BER) better than or equal to 2.5×10^{-10}.
    - At the Beginning of Life (BOL)
    - Over the specified operating temperature and voltage ranges
    - Input symbol pattern is the FDDI test pattern defined in FDDI PMD Annex A.5 with 4B/5B NRZI encoded data that contains a duty cycle base-line wander effect of 50 kHz. This sequence causes a near worst case condition for inter-symbol interference.
    - Receiver data window time-width is 2.13 ns or greater and centered at mid-symbol. This worst case window time-width is the minimum allowed eye-opening presented to the FDDI PHY PM_Data indication input (PHY input) per the example in FDDI PMD Annex E. This minimum window time-width of 2.13 ns is based upon the worst case FDDI PMD Active Input Interface optical conditions for peak-to-peak DCD (1.0 ns), DDJ (1.2 ns) and RJ (0.76 ns) presented to the receiver.

    To test a receiver with the worst case FDDI PMD Active Input jitter condition requires exacting control over DCD, DDJ and RJ jitter components that is difficult to implement with production test equipment. The receiver can be equivalently tested to the worst case FDDI PMD input jitter conditions and meet the minimum output data window time-width of 2.13 ns. This is accomplished by using a nearly ideal input optical signal (no DCD, insignificant DDJ and RJ) and measuring for a wider window time-width of 4.6 ns. This is possible due to the cumulative effect of jitter components through their superposition (DCD and DDJ are directly additive and RJ components are rms additive). Specifically, when a nearly ideal input optical test signal is used and the maximum receiver peak-to-peak jitter contributions of DCD (0.4 ns), DDJ (1.0 ns), and RJ (2.14 ns) exist, the minimum window time-width becomes 8.0 ns -0.4 ns - 1.0 ns - 2.14 ns = 4.46 ns, or conservatively 4.6 ns. This wider window time-width of 4.6 ns guarantees the FDDI PMD Annex E minimum window time-width of 2.13 ns under worst case input jitter conditions to the Avago Technologies receiver.
    - Transmitter operating with an IDLE Line State pattern, 125 MBd (62.5 MHz square-wave), input signal to simulate any cross-talk present between the transmitter and receiver sections of the transceiver.
20. All conditions of Note 19 apply except that the measurement is made at the center of the symbol with no window time-width.
21. This value is measured during the transition from low to high levels of input optical power. At Signal Detect Deassert, the receiver outputs Data Out and Data Out Bar go to steady PECL levels High and Low respectively.

22. The Signal Detect output shall be asserted within 100 µs after a step increase of the Input Optical Power. The step will be from a low Input Optical Power, -45 dBm, into the range between greater than P_A, and -14 dBm. The BER of the receiver output will be 10^{-2} or better during the time, LS_Max (15 µs) after Signal Detect has been asserted. See Figure 14 for more information.
23. This value is measured during the transition from high to low levels of input optical power. The maximum value will occur when the input optical power is either -45 dBm average or when the input optical power yields a BER of 10^{-2} or larger, whichever power is higher.
24. Signal detect output shall be de-asserted within 350 µs after a step decrease in the Input Optical Power from a level which is the lower of; -31 dBm or P_D + 4 dB (P_D is the power level at which signal detect was deasserted), to a power level of -45 dBm or less. This step decrease will have occurred in less than 8 ns. The receiver output will have a BER of 10^{-2} or better for a period of 12 µs or until signal detect is deasserted. The input data stream is the Quiet Line State. Also, signal detect will be deasserted within a maximum of 350 µs after the BER of the receiver output degrades above 10^{-2} for an input optical data stream that decays with a negative ramp function instead of a step function. See Figure 14 for more information. At Signal Detect Deassert, the receiver outputs Data Out and Data Out Bar go to steady PECL levels High and Low respectively.

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