19-0891; Rev 1; 8/93

MAXIM

CMOS High Speed 8 Bit A/D Converter with Reference and Track/Hold Function

General Description

The MAX150/MX7820 is a high speed, microprocessor compatible, 8 bit analog to digital converter which uses a half-flash technique to achieve a conversion time of 1.34 μs. The converter has a 0V to +5V analog input range and uses a single +5V supply.

A built-in track-and-hold function is included, eliminating the need for an external track-and-hold for input slew rates up to 100mV/μs. The MAX150 also provides an on-chip 2.5 V reference output, making it a complete analog to digital converter.

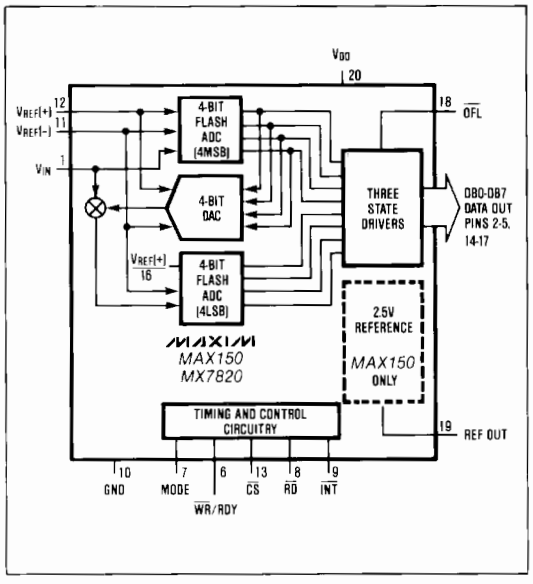
The A/Ds easily interface with microprocessors by appearing as a memory location or I/O port without the need for external interfacing logic. The data outputs use latched, three-state buffer circuitry to allow direct connection to a microprocessor data bus or system input port. An over-flow output is also provided for cascading devices to achieve higher resolution.

The MX7820 is pin compatible with Analog Devices' AD7820. The MAX150 is also compatible with the MX7820 but also includes an internal 2.5V reference.

Applications

Digital Signal Processing
High Speed Data Acquisition
Telecommunications
High Speed Servo Loops
Audio Systems

Functional Block Diagram



Features

- **Fast Conversion Time: 1.34μs Max.**
- **Built-in Track-and-Hold Function**
- **No Adjustment Required**
- **No External Clock**
- **Single +5V Supply**
- **Easy Interface To Microprocessors**
- **Internal 2.5V Reference (MAX150 only)**

Ordering Information

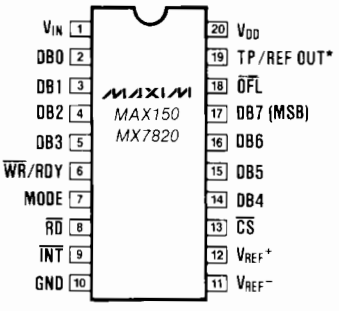
PART	TEMP. RANGE	PACKAGE†	ERROR
MAX150ACPP	0°C to +70°C	Plastic DIP	±½ LSB
MAX150BCPP	0°C to +70°C	Plastic DIP	±1 LSB
MAX150BC/D	0°C to +70°C	Dice*	±1 LSB
MAX150ACWP	0°C to +70°C	Small Outline	±½ LSB
MAX150BCWP	0°C to +70°C	Small Outline	±1 LSB
MAX150AEPP	-40°C to +85°C	Plastic DIP	±½ LSB
MAX150BEPP	-40°C to +85°C	Plastic DIP	±1 LSB
MAX150AEWP	-40°C to +85°C	Small Outline	±½ LSB
MAX150BEWP	-40°C to +85°C	Small Outline	±1 LSB
MAX150AMJP	-55°C to +125°C	CERDIP	±½ LSB
MAX150BMJP	-55°C to +125°C	CERDIP	±1 LSB

† *All devices — 20 lead packages*
* *Consult factory for dice specifications.*

Ordering Information continued on last page

Pin Configuration

Top View



*REF OUT — MAX150 only.

Call toll free 1-800-998-8800 for free samples or literature.

CMOS High Speed 8 Bit A/D Converter with Reference and Track/Hold Function

ABSOLUTE MAXIMUM RATINGS

Supply Voltage, V_{DD} to GND ..... 0V, +10V
Voltage at any other pins
(Pins 1-9, 11-19) ..... GND - 0.3V, V_{DD} +0.3V
Output current (Pin 19) 30mA
Power Dissipation (Any Package) to 75°C 450mW
Derate Above +75°C by ..... 6mW/°C

Operating Temperature Ranges
MAX150XCXX, MX7820LN/KN/LCWP/KCWP ... 0°C to +70°C
MX7820BQ/CQ ..... -25°C to +85°C
MAX150XEXX ..... -40°C to +85°C
MAX150XMXX, MX7820TQ/UQ ..... -55°C to +125°C
Storage Temperature Range ..... -65°C to +160°C
Lead Temperature (Soldering 10 seconds) ..... +300°C

Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions above those indicated in the operational sections of the specification is not implied. Exposure to absolute maximum ratings conditions for extended periods may affect the device reliability.

ELECTRICAL CHARACTERISTICS

(V_{DD} = +5V, V_{REF}^+ = +5V, V_{REF}^- = GND, RD-MODE, T_A = T_{MIN} to T_{MAX}, unless otherwise noted)

PARAMETER	SYMBOL	CONDITIONS	MIN.	TYP.	MAX.	UNITS
ACCURACY						
Resolution			8			bits
Total Unadjusted Error (Note 1)		MAX150A, MX7820L/C/U MAX150B, MX7820K/B/T			±1/2 ±1	LSB
No Missing Codes Resolution			8			bits
REFERENCE INPUT						
Reference Resistance		T_A = +25°C T_A = T_{MIN} to T_{MAX}	1.4 1.25	2.2	4.0 4.0	kΩ
V_{REF}^+ Input Voltage Range			V_{REF}^-		V_{DD} + 0.1	V
V_{REF}^- Input Voltage Range			GND - 0.1		V_{REF}^+	V
REFERENCE OUTPUT MAX150 ONLY (Note 2)						
Output Voltage	**REF OUT**	**T_A = +25°C**	**2.47**	**2.50**	**2.53**	V
Load Regulation		**I_L = 0 to 10mA T_A = +25°C**		**-6**	**-10**	mV
Power Supply Sensitivity		**V_{DD} ±5% T_A = +25°C**		**±1**	**±3**	mV
Temperature Drift (Note 3)		**MAX150XC T_A = 0°C to +70°C** **MAX150XE T_A = -40°C to +85°C** **MAX150XM T_A = -55°C to +125°C**		**40** **40** **60**	**70** **70** **100**	ppm/°C
Output Noise				**200**		µV/rms
Capacitive Load					**0.01**	µF
ANALOG INPUT						
Analog Input Voltage Range	V_{INR}		GND - 0.1		V_{DD} + 0.1	V
Analog Input Capacitance	C_{VIN}			45		pF
Analog Input Current	I_{VIN}	V_{IN} = 0V to +5V T_A = +25°C T_A = T_{MIN} to T_{MAX}			±0.3 ±3	µA
Slew Rate, Tracking (Note 4)	SR			0.2	0.1	V/µs
LOGIC INPUTS						
Input HIGH Voltage	V_{INH}	$\overline{CS}$, $\overline{WR}$, $\overline{RD}$; MAX150 MX7820 MODE	2.0 2.4 3.5			V
Input LOW Voltage	V_{INL}	$\overline{CS}$, $\overline{WR}$, $\overline{RD}$ MODE			0.8 1.5	V
Input High Current	I_{INH}	$\overline{CS}$, $\overline{RD}$; T_A = +25°C T_{MIN} to T_{MAX} $\overline{WR}$; T_A = +25°C T_{MIN} to T_{MAX} MODE; T_A = +25°C T_{MIN} to T_{MAX}		 50	0.3 1 0.3 3 150 200	µA

Note 1: Total unadjusted error includes offset, full-scale and linearity errors.
Note 2: Specified with no external load unless otherwise noted.
Note 3: Temperature drift is defined as change in output voltage from +25°C to T_{MIN} or T_{MAX} divided by (25 - T_{MIN}) or (T_{MAX} - 25).
Note 4: Sample tested at +25°C by Quality Assurance to ensure compliance.

CMOS High Speed 8 Bit A/D Converter with Reference and Track/Hold Function

ELECTRICAL CHARACTERISTICS (continued)

(V_{DD} = +5V, V_{REF}^+ = +5V, V_{REF}^- = GND, RD-MODE, T_A = T_{MIN} to T_{MAX}, unless otherwise noted)

PARAMETER	SYMBOL	CONDITIONS	MIN.	TYP.	MAX.	UNITS
LOGIC INPUTS (continued)						
Input Low Current	I_{INL}	$\overline{CS}$, $\overline{RD}$, $\overline{WR}$, MODE T_A = +25°C T_{MIN} to T_{MAX}			-0.3 -1	µA
Input Capacitance (Note 5)	C_{IN}	$\overline{CS}$, $\overline{RD}$, $\overline{WR}$, MODE		5	8	pF
LOGIC OUTPUTS						
Output HIGH Voltage	V_{OH}	DB0-DB7, $\overline{OFL}$, $\overline{INT}$ V_{DD} = +4.75V I_{OUT} = -360µA V_{DD} = +4.75V I_{OUT} = -10µA	4.0 4.5			V
Output LOW Voltage	V_{OL}	DB0-DB7, $\overline{OFL}$, $\overline{INT}$, RDY V_{DD} = +4.75V I_{OUT} = 1.6mA			0.4	V
Three-state Output Current		DB0-DB7, RDY T_A = +25°C T_{MIN} to T_{MAX}			±0.3 ±3	µA
Output Source Current	I_{SRC}	DB0-DB7, $\overline{OFL}$, $\overline{INT}$; V_{OUT} = 0	-10	-25		mA
Output Sink Current	I_{SINK}	DB0-DB7, $\overline{OFL}$, $\overline{INT}$, RDY; V_{OUT} = V_{DD}	15	40		mA
Output Capacitance (Note 5)	C_{OUT}	DB0-DB7, $\overline{OFL}$, $\overline{INT}$, RDY		5	8	pF
POWER SUPPLY						
Supply Voltage	V_{DD}	+5V ±5% for specified performance	4.75		5.25	V
Supply Current	I_{DD}	$\overline{CS}$ = $\overline{WR}$ = $\overline{RD}$ = 0 T_A = +25°C T_{MIN} to T_{MAX}		5	10 15	mA
Power Dissipation		$\overline{CS}$ = $\overline{WR}$ = $\overline{RD}$ = 0		25		mW
Power Supply Sensitivity	PSS	V_{DD} = ±5%		±1/16	±1/4	LSB

Note 5: Guaranteed by design.

Pin Description

PIN	NAME	FUNCTION
1	V_{IN}	Analog input; range = GND < V_{IN} < V_{DD}.
2	DB0	Three-state data output, bit 0 (LSB).
3	DB1	Three-state data output, bit 1.
4	DB2	Three-state data output, bit 2.
5	DB3	Three-state data output, bit 3.
6	$\overline{WR}$/RDY	WRITE control input/READY status output. See Digital Interface section.
7	MODE	Mode selection input. This input is internally pulled low with a 50µA current source. RD Mode: MODE low/open. WR-RD Mode: MODE high.
8	$\overline{RD}$	READ input. $\overline{RD}$ must be low to access data. See Digital Interface section.
9	$\overline{INT}$	INTERRUPT output. $\overline{INT}$ going low indicates the completion of a conversion. See Digital Interface section.
10	GND	Ground.

PIN	NAME	FUNCTION
11	V_{REF}^-	Lower limit of reference span. Sets the zero code voltage. Range: GND to V_{REF}^+.
12	V_{REF}^+	Upper limit of reference span. Sets the Full Scale input voltage. Range: V_{REF}^- to V_{DD}.
13	$\overline{CS}$	CHIP-SELECT input. $\overline{CS}$ must be low for the device to recognize $\overline{WR}$ or $\overline{RD}$ inputs
14	DB4	Three-state data output, bit 4.
15	DB5	Three-state data output, bit 5.
16	DB6	Three-state data output, bit 6.
17	DB7	Three-state data output, bit 7 (MSB).
18	$\overline{OFL}$	Overflow Output. If the analog input is greater than V_{REF}^+, $\overline{OFL}$ will be high at the end of the conversion. It can be used to cascade two or more devices to increase resolution.
19	TP REF OUT	Test pin for MX7820. Do not connect pin 19 for MX7820. 2.5V Internal reference output for MAX150 only.
20	V_{DD}	Power supply voltage, +5V.

CMOS High Speed 8 Bit A/D Converter with Reference and Track/Hold Function

TIMING CHARACTERISTICS (Note 1, 2) — MAX150, MX7820

(V_{DD} = +5V, V_{REF}^+ = +5V, V_{REF}^- = GND, T_A = T_{MIN} to T_{MAX}, unless otherwise specified.)

PARAMETER	SYMBOL	CONDITIONS	T_A = +25°C			MAX150C/E MX7820K/L/B/C		MAX150M MX7820T/U		UNITS
			MIN.	TYP.	MAX.	MIN.	MAX.	MIN.	MAX.	
CS to RD, WR Setup Time	t_{CSS}		0			0		0		ns
CS to RD Setup Time	t_{CSS1}	For data-access (Note 5)	20			30		30		ns
CS to RD, WR Hold Time	t_{CSH}		0			0		0		ns
CS to RDY Delay	t_{RDY}	C_L = 50pF, R = 3kΩ		35	70		90		100	ns
Conversion Time (RD Mode)	t_{CRD}			1.2	1.6		2.0		2.5	µs
Data Access Time (RD Mode) (See Figure 4)	t_{ACC0}	(Note 3)		t_{CRD} + 10	t_{CRD} + 20		t_{CRD} + 35		t_{CRD} + 50	ns
RD to INT Delay (RD Mode)	t_{INTH}	C_L = 50pF		60	125		175		225	ns
Data Hold Time	t_{DH}	(Note 4)		40	60		80		100	ns
Delay Time Between Conversions	t_P		500			600		600		ns
Write Pulse Width	t_{WR}		600		50,000	600	50,000	600	50,000	ns
Conversion Time (WR/RD Mode)	t_{CWR-RD}		1.34			1.5		1.53		µs
Delay between WR and RD Pulses	t_{RD}		600			700		700		ns
Data Access Time (WR/RD Mode) (See Figure 6)	t_{ACC1}	$t_{RD} < t_{INTL}$, (Note 3)		110	160		225		250	ns
RD to INT Delay	t_{RI}			100	140		200		225	ns
WR to INT Delay	t_{INTL}			600	1000		1400		1700	ns
Data Access Time (WR/RD Mode) (See Figure 5)	t_{ACC2}	$t_{RD} > t_{INTL}$, (Note 3)		60	70		90		110	ns
WR to INT Delay (Stand-Alone)	t_{IHWR}	C_L = 50pF		70	100		130		150	ns
Data Access Time After INT	t_{ID}			10	50		65		75	ns

Note 1: Sample tested at +25°C by Quality Assurance to ensure compliance.
Note 2: All input control signals are specified with t_R = t_F = 20ns (10% to 90% of +5V) and timed from a voltage level of 1.6V.
Note 3: Measured with load circuits of Figure 1 and defined as the time required for an output to cross 0.8V or 2.4V.
Note 4: Defined as the time required for the data lines to change 0.5V when loaded with the circuits of Figure 2.
Note 5: Guaranteed by design. Not production tested.

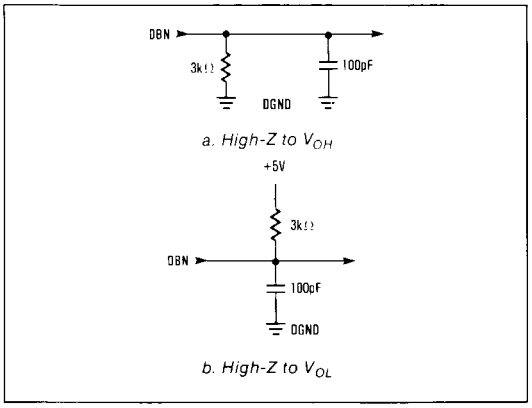


Figure 1. Load Circuits for Data Access Time Test

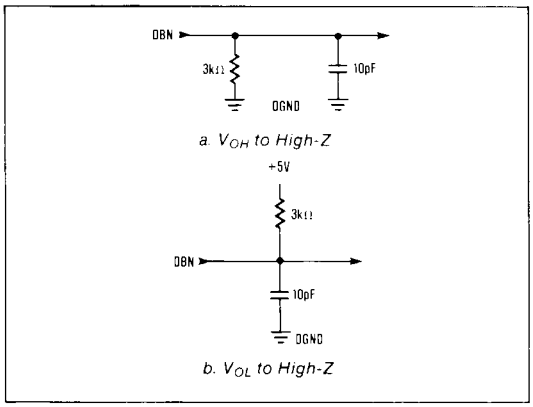
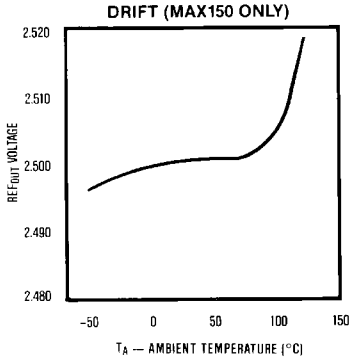


Figure 2. Load Circuits for Data Hold Time Test

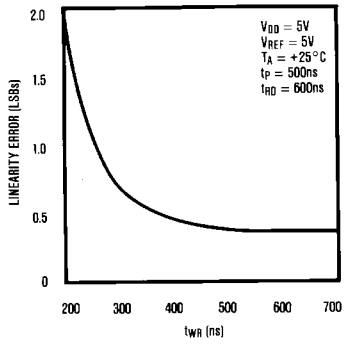
CMOS High Speed 8 Bit A/D Converter with Reference and Track/Hold Function

Typical Operating Characteristics

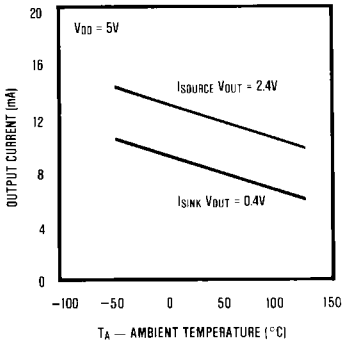
REFERENCE TEMPERATURE DRIFT (MAX150 ONLY)



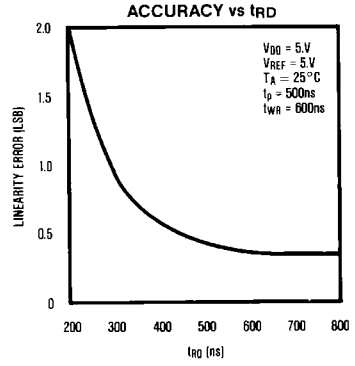
ACCURACY vs. tWR



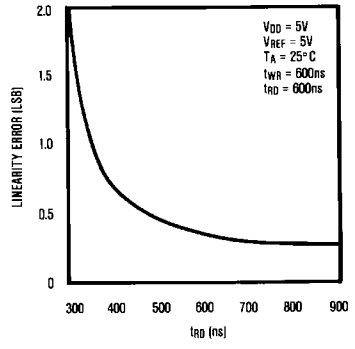
OUTPUT CURRENT vs. TEMPERATURE



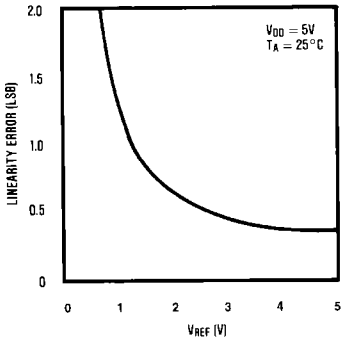
ACCURACY vs tRD



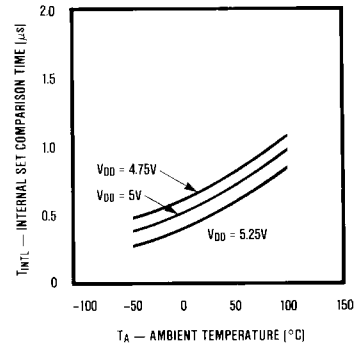
ACCURACY vs. tP



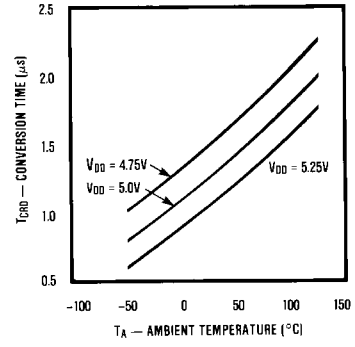
ACCURACY vs. VREF [VREF = VREF(+) - VREF(-)]



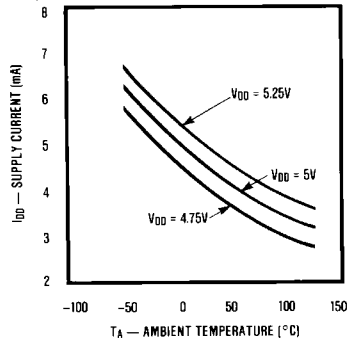
tINTL INTERNAL TIME DELAY vs. TEMPERATURE



CONVERSION TIME (RD MODE) vs. TEMPERATURE



POWER SUPPLY CURRENT vs. TEMPERATURE (NOT INCLUDING REFERENCE LADDER)



CMOS High Speed 8 Bit A/D Converter with Reference and Track/Hold Function

Detailed Description

Converter Operation

The MAX150/MX7820 uses a "half-flash" conversion technique (see Functional Block Diagram). Two 4-bit flash A/D converter sections are used to achieve an 8-bit result. Using 15 comparators, the upper 4-bit MS (most significant) flash A/D compares the unknown input voltage to the reference ladder and provides the upper four data bits.

An internal DAC uses the MS bits to generate the analog result from the first flash conversion, and generates a residue voltage which is the difference of the unknown input and the DAC voltage. The residue is then compared to the reference ladder using 15 LS (least significant) flash comparators to obtain the lower four bits of the output. An additional overrange comparator detects if the analog input is greater than the reference voltage.

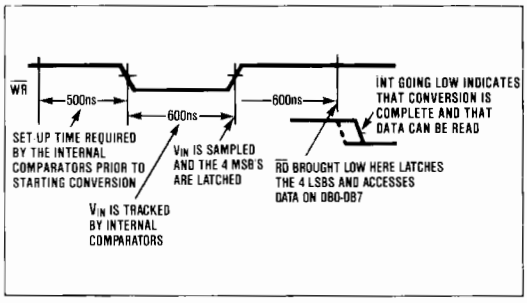


Figure 3. Operating Sequence (WR-RD Mode).

Operating Sequence

The operating sequence for the WR-RD Mode is shown in Figure 3. The conversion is initiated by a falling edge of WR. The comparator inputs track the analog input voltage for the duration of WR low. A minimum of 600ns is required for the input voltage to be acquired. When WR returns high, the MS flash result is latched into the output buffers and the LS conversion begins. INT goes low approximately 600ns later, indicating the end of the conversion, and that the lower 4 data bits are latched into the output buffers. RD going low then accesses the data.

If an externally controlled conversion time is required, the RD line can be brought low as soon as 600ns after WR goes high. This will latch the lower 4 data bits and output the conversion result on DB0-DB7. At least 500ns setup time is required from INT going low to the start of another conversion (WR going low).

Digital Interface

The MAX150/MX7820 has two basic interface modes which are set by the status of the MODE input pin. When this pin is low, the converter is in the RD mode, when this pin is high the converter is set up for the WR-RD mode.

RD Mode

In RD mode, conversion control and data access is controlled by the RD input (see Figure 4). The conversion is initiated by taking RD low. RD is then kept low until output data appears. This mode is useful for microprocessors which can be forced into a WAIT state. The processor can start a conversion, wait, and then read data with a single READ instruction.

Pin 6 (WR/RDY) is configured as a status output (RDY) in RD mode. This output can be used to drive the READY or WAIT input of a processor. RDY is an open collector output (with no internal pull-up device) which goes low after the falling edge of CS and goes high impedance at the end of the conversion. An INT output is also provided which goes low at the end of the conversion and returns high on the rising edge of CS or RD.

WR-RD Mode

In the WR-RD mode, pin 6 (WR/RDY) is configured as the WRITE input for the converter. With CS low, a conversion is initiated on the falling edge of WR. Several options exist for reading the data from the converter.

Using Internal Delay

In the first of these options the processor waits for INT output to go low before reading the data (Figure 5). INT typically goes low 600ns after the rising edge of WR, indicating that the conversion is complete and the result is available in the output latch. With CS low, data outputs DB0-DB7 can be accessed by pulling RD low. INT is then reset by the rising edge of CS or RD.

Reading Before Delay

An alternative option can be used to externally control the conversion time (see Figure 6). The internally generated 600ns delay varies somewhat with temperature and supply voltage (see Typical Operating Characteristics) and can be overridden with RD. To achieve this, the status of INT is ignored and RD is brought low as soon as 600ns after the rising edge of WR. This completes the conversion and enables the output buffers, DB0-DB7, which contain the conversion result. INT also goes low after the falling edge of RD and is reset on the rising edge of RD or CS.

CMOS High Speed 8 Bit A/D Converter with Reference and Track/Hold Function

Pipelined Operation

In addition to the two standard WR-RD mode options, "pipe-lined" operation can be achieved by tying $\overline{WR}$ and $\overline{RD}$ together (see Figure 7). With $\overline{CS}$ low, $\overline{WR}$ and $\overline{RD}$ going low initiates a conversion, and reads the result of the previous conversion at the same time.

Stand-Alone Operation

The converter can also be used in a stand-alone operation (see Figure 8). $\overline{CS}$ and $\overline{RD}$ are tied low and a conversion is initiated by pulling $\overline{WR}$ low. Output data is valid approximately 600ns after the rising edge of $\overline{WR}$.

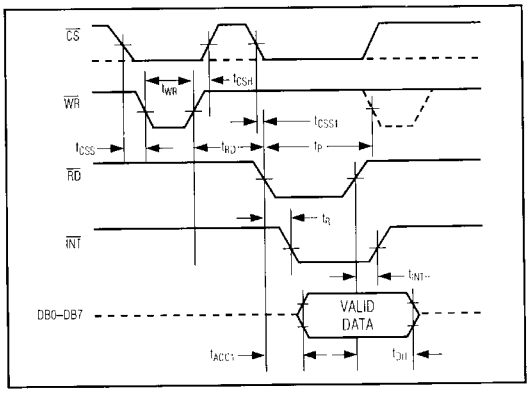


Figure 6. WR-RD Mode Timing ($t_{RD} < t_{INTL}$).

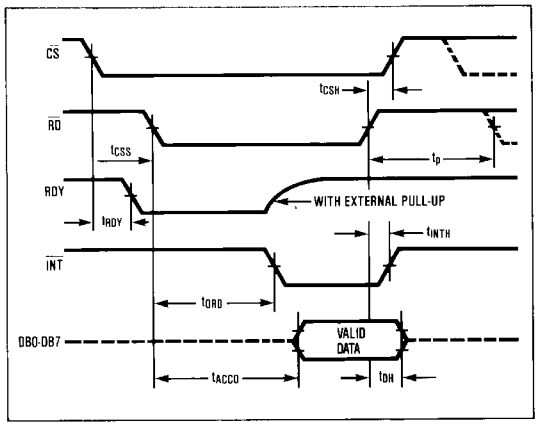


Figure 4. RD Mode Timing.

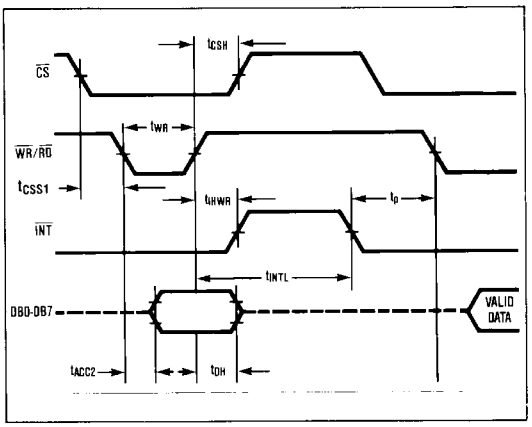


Figure 7. WR-RD Mode Pipe-Lined Timing $\overline{WR} = \overline{RD}$.

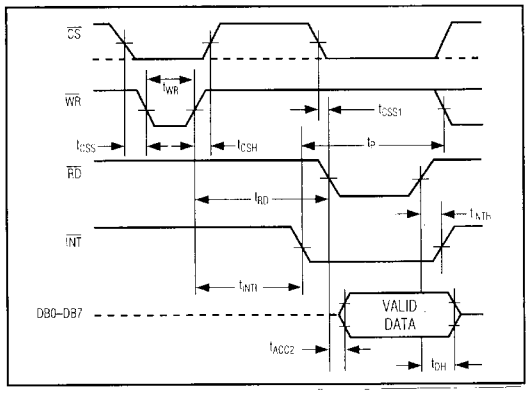


Figure 5. WR-RD Mode Timing ($t_{RD} > t_{INTL}$).

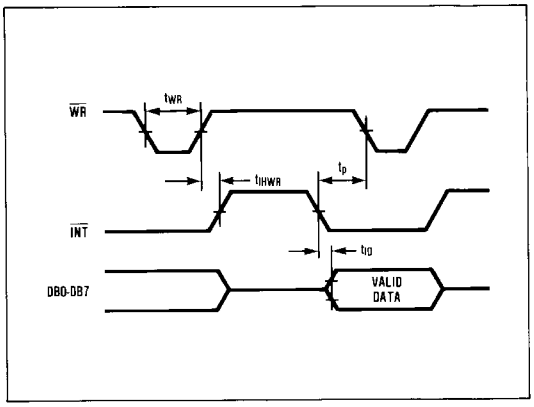


Figure 8. WR-RD Mode Stand-Alone Timing $\overline{CS} = \overline{RD} = 0$.

CMOS High Speed 8 Bit A/D Converter with Reference and Track/Hold Function

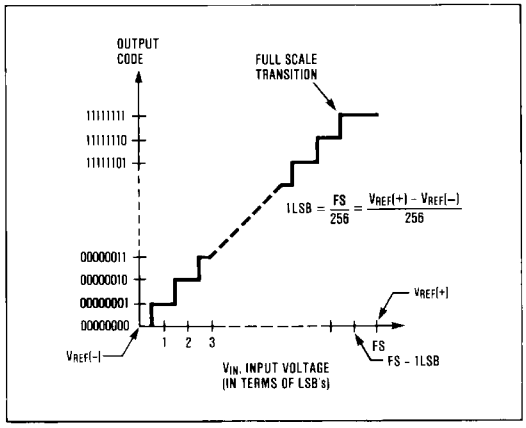


Figure 9. Transfer Function.

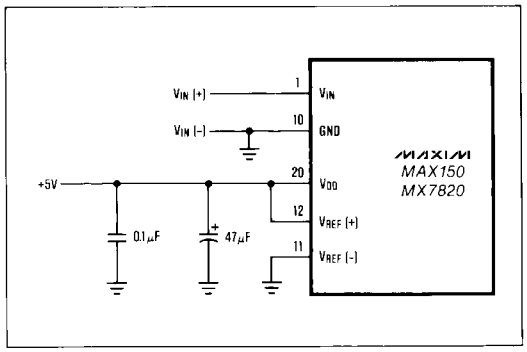


Figure 10a. Power Supply as Reference.

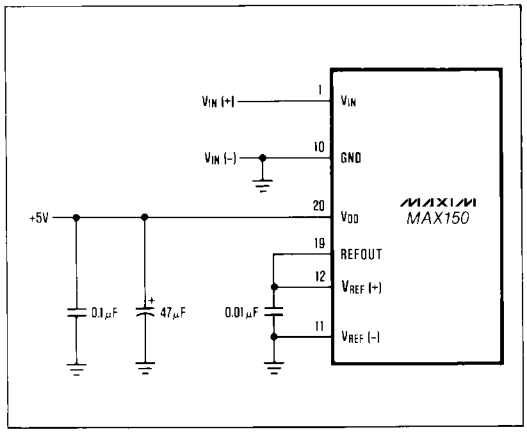


Figure 10c. Internal Reference (MAX150 only).

Analog Considerations

Reference

The MAX150 includes an internal 2.5V reference (REFOUT) which is appropriate for the majority of 8 bit measurement applications. To use the on-chip reference, connect REFOUT, pin 19, to V_{REF}^+, pin 12, and connect V_{REF}^-, pin 11, to ground. The 2.5V output is referred to GND, pin 10. Both the MAX150 and the MX7820, which does not have an on-chip reference, can be used with an external reference if desired.

Figure 10 shows some possible reference connections. For the MAX150, a 0.01µF bypass capacitor to GND should be used to reduce the high frequency output impedance of the internal reference. Larger capacitors should not be used as this degrades the stability of the reference buffer.

The V_{REF}^+ and V_{REF}^- inputs of both converters set the full-scale and zero input voltages of the A/D. In other words, the voltage at V_{REF}^- defines the input which produces an output code of all zeroes, and the voltage at V_{REF}^+ defines the input which produces an output code of all ones (see Figure 9).

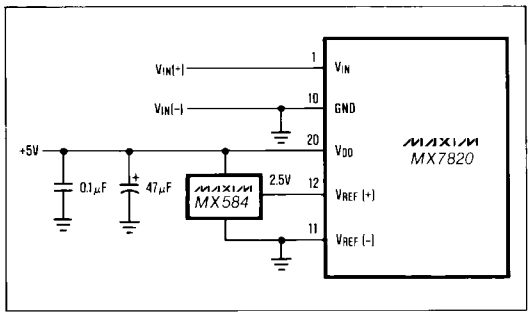


Figure 10b. External Reference 2.5V Full-Scale.

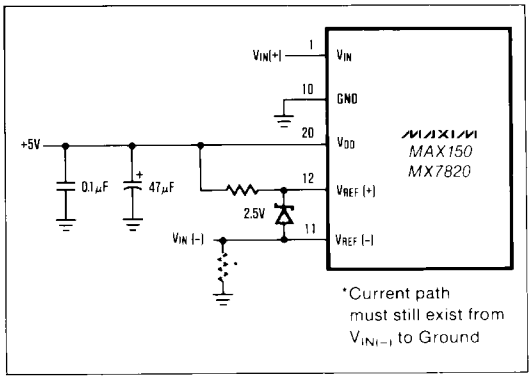


Figure 10d. Input Not Referenced to GND.

CMOS High Speed 8 Bit A/D Converter with Reference and Track/Hold Function

Bypassing

A 47μF electrolytic and 0.1μF ceramic capacitor should be used to bypass the V_{DD} pin to GND. These capacitors should have the minimum possible lead length. Excess lead length may contribute to conversion errors and instability.

If the reference inputs (pins 11, 12) are driven by long lines, they should be bypassed to GND with 0.1 μF capacitors at the V_{REF} pins.

Input Current

The MAX150/MX7820 analog input behaves somewhat differently from conventional A/D converters. The sampled data comparators take varying amounts of current from the input depending on the cycle they are in.

The equivalent circuit of the converter is shown in Figure 11. When the conversion starts and $\overline{WR}$ is low, V_{IN} is connected to the MS and LS comparators. Thus, V_{IN} is connected to thirty-one 1pF capacitors.

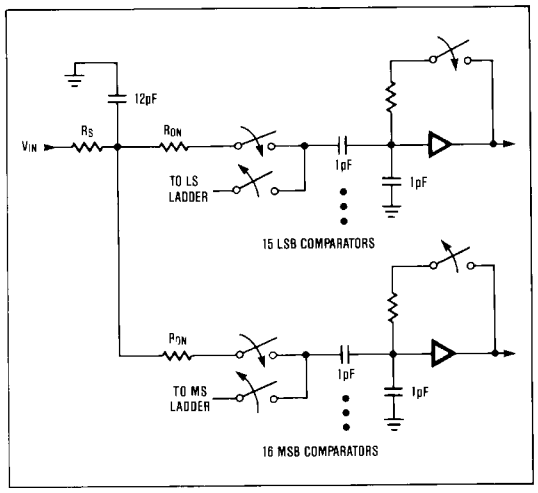


Figure 11a. Equivalent Input Circuit.

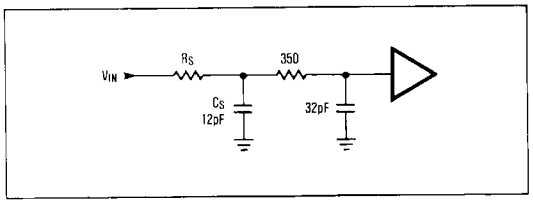


Figure 11b. RC Network Model.

During this acquisition phase ($\overline{WR}$ = Low in the WR-RD Mode) the input capacitors must be charged to the input voltage through the resistance of the internal analog switches (about 2kΩ to 5kΩ). In addition, about 12pF of stray capacitance must be charged. The input can be modelled as an equivalent RC network shown in Figure 11. As R_S (source impedance) increases, the capacitors take longer to charge.

Typical input capacitances of 45pF allow source resistances of up to 1kΩ to be used without settling problems. For larger resistances, the width of the $\overline{WR}$ pulse must be increased from 600ns. Since the length of this acquisition time is internally set when in the RD mode, large source resistances (greater than 1kΩ) may cause settling errors. In this case, use the WR-RD mode and greater than 600ns $\overline{RD}$ time or use a buffer to drive the analog input.

Input Filtering

The transients in the analog input due to the sampled data comparators do not degrade the converter's performance since the A/D does not "look" at the input when these transients occur. The comparator's outputs track the input while $\overline{WR}$ is low, and are latched once $\overline{WR}$ goes high. Therefore, at least 600ns will be provided to charge the ADC's input capacitance. It is not necessary to filter these transients with an external capacitor on the V_{IN} terminal.

Inherent Track-and-Hold

Due to its sampling behavior, the MAX150/MX7820 has the ability to measure a variety of high speed input signals without the help of an external sample-and-hold. In a conventional SAR type converter, the analog input must remain stable within 1/2 LSB for the duration of the conversion to maintain accuracy. This requires the use of external sample-and-holds whenever the input is a high speed signal. Although the conversion time for the MAX150/MX7820 is 1.34μs, the time for which the input must be stable is much less.

The MAX150/MX7820 tracks the input while $\overline{WR}$ is low (in the WR-RD mode) and finishes sampling it approximately 100ns after the rising edge of $\overline{WR}$. This aperture delay is caused by the internal logic propagation delay. Input signals with slew rates typically below 200mV/μs can be converted without error. However, faster signals may cause differential linearity errors due different delays through the MS and LS comparators. Still, the errors caused by fast input signals are far less than the errors caused in a conventional SAR type ADC without a sample-and-hold. A 1μs SAR converter would still not be able to measure a 1kHz, 5V sine wave without the aid of an external sample-and-hold. The MAX150/MX7820 with no such help, can typically measure 5V, 10kHz waveforms.

CMOS High Speed 8 Bit A/D Converter with Reference and Track/Hold Function

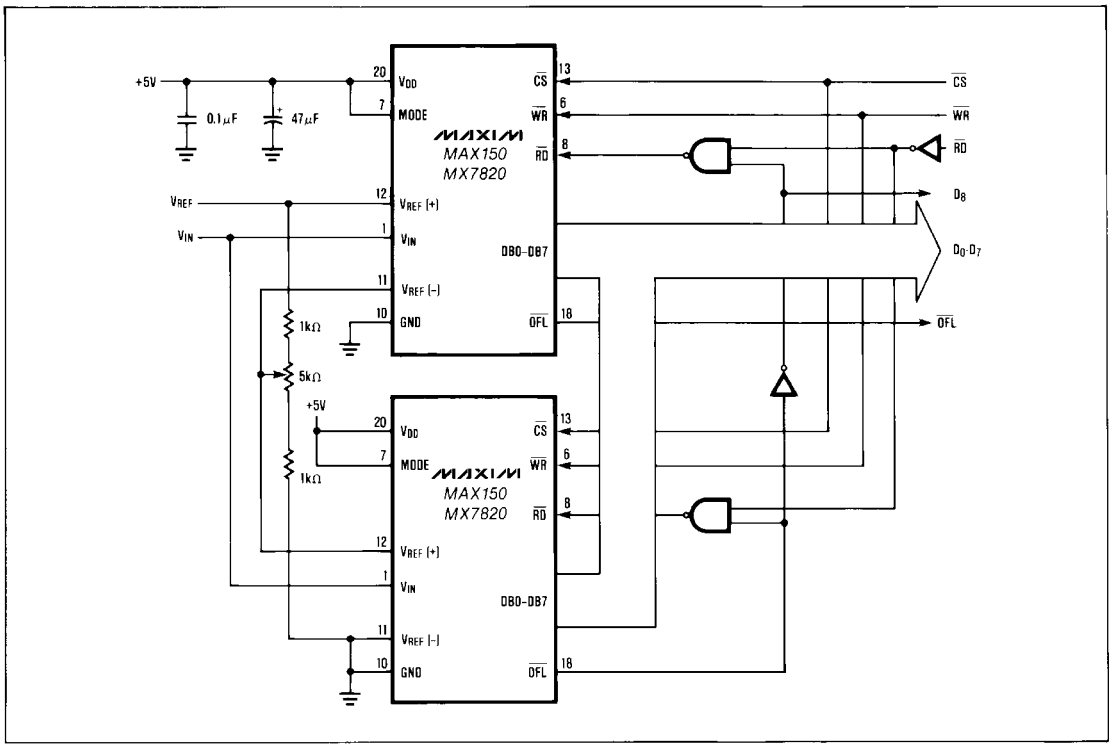


Figure 12. 9-Bit Resolution

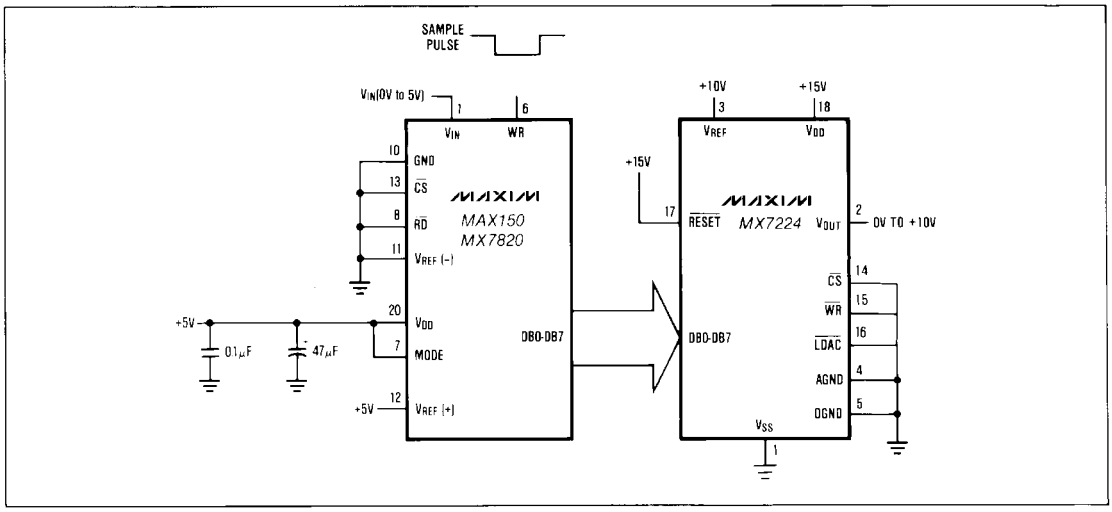


Figure 13. Fast Sample-and-Infinite Hold

CMOS High Speed 8 Bit A/D Converter with Reference and Track/Hold Function

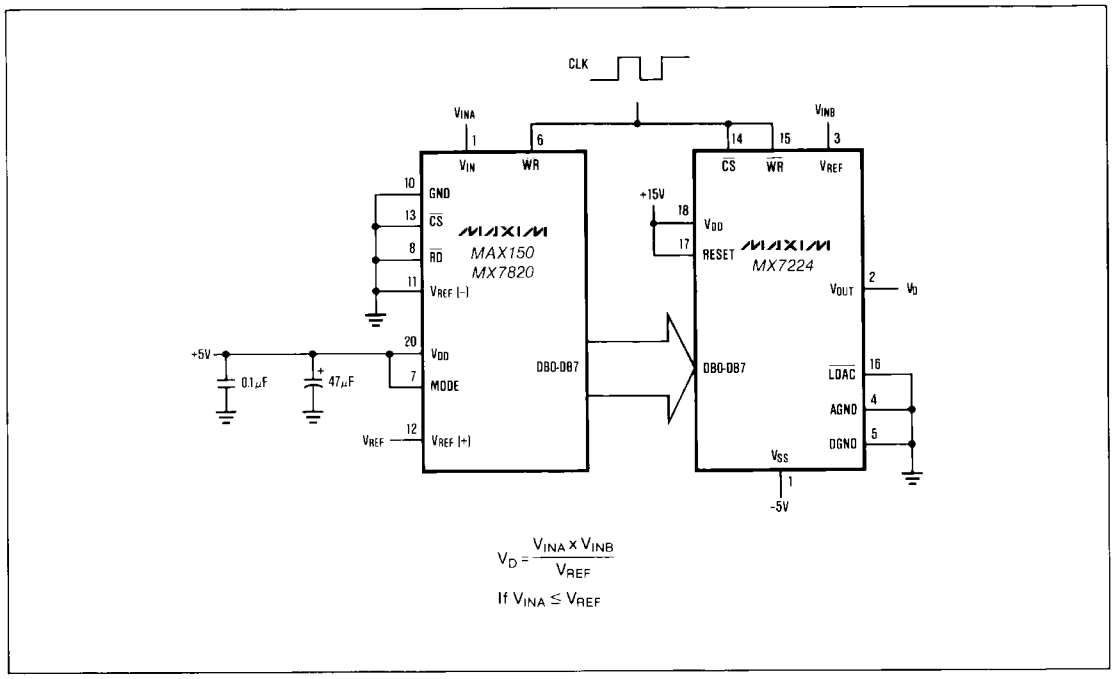


Figure 14. 8-Bit Analog Multiplier

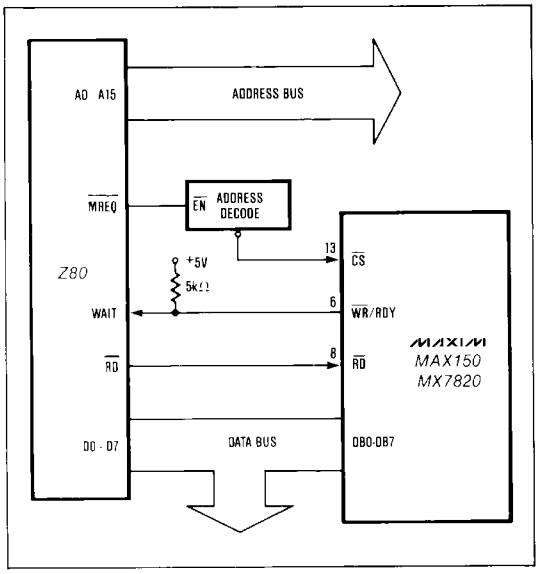


Figure 15. Simple RD-Mode Interface

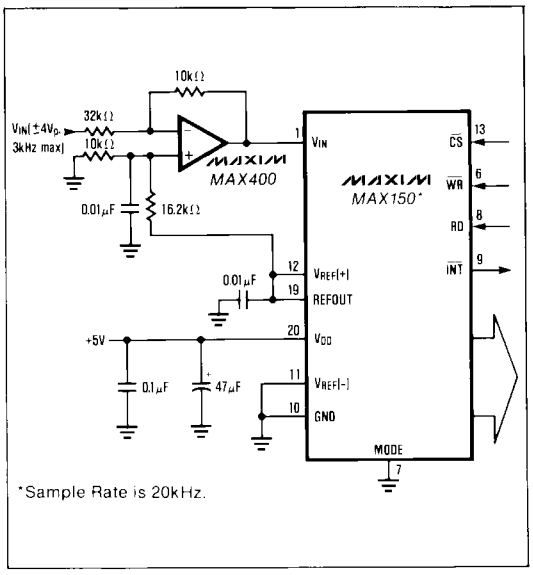


Figure 16. Telecom A/D Converter

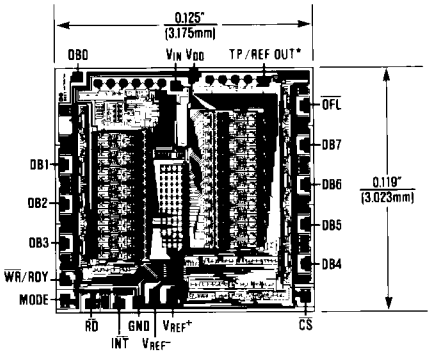
CMOS High Speed 8 Bit A/D Converter with Reference and Track/Hold Function

Ordering Information (continued)

PART	TEMP. RANGE	PACKAGE†	ERROR
MX7820LN	0° C to +70° C	Plastic DIP	±½ LSB
MX7820KN	0° C to +70° C	Plastic DIP	±1 LSB
MX7820LCWP	0° C to +70° C	Small Outline	±½ LSB
MX7820KCWP	0° C to +70° C	Small Outline	±1 LSB
MX7820CQ	-25° C to +85° C	CERDIP	±½ LSB
MX7820BQ	-25° C to +85° C	CERDIP	±1 LSB
MX7820UQ	-55° C to +125° C	CERDIP	±½ LSB
MX7820TQ	-55° C to +125° C	CERDIP	±1 LSB

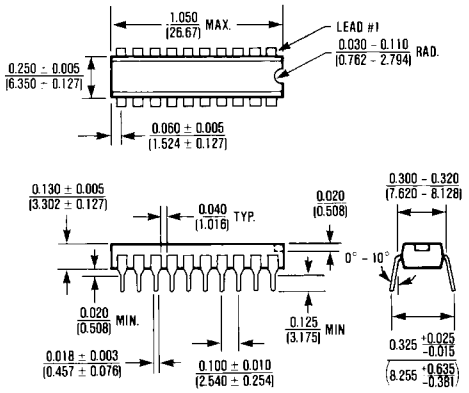
† *All devices — 20 lead packages*

Chip Topography

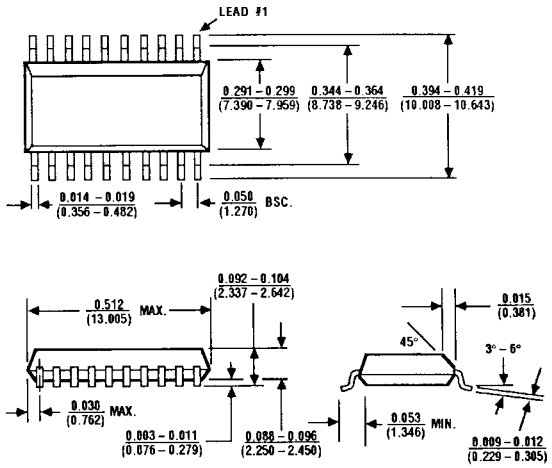


*MAX150 Only.

Package Information



20 Lead Plastic DIP (PP)
θ_{JA} = 125°C/W
θ_{JC} = 60°C/W



20 Lead Small Outline, Wide (WP)
θ_{JA} = 90°C/W
θ_{JC} = 50°C/W

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