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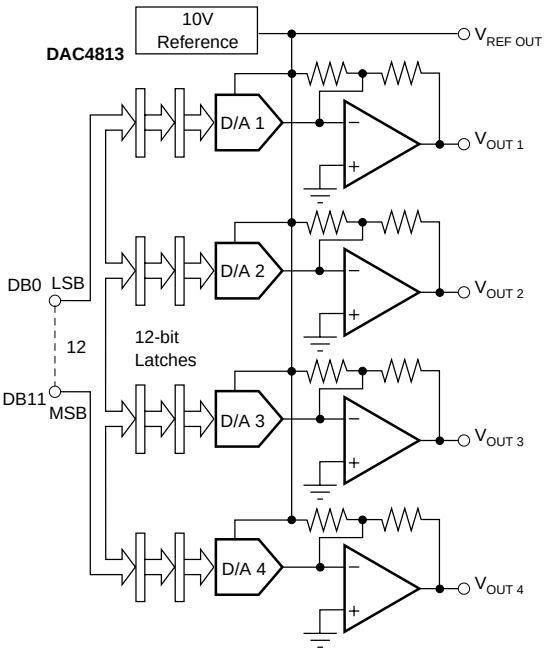


DAC4813

QUAD 12-BIT DIGITAL-TO-ANALOG CONVERTER (12-bit port interface)

FEATURES

- COMPLETE WITH REFERENCE AND OUTPUT AMPLIFIERS
- 12-BIT PORT INTERFACE
- ANALOG OUTPUT RANGE: ±10V
- MONOTONICITY GUARANTEED OVER TEMPERATURE
- INTEGRAL LINEARITY ERROR: ±1/2LSB max
- ±12V to ±15V SUPPLIES
- 28-PIN PLASTIC DIP PACKAGE



DESCRIPTION

DAC4813 is a complete quad 12-bit digital-to-analog converter with bus interface logic. Each package includes a precision +10V voltage reference, double-buffered bus interface including a RESET function and 12-bit D/A converters with voltage-output operational amplifiers.

The double-buffered interface consists of a 12-bit input latch and a D/A latch for each D/A converter. A RESET control allows the D/A outputs to be asynchronously reset to bipolar zero, a feature useful for power-up reset, system initialization and recalibration.

DAC4813 D/A converters are committed to the ±10V output range only. Gain and offset are not externally adjustable.

DAC4813 is available with a integral linearity error of 1/2LSB and 12-bit monotonicity guaranteed over temperature. It is packaged in a 28-pin 0.6in. wide plastic DIP package and specified over –40°C to +85°C and 0°C to +70°C.

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SPECIFICATIONS

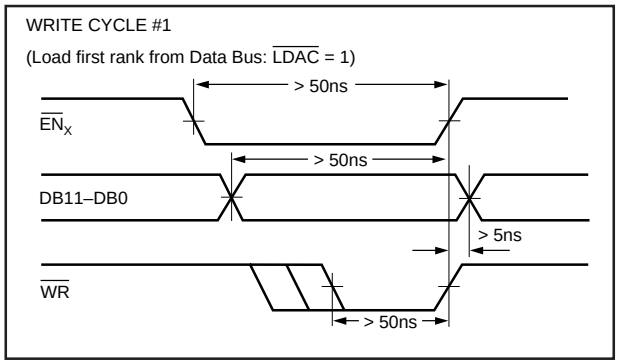
ELECTRICAL

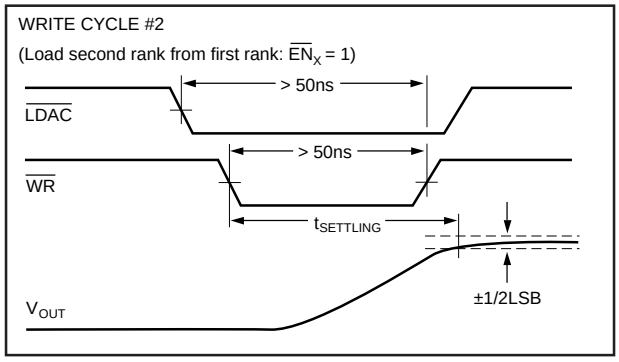
T_A = +25°C, $+V_{CC}$ = +12V or +15V, $-V_{CC}$ = –12V or –15V, unless otherwise noted.

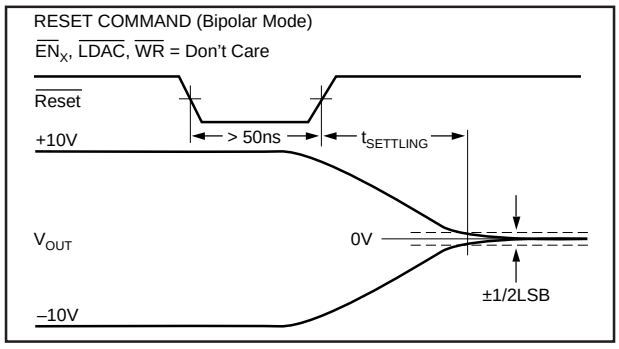
PARAMETER	CONDITIONS	DAC4813AP, JP MIN	DAC4813AP, JP TYP	DAC4813AP, JP MAX	UNITS
INPUTS					
DIGITAL INPUTS	Over Temperature				
Input Code [1]	Range		Bipolar Offset Binary		
Logic Levels [2]					
V_{IH} [3]		+2		+5.5	V
V_{IL}		0		+0.8	V
Logic Input Currents					
DB0-DB11, $\overline{WR}$, $\overline{LDAC}$, $\overline{RESET}$,$\overline{EN_X}$					
I_{IH}	V_I = +2.7V			±40	µA
I_{IL}	V_I = +0.4V			±40	µA
TRANSFER CHARACTERISTICS					
ACCURACY					
Linearity Error			±1/4	±1/2	LSB
Differential Linearity Error			±1/2	±1	LSB
Gain Error			±0.05	±0.2	%
Bipolar Zero Error [5]			±0.05	±0.2	%FSR[4]
Power Supply Sensitivity					
Of Full Scale $+V_{CC}$			±5	±20	ppmFSR/%$+V_{CC}$
$-V_{CC}$			±1	±10	ppmFSR/%$-V_{CC}$
DRIFT	Over Specification Temperature Range				
Gain			±5	±30	ppm/°C
Bipolar Zero Drift			±5	±15	ppmFSR/°C
Linearity Error over Temperature			±1/2	±3/4	LSB
Monotonicity			Guaranteed		
DYNAMIC CHARACTERISTICS					
SETTLING TIME [6]	To within ±0.012%FSR of Final Value 5kΩ || 500pF Load				
Full Scale Range Change	20V Range		4.5	6	µs
1LSB Output Step [7] At Major Carry		2			µs
Slew Rate			10		V/µs
Crosstalk [8]	5kΩ Loads		0.2		LSB
OUTPUT					
Output Voltage Range	$\pm V_{CC} \geq$ ±11.4V			±10	V
Output Current		±5			mA
Output Impedance			0.2		Ω
Short Circuit to ACOM Duration	at DC		Indefinite		
REFERENCE VOLTAGE					
Voltage		+9.95	+10.00	+10.05	V
Source Current Available for External Loads		2			mA
Impedance			0.2		Ω
Temperature Coefficient			±5	±25	ppm/°C
Short Circuit to Common Duration	at DC		Indefinite		
POWER SUPPLY REQUIREMENTS					
Voltage: $+V_{CC}$		+11.4	+15	+16.5	V
$-V_{CC}$		–11.4	–15	–16.5	V
Current:	No Load $\pm V_{CC}$ = ±15V				
$+V_{CC}$			48	60	mA
$-V_{CC}$			24	28	mA
Power Dissipation			1080	1320	mW
Potential at DCOM with Respect to ACOM [9]		–3		+3	V
TEMPERATURE RANGES					
Specification: AP		–40		+85	°C
JP		0		+70	°C
Storage		–60		+100	°C
Thermal Resistance, θ_{JA},Plastic DIP				30	°C/W

NOTES: (1) For Two's Complement Input Coding invert the MSB with an external logic inverter. (2) Digital inputs are TTL and +5V CMOS compatible over the specification temperature range. (3) Open DATA input lines will be pulled above +5.5V. See discussion under LOGIC INPUT COMPATIBILITY in the OPERATION section. (4) FSR means Full Scale Range. For example, for ±10V output, FSR = 20V. (5) Error at input code 800_{HEX}. (6) Maximum represents the 3σ limit. Not 100% tested for this parameter. (7) For the worst-case code change: $7FF_{HEX}$ to 800_{HEX} and 800_{HEX} to $7FF_{HEX}$. (8) Crosstalk is defined as the change in any output as a result of any other output being driven from –10V to +10V at rated output current. (9) The maximum voltage at which ACOM and DCOM may be separated without affecting accuracy specifications.

TIMING DIAGRAMS







ABSOLUTE MAXIMUM RATINGS

$+V_{CC}$ to ACOM	0 to +18V
$-V_{CC}$ to ACOM	0 to –18V
$+V_{CC}$ to $-V_{CC}$	0 to +36V
ACOM to DCOM	±4V
Digital Inputs to DCOM	–1V to $+V_{CC}$
External Voltage applied to BPO Resistor	±18V
$V_{REF\ OUT}$	Indefinite short to ACOM
V_{OUT}	Momentary to ±18V
Lead Temperature, soldering 10s	+300°C
Max Junction Temperature	165°C

NOTE: Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. Exposure to absolute maximum conditions for extended periods may affect device reliability.

PACKAGE/ORDERING INFORMATION

PRODUCT	PACKAGE	PACKAGE DRAWING NUMBER(1)	TEMPERATURE RANGE
DAC4813AP	28-Pin Plastic DBL Wide DIP	215	–40°C to +85°C
DAC4813JP	28-Pin Plastic DBL Wide DIP	215	0°C to +70°C

NOTE: (1) For detailed drawing and dimension table, please see end of data sheet, or Appendix C of Burr-Brown IC Data Book.

ELECTROSTATIC DISCHARGE SENSITIVITY

Electrostatic discharge can cause damage ranging from performance degradation to complete device failure. Burr-Brown Corporation recommends that all integrated circuits be handled and stored using appropriate ESD protection methods.

TRUTH TABLE

WR	EN1	EN2	EN3	EN4	LDAC	RESET	OPERATION
X	X	X	X	X	X	0	Reset all D/A Latches
1	X	X	X	X	X	1	No Operation
X	1	1	1	1	1	1	No Operation
0	1	1	1	0	1	1	Load Data into First Rank for D/A 4
0	1	1	0	1	1	1	Load Data into First Rank for D/A 3
0	1	0	1	1	1	1	Load Data into First Rank for D/A 2
0	0	1	1	1	1	1	Load Data into First Rank for D/A 1
0	1	1	1	1	0	1	Load Second Rank from First Rank, All D/As
0	0	0	0	0	0	1	All Latches Transparent

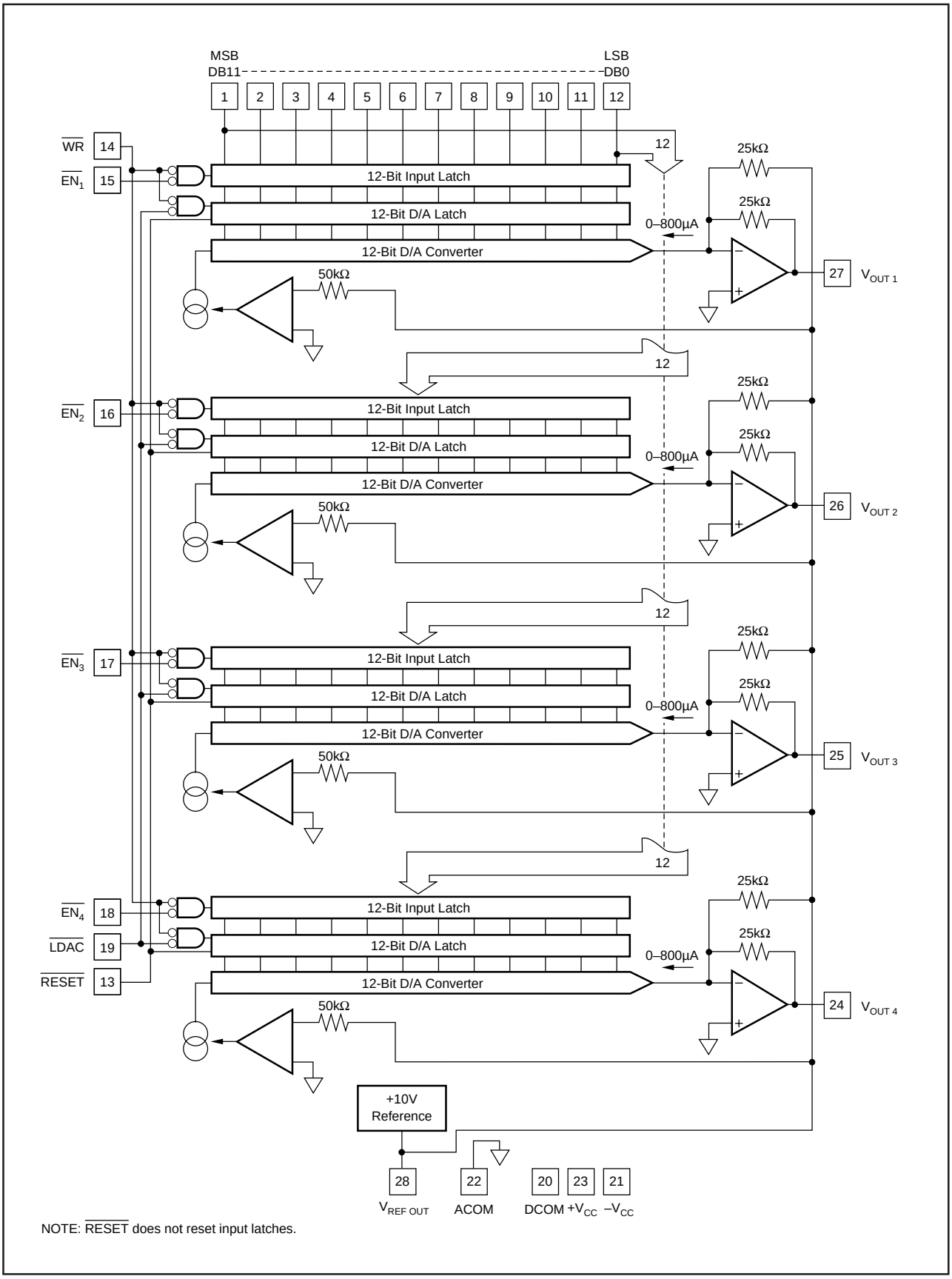
"X" = Don't Care

PIN DESCRIPTIONS

PIN	NAME	FUNCTION
1	DB11	DATA, MSB, positive true.
2	DB10	DATA
3	DB9	DATA
4	DB8	DATA
5	DB7	DATA
6	DB6	DATA
7	DB5	DATA
8	DB4	DATA
9	DB3	DATA
10	DB2	DATA
11	DB1	DATA
12	DB0	DATA, LSB.
13	$\overline{\text{RESET}}$	Resets output of all D/As to bipolar-zero. The D/A remains in this state until overwritten by a $\overline{\text{LDAC}}$-$\overline{\text{WR}}$ command. RESET does not reset the input latch. After power–up and reset, input latches will be in an indeterminant state.
14	$\overline{\text{WR}}$	Write strobe. Must be low for data transfer to any latch (except RESET).
15	$\overline{\text{EN1}}$	Enable for 12-bit input data latch of D/A1. NOTE: This logic path is slower than the $\overline{\text{WR}}$/ path.
16	$\overline{\text{EN2}}$	Enable for 12-bit input data latch of D/A2. NOTE: This logic path is slower than the $\overline{\text{WR}}$/ path.
17	$\overline{\text{EN3}}$	Enable for 12-bit input data latch of D/A3. NOTE: This logic path is slower than the $\overline{\text{WR}}$ /path.
18	$\overline{\text{EN4}}$	Enable for 12-bit input data latch of D/A4. NOTE: This logic path is slower than the $\overline{\text{WR}}$/ path.
19	$\overline{\text{LDAC}}$	Load DAC enable. Must be low with $\overline{\text{WR}}$ for data transfer to the D/A latch and simultaneous update of all D/A converters.
20	DCOM	Digital common, logic currents return.
21	$-V_{CC}$	Analog supply input, nominally –12V or –15V referred to ACOM.
22	ACOM	Analog common, $+V_{CC}$, $-V_{CC}$ supply return.
23	$+V_{CC}$	Analog supply input, nominally +12V or +15V referred to ACOM.
24	$V_{OUT\ 4}$	D/A 4 analog output.
25	$V_{OUT\ 3}$	D/A 3 analog output.
26	$V_{OUT\ 2}$	D/A 2 analog output.
27	$V_{OUT\ 1}$	D/A 1 analog output.
28	$V_{REF\ OUT}$	+10V reference output.

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BLOCK DIAGRAM

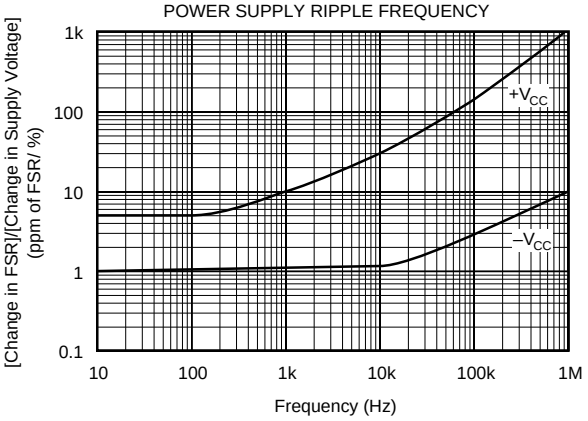


NOTE: $\overline{\text{RESET}}$ does not reset input latches.

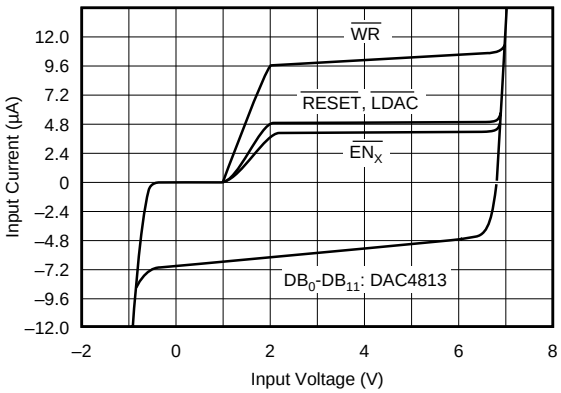
TYPICAL PERFORMANCE CURVES

T_A = +25°C, V_{CC} = ±15V unless otherwise noted.

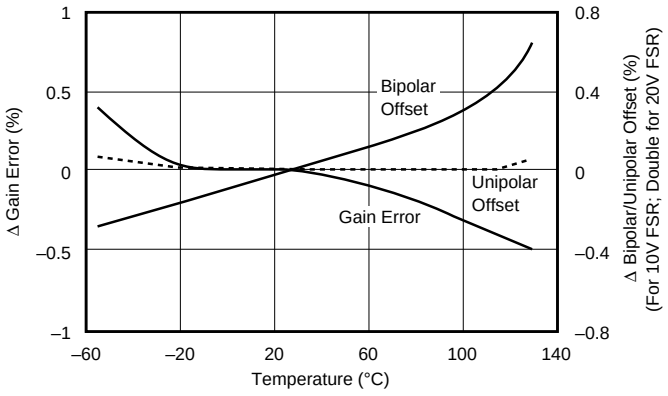
POWER SUPPLY REJECTION vs
POWER SUPPLY RIPPLE FREQUENCY



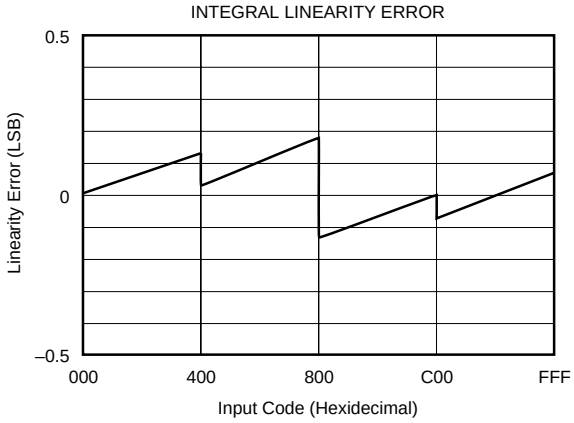
DIGITAL INPUT CURRENT vs INPUT VOLTAGE



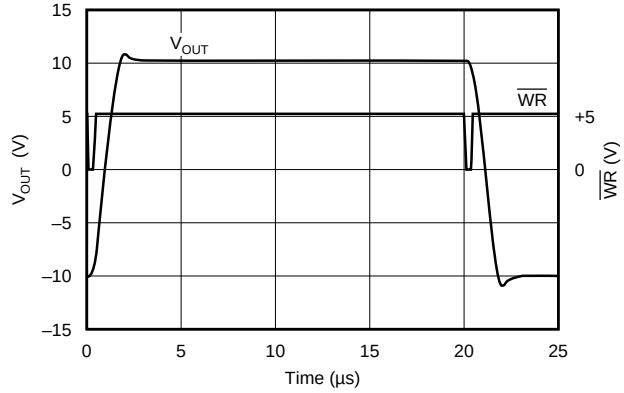
CHANGE OF GAIN AND OFFSET ERROR
vs TEMPERATURE



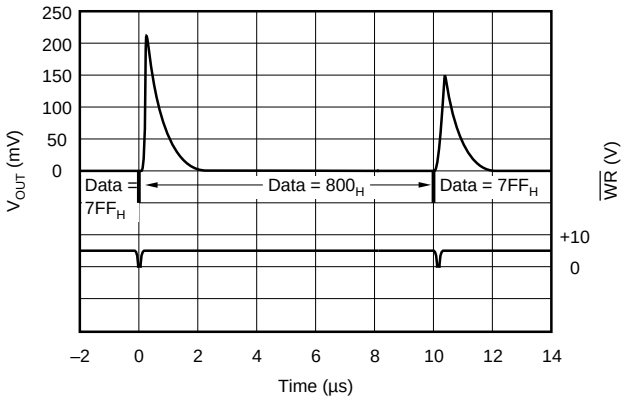
INTEGRAL LINEARITY ERROR



± FULL SCALE OUTPUT SWING



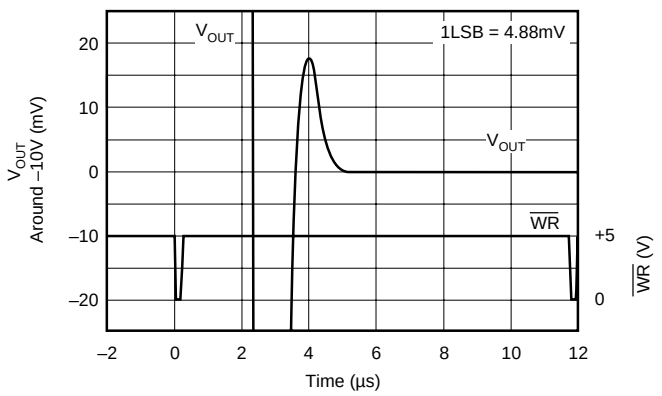
MAJOR CARRY GLITCH



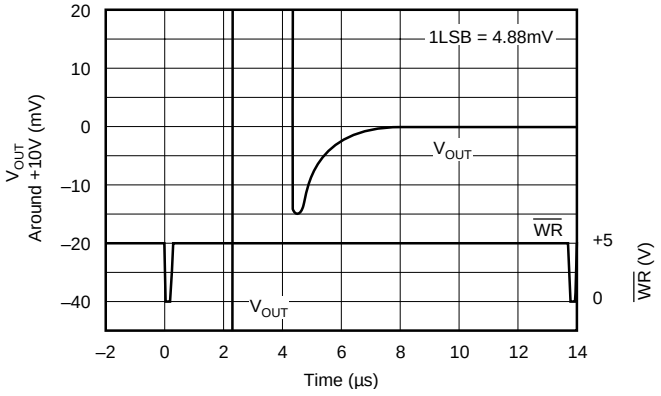
TYPICAL PERFORMANCE CURVES (CONT)

T_A = +25°C, V_{CC} = ±15V unless otherwise noted.

SETTLING TIME, +10V TO –10V



SETTLING TIME, –10V TO +10V



DISCUSSION OF SPECIFICATIONS

LINEARITY ERROR

Linearity error is defined as the deviation of the analog output from a straight line drawn between the end points (digital inputs all "1s" and all "0s"). DAC4813 linearity error is ±1/2LSB max at +25°C.

DIFFERENTIAL LINEARITY ERROR

Differential Linearity Error (DLE) is the deviation from a 1LSB output change from one adjacent state to the next. A DLE specification of 1/2LSB means that the output step size can range from 1/2LSB to 3/2LSB when the digital input code changes from one code word to the adjacent code word If the DLE is more positive than –1LSB, the D/A is said to be monotonic.

MONOTONICITY

A D/A converter is monotonic if the output either increases or remains the same for increasing digital input values. DAC4813 is monotonic over their specification temperature range –40°C to +85°C.

DRIFT

Gain Drift is a measure of the change in the Full Scale Range (FSR) output over the specification temperature range. Gain Drift is expressed in parts per million per degree Celsius (ppm/°C).

Bipolar Zero Drift is measured with a data input of 800_{HEX}. The D/A is configured for bipolar output. Bipolar Zero Drift is expressed in parts per million of Full Scale Range per degree Celsius (ppm of FSR/°C).

SETTLING TIME

Settling Time is the total time (including slew time) for the output to settle to within an error band around its final value after a change in input. Settling times are specified to ±0.01% of Full Scale Range (FSR) for two conditions: one for a FSR output change of 20V (25kΩ feedback) and one for a 1LSB change. The 1LSB change is measured at the Major Carry ($7FF_{HEX}$ to 800_{HEX}, and 800_{HEX} to $7FF_{HEX}$), the input code transition at which worst-case settling time occurs.

OPERATION

INTERFACE LOGIC

The bus interface logic of the DAC4813 consists of two independently addressable latches in two ranks for each D/A converter. The first rank consists of one 12-bit input latch which can be loaded directly from a 12- or 16-bit microprocessor/microcontroller bus. The input latch holds data temporarily before it is loaded into the second latch, the D/A latch. This double buffered organization permits simultaneous update of all D/As.

All latches are level-triggered. Data present when the control signals are logic "0" will enter the latch. When the control signals return to logic "1", the data is latched.

CAUTION: DAC4813 was designed to use $\overline{WR}$ as the fast strobe. $\overline{WR}$ has a much faster logic path than $\overline{EN}_X$ (or $\overline{LDAC}$). Therefore, if one permanently wires $\overline{WR}$ to DCOM and uses only $\overline{EN}_X$ to strobe data into the latches, the DATA HOLD time will be long, approximately 20ns to 30ns, and this time will vary considerably in this range from unit to unit. DATA HOLD time using $\overline{WR}$ is 5ns max.

RESET FUNCTION

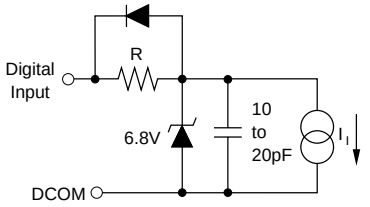
The Reset function resets only the D/A latch. Therefore, after a RESET, good data must be written to **all** the input latches before an $\overline{LDAC}$ – $\overline{WR}$ command is issued. Otherwise, old data or unknown data is present in the input latches and will be transferred to the D/A latch producing an analog output value that may be unwanted.

LOGIC INPUT COMPATIBILITY

DAC4813 digital inputs are TTL compatible (1.4V switching level) over the operating range of $+V_{CC}$. Each input has low leakage and high input impedance. Thus the inputs are suitable for being driven by any type of 5V logic. An equivalent circuit of a digital input is shown in Figure 1.

Open DATA input lines will float to 7V or more. Although this will not harm the DAC4813, current spikes will occur in the input lines when a logic 0 is asserted and, in addition, the speed of the interface will be slower. A digital output driving a DATA input line of the DAC4813 must not drive, **or let the DATA input float**, above +5.5V. Unused DATA inputs should be connected to DCOM.

Unused control inputs should be connected to a voltage greater than +2V but not greater than +5.5V. If this voltage is not available, the control inputs can be connected to $+V_{CC}$ through a 100kΩ resistor to limit the input current.



DIGITAL INPUT	DAC4813 RΩ
Data, $\overline{LDAC}$, $\overline{WR}$, $\overline{RESET}$	250
$\overline{EN_x}$	330

FIGURE 1. Equivalent Digital Input Circuit.

INPUT CODING

DAC4813 accepts positive-true binary input codes.

Input coding for bipolar analog outputs is Bipolar Offset Binary (BOB), where an input code of 000_{HEX} gives a minus full-scale output, an input of FFF_{HEX} gives an output 1LSB below positive full scale, and zero occurs for an input code of 800_{HEX}.

DAC4813 can be used with two's complement coding if a logic inverter is used ahead of the MSB input (DB11).

INTERNAL/EXTERNAL REFERENCE USE

DAC4813 contains a +10V ±50mV voltage reference, $V_{REF\ OUT}$. $V_{REF\ OUT}$ is available to drive external loads sourcing up to 2mA. The load current should be constant, otherwise the gain (and bipolar offset, if connected) of the D/A converters will vary.

Because of the lack of additional pins required for external reference inputs, $V_{REF\ OUT}$ is connected internally to all 4 D/A converters. $V_{REF\ OUT}$ is available for external use on pin 28.

GAIN AND OFFSET ADJUSTMENTS

DAC4813 has no Gain and Offset Adjustment option.

INSTALLATION

POWER SUPPLY CONNECTIONS

Power supply decoupling capacitors should be added. Best settling time performance occurs using a 1 to 10µF tantalum capacitor at $-V_{CC}$. Applications with less critical settling time may be ale to use 0.01µF at $-V_{CC}$ as well as at $+V_{CC}$. The capacitors should be located close to the package.

DAC4813 features separate digital and analog power supply returns to permit optimum connections for low noise and high speed performance. It is recommended that both DIGITAL COMMON (DCOM) and ANALOG COMMON (ACOM) be connected directly to a ground plane under the package. If a ground place is not used, connect the ACOM and DCOM pins together close to the package. Since the reference point for V_{OUT} and $V_{REF\ OUT}$ is the ACOM pin, it is also important to connect the load directly to the ACOM pin. The change in current in the ACOM pin due to an input date word change from 000_{HEX} to FFF_{HEX} is only 1mA for each D/A converter.

OUTPUT VOLTAGE SWING AND RANGE CONNECTIONS

DAC4813 output amplifiers provide a ±10V output swing while operating on supplies as low as ±12V ±5%.

DAC4813 is fully committed to ±10V output ranges. Optional ranges are not pin programmable.

12- AND 16-BIT BUS INTERFACES

DAC4813 data is latched into the input latches of each D/A by asserting low each $\overline{ENx}$ individually and transferring the data from the bus to each input latch by asserting $\overline{WR}$ low. All D/A outputs in each package are then updated simultaneously by asserting $\overline{LDAC}$ and $\overline{WR}$ low.

Be sure to read the CAUTION statement in the LOGIC INPUT COMPATIBILITY section.