ADDING OVERCURRENT PROTECTION TO ISODRIVERS

1. Introduction

The high peak currents in large switch mode power systems require fast response current protection (OCP) circuits to ensure reliable operation. OCP circuits tend to be complex and often use power-inefficient resistive current sensing. This application note discusses OCP circuits based on the Si850x/1x ac current sensor, including high-side and high-side/low-side OCP techniques using latch-off protection and cycle-by-cycle current limiting.

2. Si850x/1x AC Current Sensor Overview

The Si850x/1x family of isolated ac current sensors operate over a 50 kHz to 1 MHz frequency range and are available in full-scale measurement options of 5, 10, and 20 A. These devices offer smaller size (4 mm x 4 mm x 1 mm), lower loss (1.3 mΩ primary series resistance), higher measurement accuracy (±5% of measurement), and lower external BOM compared to current sense transformers.

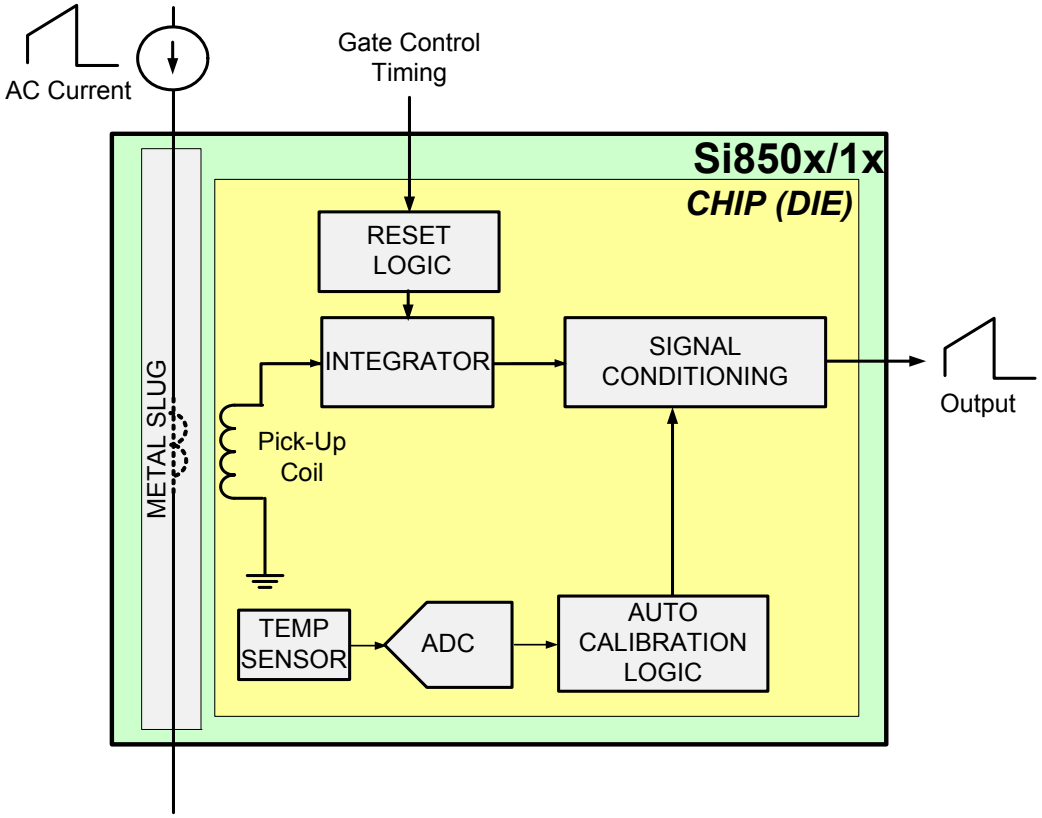


Figure 1. Si850x/1x Block Diagram

Referring to Figure 1, ac current flowing through the sensor primary (metal slug) induces voltage Lmdi/dt into the on-die pick-up coil. Integrated signal processing circuitry "reconstructs" the current waveform by performing a finite integral over the switching period (i.e. integration of the first derivative). The resulting current waveform is corrected for temperature and offset error, then gained-up and buffered to produce a 2 Vpp full-scale, low-noise current signal. Local system gate control signals are used to reset the on-chip integrator before each measurement cycle, eliminating the need for external components commonly required for current transformer core reset. For more information, see the Si85xx AC Current Sensor data sheet.

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3. OCP Circuit Examples

3.1. High-Side Latch-Off Protection

Figure 2 shows a high-side OCP circuit in a half-bridge application. AC current is measured by U1 (Si850x), and monitored by comparator U2 with the value of R1 determining the OCP threshold.

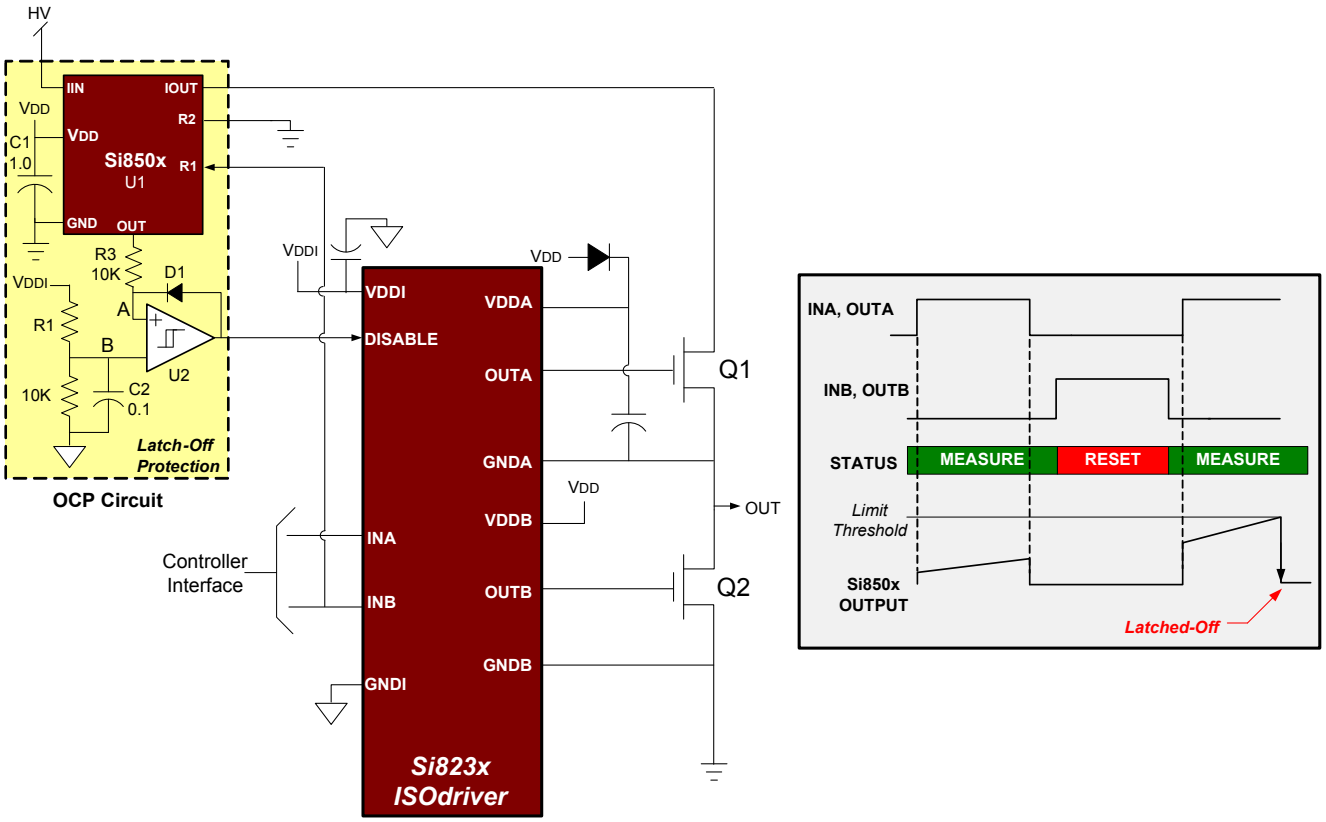


Figure 2. ISOdriver with High-Side Latch-Off OCP

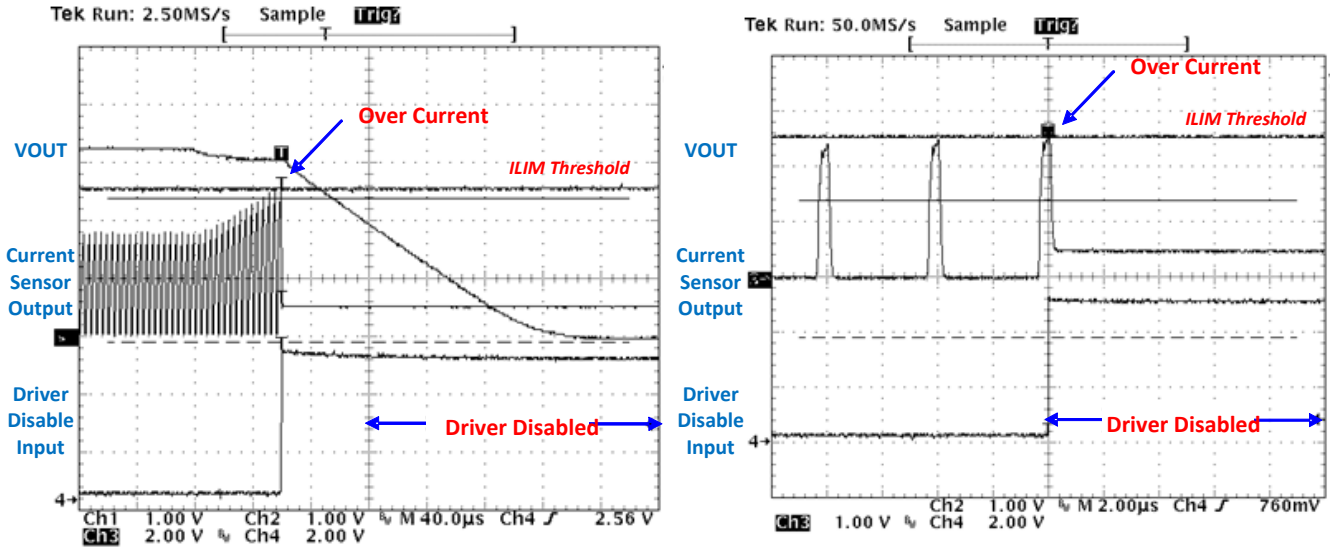
The output of U2 is latched high through D1 when the voltage at Point A exceeds that at Point B (Figures 3a and 3b). Latching action disables the ISOdriver and maintains outputs OUTA and OUTB low until the latch is reset by cycling power. Comparator U2 can be a low-cost type with response times between 1 and 4 µs depending on the system modulation frequency and/or ON time (t_{ON}).

Note: This circuit can be used as a low-side current limiter by inserting the Si850x in the low-side ground path with IIN connected to ground and IOUT connected to Q2 source.

To achieve rated accuracy, the Si85xx integrator reset period must be a minimum of 150 ns in duration while current flow through the sensor is zero. Reset must be discontinued prior to the start of the next measurement cycle. The circuit of Figure 2 uses the gate control signal at INB to reset the Si850x integrator and meets the prescribed criteria for a valid reset for this application. For high-frequency and/or high-duty-cycle applications that cannot afford the full 150 ns reset period, an on-chip one-shot reset mode can be invoked allowing the user to trade off some degree of accuracy in exchange for a shorter reset period. For further reset details and reset configuration examples, see the Si850x/1x AC Current Sensor data sheet.

Implementing OCP begins with choosing the Si850x/1x that has a full-scale current range closest to the target over current threshold. Note that the 5 A and 10 A full-scale product versions can safely and accurately measure currents up to 50% higher than their rated full-scale values, provided that VDD is high enough to support the larger output signal and the amount of current passing through the Si850x/1x is 20 A or less. This added flexibility is helpful when selecting the Si850x/1x full-scale value. For example, a system having a maximum operating current of 4 A with a target overcurrent threshold of 8 A would select the Si8502/12 (10 A full scale).

However, the same system with a target overcurrent threshold of 6 A could select either the Si8502/12 described above or the 5 A full-scale Si8501/11 and over-drive to 6 A during OCP.



A) 40 µS/Division View

B) 2 µS/Division View

Figure 3. Overcurrent Latch-Off Protection Waveforms

3.2. High-Side, Cycle-by-Cycle Limiting

Cycle-by-cycle current limiting is less intrusive than latch-off protection because it limits current to a safe level, allowing the system to continue operation. The cycle-by-cycle OCP circuit in Figure 4 is substantially the same as that of Figure 2 except that the U2 latch is automatically reset through D2 at the end of each high-side cycle. Unlike the latch-off version, the response time of comparator U2 must be fast enough to disable the ISOdriver at minimum system ON time and will likely have a response time in the tens of nanoseconds.

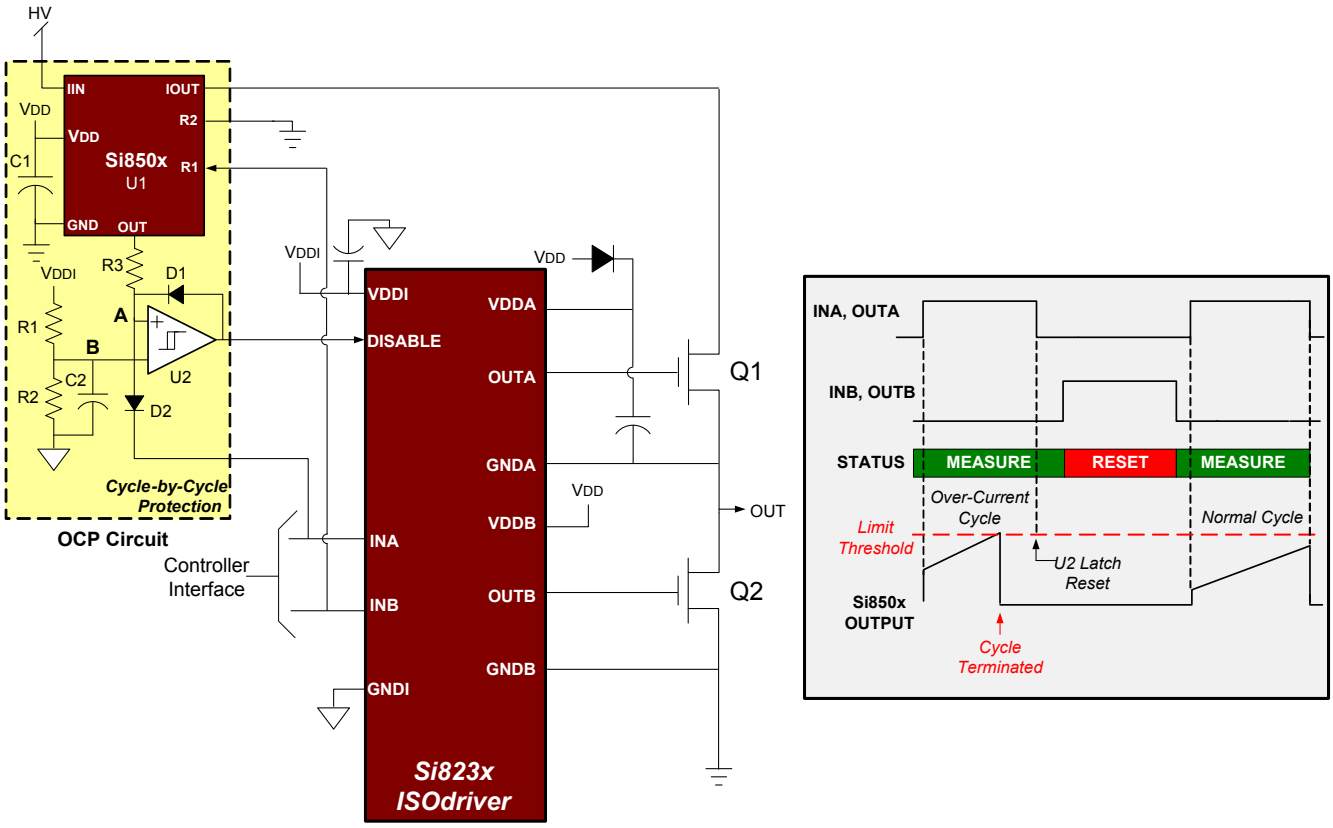


Figure 4. Cycle-by-Cycle OCP

Figure 5 shows circuit operation where dc load current gradually increases until the ILIM threshold is reached, at which time output current is limited to approximately the OCP threshold value. Notice that pulses to the driver disable input appear at the onset of overcurrent, and the slight output voltage droop results from insufficient load current. Figure 6 shows the second current pulse being terminated by the driver disable pulse during an overcurrent event.

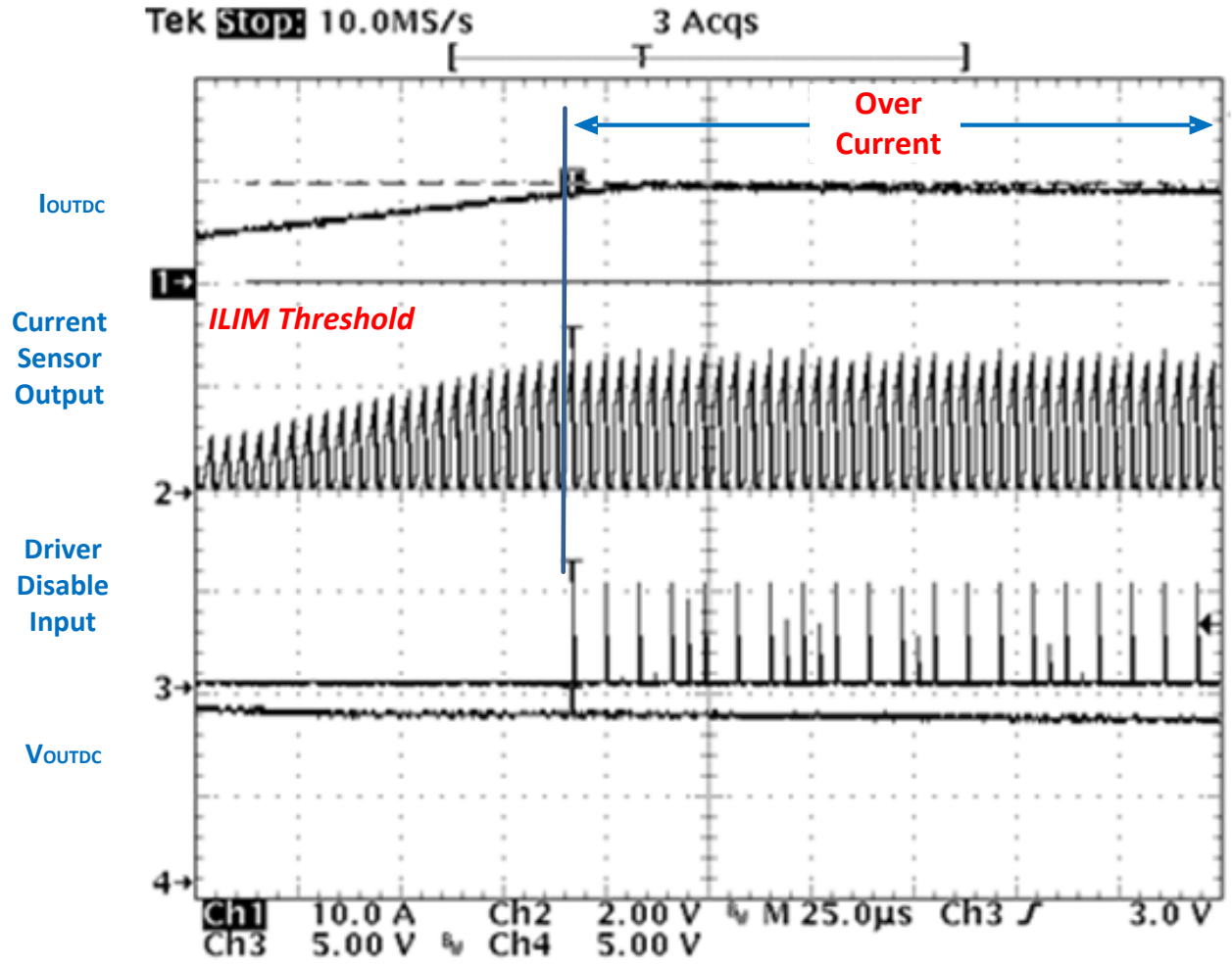


Figure 5. Cycle-By-Cycle Current Limiting Waveforms

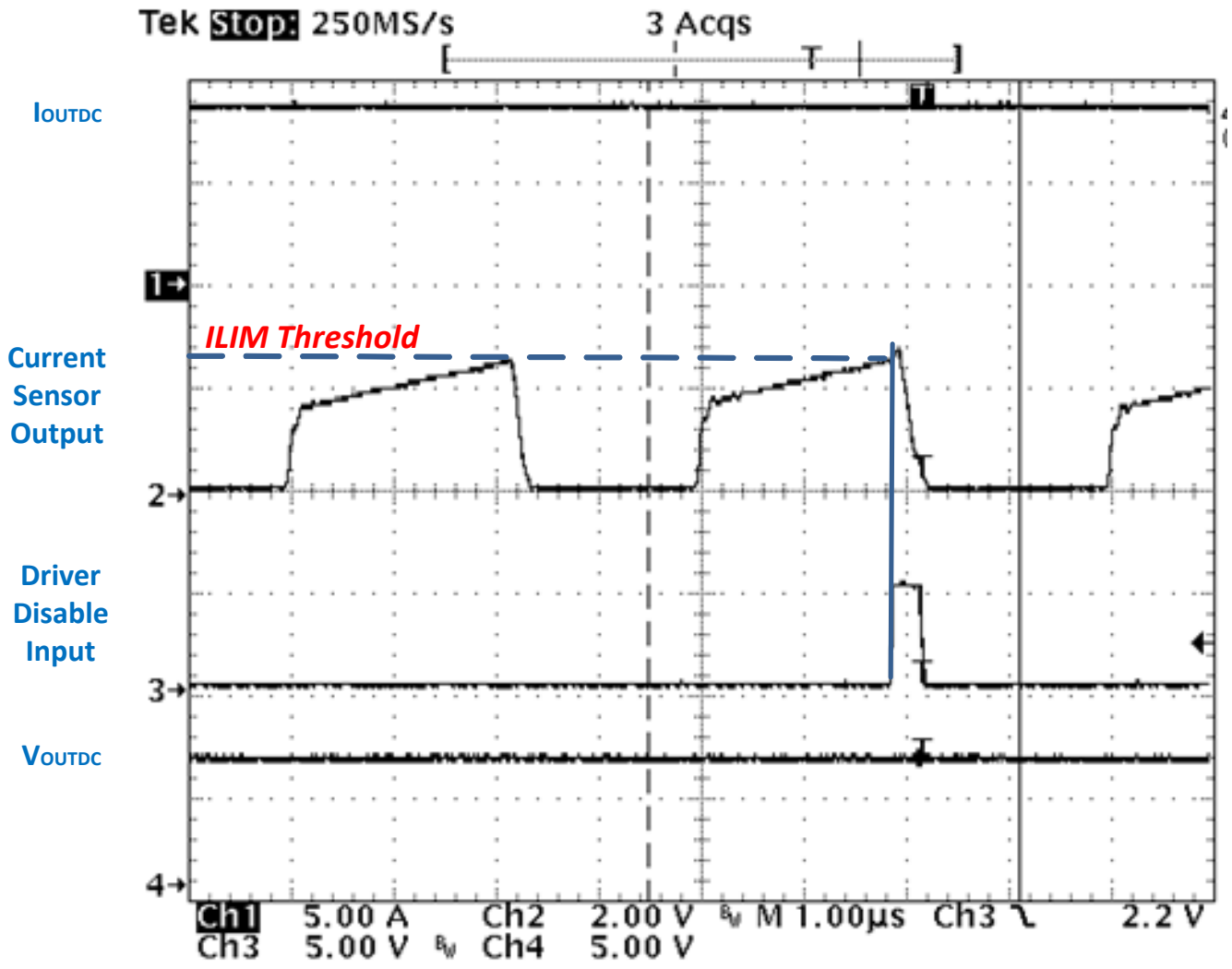


Figure 6. Driver Disable Pulse

3.3. High-Side/Low-Side OCP

The Si851x versions have two additional features compared to the Si850x: expanded reset logic with two additional reset inputs for greater reset timing flexibility and a “ping-pong” output mode (useful in full-bridge and push-pull applications) that alternately routes every other current measurement to the second output pin, allowing current from each power stage to be monitored separately.

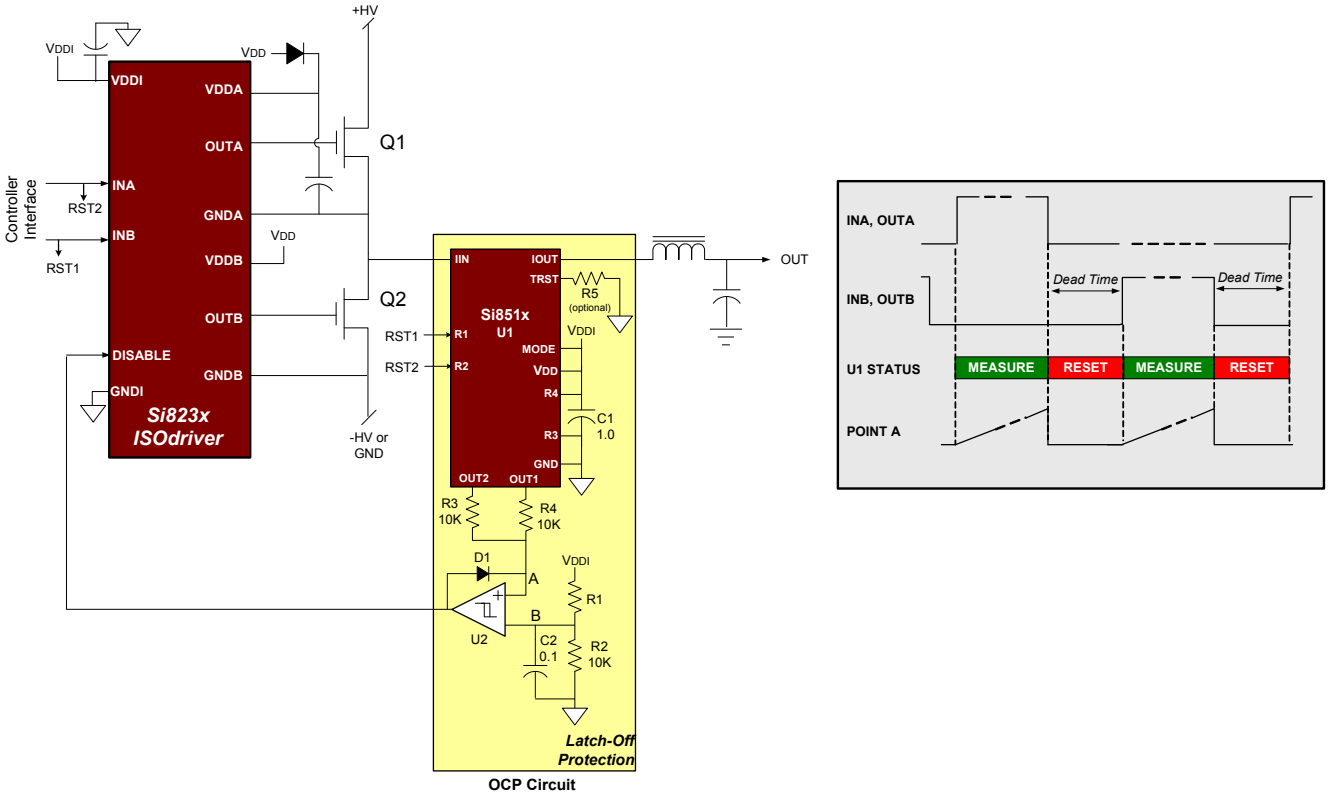


Figure 7. High Side/Low Side Latch-Off OCP

The high-side/low-side OCP circuit of Figure 7 connects the two outputs together through R3 and R4 to form a single output. Only one of the two outputs is active at any given time; so, the signal amplitude at Point A is half the value of the active output due to the voltage divider action of R3 and R4. This amplitude difference must be taken into account when choosing the value of R1.

The Si851x reset period occurs during dead time, which must be at least 150 ns to achieve rated measurement accuracy. If dead time is less than 150 ns, it is recommended that the one-shot mode be used by inserting resistor R5 from the TRST input to ground. In one-shot mode, reset signals act as a trigger, with the value of R5 determining the duration of the one-shot period. This feature allows the user to trade reduced accuracy for a shorter reset period. For more information on one-shot reset mode, see the Si850x/1x AC Current Sensor data sheet. The remainder of the circuit in Figure 7 is substantially the same as the high-side examples of Figures 2 and 3. Likewise, the circuit of Figure 7can be converted to cycle-by-cycle using the diode arrangement shown in Figure 4.

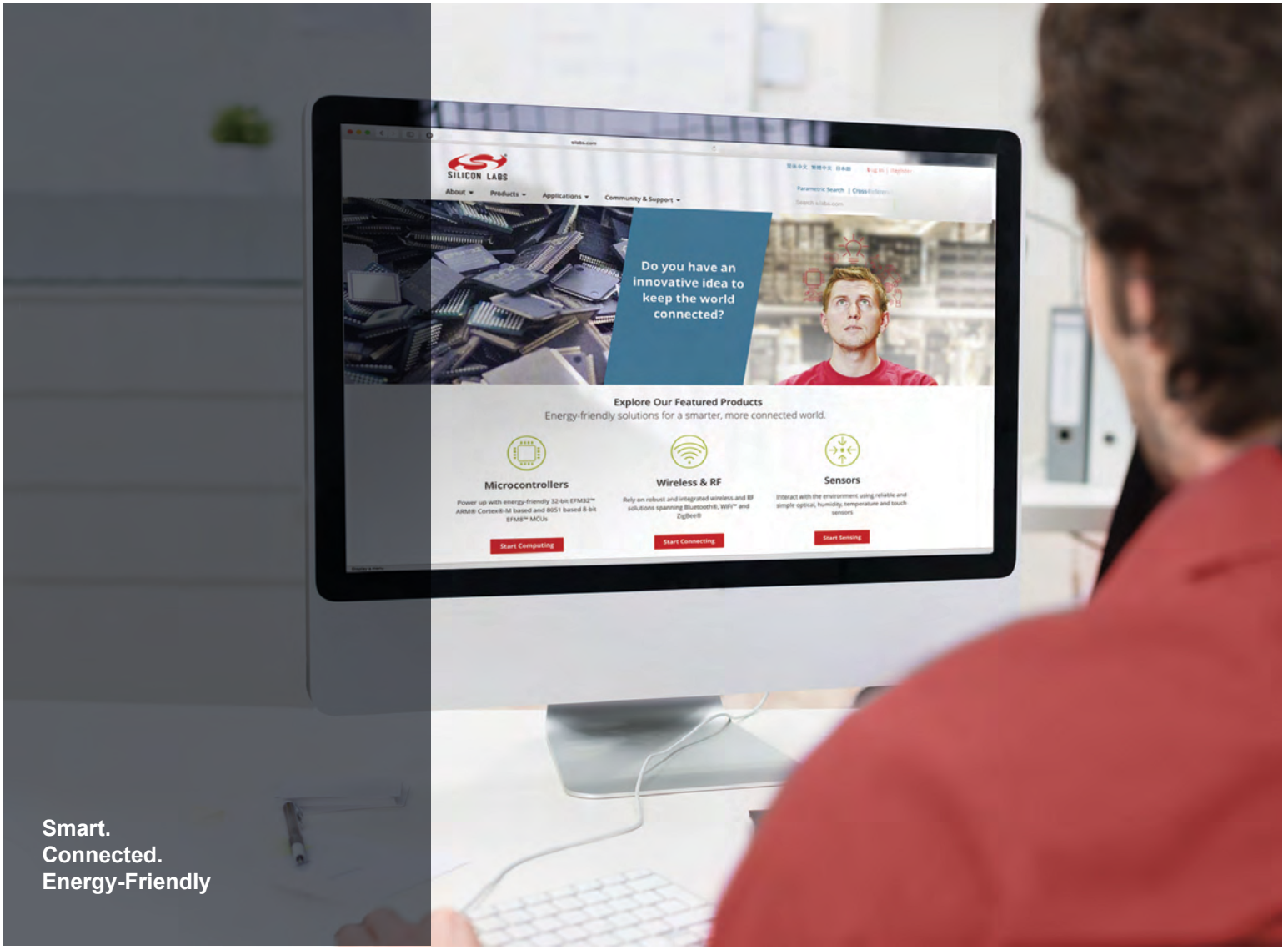
4. Summary

Many switch mode applications require local overcurrent protection. Discrete OCP circuits tend to have a large footprint and are often high-loss. The Si850x/1x can be used to make highly-efficient, accurate OCP circuits that are smaller and more power efficient.

4.1. Related Documents

- Si850x/1x AC Current Sensor data sheet
- Si823x ISOdriver data sheet

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