SONY

CXA2067AS

Preamplifier for High-Resolution Computer Display

Description

The CXA2067AS is a bipolar IC developed for high-resolution computer displays.

Features

- Wide-band amplifier: 170 MHz@–3 dB (Typ)
- Input dynamic range: 1.0 Vp-p (typ)
- High gain preamplifier (17 dB)
- R, G and B in a single package (SDIP 30 pins)
- I^2C bus control
  - Contrast control
  - Sub contrast control
  - Brightness control
  - OSD contrast control
  - Cut-off control: 4 channels of DAC output
  - 2 blanking level modes
  - (0.5 V fixed, pedestal –0.3 V)
- Sync separator for sync-on-green
- Blanking mixing function
- OSC mixing function
- Video interval detection function
- VBLK sync DAC refresh system
- 12 V power supply interlocked power saving function

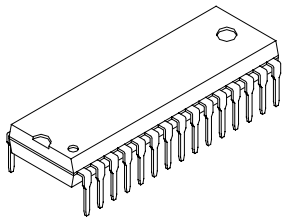
Applications

High-resolution computer displays

Structure

Bipolar silicon monolithic IC

30 pin SDIP (Plastic)



Absolute Maximum Ratings (Ta=25 °C, GND=0 V)

• Supply voltage	V_{CC}/R/G/B	14	V
	V_{CC}	7	V
• Operating temperature	Topr	–20 to +75	°C
• Storage temperature	Tstg	–65 to +150	°C
• Allowable power dissipation			
	P_D	2.05	W

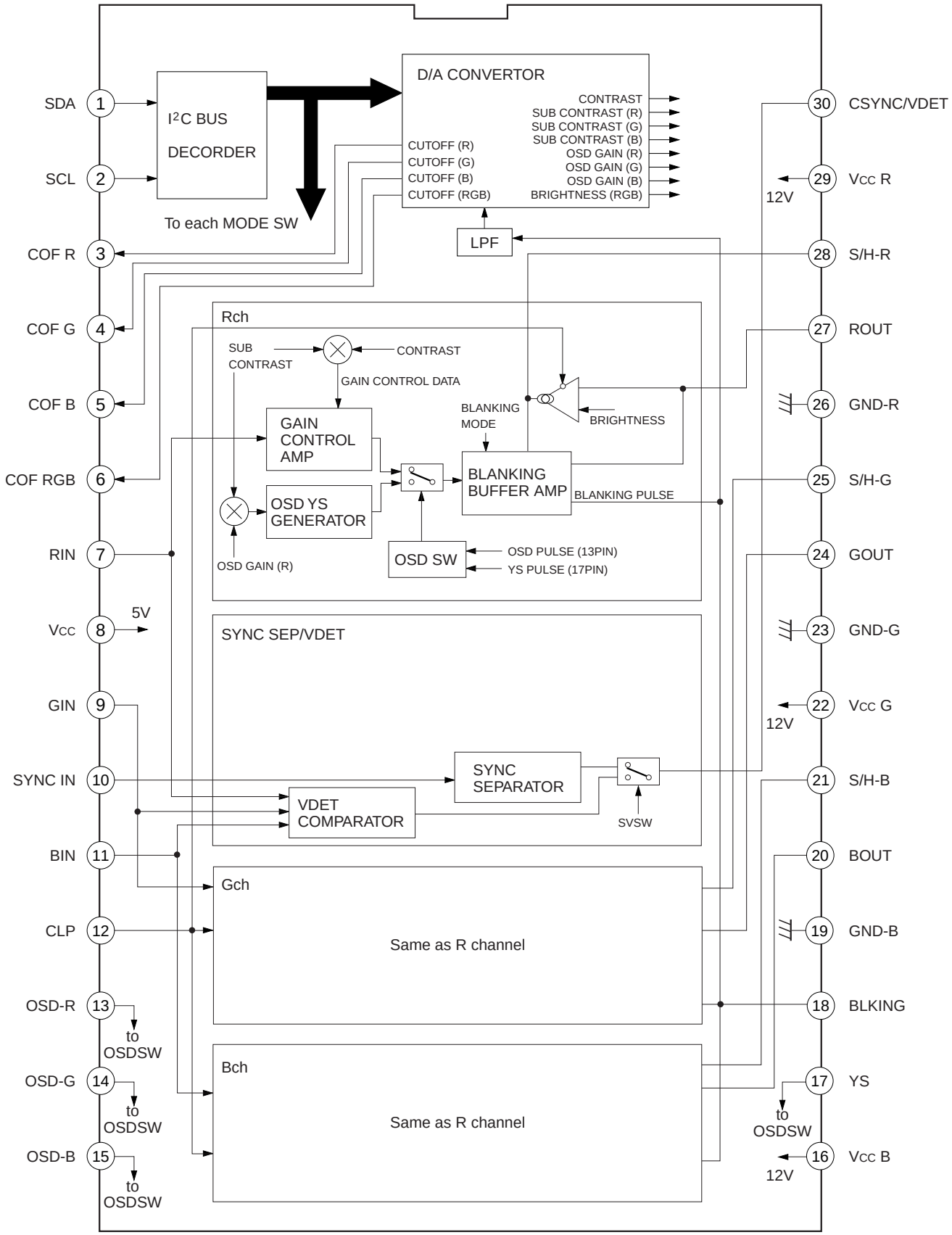
Recommended Operating Conditions

Supply voltage	V_{CC}/R/G/B	12±0.5	V
	V_{CC}	5±0.5	V

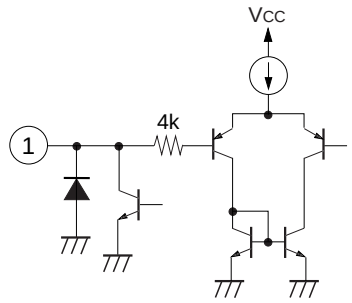
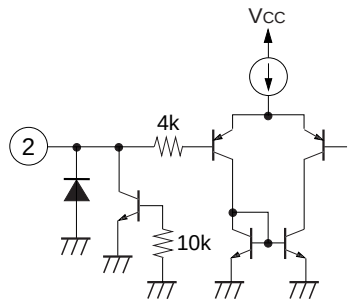
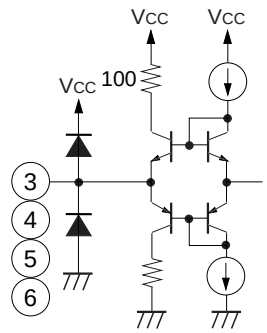
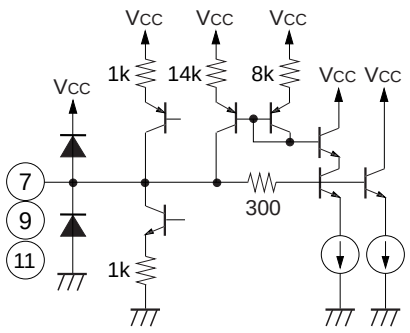
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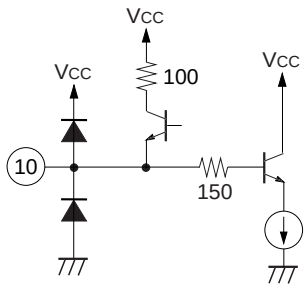
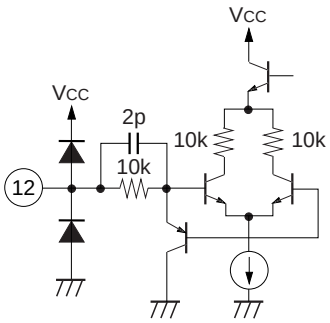
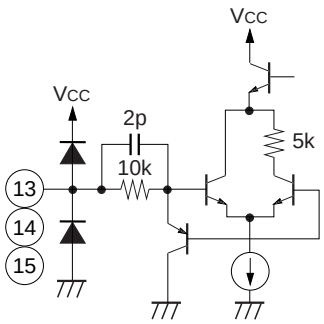
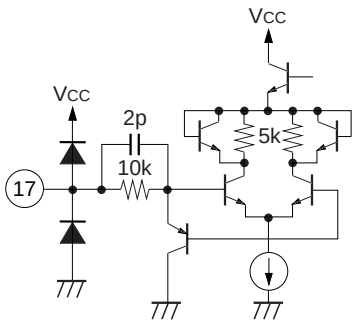
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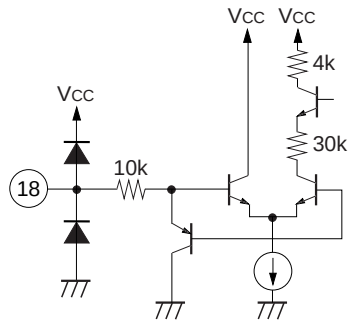
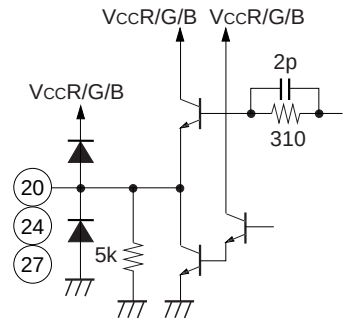
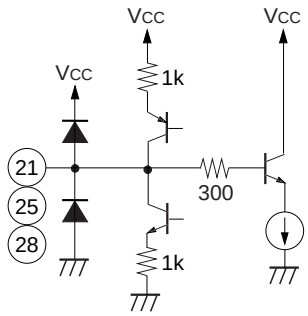
Block Diagram

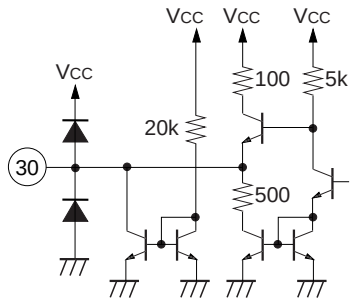


Pin Description

Pin No.	Symbol	Pin voltage	Equivalent circuit	Description
1	SDA	—		I²C bus standard SDA (serial data) input/output. VILMAX=1.5 V VIHMIN=3.5 V VOLMAX=0.4 V
2	SCL	—		I²C bus standard SCL (serial clock) input/output. VILMAX=1.5 V VIHMIN=3.5 V
3 4 5 6	COF R COF G COF B COF RGB	—		DAC output for cut-off adjustment. Output DC is 1 to 4 V.
7 9 11	RIN GIN BIN	1.8 V (Clamp)		R, G and B signal inputs. Input via a capacitor.
8	Vcc	5 V		5 V power supply.

Pin No.	Symbol	Pin voltage	Equivalent circuit	Description
10	SYNC IN	2.8 V		Sync-on-green signal input. Input via a capacitor.
12	CLP	—		Clamp pulse (positive polarity) input. VILMAX=0.8 V VIHMIN=2.8 V
13	OSD-R	—		OSD control inputs. VILMAX=0.8 V VIHMIN=2.8 V
14	OSD-G			
15	OSD-B			
16	Vcc B	12 V		12 V power supply. (B channel)
17	YS	—		YS (OSD BLK) control input. VILMAX=0.8 V VIHMIN=2.8 V

Pin No.	Symbol	Pin voltage	Equivalent circuit	Description
18	BLKING	—		Blanking pulse input. Set the V blanking pulse width to 300 µs or more. VILMAX=0.8 V VIHMIN=2.8 V
19	GND-B	0 V		Ground.
23	GND-G			
26	GND-R			
20	BOUT	—		R, G and B outputs.
24	GOUT			
27	ROUT			
21	S/H-B	—		Brightness sample-and-hold. Connect to GND via a capacitor.
25	S/H-G			
28	S/H-R			
22	Vcc G	12 V		12 V power supply. (G channel)
29	Vcc R	12 V		12 V power supply. (R channel)

Pin No.	Symbol	Pin voltage	Equivalent circuit	Description
30	CSYNC /VDET	—		Sync-on-green signal sync separator output/video detector output. Either of them is selected by SVSW of I²C bus. Typ. : High=4.3 V Low=0.2 V (positive polarity)

Definitions of I²C Bus Register

Slave Address

SLAVE RECEIVER : 40 (HEX)

Register Table

SUB ADDRESS	BIT7	BIT6	BIT5	BIT4	BIT3	BIT2	BIT1	BIT0
00h	CONTRAST							
01h	0	BLK MODE	BRIGHTNESS					
02h	CUT OFF R							
03h	CUT OFF G							
04h	CUT OFF B							
05h	VDET LEVEL		OSD GAIN					
06h	CUT OFF RGB							
07h	SUB CONTRAST R							
08h	SUB CONTRAST G							
09h	SUB CONTRAST B							
0Ah	VDET OFF	SVSW	*	*	*	*	*	VSOFF

Note) *: don't care

Sub Address 0000 CONTRAST (8): Performs the gain control for R, G and B channels in common. Control is performed by the multiplication with SUB CONTRAST. The white balance is adjusted by SUB CONTRAST and the luminance is adjusted by CONTRAST.

0 : Gain minimum (–30 dB or less)

255 : Gain maximum (+17 dB)

Sub Address 0001 BLK MODE (1): Switches the blanking level.

0 : Pedestal–0.3 V

1 : 0.3 V fixed

Sub Address 0001 BRIGHTNESS (6): Performs the black level control for R, G and B channels in common.

0 : Black level minimum (0.9 V)

63 : Black level maximum (2.8 V)

Sub Address 0010 CUT OFF R (8): Performs the Pin 3 (COF R) output voltage control.

0 : Output voltage minimum (1 V)

255 : Output voltage maximum (4 V)

Sub Address 0011 CUT OFF G (8): Performs the Pin 4 (COF G) output voltage control.

0 : Output voltage minimum (1 V)

255 : Output voltage maximum (4 V)

Sub Address 0100 CUT OFF B (8): Performs the Pin 5 (COF B) output voltage control.

0 : Output voltage minimum (1 V)

255 : Output voltage maximum (4 V)

Sub Address 0101 VDET LEVEL (2): Controls the signal detection (VDET) slice level.
0 : Slice level minimum (RIN or GIN or BIN=30 mV)
1 : Slice level maximum (RIN or GIN or BIN=220 mV)

Sub Address 0110 OSD GAIN (6): Performs the OSD gain control for R, G and B channels in common. Control is performed by the multiplication with SUB CONTRAST (upper 6 bits) so that the video white balance and tracking are obtained.
0 : Gain minimum (0 Vp-p)
63 : Gain maximum (5 Vp-p)

Sub Address 0110 CUT OFF RGB (8): Performs the Pin 6 (COF RGB) output voltage.
0 : Output voltage minimum (1 V)
255 : Output voltage maximum (4 V)

Sub Address 0111 SUB CONTRAST R (8): Performs the R channel gain control. Control is performed by the multiplication with CONTRAST. Use for the white balance adjustment.
0 : Gain minimum (–30 dB or less)
255 : Gain maximum (+17 dB)

Sub Address 1000 SUB CONTRAST G (8): Performs the G channel gain control. Control is performed by the multiplication with CONTRAST. Use for the white balance adjustment.
0 : Gain minimum (–30 dB or less)
255 : Gain maximum (+17 dB)

Sub Address 1001 SUB CONTRAST B (8): Performs the B channel gain control. Control is performed by the multiplication with CONTRAST. Use for the white balance adjustment.
0 : Gain minimum (–30 dB or less)
255 : Gain maximum (+17 dB)

Sub Address 1010 VDET OFF (1): Performs the Pin 30 output control.
0 : Output ON
1 : Output OFF

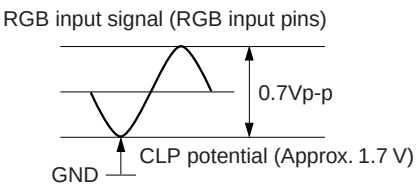
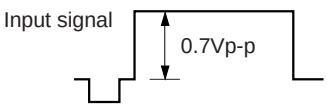
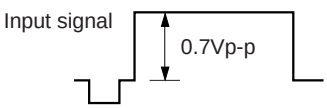
Sub Address 1010 SV SW (1): Switches the Pin 30 output signal (sync separator/video detector).
0 : Sync separator output
1 : Video detector output

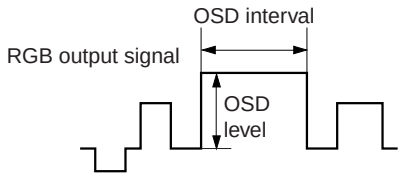
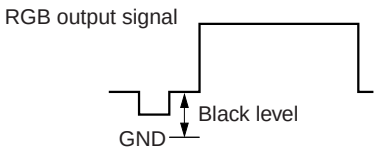
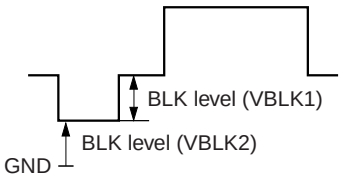
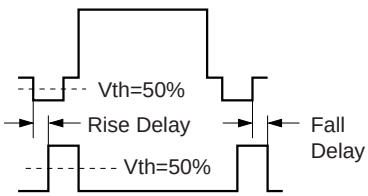
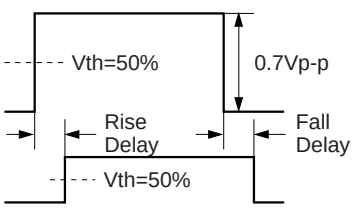
Sub Address 1010 VS OFF (1): Performs the control of VBLK sync DAC refresh function.
0 : Function operation ON
1 : Function operation OFF

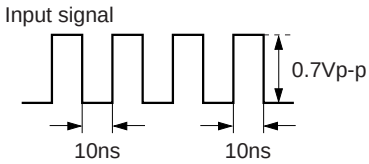
I²C Bus Logic System

No.	Item	Symbol	Min.	Typ.	Max.	Unit
1	High level input voltage	V_{IH}	3.0	—	5.0	V
2	Low level input voltage	V_{IL}	0	—	1.5	V
3	Low level output voltage with 3 mA SDA current inflow	V_{OL}	0	—	0.4	V
4	Maximum clock frequency	f_{SCL}	0	—	400	kHz
5	Minimum waiting time for data change	t_{BUF}	4.0	—	—	µs
6	Minimum waiting time for data transmission start	t_{HD} : STA	4.0	—	—	µs
7	Low level clock pulse width	t_{LOW}	4.7	—	—	µs
8	High level clock pulse width	t_{HIGH}	4.0	—	—	µs
9	Minimum waiting time for start preparation	t_{SU} : STA	4.7	—	—	µs
10	Minimum data hold time	t_{HD} : DAT	0	—	—	ns
11	Minimum data preparation time	t_{SU} : DAT	250	—	—	ns
12	Rise time	t_R	—	—	1	µs
13	Fall time	t_F	—	—	300	ns
14	Minimum waiting time for stop preparation	t_{SU} : STO	4.7	—	—	µs

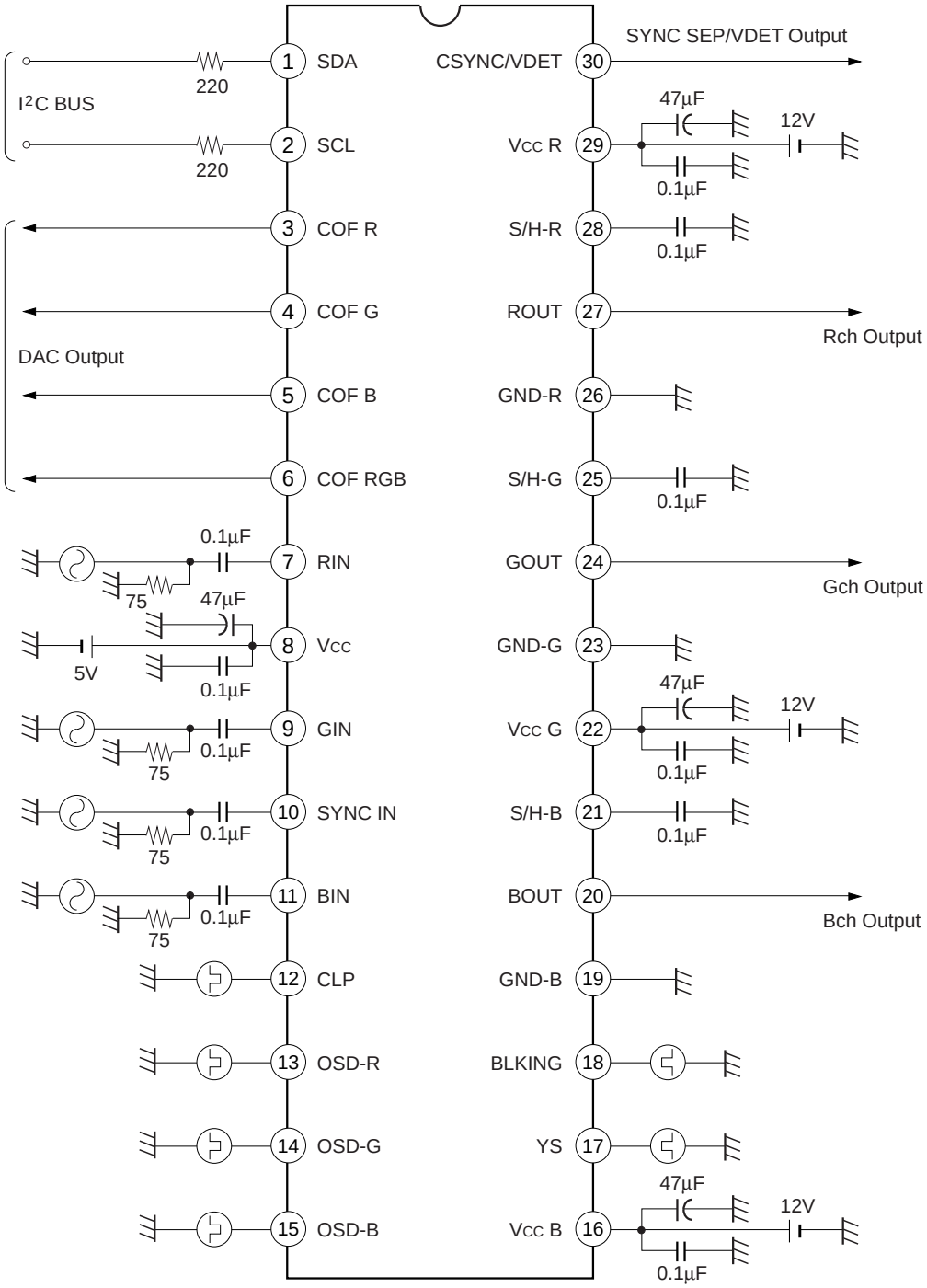
Electrical Characteristics

No.	Measurement item	Symbol	Measurement contents	Min.	Typ.	Max.	Unit
1	Current consumption (5 V)	$I_{CC}1$	V_{CC} (5 V) pin inflow current RGB signal input: None	85	115	140	mA
2	Current consumption (12 V)	$I_{CC}2$	V_{CC} R/G/B (12 V) pin inflow current RGB signal input: None	29.5	45	55.5	mA
3	Current consumption (12 V OFF)	$I_{CC}3$	V_{CC} pin inflow current for 12 V OFF RGB signal input: None	20	30	40	mA
4	Frequency response (50 MHz)	F50	Input the continuous 1 MHz, 50 MHz and 100 MHz sine waves (0.7 Vp-p). Measure the output amplitude gain difference at this time. Gain difference [dB]=20 log $\frac{\text{Vout (50 MHz)}}{\text{Vout (1 MHz)}}$ Gain difference [dB]=20 log $\frac{\text{Vout (100 MHz)}}{\text{Vout (1 MHz)}}$	–1.5	0	1.9	dB
5	Frequency response (100 MHz)	F100		–3.0	0	3.0	dB
6	Contrast control 1	GCONT1	Measure the output signal amplitude Vout level when a 0.7 Vp-p video signal is input. GCONT1 : Contrast=SubContrast=FF GCONT2 : Contrast=00/SubContrast=FF	5.6	6.2	—	Vp-p
7	Contrast control 2	GCONT2		—	0	100	mVp-p
8	Sub contrast control	GSUB	Measure the output signal amplitude Vout level when a 0.7 Vp-p video signal is input. Contrast=FF/SubContrast=00 	—	0	100	mVp-p

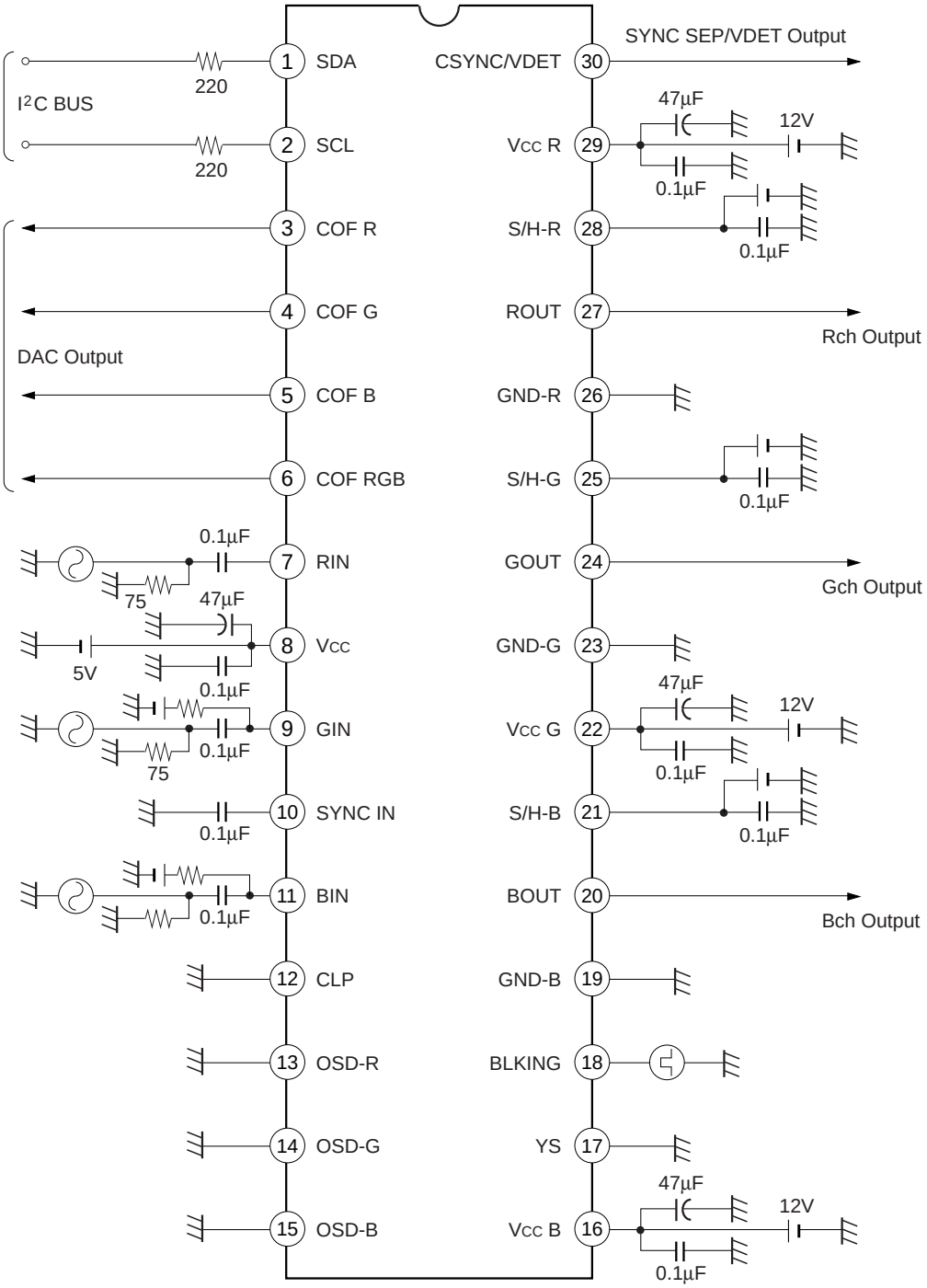
No.	Measurement item	Symbol	Measurement contents	Min.	Typ.	Max.	Unit
9	OSD gain control	GOSD1	Measure the OSD level of the output signal when the OSD pulse is input. GOSD1 : OSD=3F/SubContrast=FF GOSD2 : OSD=00/SubContrast=FF 	4.5	5	—	Vp-p
		GOSD2		—	0	150	mVp-p
10	Brightness control	VBRT1	Measure the black level of the RGB output signal. VBRT1 : Brightness=00 VBRT2 : Brightness=3F 	0.4	0.7	1	V
		VBRT2		2.2	2.6	3	
11	BLK control (BLK MODE=0)	VBLK1	Measure the BLK level of the output signal when the BLK pulse is input. 	—	0.3	0.6	V
	BLK control (BLK MODE=1)	VBLK2		—	0.3	0.6	
12	Sync separator output rise delay	SDLYR		—	30	40	ns
	Sync separator output fall delay	SDLYF		—	60	80	
13	VDET output rise delay	DDLYR		—	20	40	ns
	VDET output fall delay	DDLYF		—	30	60	

No.	Measurement item	Symbol	Measurement contents	Min.	Typ.	Max.	Unit
14	DAC output voltage (COFF=00)	VCUT1	Measure the DAC output voltage (Pin 6) for COFF=00/FF.	—	1	1.3	V
	DAC output voltage (COFF=FF)	VCUT2		3.9	4	—	
15	VDET output amplitude	VDET	Input the crosshatch signal of DotClock=100 MHz/0.7 Vp-p and measure the VDET output amplitude. SW SW=1/VDET LEVEL=0 	3.85	4	—	Vp-p

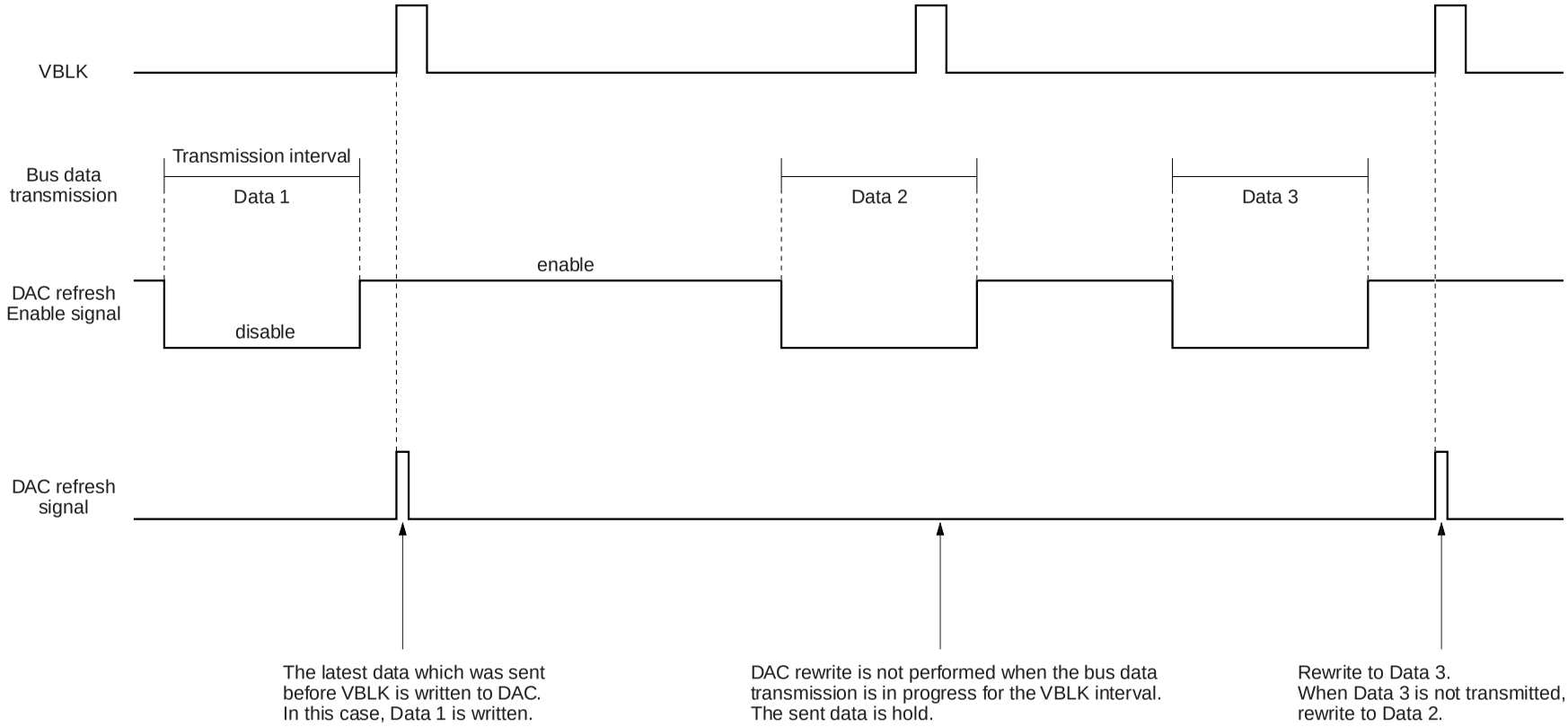
Electrical Characteristics Measurement Circuit



Electrical Characteristics Measurement Circuit (Frequency response)

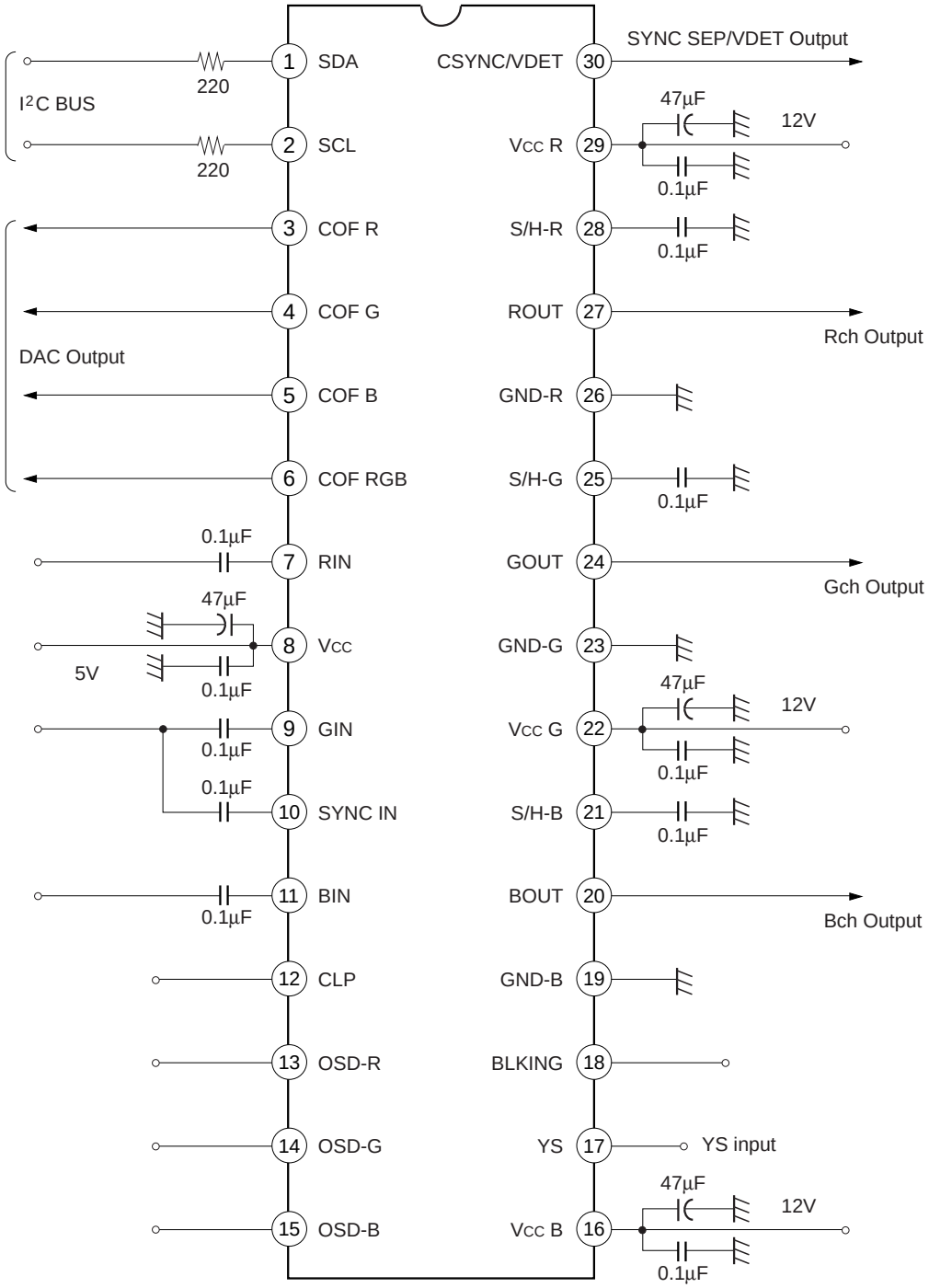


VBLK Sync DAC Refresh System



The VBLK signal is extracted form the composite BLK signal input to Pin 18. The DAC data rewrite for each control is simultaneously performed, synchronizing to the VBLK signal. The received I²C bus data is held by the latch till the next VBLK signal comes. Therefore, the timing of I²C bus data transmission from the microcomputer is free. The V blanking pulse width input to Pin 18 should be 300µs or more.

Application Circuit



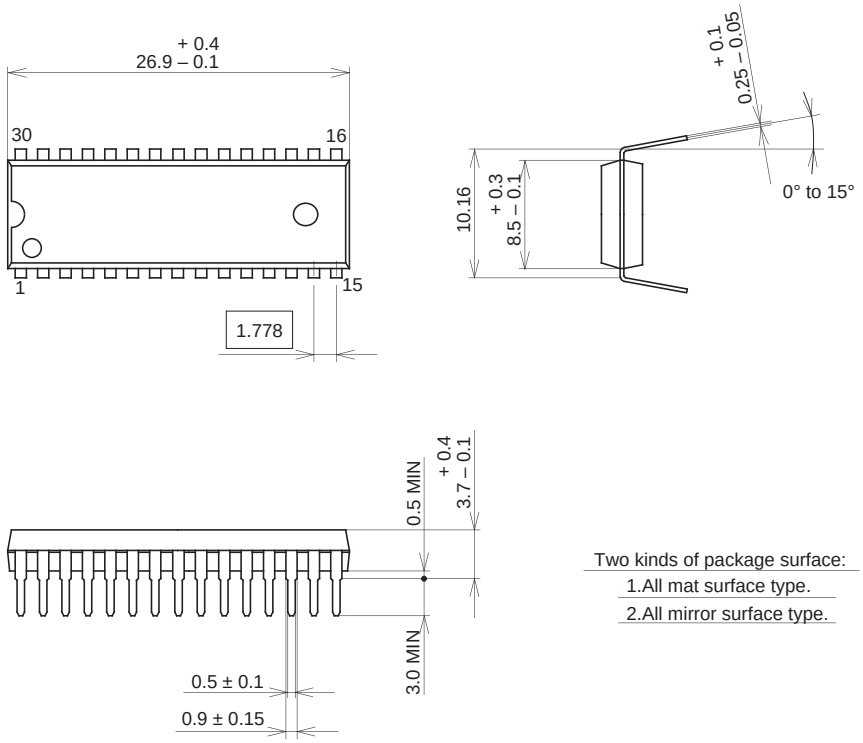
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Notes on Operation

1. The ROUT, GOUT and BOUT outputs should be received in the high impedance state.
2. The wiring from ROUT, GOUT and BOUT to the power amplifier should be as short as possible.
3. For the decoupling capacitors for V_{CC} and V_{CC} R/G/B, the ceramic capacitor and the electrolysis capacitor should be connected in parallel as closely to the IC as possible.
4. The clamp capacitors for RIN, GIN, BIN, S/H R, S/H G and S/H B should be connected as close to the IC as possible.
5. The signals to RIN, GIN and BIN should be input via a clamp capacitor with the low impedance.
6. Set the output OFF when the VDET/CSYNC output is not used. (The cross talk may deteriorate)

Package Outline Unit : mm

30PIN SDIP (PLASTIC)



Two kinds of package surface:
1.All mat surface type.
2.All mirror surface type.

SONY CODE	SDIP-30P-01
EIAJ CODE	SDIP030-P-0400
JEDEC CODE	————

PACKAGE STRUCTURE

MOLDING COMPOUND	EPOXY RESIN
LEAD TREATMENT	SOLDER/PALLADIUM PLATING
LEAD MATERIAL	COPPER ALLOY
PACKAGE MASS	1.8g