



SPN340T06

N-Channel Enhancement Mode MOSFET

DESCRIPTION

The SPN340T06 is the N-Channel enhancement mode power field effect transistor which is produced using super high cell density DMOS trench technology. This high density process is especially tailored to minimize on-state resistance. These devices are particularly suitable for synchronous rectifier application, Motor control power management and other Power Tool circuits. It has been optimized for low gate charge, low $R_{DS(ON)}$ and fast switching speed..

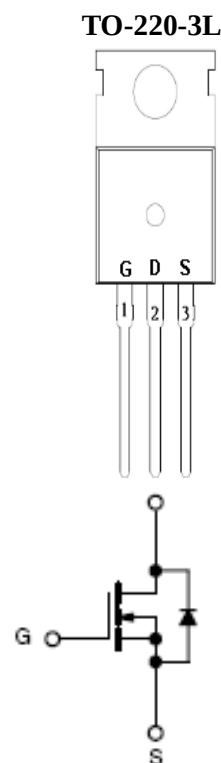
FEATURES

- ◆ 60V/340A, $R_{DS(ON)}=1.9m\Omega@V_{GS}=10V$
- ◆ Super high density cell design for extremely low $R_{DS(ON)}$
- ◆ Exceptional on-resistance and maximum DC current capability
- ◆ Enhanced Avalanche Ruggedness
- ◆ TO-220-3L package design

APPLICATIONS

- DC/DC Converter
- Hard Switching and High Speed Circuit
- Synchronous Buck Converter
- Power Tools
- UPS
- Motor Control

PIN CONFIGURATION



PART MARKING





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PIN DESCRIPTION

Pin	Symbol	Description
1	G	Gate
2	D	Drain
3	S	Source

ORDERING INFORMATION

Part Number	Package	Part Marking
SPN340T06T220TGB	TO-220-3L	SPN340T06

※ SPN340T060T220TGB: Tube ; Pb – Free; Halogen – Free

ABSOLUTE MAXIMUM RATINGS

(T_A=25°C Unless otherwise noted)

Parameter		Symbol	Typical	Unit
Drain-Source Voltage		V _{DSS}	60	V
Gate –Source Voltage		V _{GSS}	±20	V
Continuous Drain Current(Silicon Limited)	T _C =25°C	I _D	340	A
	T _C =70°C		240	
Continuous Drain Current(Package Limited)	T _C =25°C		120	
Pulsed Drain Current		I _{DM}	900	A
Power Dissipation	T _A =25°C	P _D	104	W
Avalanche Energy with Single Pulse (T _C =25°C , L =1mH)		E _{AS}	702	mJ
Operating Junction Temperature		T _J	-55/150	°C
Storage Temperature Range		T _{STG}	-55/150	°C
Thermal Resistance-Junction to Case		R _{θJC}	1.2	°C/W



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ELECTRICAL CHARACTERISTICS

(T_A=25°C Unless otherwise noted)

Parameter	Symbol	Conditions	Min.	Typ	Max.	Unit
Static						
Drain-Source Breakdown Voltage	V _{(BR)DSS}	V _{GS} =0V, I _D =250μA	60			V
Gate Threshold Voltage	V _{GS(th)}	V _{DS} =V _{GS} , I _D =250μA	2	3	4	
Gate Leakage Current	I _{GSS}	V _{DS} =0V, V _{GS} =±20V			±100	nA
Zero Gate Voltage Drain Current	I _{DSS}	V _{DS} =60V, V _{GS} =0V T _J = 25 °C			1	μA
		V _{DS} =60V, V _{GS} =0V T _J =100 °C			100	
On-State Drain Current	I _{D(on)}	V _{DS} ≥5V, V _{GS} =10V	60			A
Drain-Source On-Resistance	R _{DS(on)}	V _{GS} =10V, I _D =20A		1.67	1.9	mΩ
Forward Transconductance	g _{fs}	V _{DS} =5V, I _D =20A		92		S
Gate Resistance	R _G	V _{GS} =0V, V _{DS} =Open, f=1MHz		0.7		Ω
Diode Forward Voltage	V _{SD}	I _F =20A, V _{GS} =0V		0.9	1.2	V
Dynamic						
Total Gate Charge	Q _g	V _{DS} =30V, V _{GS} =10V I _D =20A		124		nC
Gate-Source Charge	Q _{gs}			30		
Gate-Drain Charge	Q _{gd}			20		
Input Capacitance	C _{iss}	V _{DS} =30V, V _{GS} =0V f=1MHz		10570		pF
Output Capacitance	C _{oss}			4050		
Reverse Transfer Capacitance	C _{rss}			84		
Turn-On Time	t _{d(on)}	V _{DD} =30V, I _D =20A, V _{GS} =10V, R _G =3Ω		35		nS
	t _r			27		
Turn-Off Time	t _{d(off)}			70		
	t _f			15		



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TYPICAL CHARACTERISTICS

Fig 1. Typical Output Characteristics

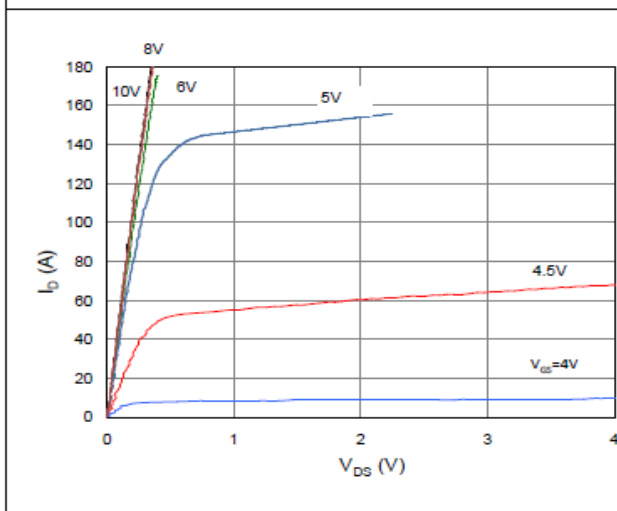


Figure 2. On-Resistance vs. Gate-Source Voltage

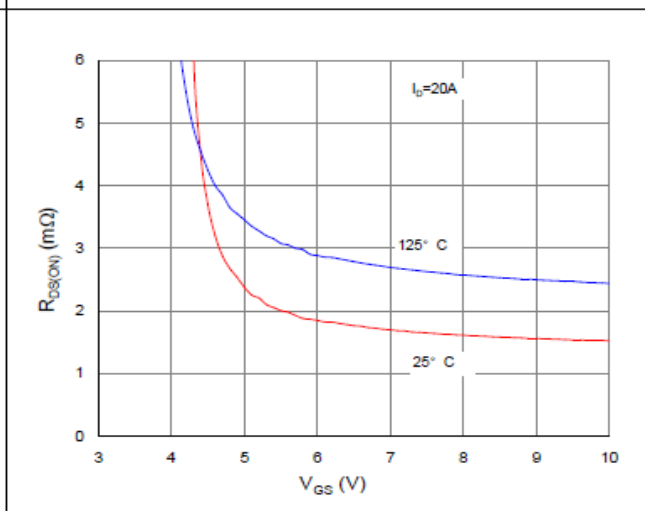


Figure 3. On-Resistance vs. Drain Current and Gate Voltage

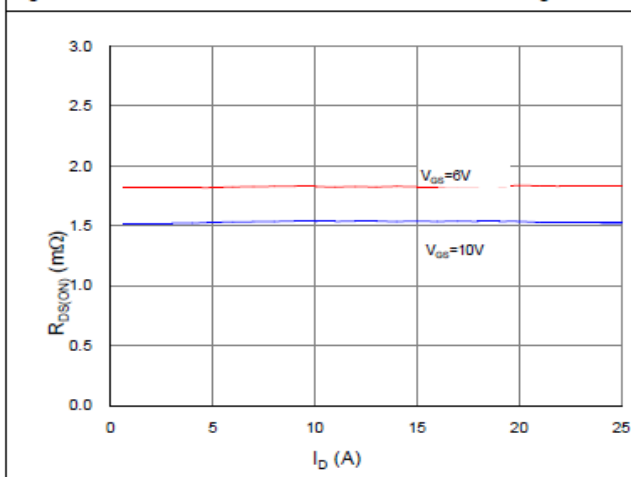


Figure 4. Normalized On-Resistance vs. Junction Temperature

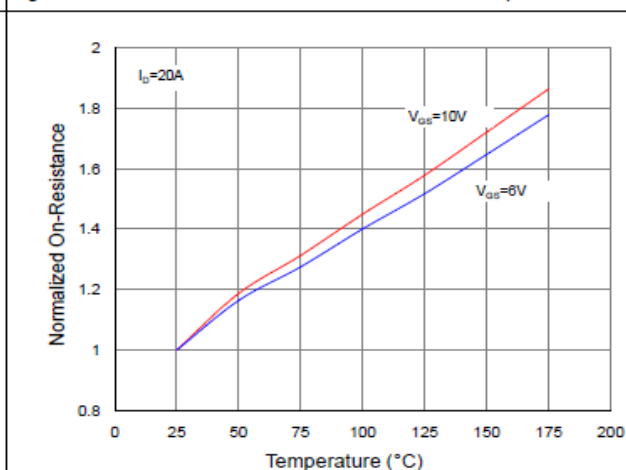


Figure 5. Typical Transfer Characteristics

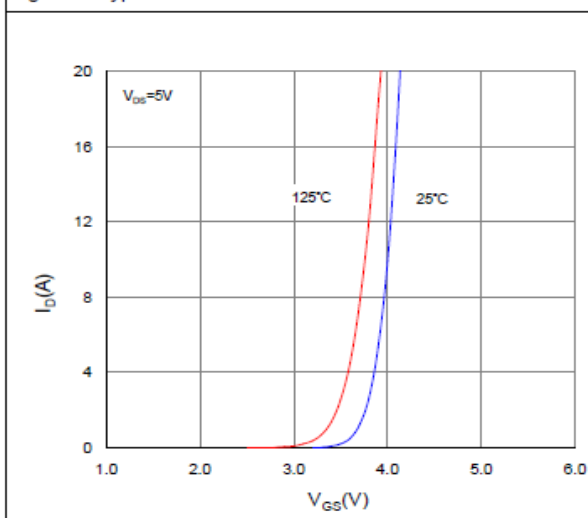
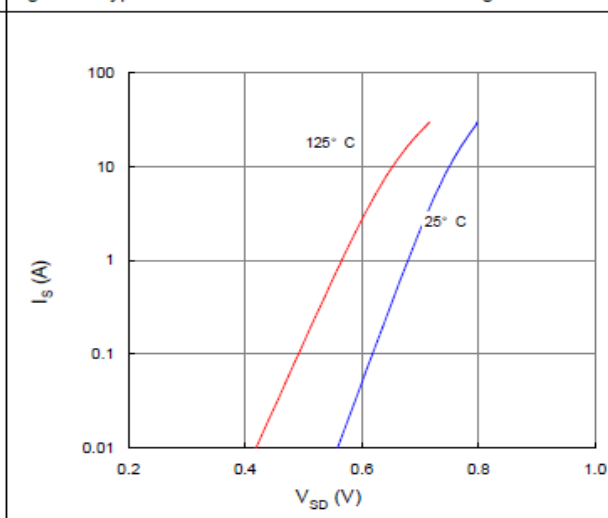


Figure 6. Typical Source-Drain Diode Forward Voltage





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TYPICAL CHARACTERISTICS

Figure 7. Typical Gate-Charge vs. Gate-to-Source Voltage

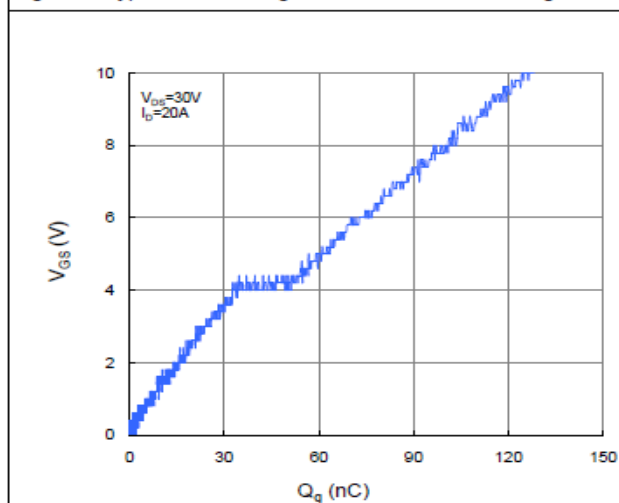


Figure 8. Typical Capacitance vs. Drain-to-Source Voltage

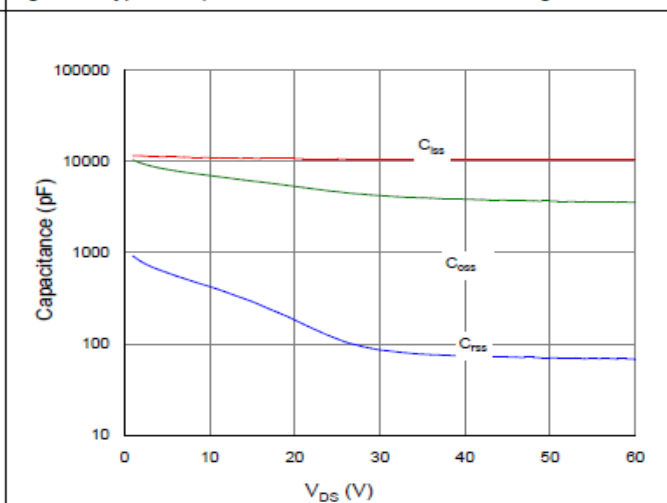


Figure 9. Maximum Safe Operating Area

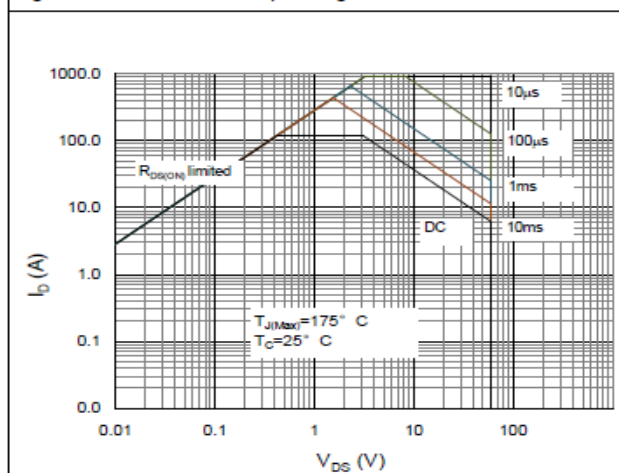


Figure 10. Maximum Drain Current vs. Case Temperature

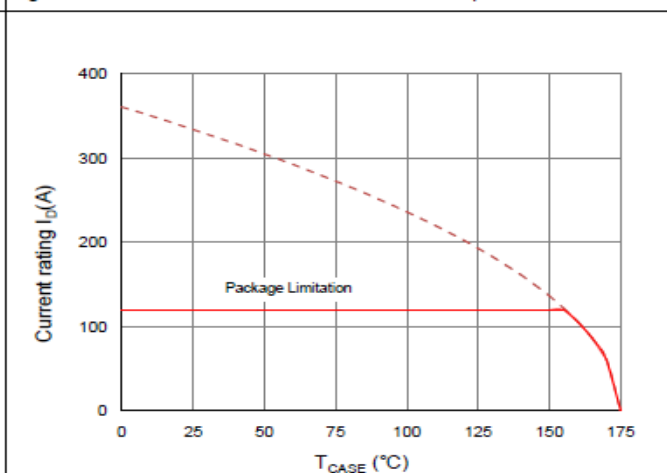
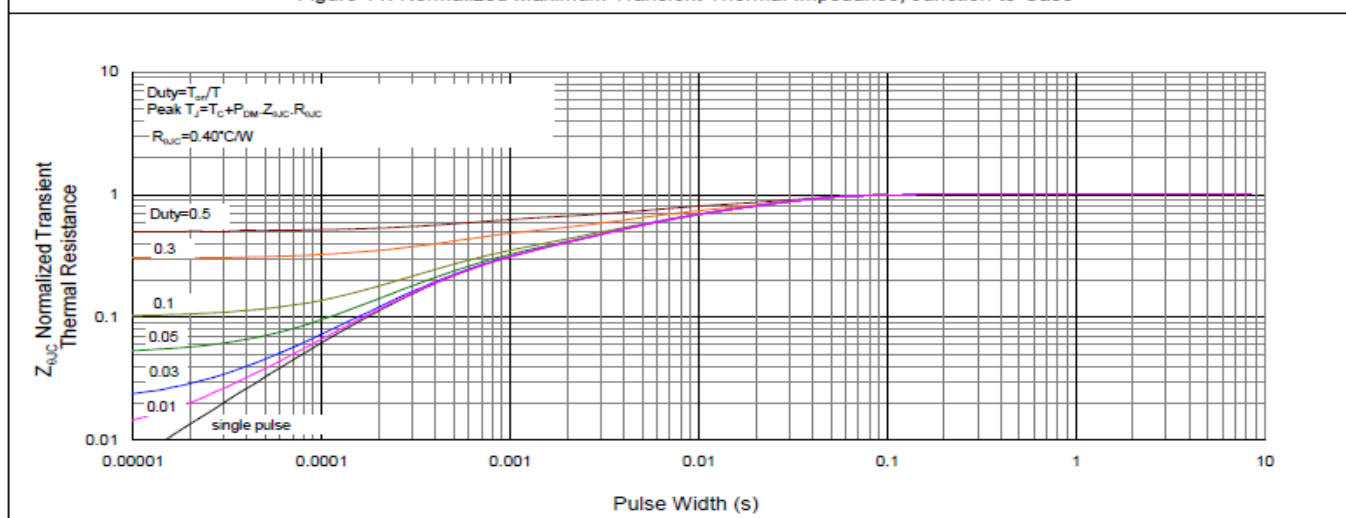


Figure 11. Normalized Maximum Transient Thermal Impedance, Junction-to-Case





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