MAX 5000

Programmable Logic Device Family

June 1996, ver. 3 Data Sheet

Features...

- Advanced Multiple Array MatriX (MAX) 5000 architecture combining speed and ease-of-use of PAL devices with the density of programmable gate arrays
- Complete family of high-performance, erasable CMOS EPROM EPLDs for designs ranging from fast 28-pin address decoders to 100-pin LSI custom peripherals
- 600 to 3,750 usable gates (see Table 1)
- Fast, 15-ns combinatorial delays and 83.3-MHz counter frequencies
- Configurable expander product-term distribution allowing more than 32 product terms in a single macrocell
- 28 to 100 pins available in DIP, J-lead, PGA, SOIC, and QFP packages
- Programmable registers providing D, T, JK, and SR flipflop functionality with individual clear, preset, and clock controls
- Programmable security bit for protection of proprietary designs
- Software design support featuring Altera's MAX+PLUS II development system on 486- or Pentium-based PCs, and Sun SPARCstation, HP 9000 Series 700, and IBM RISC System/6000 workstations

Table 1. MAX 5000 Device Features

Feature	EPM5032	EPM5064	EPM5128	EPM5130	EPM5192
Usable gates	600	1,250	2,500	2,500	3,750
Macrocells	32	64	128	128	192
Logic array blocks (LABs)	1	4	8	8	12
Expanders	64	128	256	256	384
Routing	Global	PIA	PIA	PIA	PIA
Maximum user I/O pins	24	36	60	68, 84	72
t_{PD} (ns)	15	25	25	25	25
t_{ASU} (ns)	4	4	4	4	4
t_{CO} (ns)	10	14	14	14	14
f_{CNT} (MHz)	76.9	50	50	50	50

...and More Features

- Programming support with Altera's Master Programming Unit (MPU) or programming hardware from other manufacturers
- Additional design entry and simulation support provided by EDIF, LPM, Verilog HDL, VHDL, and other interfaces to popular EDA tools from manufacturers such as Cadence, Data I/O, Exemplar, Mentor Graphics, MINC, OrCAD, Synopsys, VeriBest, and Viewlogic

General Description

The MAX 5000 family combines innovative architecture and advanced process technologies to offer optimum performance, flexibility, and the highest logic-to-pin ratio of any general-purpose programmable logic device (PLD) family. The MAX 5000 family provides 600 to 3,750 usable gates, pin-to-pin delays as fast as 15 ns, and counter frequencies of up to 83.3 MHz. See Table 2.

Table 2. MAX 5000 Timing Parameter Availability

Device	Speed (t_{PD1})				
	15 ns	20 ns	25 ns	30 ns	35 ns
EPM5032	✓	✓	✓		
EPM5064			✓	✓	✓
EPM5128			✓	✓	✓
EPM5130			✓		✓
EPM5192			✓		✓

The MAX 5000 architecture supports 100% TTL emulation and high-density integration of multiple SSI, MSI, and LSI logic functions. For example, an EPM5192 device can replace over 100 74-series devices; it can integrate complete subsystems into a single package, saving board area and reducing power consumption. MAX 5000 EPLDs are available in a wide range of packages (see Table 3), including the following:

- Windowed ceramic and plastic dual in-line (CerDIP and PDIP)
- Windowed ceramic and plastic J-lead chip carrier (JLCC and PLCC)
- Windowed ceramic pin-grid array (PGA)
- Plastic small-outline integrated circuit (SOIC)
- Ceramic and plastic quad flat pack (CQFP and PQFP)

Table 3. MAX 5000 Pin Count & Package Options *Note (1)*

Device	Pin Count				
	28	44	68	84	100
EPM5032	CerDIP PDIP JLCC PLCC SOIC				
EPM5064		JLCC PLCC			
EPM5128			JLCC PLCC PGA		
EPM5130				JLCC PLCC	PGA PQFP
EPM5192				JLCC PLCC PGA	

Note:
(1) Contact Altera for up to date information on package availability.

MAX 5000 EPLDs have between 32 and 192 macrocells that are combined into groups called logic array blocks (LABs). Each macrocell has a programmable-AND/fixed-OR array and a configurable register that provides D, T, JK, or SR operation with independent programmable clock, clear, and preset functions. To build complex logic functions, each macrocell can be supplemented with shareable expander product terms ("shared expanders") to provide more than 32 product terms per macrocell.

The MAX 5000 family is supported by Altera's MAX+PLUS II development system, a single, integrated package that offers schematic, text—including the Altera Hardware Description Language (AHDL)—and waveform design entry; compilation and logic synthesis; simulation and timing analysis; and device programming. MAX+PLUS II provides EDIF 2 0 0 and 3 0 0, LPM, VHDL, Verilog HDL, and other interfaces for additional design entry and simulation support from other industry-standard PC- and workstation-based EDA tools. MAX+PLUS II runs on 486- and Pentium-based PCs, and Sun SPARCstation, HP 9000 Series 700, IBM RISC System/6000 workstations.



For more information, go to the *MAX+PLUS II Programmable Logic Development System & Software Data Sheet* in this data book.

Functional Description

This section provides a functional description of MAX 5000 EPLDs, which have the following architectural features:

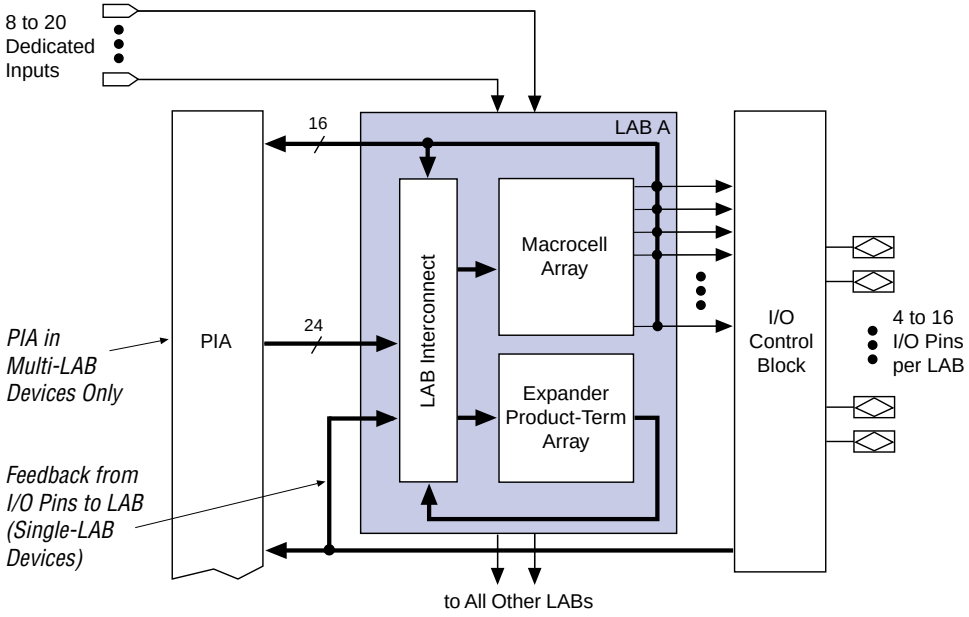
- Logic array blocks
- Macrocells
- Clocking options
- Expander product terms
- Programmable interconnect array
- I/O control blocks

The MAX 5000 architecture is based on the concept of linking high-performance, flexible logic array modules called logic array blocks (LABs). Multiple LABs are linked via the programmable interconnect array (PIA), a global bus that is fed by all I/O pins and macrocells. In addition to these basic elements, the MAX 5000 architecture includes 8 to 20 dedicated inputs, each of which can be used as a high-speed, general-purpose input. Alternatively, one of the dedicated inputs can be used as a high-speed global clock for registers.

Logic Array Blocks

MAX 5000 EPLDs contain 1 to 12 LABs. The EPM5032 has a single LAB, while the EPM5064, EPM5128, EPM5130, and EPM5192 contain multiple LABs. Each LAB consists of a macrocell array and an expander product-term array. See Figure 1. The number of macrocells and expanders in the arrays varies with each device.

Figure 1. MAX 5000 Architecture

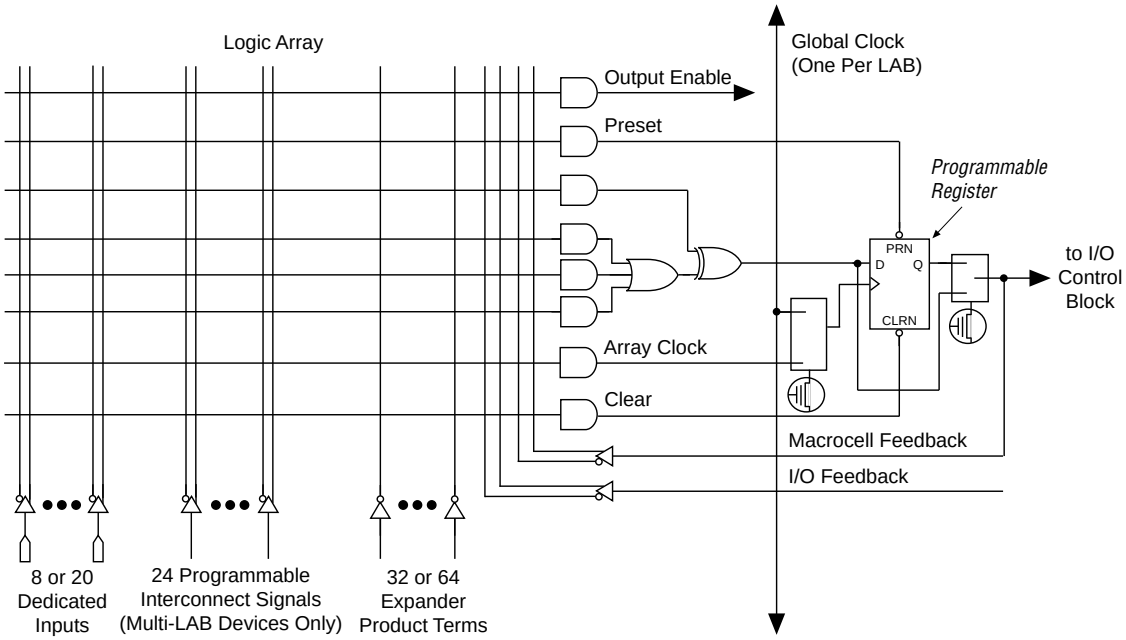


Macrocells are the primary resource for logic implementation. Additional logic capability is available from expanders, which can be used to supplement the capabilities of any macrocell. The expander product-term array consists of a group of unallocated, inverted product terms that can be used and shared by all macrocells in the LAB to create combinatorial and registered logic. These flexible macrocells and shareable expanders facilitate variable product-term designs without the inflexibility of fixed product-term architectures. All macrocell outputs are globally routed within an LAB via the LAB interconnect. The outputs of the macrocells also feed the I/O control block, which consists of groups of programmable tri-state buffers and I/O pins. In the EPM5064, EPM5128, EPM5130, and EPM5192 devices, multiple LABs are connected by a PIA. All macrocells feed the PIA to provide efficient routing for high-fan-in designs.

Macrocells

The MAX 5000 macrocell consists of a programmable logic array and an independently configurable register (see Figure 2). The register can be programmed to emulate D, T, JK, or SR operation, as a flow-through latch, or bypassed for combinatorial operation. Combinatorial logic is implemented in the programmable logic array, in which three product terms that are ORed together feed one input to an XOR gate. The second input to the XOR gate is used for complex XOR arithmetic logic functions and for De Morgan's inversion. The output of the XOR gate feeds the programmable register or bypasses it for combinatorial operation.

Figure 2. MAX 5000 Device Macrocell



Additional product terms—called secondary product terms—are used to control the output enable, preset, clear, and clock signals. Preset and clear product terms drive the active-low asynchronous preset and asynchronous clear inputs to the configurable flipflop. The clock product term allows each register to have an independent clock and supports positive- and negative-edge-triggered operation. Macrocells that drive an output pin can use the output enable product term to control the active-high tri-state buffer in the I/O control block.

The MAX 5000 macrocell configurability makes it possible to efficiently integrate complete subsystems into a single device.

Clocking Options

Each LAB supports either global or array clocking. Global clocking is provided by a dedicated clock signal (CLK) that offers fast clock-to-output delay times. Since each LAB has one global clock, all flipflop clocks within the LAB can be positive-edge-triggered from the CLK pin. If the CLK pin is not used as a global clock, it can be used as a high-speed dedicated input.

In the array clocking mode, each flipflop is clocked by a product term. Any input pin or internal logic can be used as a clock source. Array clocking allows each flipflop to be configured for positive- or negative-edge-triggered operation, giving the macrocell increased flexibility. Systems that require multiple clocks are easily integrated into MAX 5000 EPLDs.

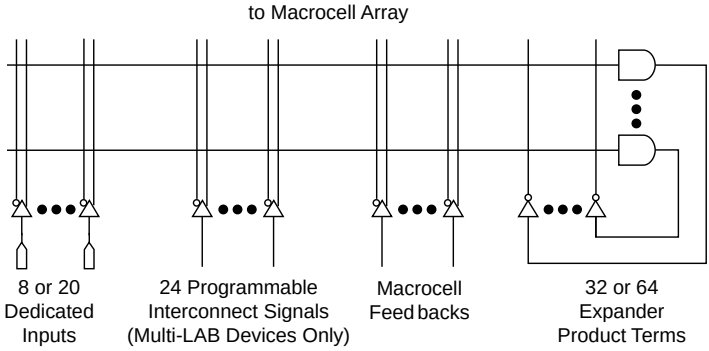
Each flipflop in an LAB can be clocked by a different array-generated clock; however, global and array clocking modes cannot be mixed in the same LAB.

Expander Product Terms

While most logic functions can be implemented with the product terms available in each macrocell, some logic functions are more complex and require additional product terms. Although additional macrocells can be used to supply the needed logic resources, the MAX 5000 architecture can also use shared expander product terms that provide additional product terms directly to any macrocell in the same LAB. These expanders help ensure that logic is synthesized with the fewest possible logic resources to obtain the fastest possible speed.

Each LAB has 32 shared expanders (except for the EPM5032 device, which has 64). The expanders can be viewed as a pool of uncommitted product terms. The expander product-term array (see Figure 3) contains unallocated, inverted product terms that feed the macrocell array. Expanders can be used and shared by all product terms in the LAB. Wherever extra logic is needed (including register control functions), expanders can be used to implement the logic. These expanders provide the flexibility to implement register- and product-term-intensive designs in MAX 5000 EPLDs.

Figure 3. Expander Product Terms



Expanders are fed by all signals in the LAB. One expander can feed all macrocells in the LAB or multiple product terms in the same macrocell. Since expanders also feed the secondary product terms of each macrocell, complex logic functions can be implemented without using additional macrocells. Expanders can also be cross-coupled to build additional flipflops, latches, or input registers. A small delay (t_{SEXP}) is incurred when shared expanders are used.

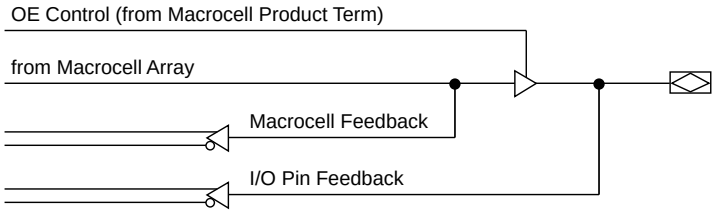
Programmable Interconnect Array

The higher-density MAX 5000 devices—EPM5064, EPM5128, EPM5130, and EPM5192—use a programmable interconnect array (PIA) to route signals between the various LABs. The PIA, which is fed by all macrocell and I/O pin feedbacks, routes only the signals required for implementing logic in an LAB. While the routing delays of channel-based routing schemes in masked or field-programmable gate arrays (FPGAs) are cumulative, variable, and path-dependent, the MAX 5000 PIA has a fixed delay. The PIA thus eliminates skew between signals and makes timing performance easy to predict.

I/O Control Blocks

Each LAB has an I/O control block that allows each I/O pin to be individually configured for input, output, or bidirectional operation. See Figure 4. The I/O control block is fed by the macrocell array. A dedicated macrocell product term controls a tri-state buffer, which drives the I/O pin.

Figure 4. I/O Control Block



The MAX 5000 architecture provides dual I/O feedback in which macrocell and I/O pin feedbacks are independent, allowing maximum flexibility. When an I/O pin is configured as an input, the associated macrocell can be used for buried logic. Using an I/O pin as an input in single-LAB devices reduces the number of available expanders by two. In multi-LAB devices, I/O pins feed the PIA directly.

Design Security

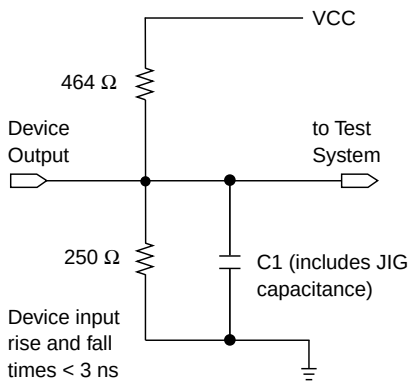
All MAX 5000 EPLDs contain a programmable security bit that controls access to the data programmed into the device. When this bit is programmed, a proprietary design implemented in the device cannot be copied or retrieved. This feature provides a high level of design security, since programmed data within EPROM cells is invisible. The security bit that controls this function, as well as all other program data, is reset when an EPLD is erased.

Generic Testing

MAX 5000 EPLDs are fully functionally tested. Complete testing of each programmable EPROM bit and all internal logic elements ensures 100% programming yield. AC test measurements are taken under conditions equivalent to those in Figure 5.

Figure 5. AC Test Conditions

Power supply transients can affect AC measurements. Simultaneous transitions of multiple outputs should be avoided for accurate measurement. Threshold tests must not be performed under AC conditions. Large-amplitude, fast ground-current transients normally occur as the device outputs discharge the load capacitances. When these transients flow through the parasitic inductance between the device ground pin and the test system ground, significant reductions in observable noise immunity can result.



Test patterns can be used and then erased during early stages of the device production flow. EPROM-based EPLDs in one-time-programmable windowless packages also contain on-board logic test circuitry to allow verification of function and AC specifications during the production flow.

Device Programming

All MAX 5000 EPLDs can be programmed on 486- and Pentium-based PCs with an Altera Logic Programmer card, the Master Programming Unit (MPU), and the appropriate device adapter. The MPU checks continuity to ensure adequate electrical contact between the adapter and the device.



For more information, see *Altera Programming Hardware Data Sheet* in this data book.

MAX+PLUS II software can use text- or waveform-format test vectors created with the MAX+PLUS II Text or Waveform Editor to test a programmed device. For added design verification, designers can perform functional testing to compare the functional behavior of a MAX 5000 EPLD with the simulation results. (This feature requires a device adapter with the "PLM-" prefix.)

Data I/O and other programming hardware manufacturers also offer programming support for Altera devices.



For more information, see *Programming Hardware Manufacturers* in this data book.

QFP Carrier & Development Socket

MAX 5000 devices in 100-pin QFP packages are shipped in special plastic carriers to protect the fragile QFP leads. Each carrier can be used with a prototype development socket and programming hardware available from Altera or Data I/O. This carrier technology makes it possible to program, test, erase, and reprogram devices without exposing the leads to mechanical stress.



For detailed information and carrier dimensions, refer to the*QFP Carrier & Development Socket Data Sheet* in this data book.

MAX 5000 Device Absolute Maximum Ratings *Note (1)*

Symbol	Parameter	Conditions	Min	Max	Unit
V_{CC}	Supply voltage	With respect to GND	–2.0	7.0	V
V_I	DC input voltage	*Note (2)*	–2.0	7.0	V
I_{OUT}	DC output current, per pin		–25	25	mA
T_{STG}	Storage temperature	No bias	–65	135	° C
T_{AMB}	Ambient temperature	Under bias	–65	135	° C
T_J	Junction temperature	Ceramic packages, under bias		150	° C
		Plastic packages, under bias		135	° C

MAX 5000 Device Recommended Operating Conditions

Symbol	Parameter	Conditions	Min	Max	Unit
V_{CC}	Supply voltage	*Notes (3)*, *(4)*	4.75 (4.5)	5.25 (5.5)	V
V_I	Input voltage		0	V_{CC}	V
V_O	Output voltage		0	V_{CC}	V
T_A	Operating temperature	For commercial use	0	70	° C
T_A	Operating temperature	For industrial use	–40	85	° C
t_R	Input rise time			100	ns
t_F	Input fall time			100	ns

MAX 5000 Device DC Operating Conditions *Note (5)*

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{IH}	High-level input voltage	*Note (3)*	2.0		V_{CC} + 0.3	V
V_{IL}	Low-level input voltage		–0.3		0.8	V
V_{OH}	High-level TTL output voltage	I_{OH} = –4 mA DC, *Note (6)*	2.4			V
V_{OL}	Low-level output voltage	I_{OL} = 8 mA DC, *Note (6)*			0.45	V
I_I	Input leakage current	$V_I = V_{CC}$ or GND	–10		10	µA
I_{OZ}	Tri-state output off-state current	$V_O = V_{CC}$ or GND	–40		40	µA

EPM5032 MAX 5000 Device Capacitance

Symbol	Parameter	Conditions	Min	Max	Unit
C_{IN}	Input pin capacitance	V_{IN} = 0 V, f = 1.0 MHz		10	pF
C_{IO}	I/O pin capacitance	V_{OUT} = 0 V, f = 1.0 MHz		12	pF

EPM5064, EPM5128, EPM5130 & EPM5192 MAX 5000 Device Capacitance

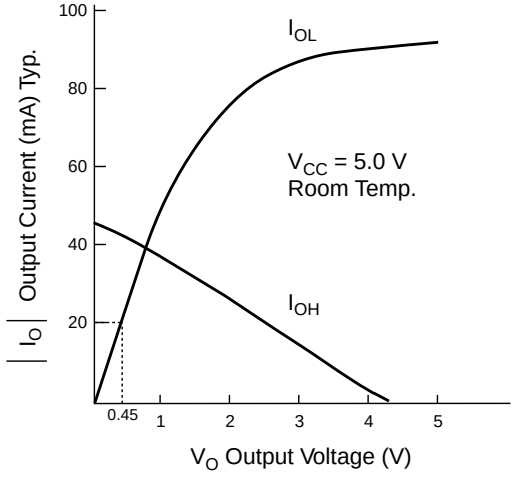
Symbol	Parameter	Conditions	Min	Max	Unit
C_{IN}	Input pin capacitance	V_{IN} = 0 V, f = 1.0 MHz		10	pF
$C_{I/O}$	I/O pin capacitance	V_{OUT} = 0 V, f = 1.0 MHz		20	pF

Notes to tables:

(1) See *Operating Requirements for Altera Devices Data Sheet* in this data book.
(2) Minimum DC input is –0.3 V. During transitions, the inputs may undershoot to –2.0 V or overshoot to 7.0 V for periods shorter than 20 ns under no-load conditions.
(3) Numbers in parentheses are for industrial-temperature-range versions.
(4) Maximum V_{CC} rise time for MAX 5000 devices is 10 ms.
(5) Typical values are for T_A = 25° C and V_{CC} = 5.0 V.
(6) The I_{OH} parameter refers to high-level TTL output current; the I_{OL} parameter refers to low-level TTL output current.

Figure 6 shows typical output drive characteristics of MAX 5000 devices.

Figure 6. Output Drive Characteristics of MAX 5000 Devices

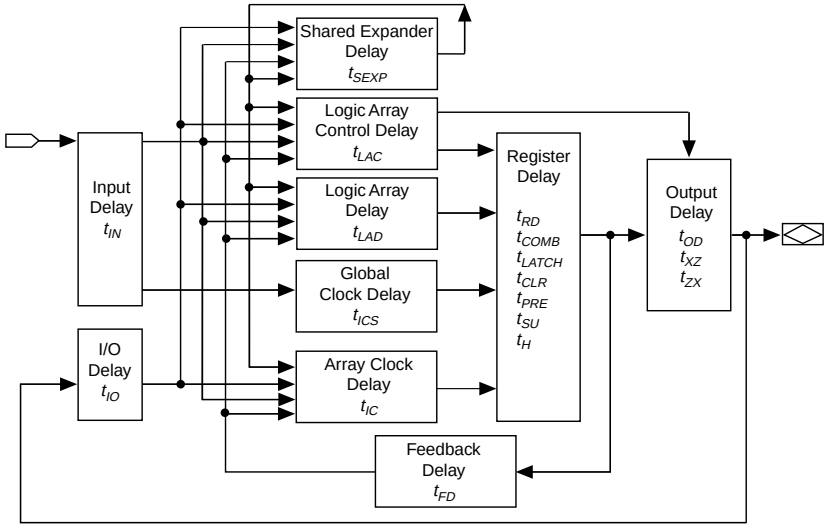


Timing Model

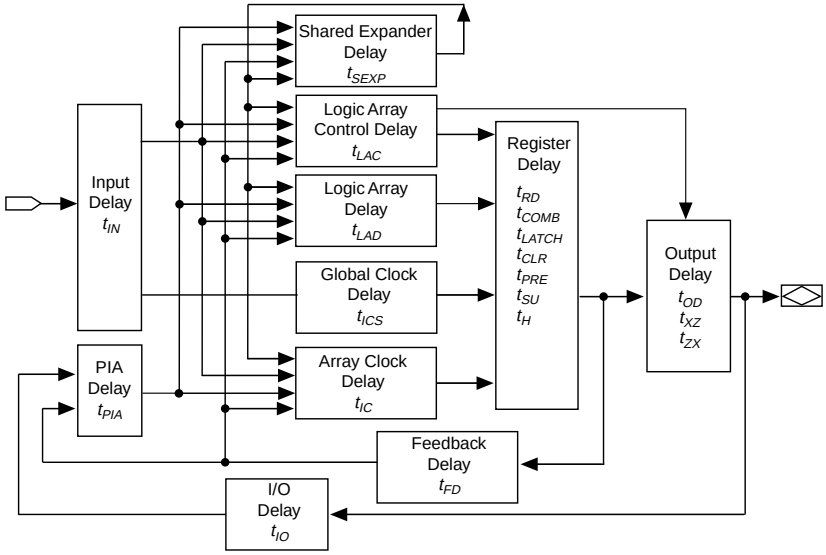
MAX 5000 EPLD timing can be analyzed with the MAX+PLUS II software, with a variety of other industry-standard EDA simulators and timing analyzers, or with the timing model shown in Figure 7. MAX 5000 EPLDs have fixed internal delays that allow the user to determine the worst-case timing for any design. MAX+PLUS II provides timing simulation, point-to-point delay prediction, and detailed timing analysis for system-level performance evaluation.

Figure 7. MAX 5000 Timing Model

Single-LAB EPLDs



Multi-LAB EPLDs



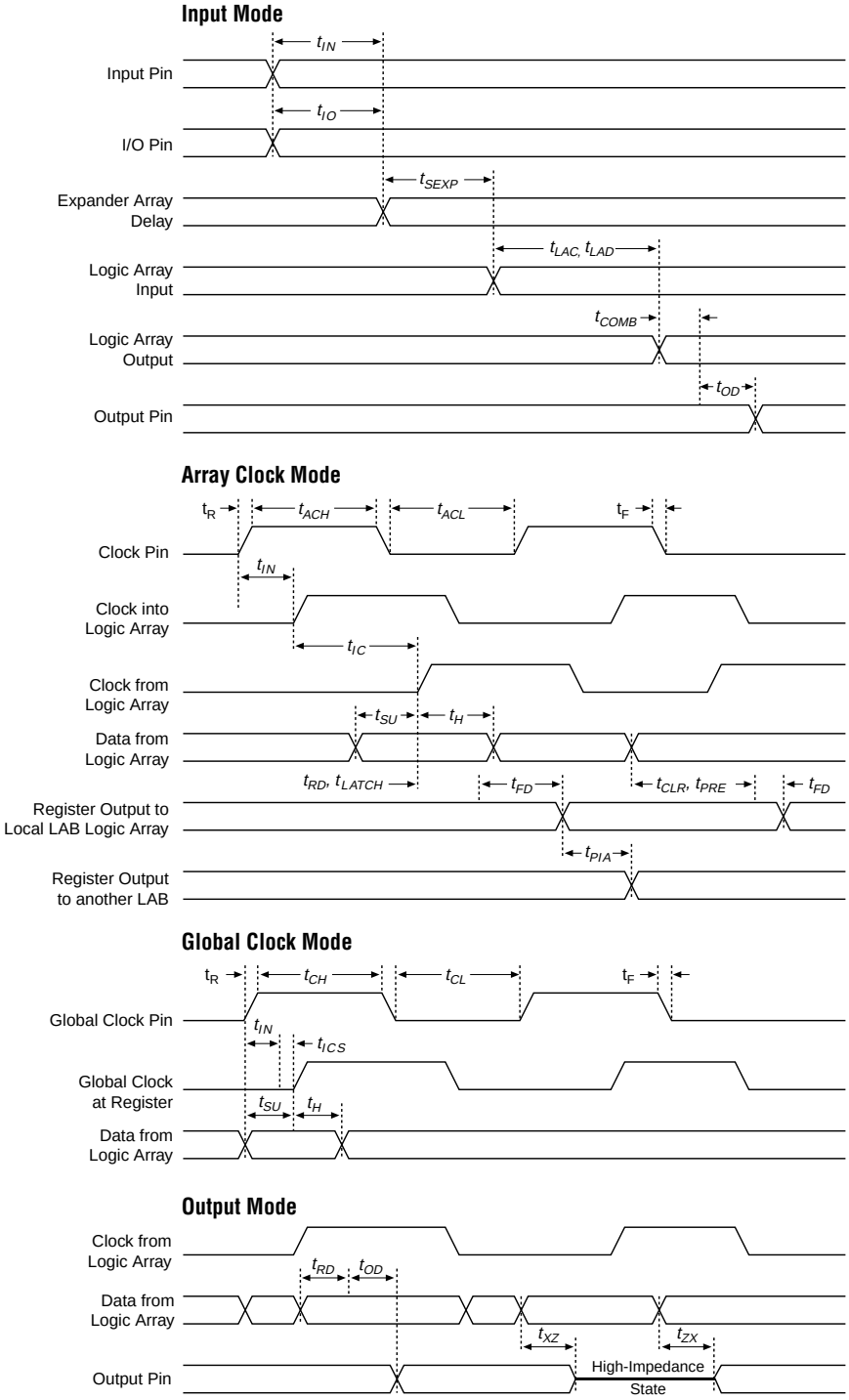
Timing information can be derived from the timing model and parameters for a particular EPLD. External timing parameters are calculated with the sum of internal parameters and represent pin-to-pin timing delays. Figure 8 shows the internal timing relationship for internal and external delay parameters.

For more information on EPLD timing, refer to *Application Note 78 (Understanding MAX 7000, MAX 5000 & Classic Timing)* in this data book.

Figure 8. Switching Waveforms

In multi-LAB EPLDs, I/O pins that are used as inputs traverse the PIA.

t_R & t_F < 3 ns. Inputs are driven at 3 V for a logic high and 0 V for a logic low. All timing characteristics are measured at 1.5 V.



EPM5032 AC Operating Conditions *Note (1)*

External Timing Parameters			EPM5032-15		EPM5032-20		EPM5032-25		
Symbol	**Parameter**	**Conditions**	**Min**	**Max**	**Min**	**Max**	**Min**	**Max**	**Unit**
t_{PD1}	Input to non-registered output	C1 = 35 pF		15		20		25	ns
t_{PD2}	I/O input to non-registered output	C1 = 35 pF		15		20		25	ns
t_{SU}	Global clock setup time		9		12		15		ns
t_{H}	Global clock hold time		0		0		0		ns
t_{CO1}	Global clock to output delay	C1 = 35 pF		10		12		15	ns
t_{CH}	Global clock high time		6		7		8		ns
t_{CL}	Global clock low time		6		7		8		ns
t_{ASU}	Array clock setup time		5		6		8		ns
t_{AH}	Array clock hold time		5		6		8		ns
t_{ACO1}	Array clock to output delay	C1 = 35 pF		15		18		22	ns
t_{ACH}	Array clock high time	*Note (3)*	6		7		9		ns
t_{ACL}	Array clock low time		7		9		11		ns
t_{ODH}	Output data hold time after clock	C1 = 35 pF *(2)*	1		1		1		ns
t_{CNT}	Min. global clock period			13		16		20	ns
f_{CNT}	Max. internal global clock frequency	*Note (4)*	76.9		62.5		50		MHz
t_{ACNT}	Min. array clock period			13		16		20	ns
f_{ACNT}	Max. internal array clock frequency	*Note (4)*	76.9		62.5		50		MHz
f_{MAX}	Max. clock frequency	*Note (5)*	83.3		71.4		62.5		MHz

Internal Timing Parameters *Note (6)*			EPM5032-15		EPM5032-20		EPM5032-25		
Symbol	**Parameter**	**Conditions**	**Min**	**Max**	**Min**	**Max**	**Min**	**Max**	**Unit**
t_{IN}	Input pad and buffer delay			3		5		7	ns
t_{IO}	I/O input pad and buffer delay			3		5		7	ns
t_{SEXP}	Expander array delay			8		10		15	ns
t_{LAD}	Logic array delay			7		10		13	ns
t_{LAC}	Logic control array delay			4		4		4	ns
t_{OD}	Output buffer and pad delay	C1 = 35 pF		4		4		4	ns
t_{ZX}	Output buffer enable delay	C1 = 35 pF		7		7		7	ns
t_{XZ}	Output buffer disable delay	C1 = 5 pF		7		7		7	ns
t_{SU}	Register setup time		4		4		5		ns
t_{LATCH}	Flow-through latch delay			1		1		1	ns
t_{RD}	Register delay			1		1		1	ns
t_{COMB}	Combinatorial delay			1		1		1	ns
t_{H}	Register hold time		5		8		10		ns
t_{IC}	Array clock delay			7		8		10	ns
t_{ICS}	Global clock delay			2		2		3	ns
t_{FD}	Feedback delay			1		1		1	ns
t_{PRE}	Register preset time			5		6		9	ns
t_{CLR}	Register clear time			5		6		9	ns

EPM5064, EPM5128, EPM5130 & EPM5192 AC Operating Conditions *Note (1)*

External Timing Parameters			EPM5064-1 EPM5128-1 EPM5130-1 EPM5192-1		EPM5064-2 EPM5128-2		EPM5064 EPM5128 EPM5130 EPM5192		
Symbol	**Parameter**	**Conditions**	**Min**	**Max**	**Min**	**Max**	**Min**	**Max**	**Unit**
t_{PD1}	Input to non-registered output	C1 = 35 pF		25		30		35	ns
t_{PD2}	I/O input to non-registered output	C1 = 35 pF		40		45		55	ns
t_{SU}	Global clock setup time		15		20		25		ns
t_{H}	Global clock hold time		0		0		0		ns
t_{CO1}	Global clock to output delay	C1 = 35 pF		14		16		20	ns
t_{CH}	Global clock high time		8		10		12.5		ns
t_{CL}	Global clock low time		8		10		12.5		ns
t_{ASU}	Array clock setup time		5		6		10		ns
t_{AH}	Array clock hold time		6		8		10		ns
t_{ACO1}	Array clock to output delay	C1 = 35 pF		25		30		35	ns
t_{ACH}	Array clock high time	*Note (3)*	11		14		16		ns
t_{ACL}	Array clock low time	*Note (3)*	9		11		14		ns
t_{CNT}	Min. global clock period			20		25		30	ns
t_{ODH}	Output data hold time after clock	C1 = 35 pF, *Note (2)*	2		2		2		ns
f_{CNT}	Max. internal global clock frequency	*Note (4)*	50		40		33.3		MHz
t_{ACNT}	Min. array clock period			20		25		30	ns
f_{ACNT}	Max. internal array clock frequency	*Note (4)*	50		40		33.3		MHz
f_{MAX}	Max. clock frequency	*Note (3)*	62.5		50		40		MHz

Internal Timing Parameters *Note (6)*			EPM5064-1 EPM5128-1 EPM5130-1 EPM5192-1		EPM5064-2 EPM5128-2		EPM5064 EPM5128 EPM5130 EPM5192		
Symbol	**Parameter**	**Conditions**	**Min**	**Max**	**Min**	**Max**	**Min**	**Max**	**Unit**
t_{IN}	Input pad and buffer delay			5		7		11	ns
t_{IO}	I/O input pad and buffer delay			6		6		11	ns
t_{SEXP}	Expander array delay			12		14		20	ns
t_{LAD}	Logic array delay			12		14		14	ns
t_{LAC}	Logic control array delay			10		12		13	ns
t_{OD}	Output buffer and pad delay	C1 = 35 pF		5		5		6	ns
t_{ZX}	Output buffer enable delay	C1 = 35 pF		10		11		13	ns
t_{XZ}	Output buffer disable delay	C1 = 5 pF		10		11		13	ns
t_{SU}	Register setup time		6		8		12		ns
t_{LATCH}	Flow-through latch delay			3		4		4	ns
t_{RD}	Register delay			1		2		2	ns
t_{COMB}	Combinatorial delay			3		4		4	ns
t_{H}	Register hold time		4		6		8		ns
t_{IC}	Array clock delay			14		16		16	ns
t_{ICS}	Global clock delay			3		2		1	ns
t_{FD}	Feedback delay			1		1		2	ns
t_{PRE}	Register preset time			5		6		7	ns
t_{CLR}	Register clear time			5		6		7	ns
t_{PIA}	Programmable interconnect array delay			14		16		20	ns

Notes to tables:

(1) Operating conditions: $V_{CC} = 5\ V \pm 5\%$, $T_A = 0°\ C$ to $70°\ C$ for commercial use.
$V_{CC} = 5\ V \pm 10\%$, $T_A = -40°\ C$ to $85°\ C$ for industrial use.

(2) This parameter is a guideline that is sample-tested only. It is based on extensive device characterization. This parameter applies for both global and array clocking.

(3) This parameter is measured with a positive-edge-triggered clock at the register. For negative-edge clocking, the $\mathbf{t_{ACH}}$ and $\mathbf{t_{ACL}}$ parameters must be swapped.

(4) For EPM5032 devices, this parameter is measured with a 32-bit counter programmed into each LAB. For EPM5064, EPM5128, EPM5130, and EPM5192 devices, this parameter is measured with a 16-bit counter programmed into each LAB. I_{CC} is characterized at 0° C.

(5) The $\mathbf{f_{MAX}}$ values represent the highest frequency for pipelined data.

(6) For information on internal timing parameters, refer to *Application Note 78 (Understanding MAX 7000, MAX 5000 & Classic Timing)* in this data book.

Figure 9 shows typical supply current versus frequency for MAX 5000 devices.

Figure 9. I_{CC} vs. Frequency for MAX 5000 Devices (Part 1 of 2)

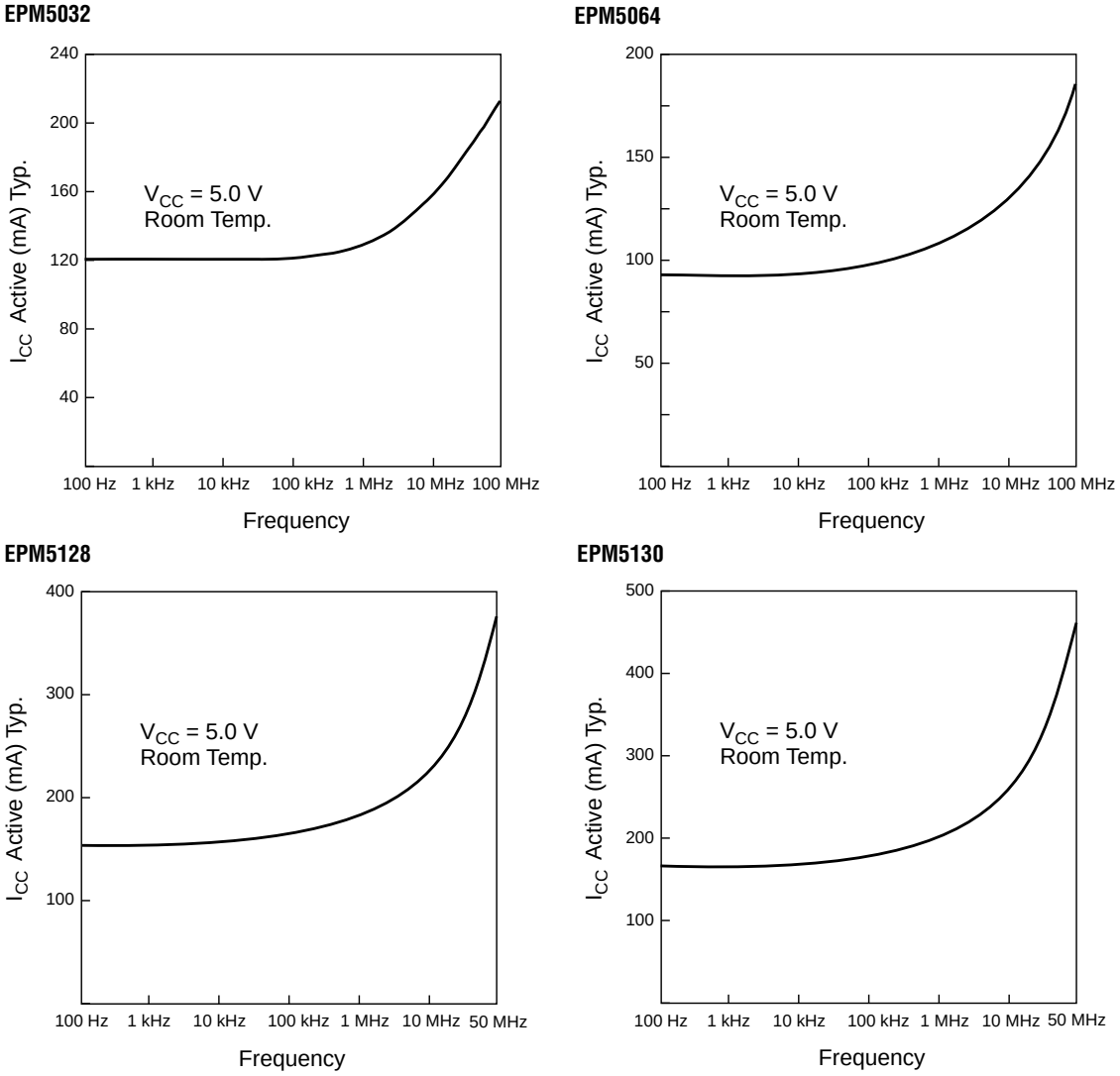
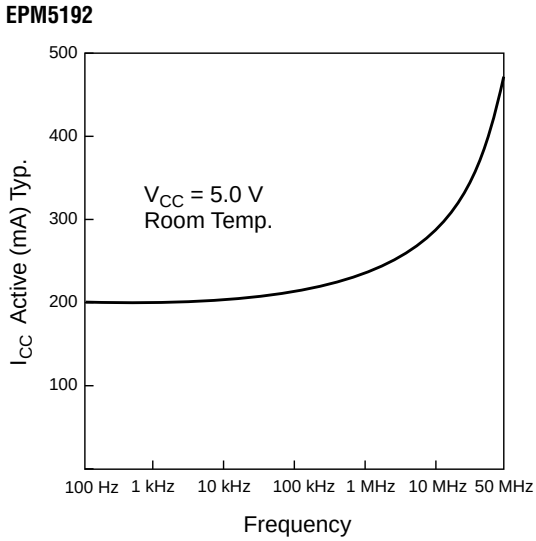


Figure 9. I_{CC} vs. Frequency for MAX 5000 Devices (Part 2 of 2)



Device Pin-Outs

Tables 4 through 13 show the pin names and numbers for the pins in each MAX 5000 device package.

Table 4. EPM5032 Dedicated Pin-Outs

Pin Name	28-Pin J-Lead	28-Pin DIP	28-Pin SOIC
INPUT/CLK	9	2	2
INPUT	6, 7, 8, 20, 21, 22, 23	1, 13, 14, 15, 16, 27, 28	1, 13, 14, 15, 16, 27, 28
GND	15, 28	8, 21	8, 21
VCC	1, 14	7, 22	7, 22

Table 5. EPM5032 I/O Pin-Outs

MC	28-Pin J-Lead	28-Pin DIP	28-Pin SOIC	MC	28-Pin J-Lead	28-Pin DIP	28-Pin SOIC
1	10	3	3	17	24	17	17
2	–	–	–	18	–	–	–
3	11	4	4	19	25	18	18
4	–	–	–	20	–	–	–
5	12	5	5	21	26	19	19
6	–	–	–	22	–	–	–
7	13	6	6	23	27	20	20
8	–	–	–	24	–	–	–
9	16	9	9	25	2	23	23
10	–	–	–	26	–	–	–
11	17	10	10	27	3	24	24
12	–	–	–	28	–	–	–
13	18	11	11	29	4	25	25
14	–	–	–	30	–	–	–
15	19	12	12	31	5	26	26
16	–	–	–	32	–	–	–

Table 6. EPM5064 Dedicated Pin-Outs

Pin Name	44-Pin J-Lead
INPUT/CLK	34
INPUT	9, 11, 12, 13, 31, 33, 35
GND	10, 21, 32, 43
VCC	3, 14, 25, 36

Table 7. EPM5064 I/O Pin-Outs

MC	LAB	44-Pin J-Lead	MC	LAB	44-Pin J-Lead
1	A	2	17	B	15
2	A	4	18	B	16
3	A	5	19	B	17
4	A	6	20	B	18
5	A	7	21	B	19
6	A	8	22	B	20
7	A	–	23	B	22
8	A	–	24	B	23
9	A	–	25	B	–
10	A	–	26	B	–
11	A	–	27	B	–
12	A	–	28	B	–
13	A	–	29	B	–
14	A	–	30	B	–
15	A	–	31	B	–
16	A	–	32	B	–
33	C	24	49	D	37
34	C	26	50	D	38
35	C	27	51	D	39
36	C	28	52	D	40
37	C	29	53	D	41
38	C	30	54	D	42
39	C	–	55	D	44
40	C	–	56	D	1
41	C	–	57	D	–
42	C	–	58	D	–
43	C	–	59	D	–
44	C	–	60	D	–
45	C	–	61	D	–
46	C	–	62	D	–
47	C	–	63	D	–
48	C	–	64	D	–

Table 8. EPM5128 Dedicated Pin-Outs

Pin Name	68-Pin J-Lead	68-Pin PGA
INPUT/CLK	1	B6
INPUT	2, 32, 34, 35, 36, 66, 68	A6, L4, L5, L6, K6, A8, A7
GND	16, 33, 50, 67	B7, E2, G10, K5
VCC	3, 20, 37, 54	B5, E10, G2, K7

Table 9. EPM5128 I/O Pin-Outs (Part 1 of 3)

MC	LAB	68-Pin J-Lead	68-Pin PGA	MC	LAB	68-Pin J-Lead	68-Pin PGA
1	A	4	A5	17	B	12	C2
2	A	5	B4	18	B	13	C1
3	A	6	A4	19	B	14	D2
4	A	7	B3	20	B	15	D1
5	A	8	A3	21	B	17	E1
6	A	9	A2	22	B	–	–
7	A	10	B2	23	B	–	–
8	A	11	B1	24	B	–	–
9	A	–	–	25	B	–	–
10	A	–	–	26	B	–	–
11	A	–	–	27	B	–	–
12	A	–	–	28	B	–	–
13	A	–	–	29	B	–	–
14	A	–	–	30	B	–	–
15	A	–	–	31	B	–	–
16	A	–	–	32	B	–	–

Table 9. EPM5128 I/O Pin-Outs (Part 2 of 3)

MC	LAB	68-Pin J-Lead	68-Pin PGA	MC	LAB	68-Pin J-Lead	68-Pin PGA
33	C	18	F2	49	D	24	J2
34	C	19	F1	50	D	25	J1
35	C	21	G1	51	D	26	K1
36	C	22	H2	52	D	27	K2
37	C	23	H1	53	D	28	L2
38	C	–	–	54	D	29	K3
39	C	–	–	55	D	30	L3
40	C	–	–	56	D	31	K4
41	C	–	–	57	D	–	–
42	C	–	–	58	D	–	–
43	C	–	–	59	D	–	–
44	C	–	–	60	D	–	–
45	C	–	–	61	D	–	–
46	C	–	–	62	D	–	–
47	C	–	–	63	D	–	–
48	C	–	–	64	D	–	–
65	E	38	L7	81	F	46	J10
66	E	39	K8	82	F	47	J11
67	E	40	L8	83	F	48	H10
68	E	41	K9	84	F	49	H11
69	E	42	L9	85	F	51	G11
70	E	43	L10	86	F	–	–
71	E	44	K10	87	F	–	–
72	E	45	K11	88	F	–	–
73	E	–	–	89	F	–	–
74	E	–	–	90	F	–	–
75	E	–	–	91	F	–	–
76	E	–	–	92	F	–	–
77	E	–	–	93	F	–	–
78	E	–	–	94	F	–	–
79	E	–	–	95	F	–	–
80	E	–	–	96	F	–	–

Table 9. EPM5128 I/O Pin-Outs (Part 3 of 3)

MC	LAB	68-Pin J-Lead	68-Pin PGA	MC	LAB	68-Pin J-Lead	68-Pin PGA
97	G	52	F10	113	H	58	C10
98	G	53	F11	114	H	59	C11
99	G	55	E11	115	H	60	B11
100	G	56	D10	116	H	61	B10
101	G	57	D11	117	H	62	A10
102	G	–	–	118	H	63	B9
103	G	–	–	119	H	64	A9
104	G	–	–	120	H	65	B8
105	G	–	–	121	H	–	–
106	G	–	–	122	H	–	–
107	G	–	–	123	H	–	–
108	G	–	–	124	H	–	–
109	G	–	–	125	H	–	–
110	G	–	–	126	H	–	–
111	G	–	–	127	H	–	–
112	G	–	–	128	H	–	–

Table 10. EPM5130 Dedicated Pin-Outs

Pin Name	84-Pin J-Lead	100-Pin PGA	100-Pin PQFP
INPUT/CLK	1	C7	16
INPUT	2, 5, 6, 7, 36, 37, 38, 41, 42, 43, 44, 47, 48, 49, 78, 79, 80, 83, 84	A5, A7, A8, A9, A10, B5, B7, B9, C6, L7, L8, M5, M7, M9, N4, N5, N6, N7, N9	9, 10, 11, 14, 15, 16, 17, 20, 21, 22, 59, 60, 61, 64, 65, 66, 67, 70, 71, 72
GND	19, 20, 39, 40, 61, 62, 81, 82	B8, C8, F2, F3, H11, H12, L6, M6	12, 13, 37, 38, 62, 63, 87, 88
VCC	3, 4, 23, 24, 45, 46, 65, 66	A6, B6, F12, F13, H1, H2, M8, N8	18, 19, 43, 44, 68, 69, 93, 94

Table 11. EPM5130 I/O Pin-Outs (Part 1 of 2)

MC	LAB	84-Pin J-Lead	100-Pin PGA	100-Pin PQFP	MC	LAB	84-Pin J-Lead	100-Pin PGA	100-Pin PQFP
1	A	8	B13	1	17	B	14	A4	23
2	A	9	C12	2	18	B	15	B4	24
3	A	10	A13	3	19	B	16	A3	25
4	A	11	B12	4	20	B	17	A2	26
5	A	12	A12	5	21	B	18	B3	27
6	A	13	B11	6	22	B	21	A1	28
7	A	–	A11	7	23	B	–	B2	29
8	A	–	B10	8	24	B	–	B1	30
9	A	–	–	–	25	B	–	–	–
10	A	–	–	–	26	B	–	–	–
11	A	–	–	–	27	B	–	–	–
12	A	–	–	–	28	B	–	–	–
13	A	–	–	–	29	B	–	–	–
14	A	–	–	–	30	B	–	–	–
15	A	–	–	–	31	B	–	–	–
16	A	–	–	–	32	B	–	–	–
33	C	22	C2	31	49	D	30	G3	41
34	C	25	C1	32	50	D	31	G1	42
35	C	26	D2	33	51	D	32	H3	45
36	C	27	D1	34	52	D	33	J1	46
37	C	28	E2	35	53	D	34	J2	47
38	C	29	E1	36	54	D	35	K1	48
39	C	–	F1	39	55	D	–	K2	49
40	C	–	G2	40	56	D	–	L1	50
41	C	–	–	–	57	D	–	–	–
42	C	–	–	–	58	D	–	–	–
43	C	–	–	–	59	D	–	–	–
44	C	–	–	–	60	D	–	–	–
45	C	–	–	–	61	D	–	–	–
46	C	–	–	–	62	D	–	–	–
47	C	–	–	–	63	D	–	–	–
48	C	–	–	–	64	D	–	–	–

Table 11. EPM5130 I/O Pin-Outs (Part 2 of 2)

MC	LAB	84-Pin J-Lead	100-Pin PGA	100-Pin PQFP	MC	LAB	84-Pin J-Lead	100-Pin PGA	100-Pin PQFP
65	E	50	M1	51	81	F	56	N10	73
66	E	51	L2	52	82	F	57	M10	74
67	E	52	N1	53	83	F	58	N11	75
68	E	53	M2	54	84	F	59	N12	76
69	E	54	N2	55	85	F	60	M11	77
70	E	55	M3	56	86	F	63	N13	78
71	E	–	N3	57	87	F	–	M12	79
72	E	–	M4	58	88	F	–	M13	80
73	E	–	–	–	89	F	–	–	–
74	E	–	–	–	90	F	–	–	–
75	E	–	–	–	91	F	–	–	–
76	E	–	–	–	92	F	–	–	–
77	E	–	–	–	93	F	–	–	–
78	E	–	–	–	94	F	–	–	–
79	E	–	–	–	95	F	–	–	–
80	E	–	–	–	96	F	–	–	–
97	G	64	L12	81	113	H	72	G11	91
98	G	67	L13	82	114	H	73	G13	92
99	G	68	K12	83	115	H	74	F11	95
100	G	69	K13	84	116	H	75	E13	96
101	G	70	J12	85	117	H	76	E12	97
102	G	71	J13	86	118	H	77	D13	98
103	G	–	H13	89	119	H	–	D12	99
104	G	–	G12	90	120	H	–	C13	100
105	G	–	–	–	121	H	–	–	–
106	G	–	–	–	122	H	–	–	–
107	G	–	–	–	123	H	–	–	–
108	G	–	–	–	124	H	–	–	–
109	G	–	–	–	125	H	–	–	–
110	G	–	–	–	126	H	–	–	–
111	G	–	–	–	127	H	–	–	–
112	G	–	–	–	128	H	–	–	–

Table 12. EPM5192 Dedicated Pin-Outs

Pin Name	84-Pin J-Lead	84-Pin PGA
INPUT/CLK	1	A6
INPUT	2, 41, 42, 43, 44, 83, 84	A5, K6, J6, J7, L7, C7, C6
GND	18, 19, 39, 40, 60, 61, 81, 82	A7, B7, E1, E2, G10, G11, K5, L5
VCC	3, 24, 45, 66	B5, E10, G2, K7

Table 13. EPM5192 I/O Pin-Outs (Part 1 of 4)

MC	LAB	84-Pin J-Lead	84-Pin PGA	MC	LAB	84-Pin J-Lead	84-Pin PGA
1	A	4	C5	17	B	12	C2
2	A	5	A4	18	B	13	B1
3	A	6	B4	19	B	14	C1
4	A	7	A3	20	B	15	D2
5	A	8	A2	21	B	–	–
6	A	9	B3	22	B	–	–
7	A	10	A1	23	B	–	–
8	A	11	B2	24	B	–	–
9	A	–	–	25	B	–	–
10	A	–	–	26	B	–	–
11	A	–	–	27	B	–	–
12	A	–	–	28	B	–	–
13	A	–	–	29	B	–	–
14	A	–	–	30	B	–	–
15	A	–	–	31	B	–	–
16	A	–	–	32	B	–	–

Table 13. EPM5192 I/O Pin-Outs (Part 2 of 4)

MC	LAB	84-Pin J-Lead	84-Pin PGA	MC	LAB	84-Pin J-Lead	84-Pin PGA
33	C	16	D1	49	D	22	G3
34	C	17	E3	50	D	23	G1
35	C	20	F2	51	D	25	F1
36	C	21	F3	52	D	26	H1
37	C	–	–	53	D	–	–
38	C	–	–	54	D	–	–
39	C	–	–	55	D	–	–
40	C	–	–	56	D	–	–
41	C	–	–	57	D	–	–
42	C	–	–	58	D	–	–
43	C	–	–	59	D	–	–
44	C	–	–	60	D	–	–
45	C	–	–	61	D	–	–
46	C	–	–	62	D	–	–
47	C	–	–	63	D	–	–
48	C	–	–	64	D	–	–
65	E	27	H2	81	F	31	L1
66	E	28	J1	82	F	32	K2
67	E	29	K1	83	F	33	K3
68	E	30	J2	84	F	34	L2
69	E	–	–	85	F	35	L3
70	E	–	–	86	F	36	K4
71	E	–	–	87	F	37	L4
72	E	–	–	88	F	38	J5
73	E	–	–	89	F	–	–
74	E	–	–	90	F	–	–
75	E	–	–	91	F	–	–
76	E	–	–	92	F	–	–
77	E	–	–	93	F	–	–
78	E	–	–	94	F	–	–
79	E	–	–	95	F	–	–
80	E	–	–	96	F	–	–

Table 13. EPM5192 I/O Pin-Outs (Part 3 of 4)

MC	LAB	84-Pin J-Lead	84-Pin PGA	MC	LAB	84-Pin J-Lead	84-Pin PGA
97	G	46	L6	113	H	54	J10
98	G	47	L8	114	H	55	K11
99	G	48	K8	115	H	56	J11
100	G	49	L9	116	H	57	H10
101	G	50	L10	117	H	–	–
102	G	51	K9	118	H	–	–
103	G	52	L11	119	H	–	–
104	G	53	K10	120	H	–	–
105	G	–	–	121	H	–	–
106	G	–	–	122	H	–	–
107	G	–	–	123	H	–	–
108	G	–	–	124	H	–	–
109	G	–	–	125	H	–	–
110	G	–	–	126	H	–	–
111	G	–	–	127	H	–	–
112	G	–	–	128	H	–	–
129	I	58	H11	145	J	64	F11
130	I	59	F10	146	J	65	E11
131	I	62	G9	147	J	67	E9
132	I	63	F9	148	J	68	D11
133	I	–	–	149	J	–	–
134	I	–	–	150	J	–	–
135	I	–	–	151	J	–	–
136	I	–	–	152	J	–	–
137	I	–	–	153	J	–	–
138	I	–	–	154	J	–	–
139	I	–	–	155	J	–	–
140	I	–	–	156	J	–	–
141	I	–	–	157	J	–	–
142	I	–	–	158	J	–	–
143	I	–	–	159	J	–	–
144	I	–	–	160	J	–	–

Table 13. EPM5192 I/O Pin-Outs (Part 4 of 4)

MC	LAB	84-Pin J-Lead	84-Pin PGA	MC	LAB	84-Pin J-Lead	84-Pin PGA
161	K	69	D10	177	L	73	A11
162	K	70	C11	178	L	74	B10
163	K	71	B11	179	L	75	B9
164	K	72	C10	180	L	76	A10
165	K	–	–	181	L	77	A9
166	K	–	–	182	L	78	B8
167	K	–	–	183	L	79	A8
168	K	–	–	184	L	80	B6
169	K	–	–	185	L	–	–
170	K	–	–	186	L	–	–
171	K	–	–	187	L	–	–
172	K	–	–	188	L	–	–
173	K	–	–	189	L	–	–
174	K	–	–	190	L	–	–
175	K	–	–	191	L	–	–
176	K	–	–	192	L	–	–

Pin-Out Diagrams

Figures 10 through 14 show the package pin-out diagrams of MAX 5000 devices.

Figure 10. EPM5032 Package Pin-Out Diagrams

Package outlines not drawn to scale. Windows in ceramic packages only.

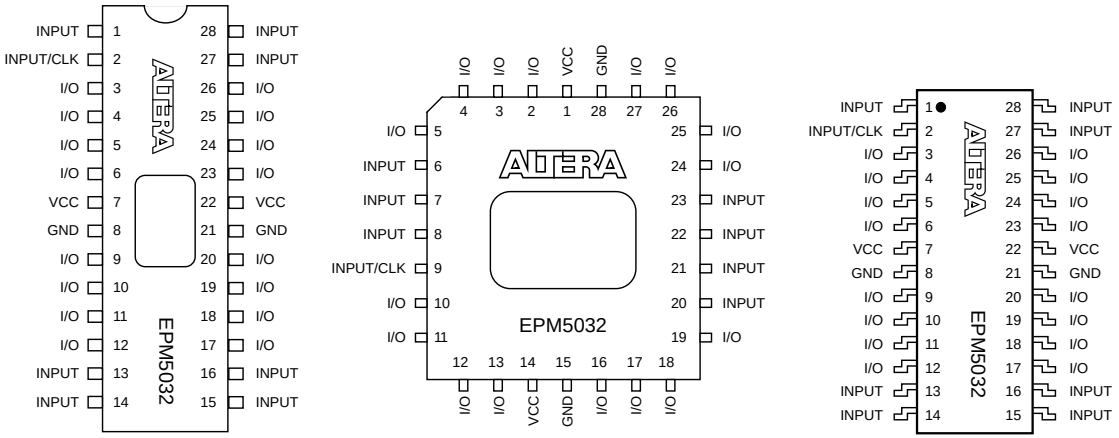


Figure 11. EPM5064 Package Pin-Out Diagrams

Package outline not drawn to scale. Windows in ceramic packages only.

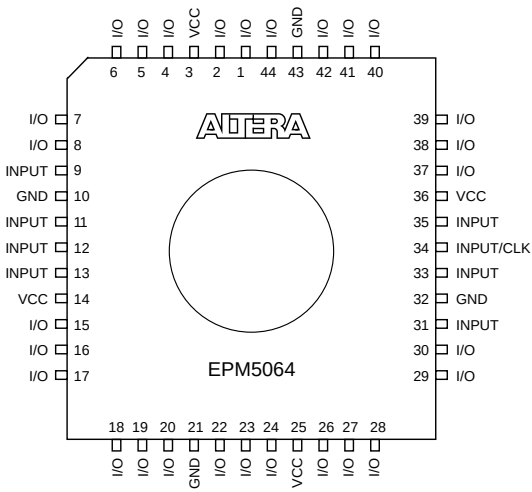
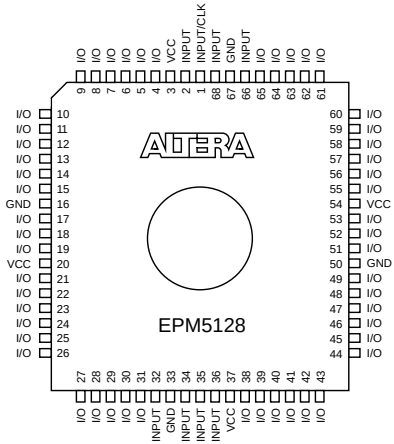
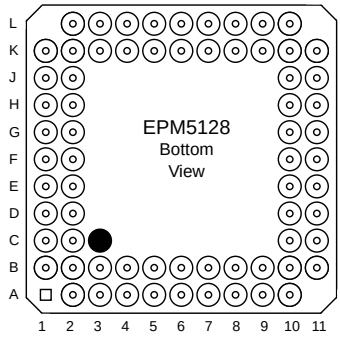


Figure 12. EPM5128 Package Pin-Out Diagrams

Package outlines not drawn to scale. Windows in ceramic packages only.



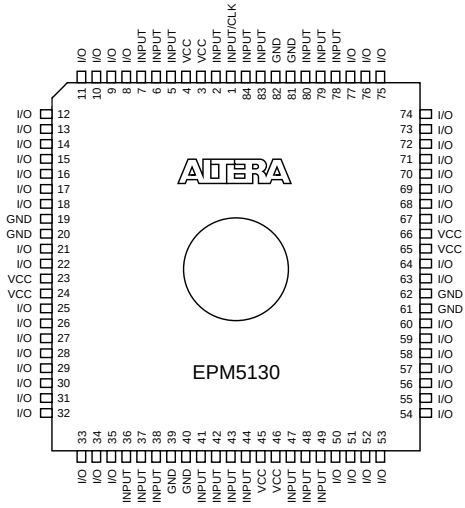
68-Pin J-Lead



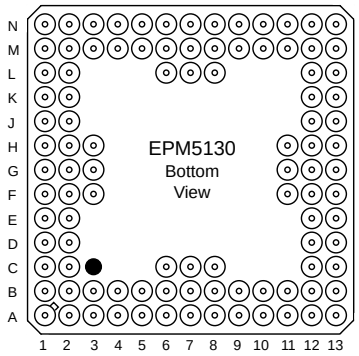
68-Pin PGA

Figure 13. EPM5130 Package Pin-Out Diagrams

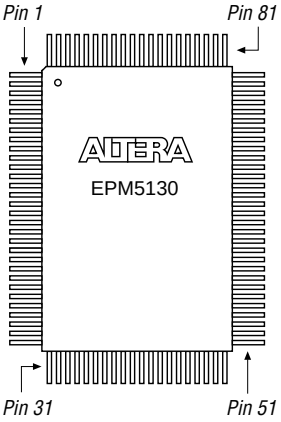
Package outlines not drawn to scale. Windows in ceramic packages only.



84-Pin J-Lead



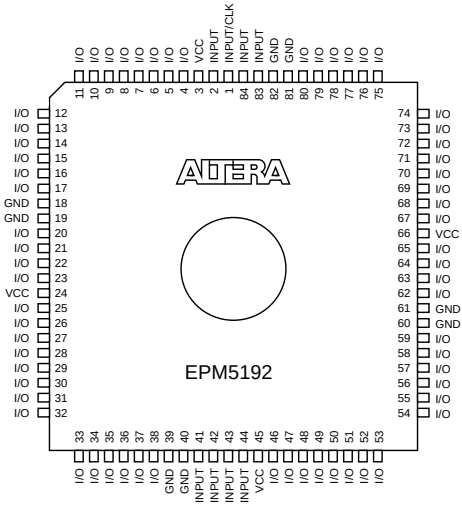
100-Pin PGA



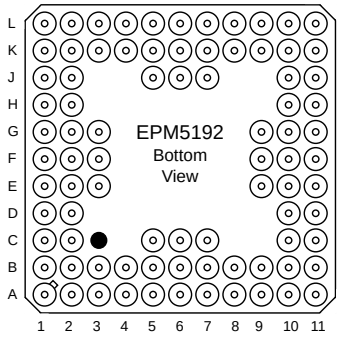
100-Pin PQFP

Figure 14. EPM5192 Package Pin-Out Diagrams

Package outlines not drawn to scale. Windows in ceramic packages only.



84-Pin J-Lead



84-Pin PGA

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