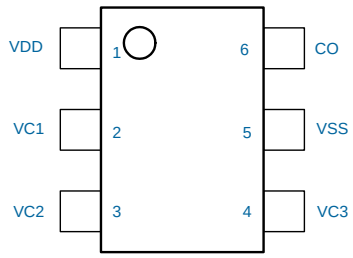
Battery Protection IC for 2-Serial/3-Serial-Cell Pack (Second Protection)

General Description

The uP8207 series is used for secondary protection of lithium-ion rechargeable batteries, and incorporates a high-accuracy voltage detection circuit and a delay circuit. Short circuits between cells accommodate series connection of two to three cells.

Pin Configuration

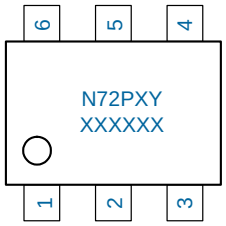


TSOT23-6L

Applications

- Lithium-Ion Rechargeable Battery Packs (for Secondary Protection)
- Notebook Computers
- Portable Instrumentation
- Portable Equipment

Marking Information



Line1 : Product Code
Line2 : Date Code Number

Features

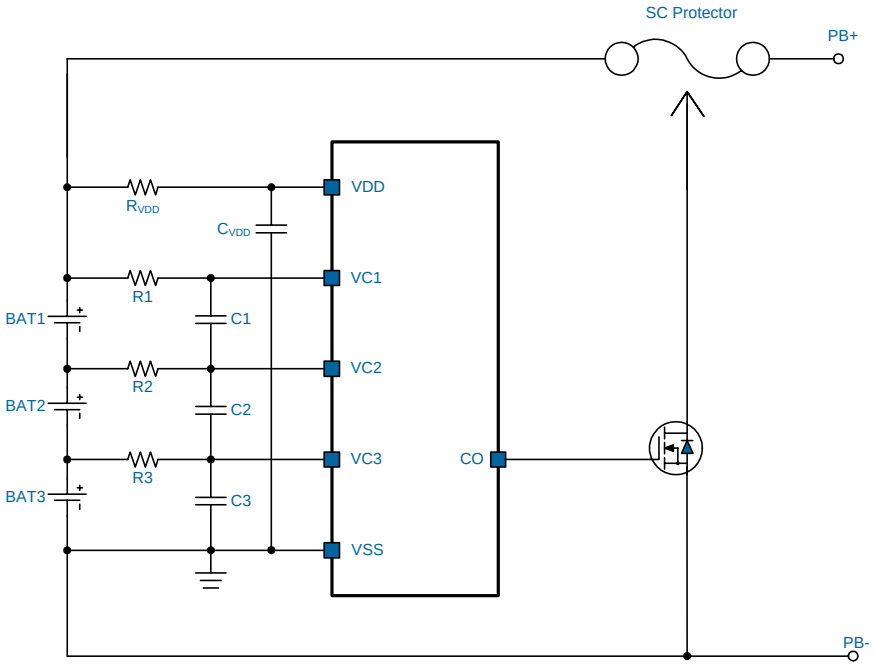
- High Accuracy Voltage Detection Circuit for Each Cell
  - Overcharge Detection Voltage n (n = 1 to 3)
    4.20V to 4.70V (in 50mV steps)
    Accuracy: 20mV (+25°C)
    Accuracy: 30mV (0°C to +60°C)
  - Overcharge Hysteresis Voltage n (n = 1 to 3)
    -0.30V±50mV
- Delay Time for Overcharge Detection Can Be Set by An Internal Circuit (No External Capacitors Required)
- High Withstand Voltage Devices:
  Absolute Maximum Rating 26V
- Wide Operating Voltage Range: 3.6V to 24V
- Wide Operating Temperature Range: -40°C to +85°C
- Low Current Consumption
  At 3.8V for Each Cell: 2.0uA max. (+25°C)
  At 2.0V for Each Cell: 0.3uA max. (+25°C)
- CO Pull Up Voltage : 4.7V
- Available in TSOT23-6L Package
- RoHS Compliant and Halogen Free

Ordering Information

Order Number	Package	Top Marking
uP8207PMT6-XY	TSOT23-6L	**N72PXY** **X: Overcharge Detection Voltage, V_{CU}** C = 4.20V; D = 4.25V; E = 4.30V; F = 4.35V; G = 4.40V; H = 4.45V; I = 4.50V; J = 4.55V; K = 4.60V; L= 4.65V; M = 4.70V. **Y: Overcharge Detection Delay Time, t_{CU}** A = 2s, B = 4s, C = 6s, D = 8s

Note:
(1) Please check the sample/production availability with uPI representatives.
(2) uPI products are compatible with the current IPC/JEDEC J-STD-020 requirement. They are halogen-free, RoHS compliant and 100% matte tin (Sn) plating that are suitable for use in SnPb or Pb-free soldering processes.

Typical Application Circuit



Cautions:

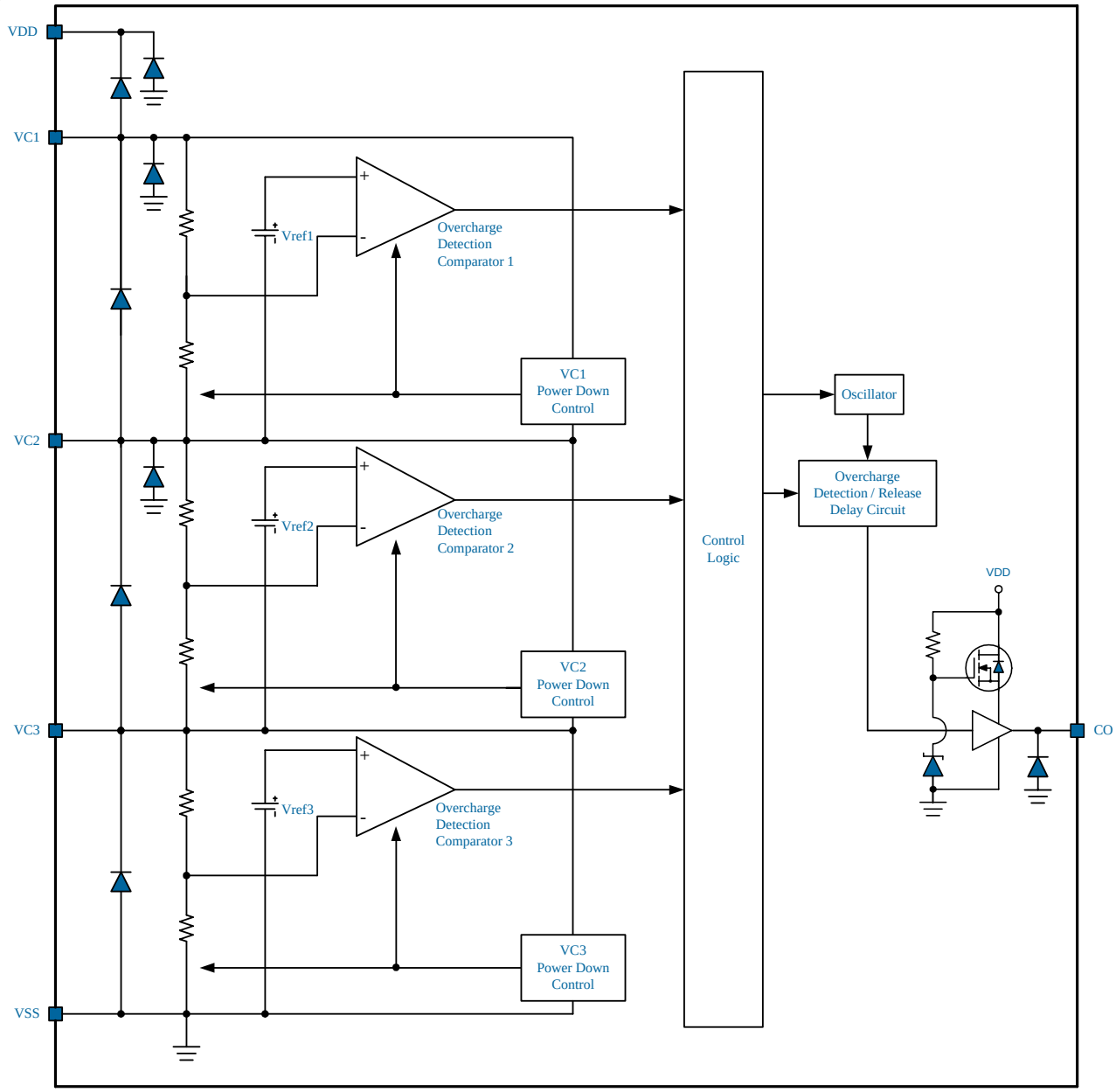
1. The above connection example does not guarantee operation. Perform thorough evaluation using the actual application.

2. Cell Connection: To prevent incorrect output activation, the VSS pin must be connected first. Follow the connecting sequence below:

Configuration of 3 serial cell: BAT3 -> BAT2 -> BAT1

Configuration of 2 serial cell: BAT2 -> BAT1

Functional Block Diagram



Functional Pin Description

Pin NO.	Name	Pin Function
1	VDD	Positive Power Input Pin
2	VC1	Positive Power Connection Pin of Battery 1.
3	VC2	Negative Voltage Connection Pin of Battery 1. Positive Voltage Connection Pin of Battery 2.
4	VC3	Negative Voltage Connection Pin of Battery 2. Positive Voltage Connection Pin of Battery 3.
5	VSS	Negative Power Input Pin. Negative Voltage Connection Pin of Battery 3.
6	CO	FET Gate Connection Pin for Charge.

Functional Description

Normal Mode

When the voltage of all cells is lower than "Overcharge Detection Voltage (V_{CUn}) + Overcharge Hysteresis (V_{HCn})", the output of CO pin turns to L (Active "H"). This is called normal mode.

Overcharge Protection Mode

When the voltage of any cell exceeds V_{CUn} during charging and lasts for equal to or longer than Overcharge Detection Delay Time (t_{CU}), CO pin turns to "H". This is called overcharge protection mode. CO pin drives the connecting FET to provide charge control and a secondary protection. Once the voltage of all cells is lower than "V_{CUn}+V_{HCn}" and lasts for equal to or longer than 1.95ms, uP8207 enters normal mode.

Test Mode

To shorten Overchage Detection Delay Time (t_{CU}), uP8207 is able to enter the test mode. The test mode can be triggered by forcing a voltage equal to or higher than 8.5V between VDD pin and VC1 for 40ms or longer. The test mode is held by internal latch even if the voltage of VDD pin drops to the same as the voltage of VC1. After overcharge event occurs, uP8207 resets the latch for retaining the test mode.

Cautions:

- During normal mode,t_{CU} = 2s (typ.);
  In product, t_{CU} = 31.25ms (typ.)
  During normal mode, t_{CU} = 4s (typ.);
  In product, t_{CU} = 62.5ms (typ.)
  During normal mode,t_{CU} = 6s (typ.);
  In product, t_{CU} = 93.75ms (typ.)
  During normal mode,t_{CU} = 8s (typ.);
  In product, t_{CU} = 125ms (typ.)
- Set the test mode when no batteries are overcharged.
- The overcharge release delay time (t_{CL}) is not shortened in the test mode.
- The overcharge timer resets delay time (t_{TR}) is not shortened in the test mode.

Overcharge Timer Reset

When an overcharge release noise that forces the voltage of the battery temporarily below the overcharge detection voltage (V_{CU}) is input during the overcharge detection delay time (t_{CU}) counting period. The overcharge detection delay time will be continuously counted if the period of overcharge release noise is shorter than the overcharge timer reset delay time (t_{TR}). Otherwise, counting of t_{CU} will be reset if the period of overcharge release noise is equal to t_{TR} or longer. After that, when V_{CU} has been exceeded, counting t_{CU} resumes.

Battery Protection IC Connection Examples:

(1) 3-serial cell

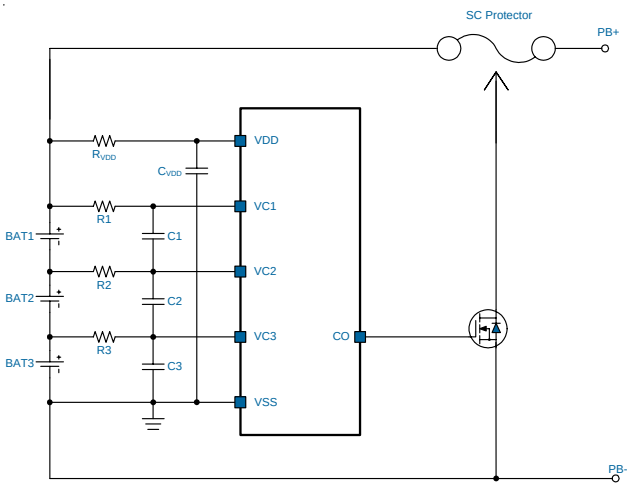


Table 1. Constants for 3-serial cell External Components

No.	Part	Min.	Typ.	Max.	Unit
1	R1 to R3	0.1	1	10	kΩ
2	C1 to C3, C_{VDD}	0.01	0.1	1	uF
3	R_{VDD}	50	100	1000	Ω

Cautions:

1. The above constants are subject to change without prior notice.
2. It has not been confirmed whether the operation is normal or not in circuits other than the above example of connection. In addition, the example of connection shown above and the constant will not guarantee successful operation. Perform thorough evaluation using the actual application to set the constant.
3. Set the same constants to R1 to R3 and to C1 to C3 and C_{VDD}.
4. Set R_{VDD}, C1 to C3, and C_{VDD} so that the condition (R_{VDD}) x (C1 to C3, C_{VDD}) $\geq 5x10^{-6}$ is satisfied.
5. Set R1 to R3, C1 to C3, and C_{VDD} so that the condition (R1 to R3) . (C1 to C3, C_{VDD}) $\geq 1x10^{-4}$is satisfied.
6. Cell connections: To prevent incorrect output activation, the VSS pin must be connected first. Connect sequences must be used as following:

   3-series cell configuration

   BAT3 → BAT2 → BAT1

(2) 2-serial cell

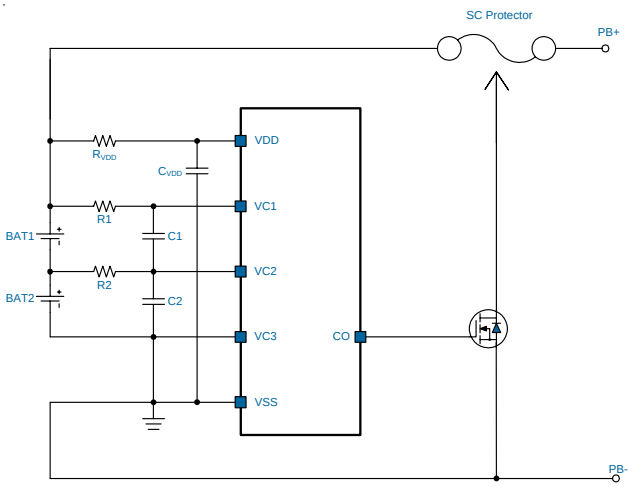


Table 2. Constants for 2-serial cell External Components

No.	Part	Min.	Typ.	Max.	Unit
1	R1 to R2	0.1	1	10	kΩ
2	C1 to C2, C_{VDD}	0.01	0.1	1	uF
3	R_{VDD}	50	100	1000	Ω

Cautions:

1. The above constants are subject to change without prior notice.

2. It has not been confirmed whether the operation is normal or not in circuits other than the above example of connection. In addition, the example of connection shown above and the constant will not guarantee successful operation. Perform thorough evaluation using the actual application to set the constant.

3. Set the same constants to R1 to R2 and to C1 to C2 and C_{VDD}.

4. Set R_{VDD}, C1 to C2, and C_{VDD} so that the condition (R_{VDD}) x (C1 to C2, C_{VDD}) ≥ $5x10^{-6}$ is satisfied.

5. Set R1 to R2, C1 to C2, and C_{VDD} so that the condition (R1 to R2) . (C1 to C2, C_{VDD}) ≥ $1x10^{-4}$is satisfied.

6. Cell connections: To prevent incorrect output activation, the VSS pin must be connected first. Connect sequences must be used as following:

2-series cell configuration

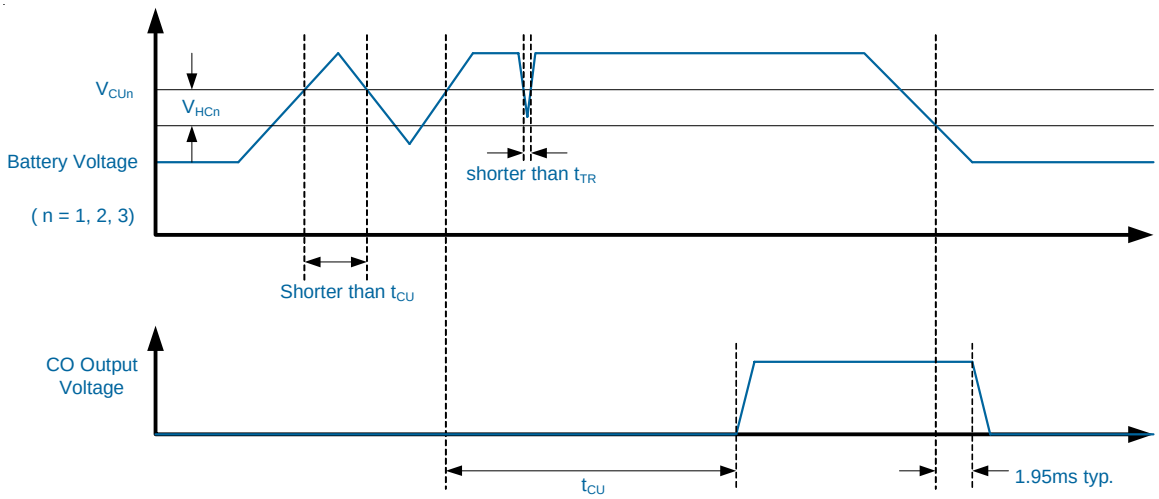
BAT2 → BAT1

Precautions

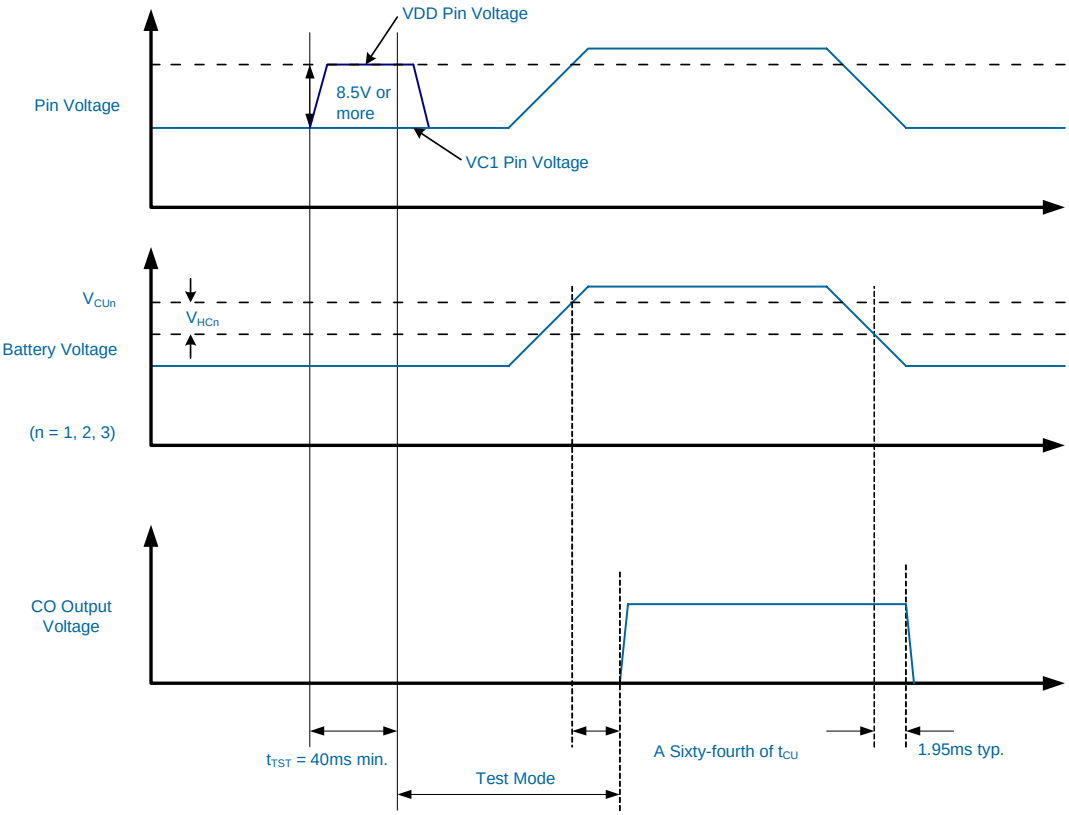
- Do not connect batteries charged with V_{CU} + V_{HC} or more. If the connected batteries include a battery charged with V_{CU} + V_{HC} or more, *H* may be output at CO after all pins are connected.
- In some application circuits, even if an overcharged battery is not included, the order of connecting batteries may be restricted to prevent transient output of CO detection pulses when the batteries are connected. Perform thorough evaluation with the actual application circuit.
- Before the battery connection, short-circuit the battery side pins R_{VDD} and R1, shown in the figure in *Battery Protection IC Connection Examples*.
- The application conditions for the input voltage, output voltage, and load current should not exceed the package power dissipation.
- Do not apply to this IC an electrostatic discharge that exceeds the performance ratings of the built-in electrostatic protection circuit.
- Connect VDD capacitor to either VC1 or VSS.
- uPI claims no responsibility for any disputes arising out of or in connection with any infringement of patents owned by a third party by products including this IC.

Timing Chart

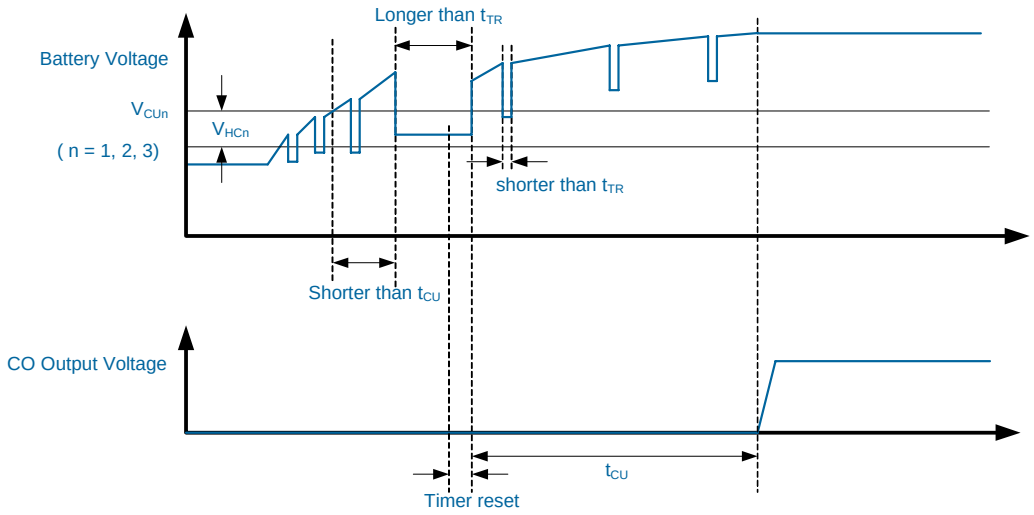
Overcharge Protection



Test Mode



Overcharge Timer Reset



Absolute Maximum Rating

(Note 1)

Supply Voltage Range between VDD and VSS ---------- VSS-0.3V to VSS+26V
Supply Input Voltage Range, VC1,VC2,VC3 ---------- VSS-0.3V to VDD+0.3V
Supply Input Voltage Range, VC1 to VC2, VC2 to VC3,VC3 to VSS ---------- -0.3V to +8V
CO Output Pin Voltage Range, CO---------- -0.3V to V_{OH1}+0.3V
Storage Temperature Range ---------- -45°C to +125°C
Junction Temperature ---------- 125°C
Lead Temperature (Soldering, 10 sec) ---------- 260°C
ESD Rating (Note 2)
HBM (Human Body Mode) ---------- 2kV
CDM (Charged Device Mode) ---------- 1kV

Thermal Information

Package Thermal Resistance (Note 3)
TSOT23 - 6L θ_{JA} ---------- 250°C/W
TSOT23 - 6L θ_{JC} ---------- 100°C/W
Power Dissipation, P_D @ T_A = 25°C
TSOT23 - 6L P_D ---------- 0.40W

Recommended Operation Conditions

(Note 4)

Operating Junction Temperature Range ---------- -40°C to +100°C
Operating Ambient Temperature Range ---------- -40°C to +85°C
Supply Voltage, VDD, VSS ---------- +3.6V to +24V
Supply Input Voltage, VC1,VC2,VC3 ---------- 0V to +25V
Input Voltage, VC3-VC2, VC2-VC1, VC1-VSS ---------- 0V to +5V

Note 1. Stresses listed as the above *Absolute Maximum Ratings* may cause permanent damage to the device. These are for stress ratings. Functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may remain possibility to affect device reliability.

Note 2. Devices are ESD sensitive. Handling precaution recommended.

Note 3. θ_{JA} is measured in the natural convection at T_A = 25°C on a low effective thermal conductivity test board of JEDEC 51-3 thermal measurement standard.

Note 4. The device is not guaranteed to function outside its operating conditions.

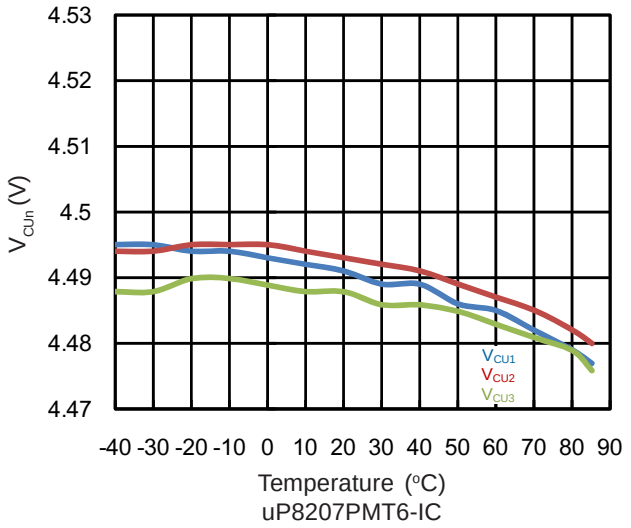
Electrical Characteristics

(T_A=25°C, unless otherwise specified)

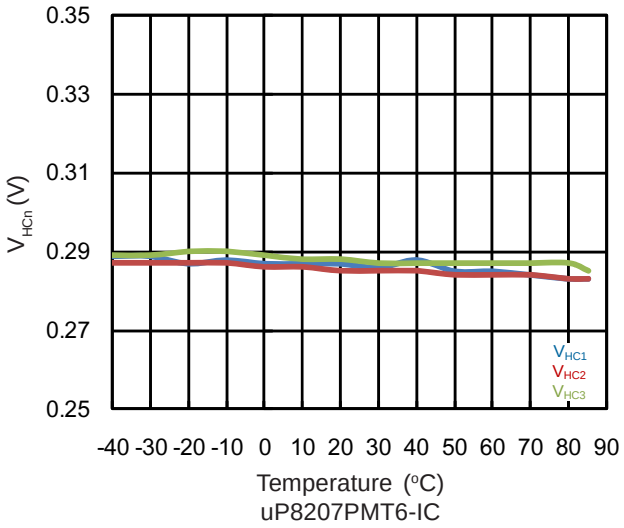
Parameter	Symbol	Test Conditions	Min	Typ	Max	Units	Test Circuit
Detection Voltage							
Overcharge Detection Voltage n (n = 1, 2, 3)	V_{CUn}	--	V_{CUn}-0.020	V_{CUn}	V_{CUn}+0.020	V	1
		T_A = 0°C to +60°C (*1)	V_{CUn}-0.030	V_{CUn}	V_{CUn}+0.030		
Overcharge Hysteresis (n = 1, 2, 3)	V_{HCn}	V_{HC} = -0.30V	V_{HCn}-0.050	V_{HCn}	V_{HCn}+0.050	V	1
Shutdown Detector Voltage Threshold	V_{SD}	Detect falling edge	3.1	3.5	3.9	V	1
Input Voltage							
Supply Voltage between VDD and VSS	V_{DSOP}	--	3.6	--	24	V	--
Input Current							
Current Consumption During Operation	I_{OPE}	V1=V2=V3=3.8V	--	--	2.0	uA	3
Current Consumption During Overdischarge	I_{PDN}	V1=V2=V3 =2.0V	--	--	0.3	uA	3
VC1 Pin Current	I_{VC1}	V1=V2=V3=3.8V	--	--	1.2	uA	4
VC2 Pin Current	I_{VC2}	V1=V2=V3=3.8V	-0.3	0	0.3	uA	4
VC3 Pin Current	I_{VC3}	V1=V2=V3=3.8V	-0.3	0	0.3	uA	4
CO Output Voltage							
CO Pch ON Voltage1	V_{OH1}	I_{OH} = 0uA, V_{CELLn} = 4.7V (n = 1,2,3)	4.0	4.7	5.4	V	5
CO Pch ON Voltage2	V_{OH2}	I_{OH} = -50uA, V_{CELLn} = 4.7V (n = 1,2,3)	V_{OH1}-0.5	V_{OH1}-0.1	--	V	5
CO Nch ON Voltage	V_{OL}	I_{OL} = 50uA, V_{CELLn} = 3.9V (n = 1,2,3)	--	0.1	0.5	V	6
Delay Time							
Overcharge Detection Delay Time	t_{CU}	--	t_{CU}x0.8	t_{CU}	t_{CU}x1.2	s	1
Transition Time to Test Mode	t_{TST}	V1=V2=V3=3.5V, VDD ≥ V1+8.5V	--	--	40	ms	2
Overcharge Timer Reset Delay Time	t_{TR}	--	1.56	1.95	2.35	ms	1
Overcharge Release Delay Time	t_{CL}	--	1.56	1.95	2.35	ms	1

Typical Operation Characteristics

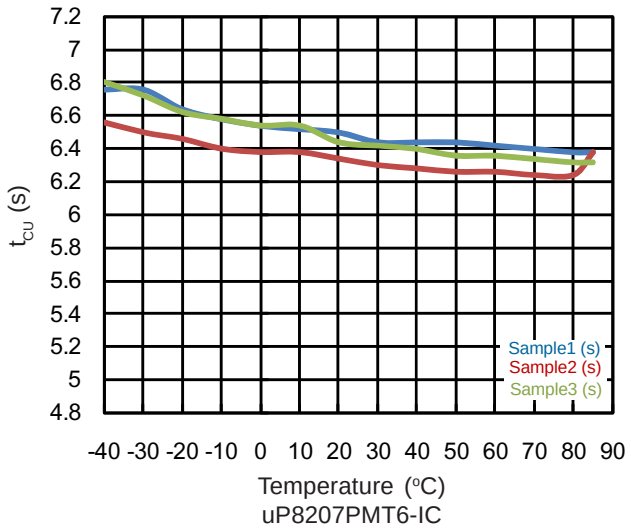
Overcharge Detection Voltage



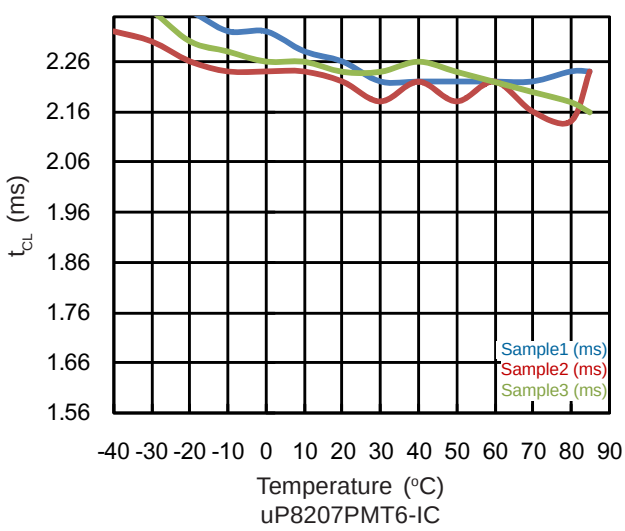
Overcharge Hysteresis



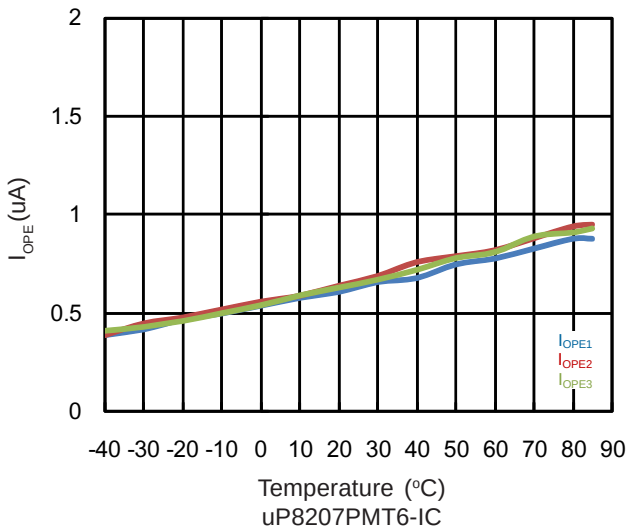
Overcharge Detection Delay Time



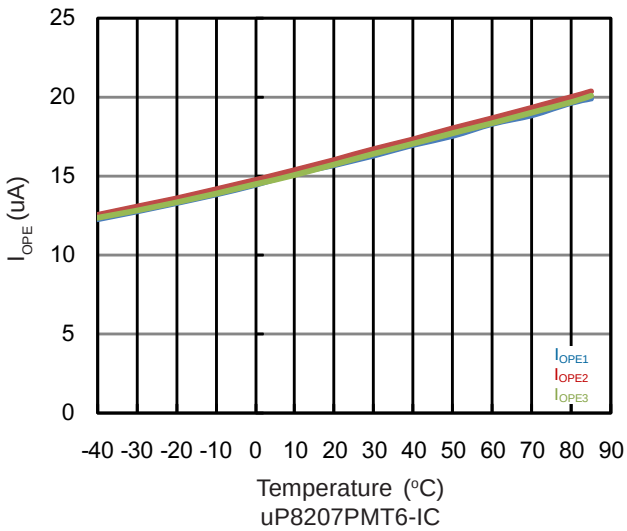
Overcharge Release Delay Time



Current Consumption during Operation

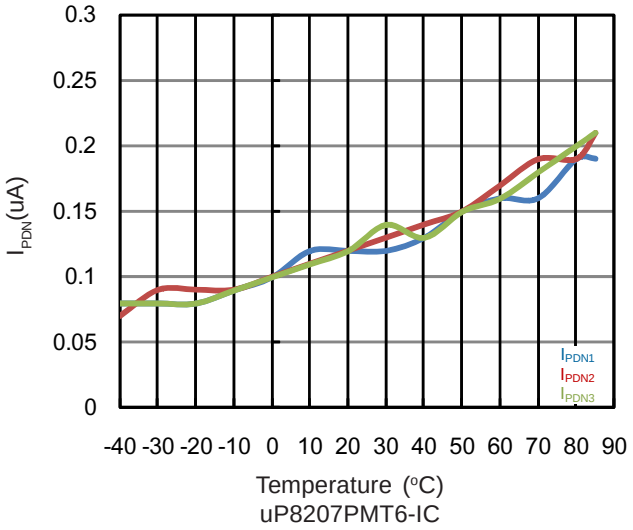


Current Consumption during Overcharge

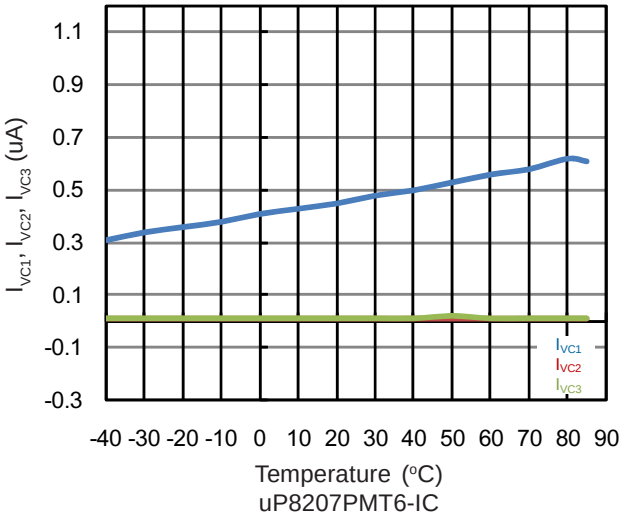


Typical Operation Characteristics

Current Consumption during Overdischarge



VCn Pin Current



Test Circuit

1. Overcharge Detection Voltage, Overcharge Hysteresis Voltage

(Test circuit 1)

1.1 Overcharge detection voltage n (V_{CUn})
Set V1 = V2 = V3 = V_{CU} - 0.05 V. The Overcharge detection voltage 1 (V_{CU1}) is the V1 voltage when the CO pin's output changes after the voltage of V1 has been gradually increased. Overcharge detection voltage V_{CUn} (n = 2, 3) can be determined in the same way as when n = 1.

1.2 Overcharge hysteresis voltage n (V_{HCn})

Set V1 = V_{CU} + 0.05 V, V2 = V3 = 2.5 V. The overcharge hysteresis voltage 1 (V_{HC1}) is the difference between V1 voltage and V_{CU1} when the CO pin's output changes after the V1 voltage has been gradually decreased. Overcharge hysteresis voltage V_{HCn} (n = 2, 3) can be determined in the same way as when n = 1.

2. CO Output Voltage

(Test circuit 5, and Test circuit 6)

2.1 CO Pch ON Voltage (V_{OH1} and V_{OH2})
As Test circuit 5, setting V1=V2=V3=4.7V. Sourcing I_{OH} from CO pin and measuring its output voltage. V_{OH1} denotes 0A been sourced. V_{OH2} denotes 50uA been sourced.
2.2 CO Nch ON Voltage (V_{OL})
As Test circuit 6, setting V1=V2=V3=3.8V. Sinking 50uA into CO pin and measuring its output voltage, V_{OL}.

3. Overcharge Detection Delay Time (t_{CU})

(Test circuit 1)

Increase V1 up to 5.0V after setting V1=V2=V3=3.5V. The overcharge detection delay time (t_{CU}) is the time period until the CO pin output changes.

4. Transition Time to Test Mode (t_{TST})

(Test circuit 2)

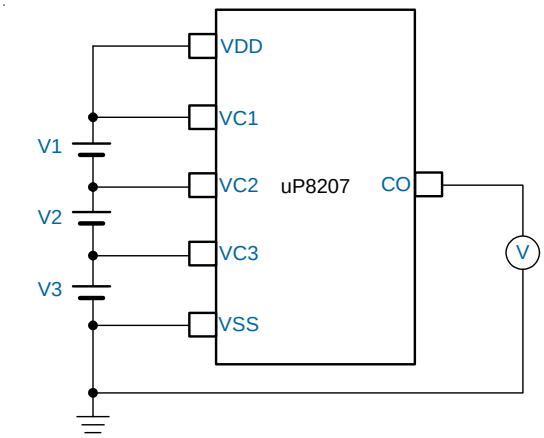
Setting V1, V2, V3, to 3.5V and V6 to 0 V, then V6 is increased to 8.5V and then halted for a quick pause and decreased back to 0V again. The transition time t_{TST} (40ms max) is defined as the duration between the rise and fall of V6. When the duration between the rise and fall of V6 is shorter than t_{TST}, it will result in overcharge detection protection after going through t_{CU}; however, when the overcharge detection time is made longer than t_{TST}, overcharge detection protection will occur within duration much shorter than t_{CU}. For detailed inllustration, please refer to the Timing Chart of Test Mode on page 7.

5. Overcharge Timer Reset Delay Time (t_{TR})

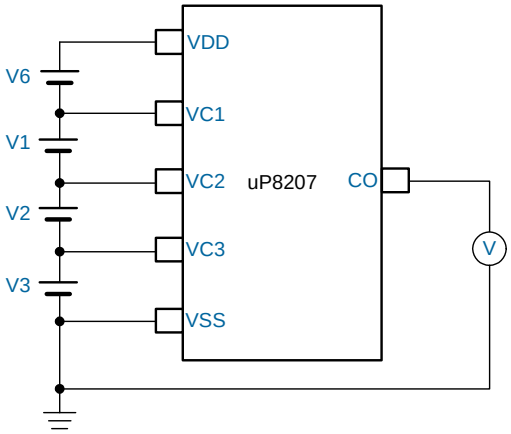
(Test circuit 1)

Set V1, V2, and V3 to 3.5V. V1 is driven up to 5.0V and this is defined as the first rise. Then V1 is lowered down to 3.5V again, and instantly resumed to 5.0V. This rise is defined as the second rise. The overcharge timer reset delay time (t_{TR}) is a duration from V1 fall to the second rise. When the duration between the V1 fall and the second rise is shorter than t_{TR}, CO turns to H after the t_{CU} following the first rise; when the duration between the V1 fall and the second rise is longer than certain period of time, CO turns to H after the duration of t_{CU} following the second rise. For detailed inllustration, please refer to the Timing Chart of Overcharger Timer Reset on page 8.

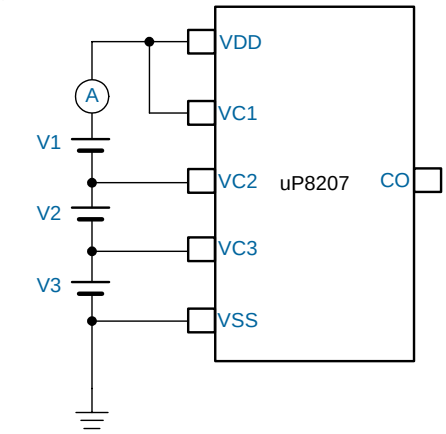
Test Circuit



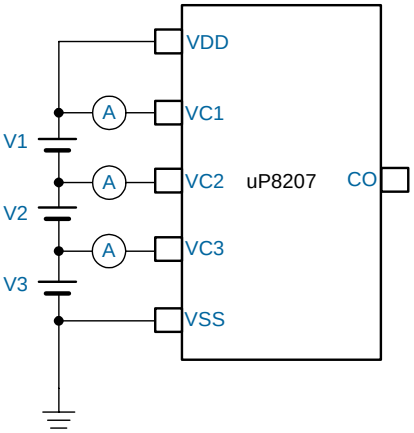
Test Circuit 1



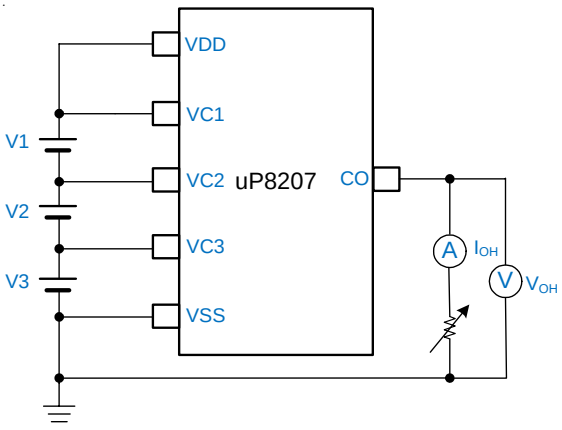
Test Circuit 2



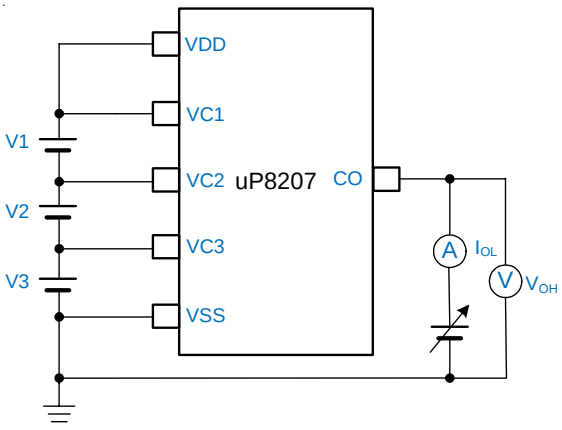
Test Circuit 3



Test Circuit 4

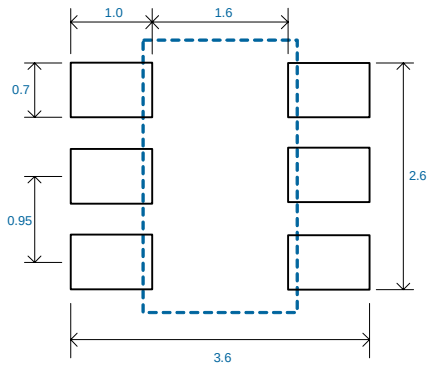


Test Circuit 5



Test Circuit 6

Recommended Footprint:

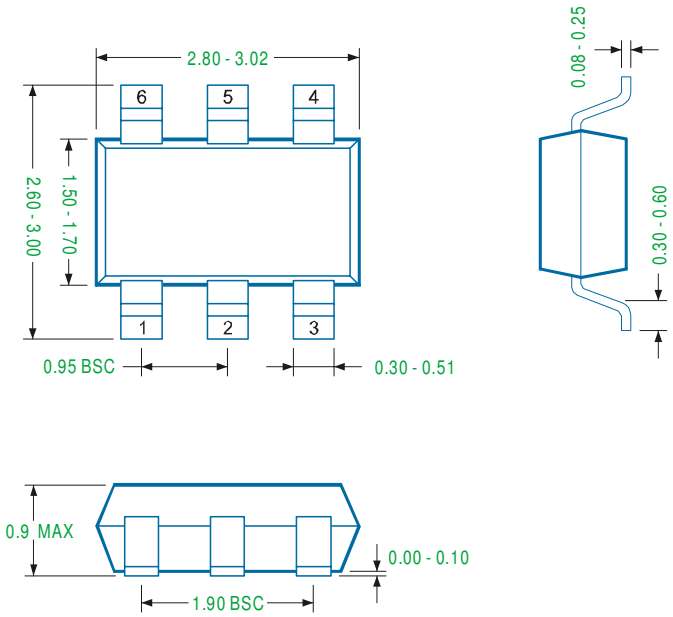


Package Type: TSOT23-6L
Tolerance: ±0.10
Unit: mm

CAUTION: The above information is for reference only. It may be adjusted based on the manufacturing parameters provided by PCB and assembly venders.

Package Information

TSOT23 - 6L



Note

1. Package Outline Unit Description:
   BSC: Basic. Represents theoretical exact dimension or dimension target
   MIN: Minimum dimension specified.
   MAX: Maximum dimension specified.
   REF: Reference. Represents dimension for reference use only. This value is not a device specification.
   TYP. Typical. Provided as a general value. This value is not a device specification.
2. Dimensions in Millimeters.
3. Drawing not to scale.
4. These dimensions do not include mold flash or protrusions. Mold flash or protrusions shall not exceed 0.15mm.

Important Notice

uPI and its subsidiaries reserve the right to make corrections, modifications, enhancements, improvements, and other changes to its products and services at any time and to discontinue any product or service without notice. Customers should obtain the latest relevant information before placing orders and should verify that such information is current and complete.

uPI products are sold subject to the taerms and conditions of sale supplied at the time of order acknowledgment. However, no responsibility is assumed by uPI or its subsidiaries for its use or application of any product or circuit; nor for any infringements of patents or other rights of third parties which may result from its use or application, including but not limited to any consequential or incidental damages. No uPI components are designed, intended or authorized for use in military, aerospace, automotive applications nor in systems for surgical implantation or life-sustaining. No license is granted by implication or otherwise under any patent or patent rights of uPI or its subsidiaries.

uPI Semiconductor Corp.
Headquarter
9F.,No.5, Taiyuan 1st St. Zhubei City,
Hsinchu Taiwan, R.O.C.
TEL : 886.3.560.1666 FAX : 886.3.560.1888

Sales Branch Office
12F-5, No. 408, Ruiguang Rd. Neihu District,
Taipei Taiwan, R.O.C.
TEL : 886.2.8751.2062 FAX : 886.2.8751.5064