LPC1102

32-bit ARM Cortex-M0 microcontroller; 32 kB flash and 8 kB SRAM

Rev. 00.04 — 23 June 2010 **Objective data sheet**

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1. General description

The LPC1102 is an ARM Cortex-M0 based, low-cost 32-bit MCU, designed for 8/16-bit microcontroller applications, offering performance, low power, simple instruction set and memory addressing together with reduced code size compared to existing 8/16-bit architectures.

The LPC1102 operates at CPU frequencies of up to 50 MHz.

The peripheral complement of the LPC1102 includes 32 kB of flash memory, 8 kB of data memory, one RS-485/EIA-485 UART, one SPI interface with SSP features, four general purpose counter/timers, a 10-bit ADC, and 11 general purpose I/O pins.

2. Features and benefits

- System:
  - ARM Cortex-M0 processor, running at frequencies of up to 50 MHz.
  - ARM Cortex-M0 built-in Nested Vectored Interrupt Controller (NVIC).
  - Serial Wire Debug.
  - System tick timer.
- Memory:
  - 32 kB on-chip flash programming memory.
  - 8 kB SRAM.
  - In-Application Programming (IAP) and In-System Programming (ISP) support via on-chip bootloader software.
- Digital peripherals:
  - 11 General Purpose I/O (GPIO) pins with configurable pull-up/pull-down resistors.
  - GPIO pins can be used as edge and level sensitive interrupt sources.
  - Four general purpose counter/timers with a total of one capture input and nine match outputs.
  - Programmable WatchDog Timer (WDT).
- Analog peripherals:
  - 10-bit ADC with input multiplexing among five pins.

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- Serial interfaces:
  - UART with fractional baud rate generation, internal FIFO, and RS-485 support.
  - One SPI controller with SSP features and with FIFO and multi-protocol capabilities (see Section 7.16).
- Clock generation:
  - 12 MHz internal RC oscillator trimmed to 1% accuracy that can optionally be used as a system clock.
  - Programmable watchdog oscillator with a frequency range of 7.8 kHz to 1.8 MHz.
  - PLL allows CPU operation up to the maximum CPU rate without the need for a high-frequency crystal. May be run from an external clock or the internal RC oscillator.
  - Clock output function with divider that can reflect the external clock, IRC clock, CPU clock, and the Watchdog clock.
- Power control:
  - Integrated PMU (Power Management Unit) to minimize power consumption during Sleep and Deep-sleep modes.
  - Two reduced power modes: Sleep and Deep-sleep modes.
  - Processor wake-up from Deep-sleep mode via a dedicated start logic using up to six of the functional pins.
  - Power-On Reset (POR).
  - Brownout detect with four separate thresholds for interrupt and forced reset.
- Unique device serial number for identification.
- Single 3.3 V power supply (1.8 V to 3.6 V).
- Available as WLCSP16 package.

3. Applications

- Mobile devices
- Consumer peripherals
- Lighting
- 8-/16-bit applications
- Portable devices

4. Ordering information

Table 1. Ordering information

Type number	Package		
	Name	Description	Version
LPC1102	WLCSP16	wafer level chip-size package; 16 bumps; 2.17 × 2.32 × 0.6 mm	-

4.1 Ordering options

Table 2. Ordering options

Type number	Flash	Total SRAM	UART RS-485	SPI	ADC channels	Package
LPC1102	32 kB	8 kB	1	1	5	WLCSP16

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5. Block diagram

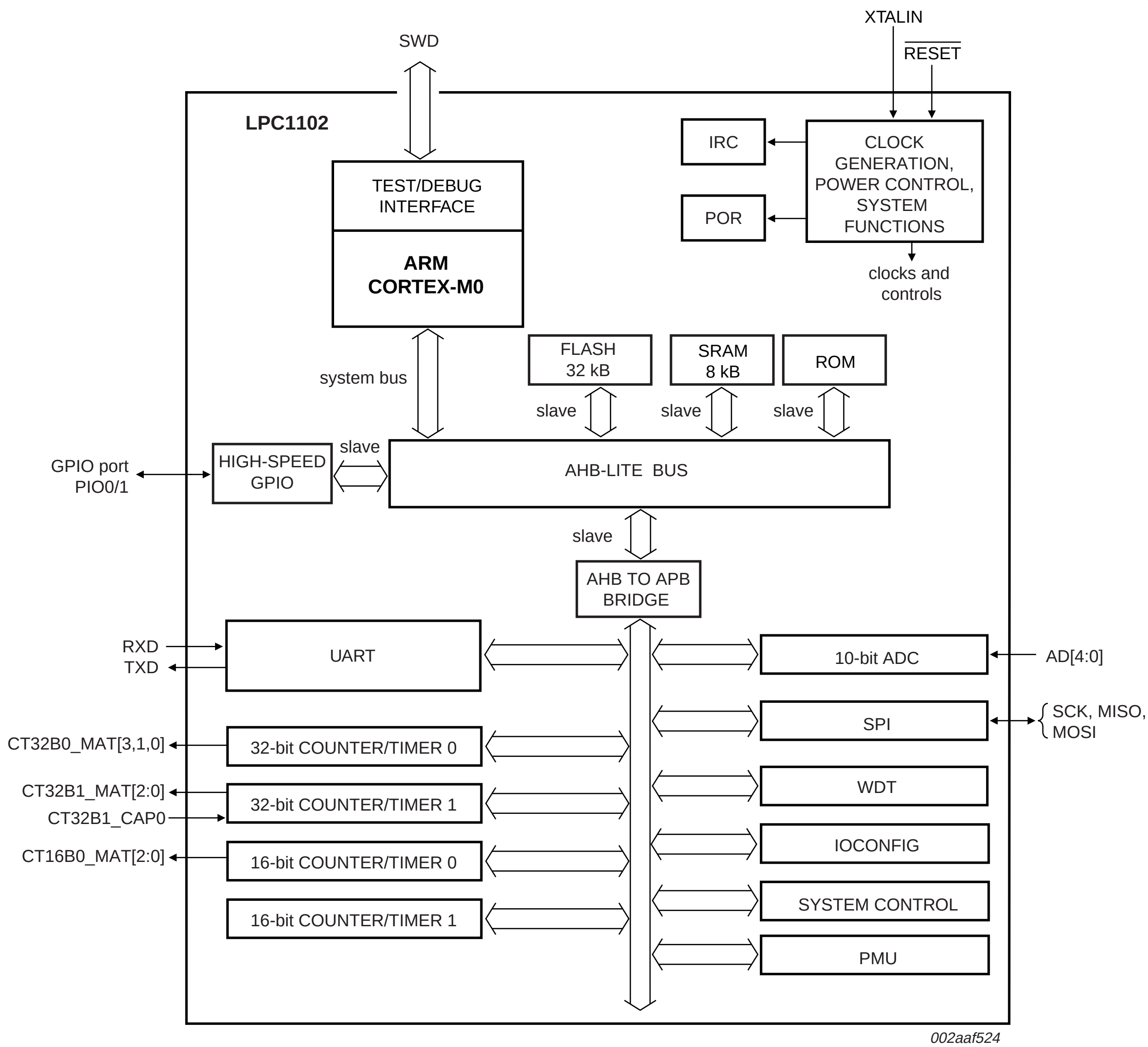


Fig 1. LPC1102 block diagram

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6. Pinning information

6.1 Pinning

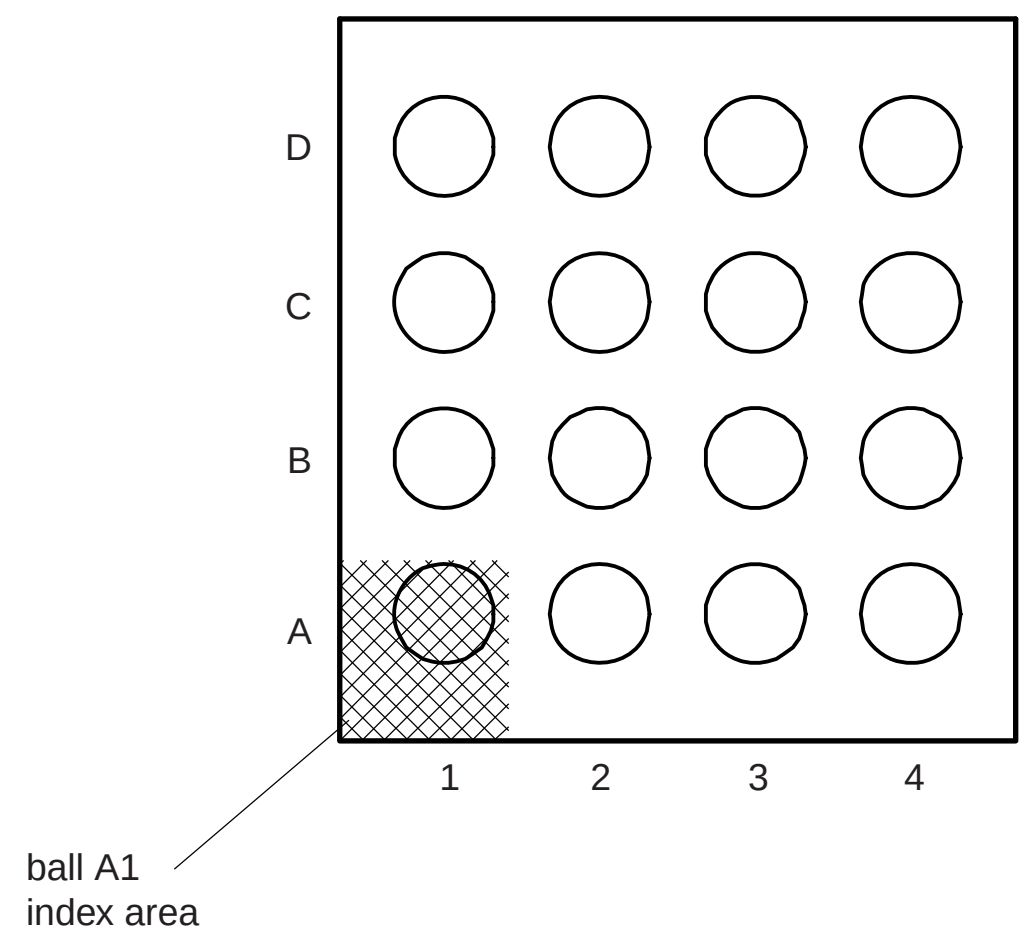


Fig 2. Pin configuration WLCSP16 package

6.2 Pin description

Table 3. LPC1102 pin description table

Symbol	Pin	Type	Reset state[1]	Wake-up function [2]	Description
RESET/PIO0_0	C1[3]	I	I; PU	DS	**RESET** — External reset input: A LOW on this pin resets the device, causing I/O ports and peripherals to take on their default states, and processor execution to begin at address 0.
		I/O	-	DS	**PIO0_0** — General purpose digital input/output pin.
PIO0_8/MISO/ CT16B0_MAT0	A2[4]	I/O	I; PU	DS	**PIO0_8** — General purpose digital input/output pin.
		I/O	-	DS	**MISO0** — Master In Slave Out for SPI.
		O	-	DS	**CT16B0_MAT0** — Match output 0 for 16-bit timer 0.
PIO0_9/MOSI/ CT16B0_MAT1	A3[4]	I/O	I; PU	DS	**PIO0_9** — General purpose digital input/output pin.
		I/O	-	DS	**MOSI0** — Master Out Slave In for SPI.
		O	-	DS	**CT16B0_MAT1** — Match output 1 for 16-bit timer 0.
SWCLK/ PIO0_10/ SCK/CT16B0_MAT2	A4[4]	I	I; PU	DS	**SWCLK** — Serial wire clock.
		I/O	-	DS	**PIO0_10** — General purpose digital input/output pin.
		I/O	-	DS	**SCK** — Serial clock for SPI.
		O	-	DS	**CT16B0_MAT2** — Match output 2 for 16-bit timer 0.
R/PIO0_11/ AD0/CT32B0_MAT3	B4[5]	-	I; PU	DS	R — Reserved.
		I/O	-	DS	**PIO0_11** — General purpose digital input/output pin.
		I	-	DS	**AD0** — A/D converter, input 0.
		I	-	DS	**CT32B0_MAT3** — Match output 3 for 32-bit timer 0.

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Table 3. LPC1102 pin description table *…continued*

Symbol	Pin	Type	Reset state[1]	Wake-up function [2]	Description
R/PIO1_0/ AD1/CT32B1_CAP0	B3[5]	-	I; PU	DS	R — Reserved.
		I/O	-	DS	**PIO1_0 —** General purpose digital input/output pin.
		I	-	DS	**AD1 —** A/D converter, input 1.
		I	-	DS	**CT32B1_CAP0 —** Capture input 0 for 32-bit timer 1.
R/PIO1_1/ AD2/CT32B1_MAT0	C4[5]	-	I; PU	-	**R —** Reserved.
		I/O	-	-	**PIO1_1 —** General purpose digital input/output pin.
		I	-	-	**AD2 —** A/D converter, input 2.
		O	-	-	**CT32B1_MAT0 —** Match output 0 for 32-bit timer 1.
R/PIO1_2/ AD3/CT32B1_MAT1	C3[5]	-	I; PU	-	**R —** Reserved.
		I/O	-	-	**PIO1_2 —** General purpose digital input/output pin.
		I	-	-	**AD3 —** A/D converter, input 3.
		O	-	-	**CT32B1_MAT1 —** Match output 1 for 32-bit timer 1.
SWDIO/PIO1_3/AD4/ CT32B1_MAT2	D4[5]	I/O	I; PU	-	**SWDIO —** Serial wire debug input/output.
		I/O	-	-	**PIO1_3 —** General purpose digital input/output pin.
		I	-	-	**AD4 —** A/D converter, input 4.
		O	-	-	**CT32B1_MAT2 —** Match output 2 for 32-bit timer 1.
PIO1_6/RXD/ CT32B0_MAT0	C2[4]	I/O	I; PU	-	**PIO1_6 —** General purpose digital input/output pin.
		I	-	-	**RXD —** Receiver input for UART.
		O	-	-	**CT32B0_MAT0 —** Match output 0 for 32-bit timer 0.
PIO1_7/TXD/ CT32B0_MAT1	D1[4]	I/O	I; PU	-	**PIO1_7 —** General purpose digital input/output pin.
		O	-	-	**TXD —** Transmitter output for UART.
		O	-	-	**CT32B0_MAT1 —** Match output 1 for 32-bit timer 0.
V_{DD}	D2; A1	I	-	-	3.3 V supply voltage to the internal regulator, the external rail, and the ADC. Also used as the ADC reference voltage.
XTALIN	B2[6]	I	-	-	External clock input and input to internal clock generator circuits. Input voltage must not exceed 1.8 V.
V_{SS}	D3; B1	I	-	-	Ground.

[1] Pin state at reset for default function: I = Input; PU = internal pull-up enabled.

[2] Wake-up functionality: DS = Deep-sleep mode wake-up pin (to be configured in the start logic).

[3] See Figure 20 for the reset pad configuration.

[4] 5 V tolerant pad providing digital I/O functions with configurable pull-up/pull-down resistors and configurable hysteresis (see Figure 19).

[5] 5 V tolerant pad providing digital I/O functions with configurable pull-up/pull-down resistors, configurable hysteresis, and analog input. When configured as a ADC input, digital section of the pad is disabled and the pin is not 5 V tolerant (see Figure 19).

[6] When the external clock is not used, connect XTALIN as follows: XTALIN can be left floating or can be grounded (grounding is preferred to reduce susceptibility to noise).

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7. Functional description

7.1 ARM Cortex-M0 processor

The ARM Cortex-M0 is a general purpose, 32-bit microprocessor, which offers high performance and very low power consumption.

7.2 On-chip flash program memory

The LPC1102 contain 32 kB of on-chip flash memory.

Remark: The LPC1102 supports In-Application Programming (IAP) and In-System Programming (ISP). For ISP, since there is no dedicated ISP entry pin, user code is required to invoke ISP functionality. Unprogrammed parts will automatically boot into ISP mode.

7.3 On-chip SRAM

The LPC1102 contain 8 on-chip static RAM memory.

7.4 Memory map

The LPC1102 incorporates several distinct memory regions, shown in the following figures. Figure 3 shows the overall map of the entire address space from the user program viewpoint following reset. The interrupt vector area supports address remapping.

The AHB peripheral area is 2 megabyte in size, and is divided to allow for up to 128 peripherals. The APB peripheral area is 512 kB in size and is divided to allow for up to 32 peripherals. Each peripheral of either type is allocated 16 kilobytes of space. This allows simplifying the address decoding for each peripheral.

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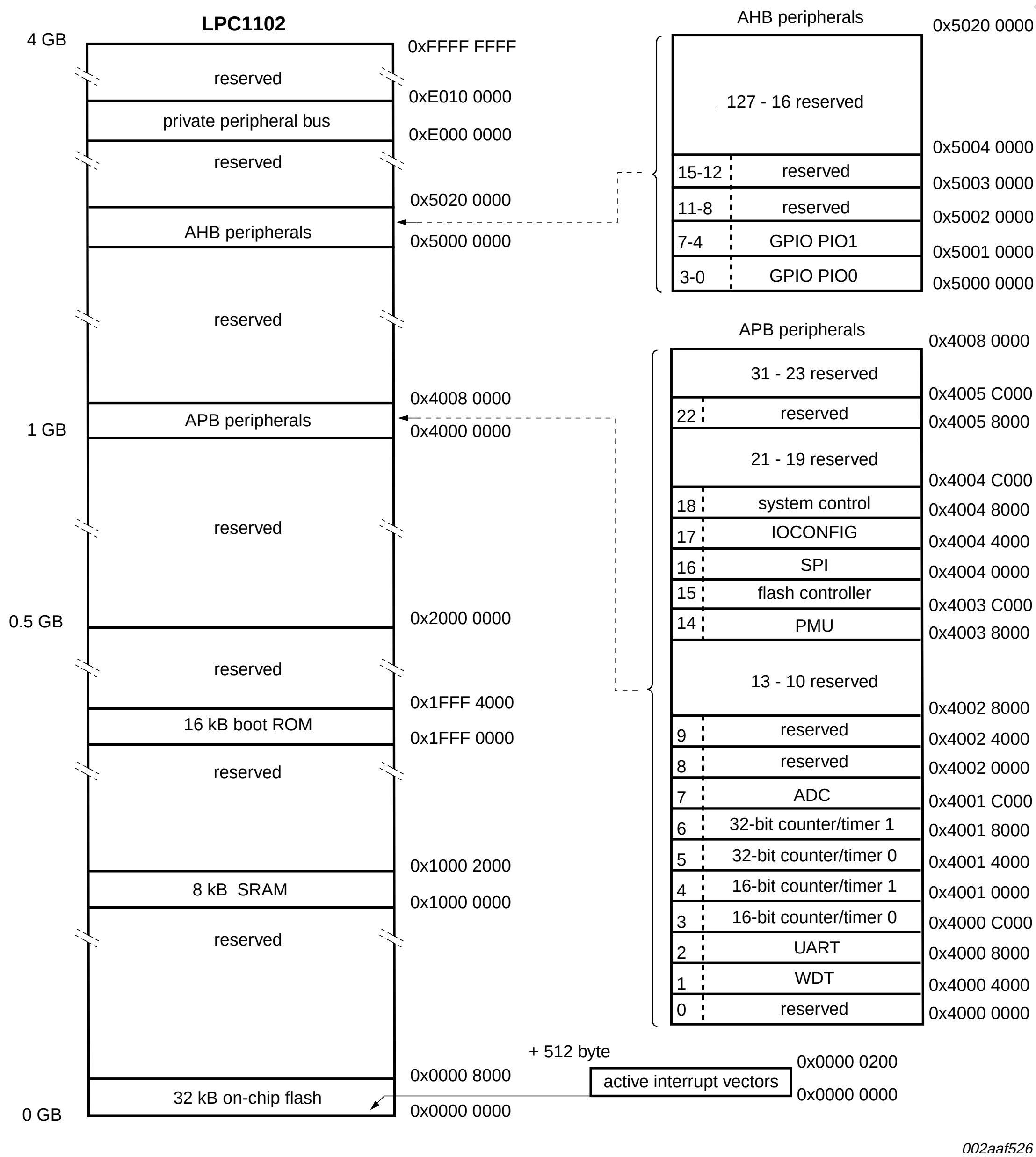


Fig 3. LPC1102 memory map

7.5 Nested Vectored Interrupt Controller (NVIC)

The Nested Vectored Interrupt Controller (NVIC) is an integral part of the Cortex-M0. The tight coupling to the CPU allows for low interrupt latency and efficient processing of late arriving interrupts.

7.5.1 Features

- Controls system exceptions and peripheral interrupts.
- In the LPC1102, the NVIC supports 19 vectored interrupts including up to 6 inputs to the start logic from individual GPIO pins.

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- Four programmable interrupt priority levels, with hardware priority level masking.
- Relocatable vector table.
- Software interrupt generation.

7.5.2 Interrupt sources

Each peripheral device has one interrupt line connected to the NVIC but may have several interrupt flags. Individual interrupt flags may also represent more than one interrupt source.

Any GPIO pin (total of up to 11 pins) regardless of the selected function, can be programmed to generate an interrupt on a level, or rising edge or falling edge, or both.

7.6 IOCONFIG block

The IOCONFIG block allows selected pins of the microcontroller to have more than one function. Configuration registers control the multiplexers to allow connection between the pin and the on-chip peripherals.

Peripherals should be connected to the appropriate pins prior to being activated and prior to any related interrupt(s) being enabled. Activity of any enabled peripheral function that is not mapped to a related pin should be considered undefined.

7.7 Fast general purpose parallel I/O

Device pins that are not connected to a specific peripheral function are controlled by the GPIO registers. Pins may be dynamically configured as inputs or outputs. Multiple outputs can be set or cleared in one write operation.

LPC1102 use accelerated GPIO functions:

- GPIO registers are a dedicated AHB peripheral so that the fastest possible I/O timing can be achieved.
- Entire port value can be written in one instruction.

Additionally, any GPIO pin (total of 11 pins) providing a digital function can be programmed to generate an interrupt on a level, a rising or falling edge, or both.

7.7.1 Features

- Bit level port registers allow a single instruction to set or clear any number of bits in one write operation.
- Direction control of individual bits.
- All I/O default to inputs with pull-ups enabled after reset.
- Pull-up/pull-down resistor configuration can be programmed through the IOCONFIG block for each GPIO pin.

7.8 UART

The LPC1102 contains one UART.

Support for RS-485/9-bit mode allows both software address detection and automatic address detection using 9-bit mode.

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The UART includes a fractional baud rate generator. Standard baud rates such as 115200 Bd can be achieved with any crystal frequency above 2 MHz.

7.8.1 Features

- Maximum UART data bit rate of 3.125 MBit/s.
- 16 Byte Receive and Transmit FIFOs.
- Register locations conform to 16C550 industry standard.
- Receiver FIFO trigger points at 1 B, 4 B, 8 B, and 14 B.
- Built-in fractional baud rate generator covering wide range of baud rates without a need for external crystals of particular values.
- FIFO control mechanism that enables software flow control implementation.
- Support for RS-485/9-bit mode.

7.9 SPI serial I/O controller

The LPC1102 contains one SPI controller and fully supports SSP features.

The SPI controller is capable of operation on a SSP, 4-wire SSI, or Microwire bus. It can interact with multiple masters and slaves on the bus. Only a single master and a single slave can communicate on the bus during a given data transfer. The SPI supports full duplex transfers, with frames of 4 bits to 16 bits of data flowing from the master to the slave and from the slave to the master. In practice, often only one of these data flows carries meaningful data.

Remark: Care must be taken when using the SPI because the SPI clock SCK and the serial wire debug clock SWCLK share the same pin on the WLCSP16 package. Once the SPI is enabled, the serial wire debugger is no longer available.

7.9.1 Features

- Maximum SPI speed of 25 Mbit/s (master) or 4.17 Mbit/s (slave) (in SSP mode)
- Compatible with Motorola SPI, 4-wire Texas Instruments SSI, and National Semiconductor Microwire buses
- Synchronous serial communication
- Master or slave operation
- 8-frame FIFOs for both transmit and receive
- 4-bit to 16-bit frame

7.10 10-bit ADC

The LPC1102 contains one ADC. It is a single 10-bit successive approximation ADC with eight channels.

7.10.1 Features

- 10-bit successive approximation ADC.
- Input multiplexing among 5 pins.
- Power-down mode.

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- Measurement range 0 V to V_{DD}.
- 10-bit conversion time $\geq$ 2.44 μs.
- Burst conversion mode for single or multiple inputs.
- Optional conversion on transition of input pin or timer match signal.
- Individual result registers for each ADC channel to reduce interrupt overhead.

7.11 General purpose external event counter/timers

The LPC1102 includes two 32-bit counter/timers and two 16-bit counter/timers. The counter/timer is designed to count cycles of the system derived clock. It can optionally generate interrupts or perform other actions at specified timer values, based on four match registers. Each counter/timer also includes one capture input to trap the timer value when an input signal transitions, optionally generating an interrupt.

7.11.1 Features

- A 32-bit/16-bit timer/counter with a programmable 32-bit/16-bit prescaler.
- Counter or timer operation.
- One capture channel that can take a snapshot of the timer value when an input signal transitions. A capture event may also generate an interrupt.
- Four match registers per timer that allow:
  - Continuous operation with optional interrupt generation on match.
  - Stop timer on match with optional interrupt generation.
  - Reset timer on match with optional interrupt generation.
- Up to four external outputs corresponding to match registers, with the following capabilities:
  - Set LOW on match.
  - Set HIGH on match.
  - Toggle on match.
  - Do nothing on match.

7.12 System tick timer

The ARM Cortex-M0 includes a system tick timer (SYSTICK) that is intended to generate a dedicated SYSTICK exception at a fixed time interval (typically 10 ms).

7.13 Watchdog timer

The purpose of the watchdog is to reset the microcontroller within a selectable time period.

7.13.1 Features

- Internally resets chip if not periodically reloaded.
- Debug mode.
- Enabled by software but requires a hardware reset or a watchdog reset/interrupt to be disabled.

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- Incorrect/Incomplete feed sequence causes reset/interrupt if enabled.
- Flag to indicate watchdog reset.
- Programmable 32-bit timer with internal prescaler.
- Selectable time period from ($T_{cy(WDCLK)} \times 256 \times 4$) to ($T_{cy(WDCLK)} \times 2^{32} \times 4$) in multiples of $T_{cy(WDCLK)} \times 4$.
- The Watchdog Clock (WDCLK) source can be selected from the Internal RC oscillator (IRC), the Watchdog oscillator, or the main clock. This gives a wide range of potential timing choices of Watchdog operation under different power reduction conditions. It also provides the ability to run the WDT from an entirely internal source that is not dependent on an external crystal and its associated components and wiring for increased reliability.

7.14 Clocking and power control

7.14.1 Crystal oscillators

The LPC1102 include two independent oscillators. These are the Internal RC oscillator (IRC) and the Watchdog oscillator. Each oscillator can be used for more than one purpose as required in a particular application.

Following reset, the LPC1102 will operate from the Internal RC oscillator until switched by software. This allows systems to operate without any external crystal and the bootloader code to operate at a known frequency.

See Figure 4 for an overview of the LPC1102 clock generation.

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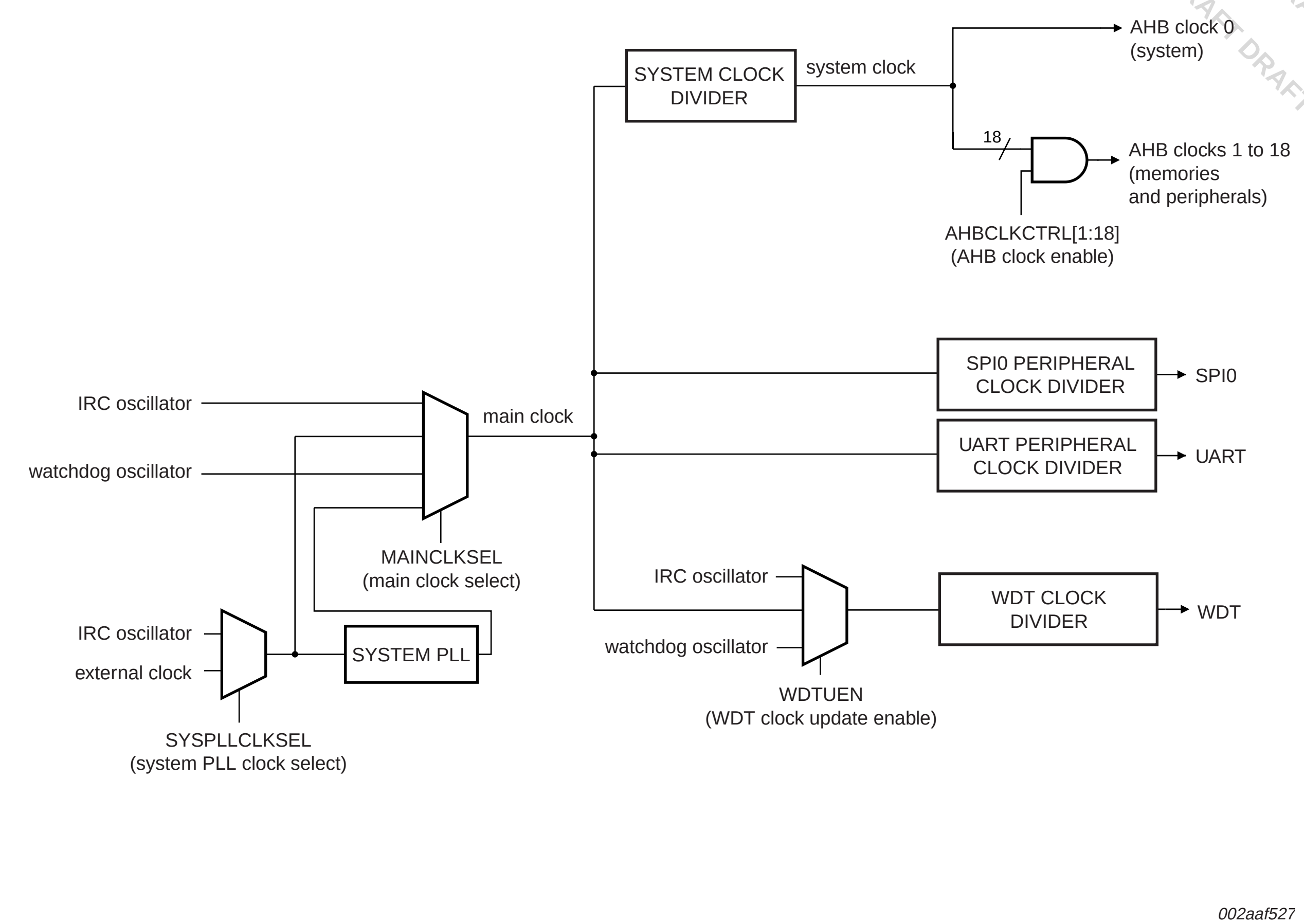


Fig 4. LPC1102 clock generation block diagram

7.14.1.1 Internal RC oscillator

The IRC may be used as the clock source for the WDT, and/or as the clock that drives the PLL and subsequently the CPU. The nominal IRC frequency is 12 MHz. The IRC is trimmed to 1 % accuracy over the entire voltage and temperature range.

Upon power-up or any chip reset, the LPC1102 use the IRC as the clock source. Software may later switch to one of the other available clock sources.

7.14.1.2 Watchdog oscillator

The watchdog oscillator can be used as a clock source that directly drives the CPU or the watchdog timer. The watchdog oscillator nominal frequency is programmable between 7.8 kHz and 1.7 MHz. The frequency spread over processing and temperature is ±40%.

7.14.2 System PLL

The PLL accepts an input clock frequency in the range of 10 MHz to 25 MHz. The input frequency is multiplied up to a high frequency with a Current Controlled Oscillator (CCO). The multiplier can be an integer value from 1 to 32. The CCO operates in the range of 156 MHz to 320 MHz, so there is an additional divider in the loop to keep the CCO within its frequency range while the PLL is providing the desired output frequency. The output divider may be set to divide by 2, 4, 8, or 16 to produce the output clock. Since the

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minimum output divider value is 2, it is insured that the PLL output has a 50 % duty cycle. The PLL is turned off and bypassed following a chip reset and may be enabled by software. The program must configure and activate the PLL, wait for the PLL to lock, and then connect to the PLL as a clock source. The PLL settling time is 100 μs.

7.14.3 Wake-up process

The LPC1102 begin operation at power-up by using the 12 MHz IRC oscillator as the clock source. This allows chip operation to resume quickly. If an external clock or the PLL is needed by the application, software will need to enable these features and wait for them to stabilize before they are used as a clock source.

7.14.4 Power control

The LPC1102 support a variety of power control features. There are two special modes of processor power reduction: Sleep mode and Deep-sleep mode. The CPU clock rate may also be controlled as needed by changing clock sources, reconfiguring PLL values, and/or altering the CPU clock divider value. This allows a trade-off of power versus processing speed based on application requirements. In addition, a register is provided for shutting down the clocks to individual on-chip peripherals, allowing fine tuning of power consumption by eliminating all dynamic power use in any peripherals that are not required for the application. Selected peripherals have their own clock divider which provides even better power control.

7.14.4.1 Sleep mode

When Sleep mode is entered, the clock to the core is stopped. Resumption from the Sleep mode does not need any special sequence but re-enabling the clock to the ARM core.

In Sleep mode, execution of instructions is suspended until either a reset or interrupt occurs. Peripheral functions continue operation during Sleep mode and may generate interrupts to cause the processor to resume execution. Sleep mode eliminates dynamic power used by the processor itself, memory systems and related controllers, and internal buses.

7.14.4.2 Deep-sleep mode

In Deep-sleep mode, the chip is in Sleep mode, and in addition all analog blocks are shut down except for the watchdog oscillator and the BOD circuit, which can be configured to remain running in Deep-sleep mode to allow a reset initiated by a timer or BOD event. Deep-sleep mode allows for additional power savings.

The GPIO pins (6 pins total, see Table 3) serve as external wake-up pins to a dedicated start logic to wake up the chip from Deep-sleep mode.

The clock source should be switched to IRC before entering Deep-sleep mode unless the watchdog oscillator remains running in Deep-sleep mode. The IRC can be switched on and off glitch-free and provides a clean clock signal after start-up.

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7.15 System control

7.15.1 Reset

Reset has four sources on the LPC1102: the $\overline{\text{RESET}}$ pin, the Watchdog reset, power-on reset (POR), and the BrownOut Detection (BOD) circuit. The $\overline{\text{RESET}}$ pin is a Schmitt trigger input pin. Assertion of chip reset by any source, once the operating voltage attains a usable level, starts the IRC and initializes the flash controller.

When the internal Reset is removed, the processor begins executing at address 0, which is initially the Reset vector mapped from the boot block. At that point, all of the processor and peripheral registers have been initialized to predetermined values.

7.15.2 Brownout detection

The LPC1102 includes four levels for monitoring the voltage on the V_{DD} pin. If this voltage falls below one of the four selected levels, the BOD asserts an interrupt signal to the NVIC. This signal can be enabled for interrupt in the Interrupt Enable Register in the NVIC in order to cause a CPU interrupt; if not, software can monitor the signal by reading a dedicated status register. Four additional threshold levels can be selected to cause a forced reset of the chip.

7.15.3 Code security (Code Read Protection - CRP)

This feature of the LPC1102 allows user to enable different levels of security in the system so that access to the on-chip flash and use of the Serial Wire Debugger (SWD) can be restricted. When needed, CRP is invoked by programming a specific pattern into a dedicated flash location. IAP commands are not affected by the CRP.

There are three levels of Code Read Protection:

1. CRP1 disables access to the chip via the SWD and allows partial flash update (excluding flash sector 0). This mode is useful when CRP is required and flash field updates are needed but all sectors can not be erased.
2. CRP2 disables access to the chip via the SWD and only allows full flash erase and update.
3. Running an application with level CRP3 selected fully disables any access to the chip via the SWD pins.

Remark: The LPC1102 does not provide an ISP entry pin to be monitored at reset. For all three CRP levels, the user's application code must provide a flash update mechanism which reinvokes ISP by defining a user-selected PIO pin for ISP entry.

CAUTION

If Code Read Protection (CRP1/2/3) is selected, no future factory testing can be performed on the device.

7.15.4 APB interface

The APB peripherals are located on one APB bus.

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7.15.5 AHBLite

The AHBLite connects the CPU bus of the ARM Cortex-M0 to the flash memory, the main static RAM, and the Boot ROM.

7.15.6 External interrupt inputs

All GPIO pins can be level or edge sensitive interrupt inputs.

7.15.7 Memory mapping control

The Cortex-M0 incorporates a mechanism that allows remapping the interrupt vector table to alternate locations in the memory map. This is controlled via the Vector Table Offset Register contained in the NVIC.

The vector table may be located anywhere within the bottom 1 GB of Cortex-M0 address space. The vector table must be located on a 128 word (512 byte) boundary.

7.16 Emulation and debugging

Debug functions are integrated into the ARM Cortex-M0. Serial wire debug with four breakpoints and two watchpoints is supported.

Remark: Care must be taken when using the SPI because the SPI clock SCK and the serial wire debug clock SWCLK share the same pin on the WLCSP16 package. Once the SPI is enabled, the serial wire debugger is no longer available.

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8. Limiting values

Table 4. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134).[1]

Symbol	Parameter	Conditions		Min	Max	Unit
V_{DD}	supply voltage (core and external rail)			1.8	3.6	V
V_I	input voltage	5 V tolerant I/O pins; only valid when the V_{DD} supply voltage is present	[2]	−0.5	+5.5	V
I_{DD}	supply current	per supply pin	[3]	-	100	mA
I_{SS}	ground current	per ground pin	[3]	-	100	mA
I_{latch}	I/O latch-up current	$-(0.5V_{DD}) < V_I < (1.5V_{DD})$; $T_j < 125$ °C		-	100	mA
T_{stg}	storage temperature		[4]	−65	+150	°C
$T_{j(max)}$	maximum junction temperature			-	150	°C
$P_{tot(pack)}$	total power dissipation (per package)	based on package heat transfer, not device power consumption		-	1.5	W
V_{ESD}	electrostatic discharge voltage	human body model; all pins	[5]	−6500	+6500	V

[1] The following applies to the limiting values:

a) This product includes circuitry specifically designed for the protection of its internal devices from the damaging effects of excessive static charge. Nonetheless, it is suggested that conventional precautions be taken to avoid applying greater than the rated maximum.

b) Parameters are valid over operating temperature range unless otherwise specified. All voltages are with respect to V_{SS} unless otherwise noted.

[2] Including voltage on outputs in 3-state mode.

[3] The peak current is limited to 25 times the corresponding maximum current.

[4] Dependent on package type.

[5] Human body model: equivalent to discharging a 100 pF capacitor through a 1.5 kΩ series resistor.

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9. Static characteristics

Table 5. Static characteristics

T_{amb} = −40 °C to +85 °C, unless otherwise specified.

Symbol	Parameter	Conditions		Min	Typ[1]	Max	Unit
V_{DD}	supply voltage (core and external rail)			1.8	3.3	3.6	V
I_{DD}	supply current	Active mode; code `while(1){}` executed from flash					
		system clock = 12 MHz V_{DD} = 3.3 V	[2][3][4][5][6]	-	2	-	mA
		system clock = 50 MHz V_{DD} = 3.3 V	[2][3][5][6][7]	-	7	-	mA
		Sleep mode; system clock = 12 MHz V_{DD} = 3.3 V	[2][3][4][5][6]	-	1	-	mA
		Deep-sleep mode; V_{DD} = 3.3 V	[2][3][8]	-	2	-	µA
Standard port pins, RESET							
I_{IL}	LOW-level input current	V_I = 0 V; on-chip pull-up resistor disabled		-	0.5	10	nA
I_{IH}	HIGH-level input current	$V_I = V_{DD}$; on-chip pull-down resistor disabled		-	0.5	10	nA
I_{OZ}	OFF-state output current	V_O = 0 V; $V_O = V_{DD}$; on-chip pull-up/down resistors disabled		-	0.5	10	nA
V_I	input voltage	pin configured to provide a digital function	[9][10]	0	-	5.0	V
V_O	output voltage	output active		0	-	V_{DD}	V
V_{IH}	HIGH-level input voltage			$0.7V_{DD}$	-	-	V
V_{IL}	LOW-level input voltage			-	-	$0.3V_{DD}$	V
V_{hys}	hysteresis voltage			-	0.4	-	V
V_{OH}	HIGH-level output voltage	$2.0\ V \le V_{DD} \le 3.6\ V$; I_{OH} = −4 mA		$V_{DD} - 0.4$	-	-	V
		$1.8\ V \le V_{DD} < 2.0\ V$; I_{OH} = −3 mA		$V_{DD} - 0.4$	-	-	V
V_{OL}	LOW-level output voltage	$2.0\ V \le V_{DD} \le 3.6\ V$; I_{OL} = 4 mA		-	-	0.4	V
		$1.8\ V \le V_{DD} < 2.0\ V$; I_{OL} = 3 mA		-	-	0.4	V
I_{OH}	HIGH-level output current	$V_{OH} = V_{DD} - 0.4$ V; $2.0\ V \le V_{DD} \le 3.6\ V$		−4	-	-	mA
		$1.8\ V \le V_{DD} < 2.0\ V$		−3	-	-	mA

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Table 5. Static characteristics *...continued*

T_{amb} = −40 °C to +85 °C, unless otherwise specified.

Symbol	Parameter	Conditions		Min	Typ[1]	Max	Unit
I_{OL}	LOW-level output current	V_{OL} = 0.4 V 2.0 V ≤ V_{DD} ≤ 3.6 V		4	-	-	mA
		1.8 V ≤ V_{DD} < 2.0 V		3	-	-	mA
I_{OHS}	HIGH-level short-circuit output current	V_{OH} = 0 V	[11]	-	-	−45	mA
I_{OLS}	LOW-level short-circuit output current	V_{OL} = V_{DD}	[11]	-	-	50	mA
I_{pd}	pull-down current	V_I = 5 V		10	50	150	μA
I_{pu}	pull-up current	V_I = 0 V; 2.0 V ≤ V_{DD} ≤ 3.6 V		−15	−50	−85	μA
		1.8 V ≤ V_{DD} < 2.0 V		−10	−50	−85	μA
		V_{DD} < V_I < 5 V		0	0	0	μA
External clock input							
$V_{i(xtal)}$	crystal input voltage			−0.5	1.8	1.95	V

[1] Typical ratings are not guaranteed. The values listed are at room temperature (25 °C), nominal supply voltages.

[2] T_{amb} = 25 °C.

[3] I_{DD} measurements were performed with all pins configured as GPIO outputs driven LOW and pull-up resistors disabled.

[4] IRC enabled; external clock disabled; system PLL disabled.

[5] BOD disabled.

[6] All peripherals disabled in the SYSAHBCLKCTRL register. Peripheral clocks to UART and SPI0/1 disabled in system configuration block.

[7] <tbd>; system PLL enabled.

[8] All oscillators and analog blocks turned off in the PDSLEEPCFG register; PDSLEEPCFG = 0x0000 18FF.

[9] Including voltage on outputs in 3-state mode.

[10] V_{DD} supply voltage must be present.

[11] Allowed as long as the current limit does not exceed the maximum current allowed by the device.

[12] To V_{SS}.

Table 6. ADC static characteristics

T_{amb} = −40 °C to +85 °C unless otherwise specified; ADC frequency 4.5 MHz, V_{DD} = 2.5 V to 3.6 V.

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
V_{IA}	analog input voltage			0	-	V_{DD}	V
C_{ia}	analog input capacitance			-	-	1	pF
E_D	differential linearity error		[1][2]	-	-	± 1	LSB
$E_{L(adj)}$	integral non-linearity		[3]	-	-	± 1.5	LSB
E_O	offset error		[4]	-	-	± 3.5	LSB
E_G	gain error		[5]	-	-	0.6	%
E_T	absolute error		[6]	-	-	± 4	LSB
R_{vsi}	voltage source interface resistance			-	-	40	kΩ
R_i	input resistance		[7][8]	-	-	2.5	MΩ

[1] The ADC is monotonic, there are no missing codes.

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[2] The differential linearity error (E_D) is the difference between the actual step width and the ideal step width. See Figure 5.

[3] The integral non-linearity ($E_{L(adj)}$) is the peak difference between the center of the steps of the actual and the ideal transfer curve after appropriate adjustment of gain and offset errors. See Figure 5.

[4] The offset error (E_O) is the absolute difference between the straight line which fits the actual curve and the straight line which fits the ideal curve. See Figure 5.

[5] The gain error (E_G) is the relative difference in percent between the straight line fitting the actual transfer curve after removing offset error, and the straight line which fits the ideal transfer curve. See Figure 5.

[6] The absolute error (E_T) is the maximum difference between the center of the steps of the actual transfer curve of the non-calibrated ADC and the ideal transfer curve. See Figure 5.

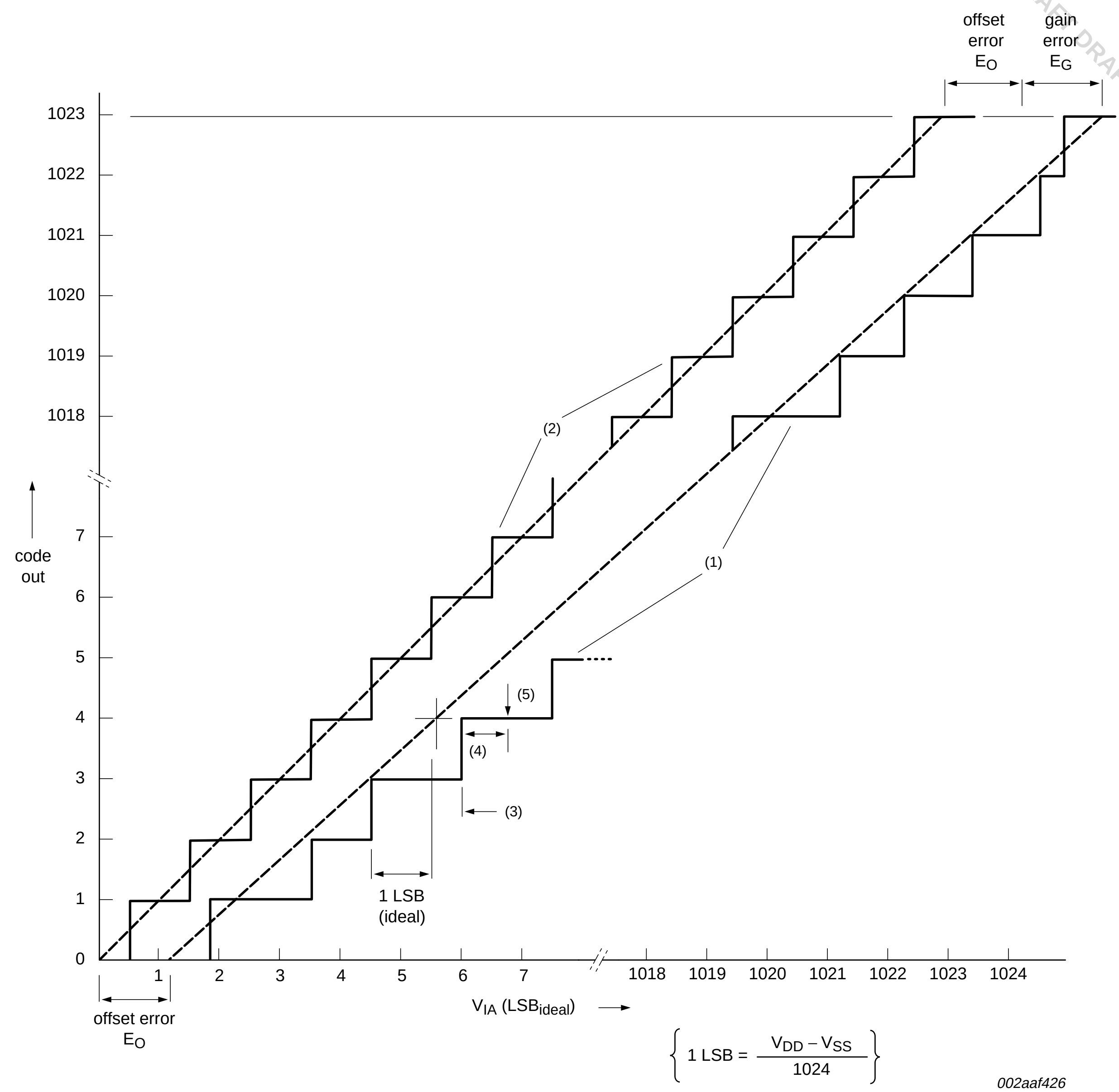
[7] T_{amb} = 25 °C; maximum sampling frequency f_s = 4.5 MHz and analog input capacitance C_{ia} = 1 pF.

[8] Input resistance R_i depends on the sampling frequency fs: $R_i = 1 / (f_s \times C_{ia})$.

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(1) Example of an actual transfer curve.

(2) The ideal transfer curve.

(3) Differential linearity error (E_D).

(4) Integral non-linearity ($E_{L(adj)}$).

(5) Center of a step of the actual transfer curve.

Fig 5. ADC characteristics

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9.1 BOD static characteristics

Table 7. BOD static characteristics[1]

T_{amb} = 25 °C.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{th}	threshold voltage	interrupt level 0				
		assertion	-	1.65	-	V
		de-assertion	-	1.80	-	V
		interrupt level 1				
		assertion	-	2.22	-	V
		de-assertion	-	2.35	-	V
		interrupt level 2				
		assertion	-	2.52	-	V
		de-assertion	-	2.66	-	V
		interrupt level 3				
		assertion	-	2.80	-	V
		de-assertion	-	2.90	-	V
		reset level 0				
		assertion	-	1.46	-	V
		de-assertion	-	1.63	-	V
		reset level 1				
		assertion	-	2.06	-	V
		de-assertion	-	2.15	-	V
		reset level 2				
		assertion	-	2.35	-	V
		de-assertion	-	2.43	-	V
		reset level 3				
		assertion	-	2.63	-	V
		de-assertion	-	2.71	-	V

[1] Interrupt levels are selected by writing the level value to the BOD control register BODCTRL, see *LPC111x user manual*.

9.2 Power consumption

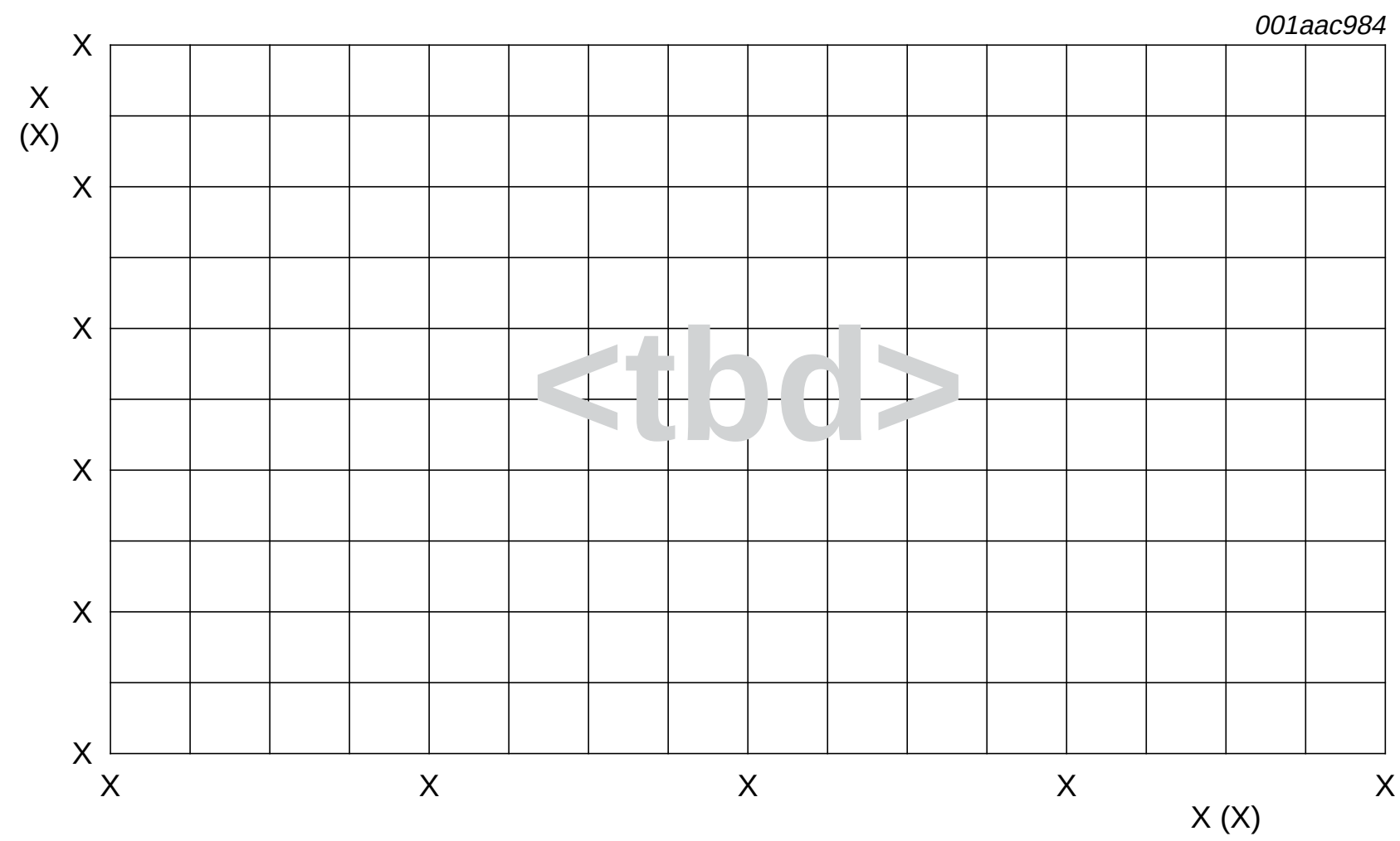
Power measurements in Active, Sleep, and Deep-sleep modes were performed under the following conditions (see *LPC111x user manual*):

- Configure all pins as GPIO with pull-up resistor disabled in the IOCONFIG block.
- Configure GPIO pins as outputs using the GPIOnDIR registers.
- Write 0 to all GPIOnDATA registers to drive the outputs LOW.

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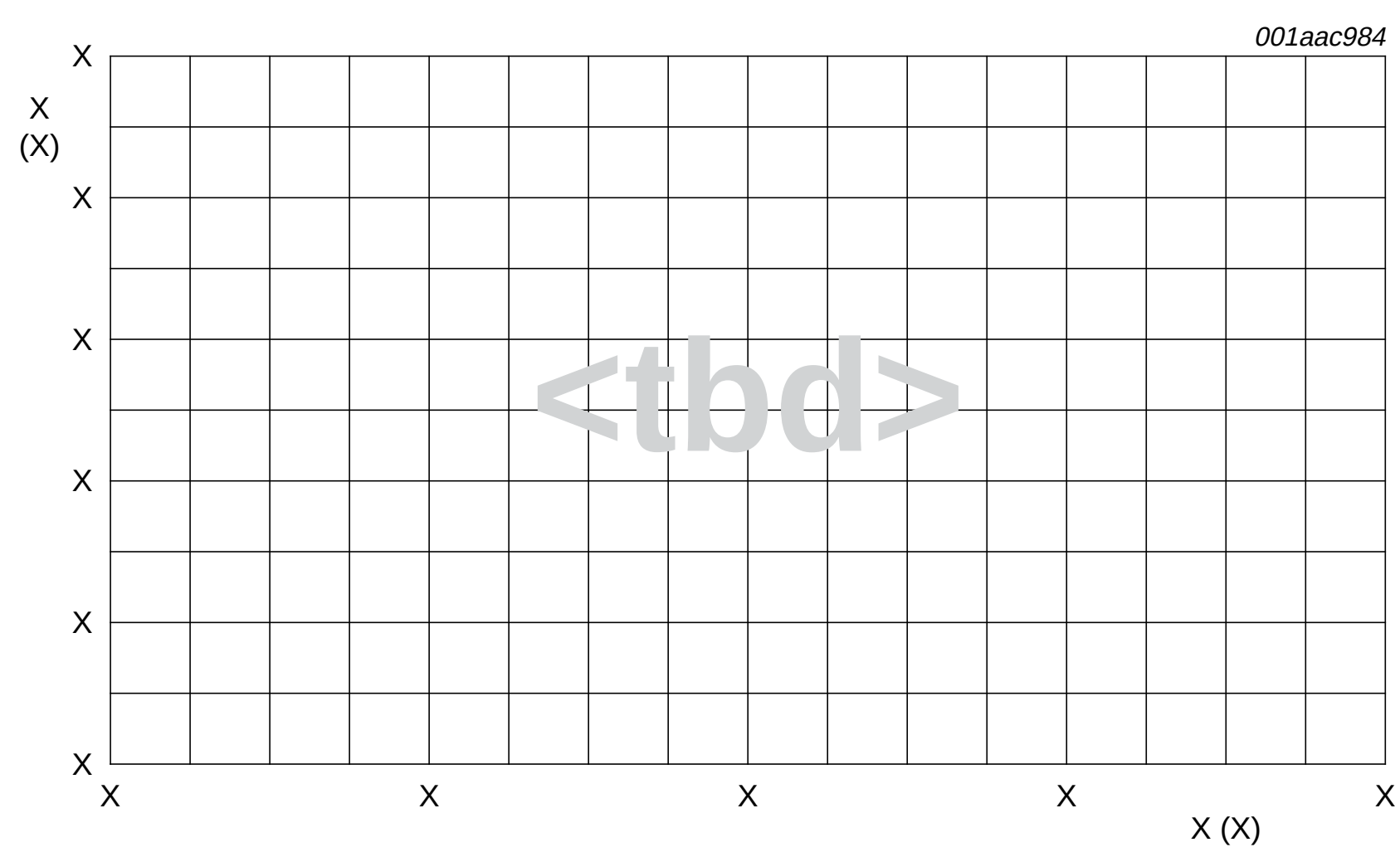


Conditions: T_{amb} = 25 °C; active mode entered executing code `while(1){}` from flash; all peripherals disabled in the SYSAHBCLKCTRL register (SYSAHBCLKCTRL= 0x1F); all peripheral clocks disabled; internal pull-up resistors disabled; BOD disabled.

(1) System PLL disabled; IRC enabled.

(2) System PLL enabled; IRC disabled.

Fig 6. Active mode: Typical supply current I_{DD} versus supply voltage V_{DD} for different system clock frequencies



Conditions: V_{DD} = 3.3 V; active mode entered executing code `while(1){}` from flash; all peripherals disabled in the SYSAHBCLKCTRL register (SYSAHBCLKCTRL= 0x1F); all peripheral clocks disabled; internal pull-up resistors disabled; BOD disabled.

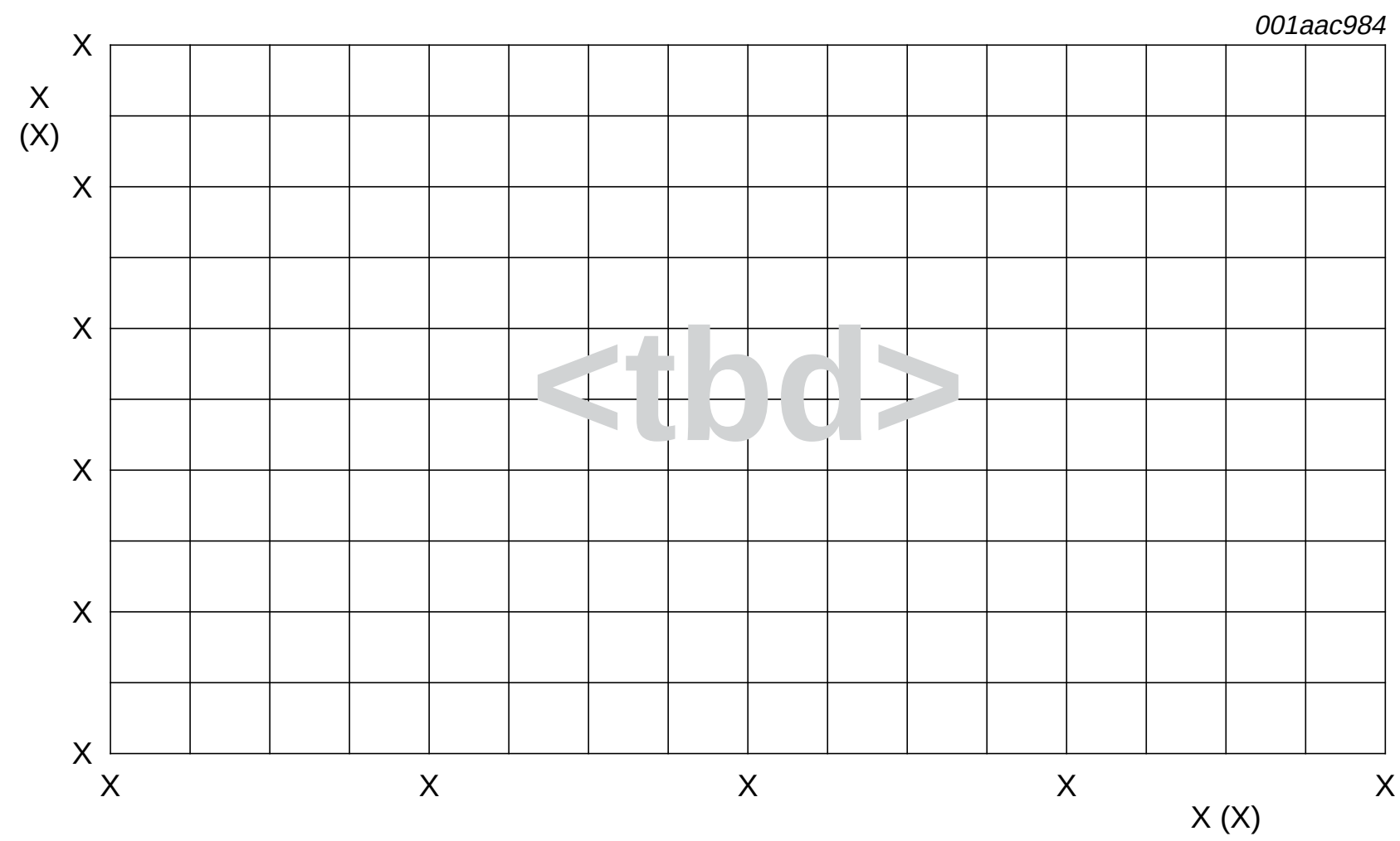
(1) System PLL disabled; IRC enabled.

(2) System PLL enabled; IRC disabled.

Fig 7. Active mode: Typical supply current I_{DD} versus temperature for different system clock frequencies

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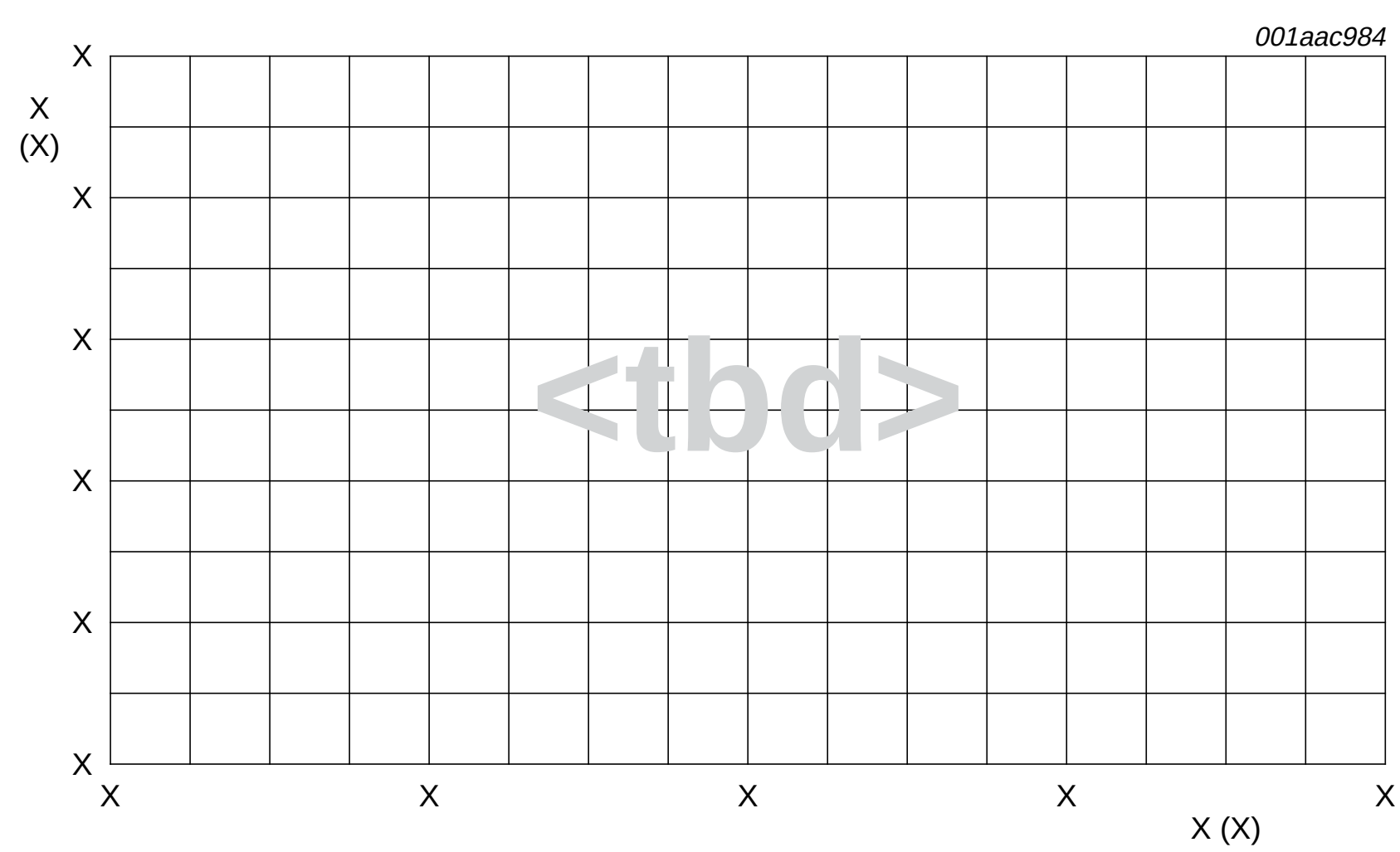


Conditions: V_{DD} = 3.3 V; sleep mode entered from flash; all peripherals disabled in the SYSAHBCLKCTRL register (SYSAHBCLKCTRL= 0x1F); all peripheral clocks disabled; internal pull-up resistors disabled; BOD disabled.

(1) System PLL disabled; IRC enabled.

(2) System PLL enabled; IRC disabled.

Fig 8. Sleep mode: Typical supply current I_{DD}versus temperature for different system clock frequencies



Conditions: BOD disabled; all oscillators and analog blocks disabled in the PDSLEEPCFG register (PDSLEEPCFG = 0x0000 18FF).

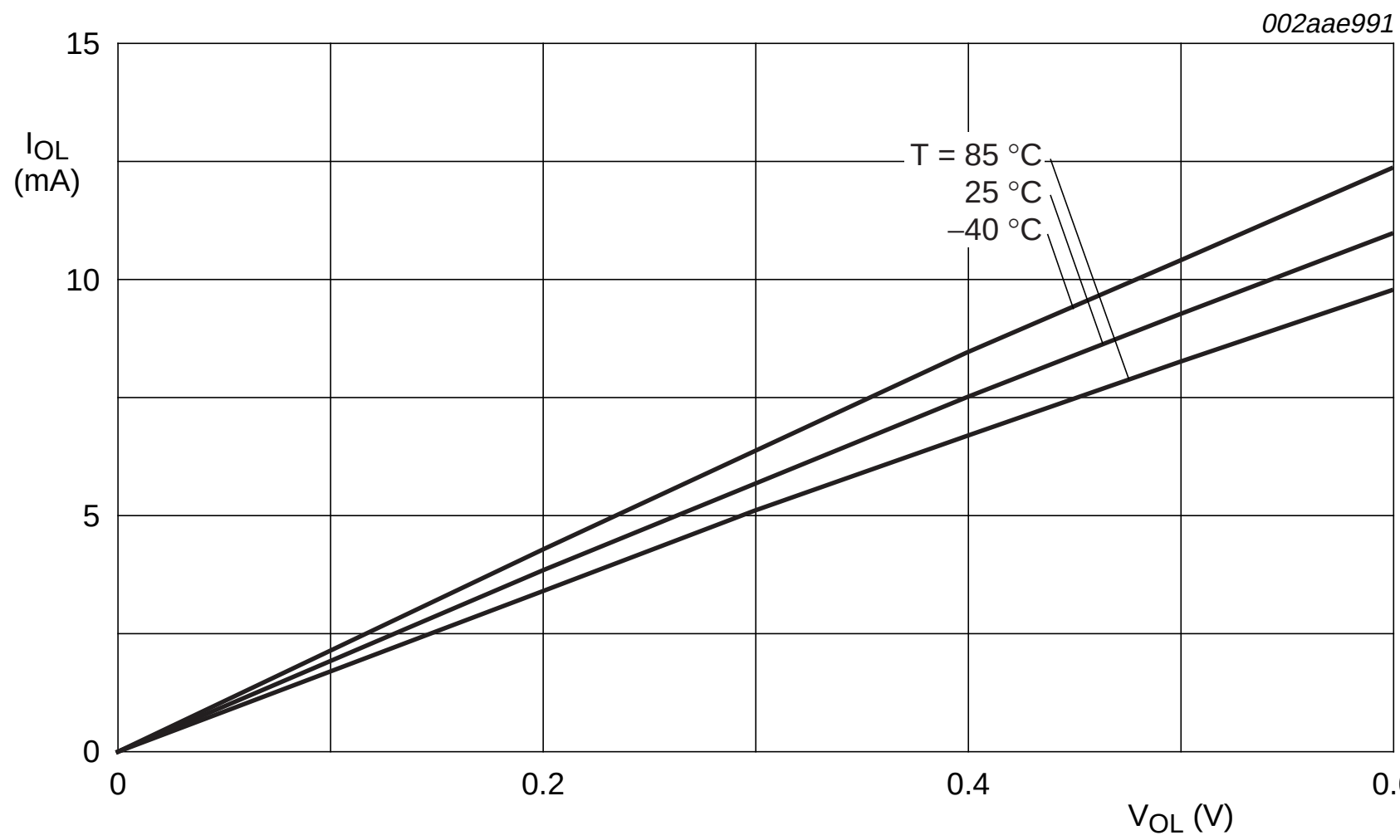
Fig 9. Deep-sleep mode: Typical supply current I_{DD} versus temperature for different supply voltages V_{DD}

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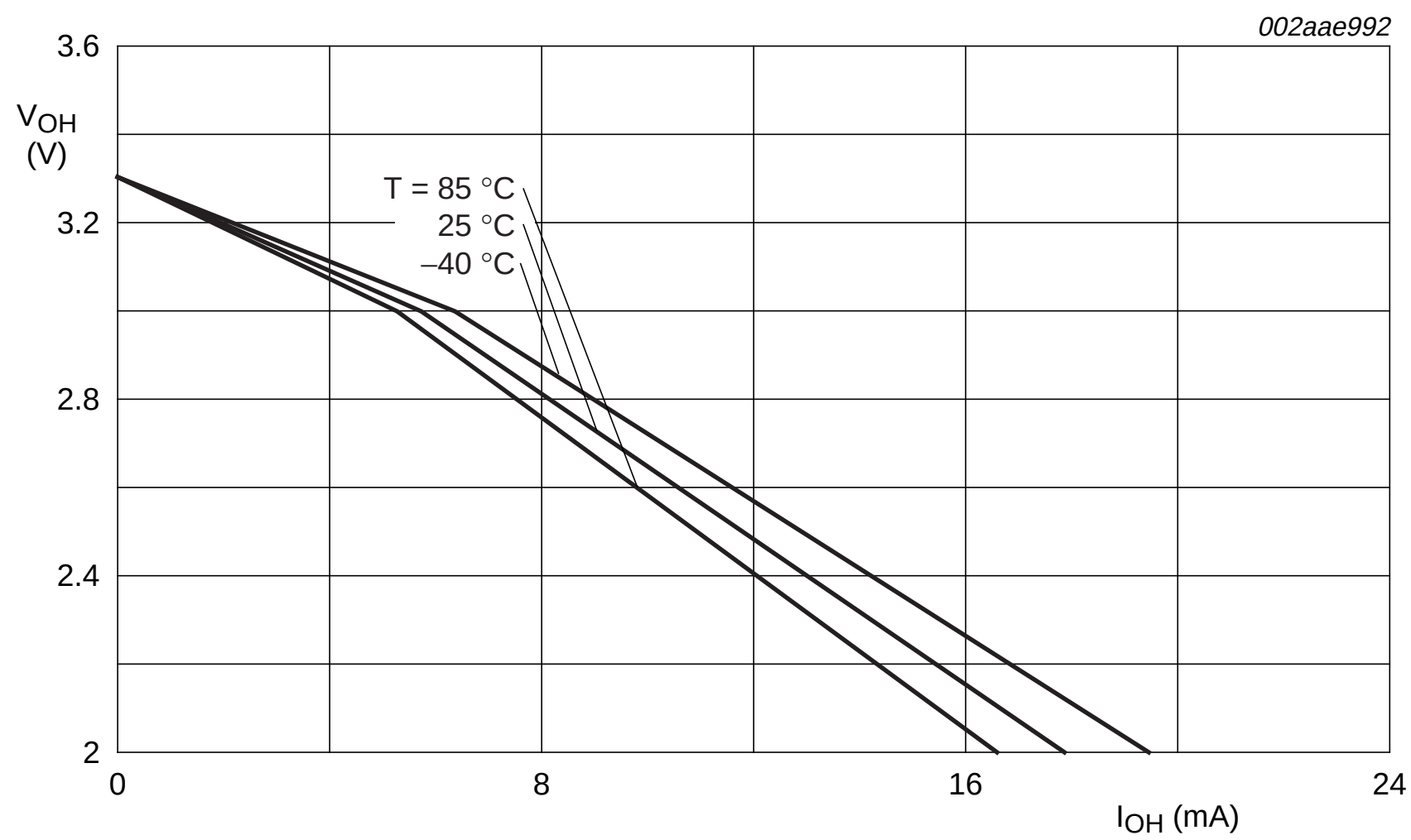
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9.3 Electrical pin characteristics



Conditions: V_{DD} = 3.3 V; standard port pins.

Fig 10. Typical LOW-level output current I_{OL} versus LOW-level output voltage V_{OL}

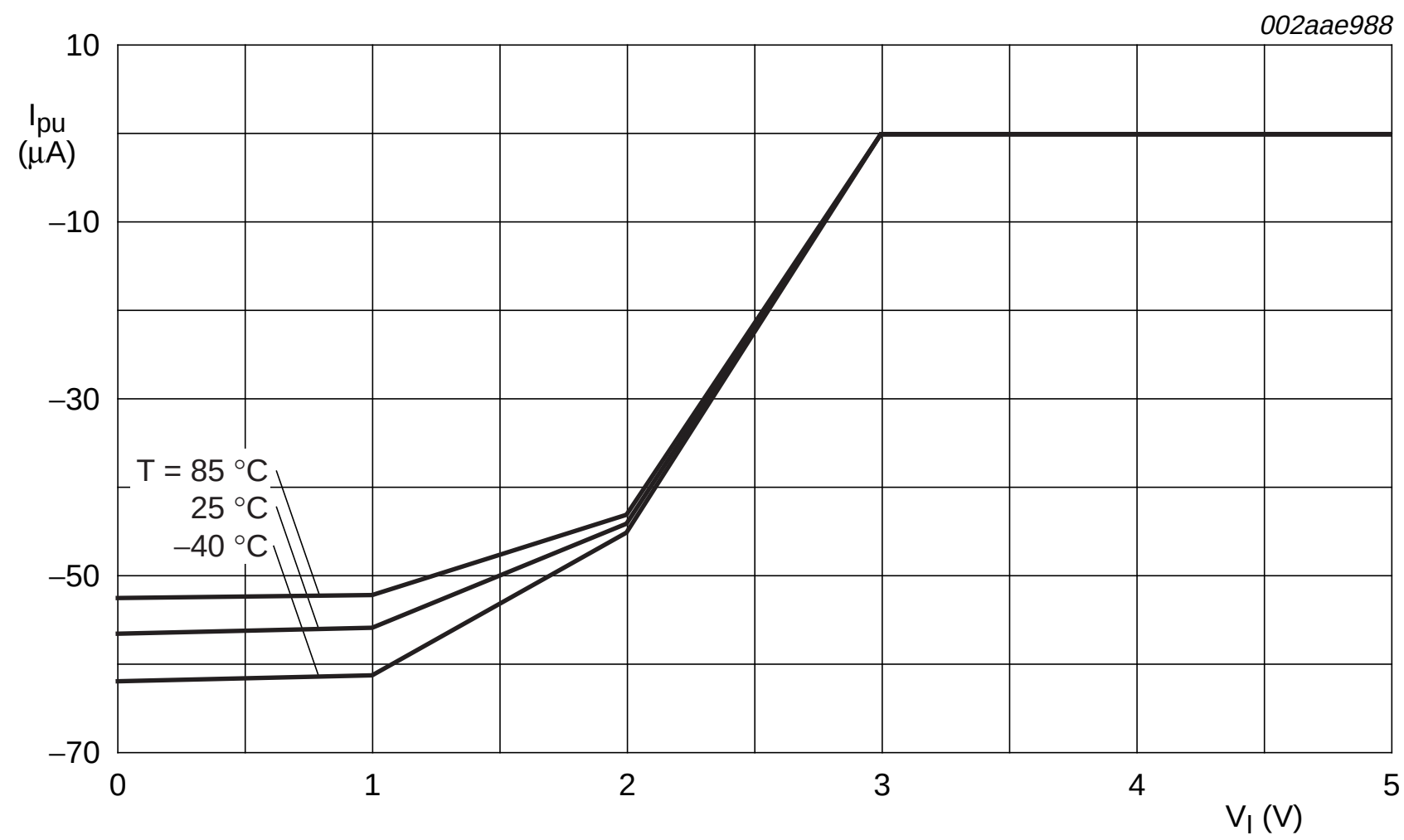


Conditions: V_{DD} = 3.3 V; standard port pins.

Fig 11. Typical HIGH-level output voltage V_{OH} versus HIGH-level output source current I_{OH}

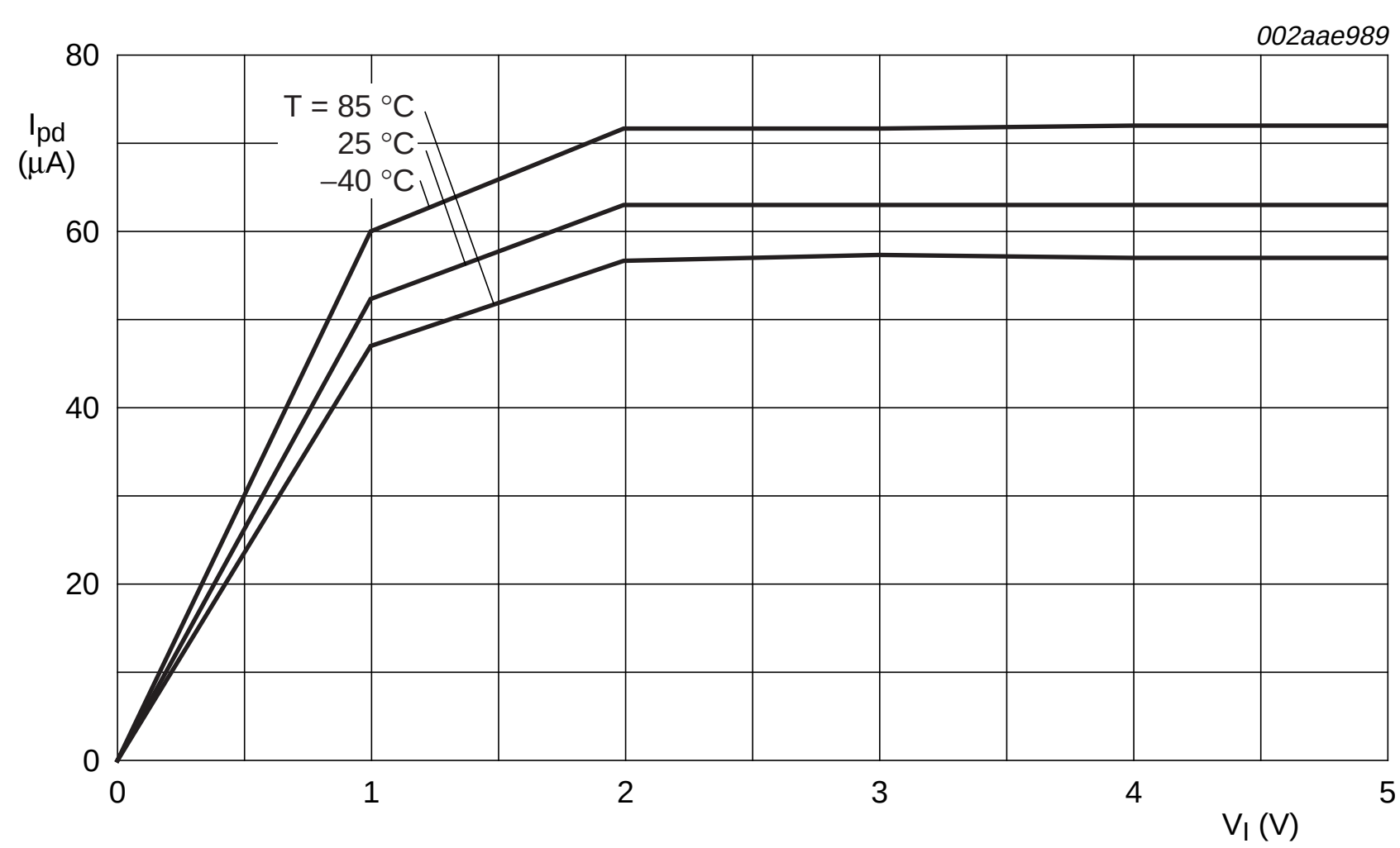
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Conditions: V_{DD} = 3.3 V; standard port pins.

Fig 12. Typical pull-up current I_{pu} versus input voltage V_I



Conditions: V_{DD} = 3.3 V; standard port pins.

Fig 13. Typical pull-down current I_{pd} versus input voltage V_I

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10. Dynamic characteristics

10.1 Flash memory

Table 8. Flash characteristics

T_{amb} = –40 °C to +85 °C, unless otherwise specified.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
N_{endu}	endurance	[1]	10000	-	-	cycles
t_{ret}	retention time	powered	10	-	-	years
		unpowered	20	-	-	years
t_{er}	erase time	sector or multiple consecutive sectors	95	100	105	ms
t_{prog}	programming time	[2]	0.95	1	1.05	ms

[1] Number of program/erase cycles.

[2] Programming times are given for writing 256 bytes from RAM to the flash. Data must be written to the flash in blocks of 256 bytes.

10.2 External clock

Table 9. Dynamic characteristic: external clock

T_{amb} = –40 °C to +85 °C; V_{DD} over specified ranges.[1]

Symbol	Parameter	Conditions	Min	Typ[2]	Max	Unit
f_{osc}	oscillator frequency		1	-	25	MHz
$T_{cy(clk)}$	clock cycle time		40	-	1000	ns
t_{CHCX}	clock HIGH time		$T_{cy(clk)} \times 0.4$	-	-	ns
t_{CLCX}	clock LOW time		$T_{cy(clk)} \times 0.4$	-	-	ns
t_{CLCH}	clock rise time		-	-	5	ns
t_{CHCL}	clock fall time		-	-	5	ns

[1] Parameters are valid over operating temperature range unless otherwise specified.

[2] Typical ratings are not guaranteed. The values listed are at room temperature (25 °C), nominal supply voltages.

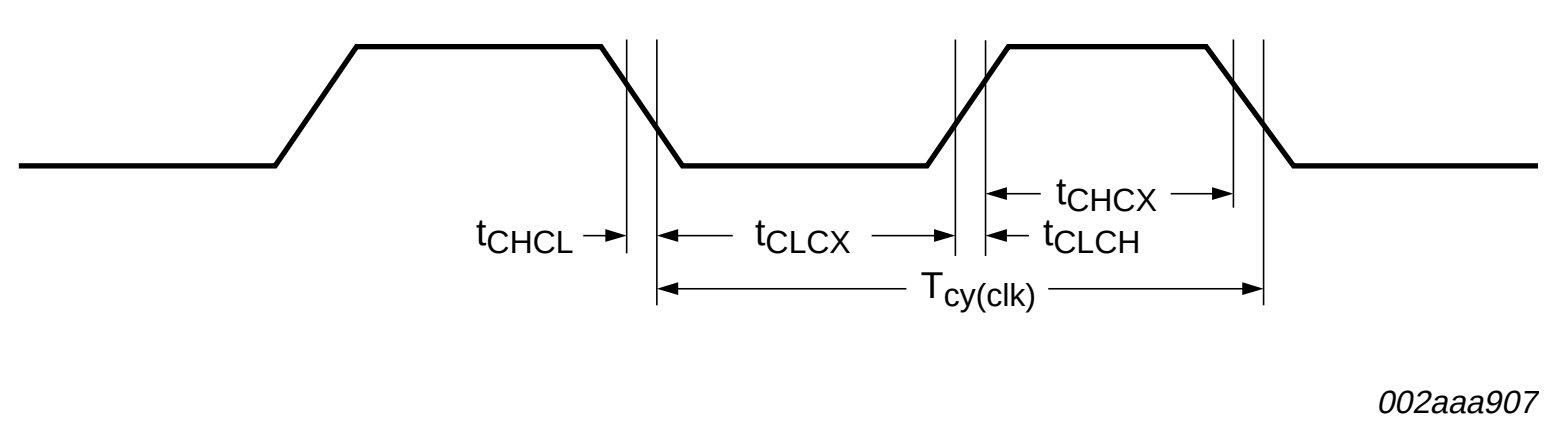


Fig 14. External clock timing (with an amplitude of at least $V_{i(RMS)}$ = 200 mV)

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10.3 Internal oscillators

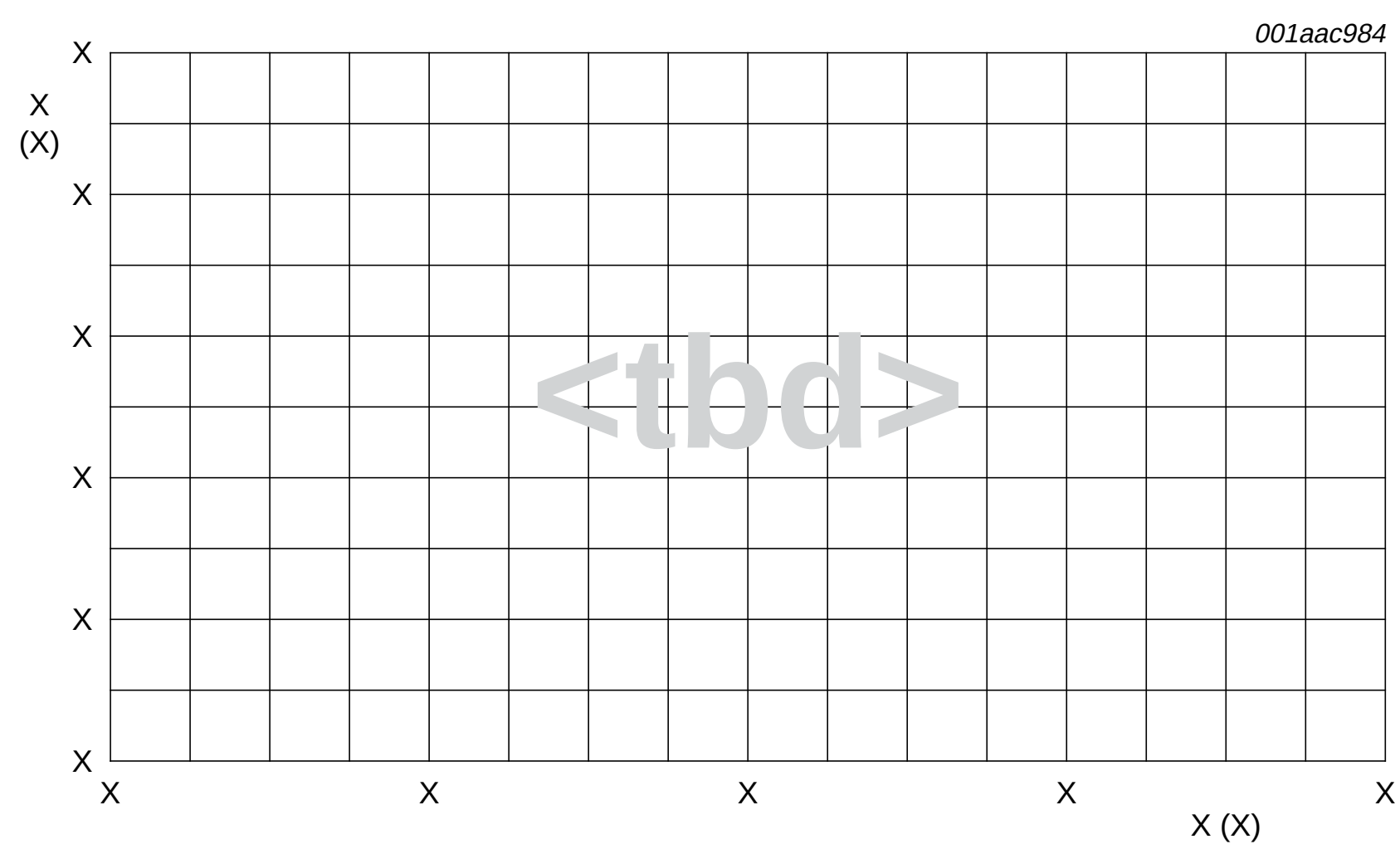
Table 10. Dynamic characteristic: internal oscillators

T_{amb} = –40 °C to +85 °C; 2.7 V ≤ V_{DD} ≤ 3.6 V.[1]

Symbol	Parameter	Conditions	Min	Typ[2]	Max	Unit
$f_{osc(RC)}$	internal RC oscillator frequency	-	11.88	12	12.12	MHz

[1] Parameters are valid over operating temperature range unless otherwise specified.

[2] Typical ratings are not guaranteed. The values listed are at room temperature (25 °C), nominal supply voltages.



Conditions: Frequency values are typical values. 12 MHz ± 1% accuracy is guaranteed for 2.7 V ≤ V_{DD} ≤ 3.6 V and T_{amb} = –40 °C to +85 °C. Variations between parts may cause the IRC to fall outside the 12 MHz ± 1% accuracy specification for voltages below 2.7 V.

Fig 15. Internal RC oscillator frequency vs. temperature

Table 11. Dynamic characteristics: Watchdog oscillator

Symbol	Parameter	Conditions		Min	Typ[1]	Max	Unit
f_{osc}	internal oscillator frequency	DIVSEL = 0x1F, FREQSEL = 0x1 in the WDTOSCCTRL register;	[2][3]	-	7.8	-	kHz
		DIVSEL = 0x00, FREQSEL = 0xF in the WDTOSCCTRL register	[2][3]	-	1700	-	kHz

[1] Typical ratings are not guaranteed. The values listed are at room temperature (25 °C), nominal supply voltages.

[2] The typical frequency spread over processing and temperature (T_{amb} = –40 °C to +85 °C) is ±40%.

[3] See the LPC111x user manual.

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10.4 I/O pins

Table 12. Dynamic characteristic: I/O pins[1]

T_{amb} = –40 °C to +85 °C; 3.0 V ≤ V_{DD} ≤ 3.6 V.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
t_r	rise time	pin configured as output	3.0	-	5.0	ns
t_f	fall time	pin configured as output	2.5	-	5.0	ns

[1] Applies to standard port pins and $\overline{\text{RESET}}$ pin.

10.5 SPI interfaces

Table 13. Dynamic characteristics of SPI pins in SPI mode

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
SPI master (in SPI mode)							
$T_{cy(clk)}$	clock cycle time	when only receiving	[1]	40	-	-	ns
		when only transmitting	[1]	27.8			ns
t_{DS}	data set-up time	in SPI mode 2.4 V ≤ V_{DD} ≤ 3.6 V	[2]	15	-	-	ns
		2.0 V ≤ V_{DD} < 2.4 V	[2]	20			ns
		1.8 V ≤ V_{DD} < 2.0 V	[2]	24	-	-	ns
t_{DH}	data hold time	in SPI mode	[2]	0	-	-	ns
$t_{v(Q)}$	data output valid time	in SPI mode	[2]	-	-	10	ns
$t_{h(Q)}$	data output hold time	in SPI mode	[2]	0	-	-	ns
SPI slave (in SPI mode)							
$T_{cy(PCLK)}$	PCLK cycle time			20	-	-	ns
t_{DS}	data set-up time	in SPI mode	[3][4]	0	-	-	ns
t_{DH}	data hold time	in SPI mode	[3][4]	$3 \times T_{cy(PCLK)} + 4$	-	-	ns
$t_{v(Q)}$	data output valid time	in SPI mode	[3][4]	-	-	$3 \times T_{cy(PCLK)} + 11$	ns
$t_{h(Q)}$	data output hold time	in SPI mode	[3][4]	-	-	$2 \times T_{cy(PCLK)} + 5$	ns

[1] $T_{cy(clk)}$ = (SSPCLKDIV × (1 + SCR) × CPSDVSR) / f_{main}. The clock cycle time derived from the SPI bit rate $T_{cy(clk)}$ is a function of the main clock frequency f_{main}, the SPI peripheral clock divider (SSPCLKDIV), the SPI SCR parameter (specified in the SSP0CR0 register), and the SPI CPSDVSR parameter (specified in the SPI clock prescale register).

[2] T_{amb} = –40 °C to 85 °C.

[3] $T_{cy(clk)} = 12 \times T_{cy(PCLK)}$.

[4] T_{amb} = 25 °C; for normal voltage supply range: V_{DD} = 3.3 V.

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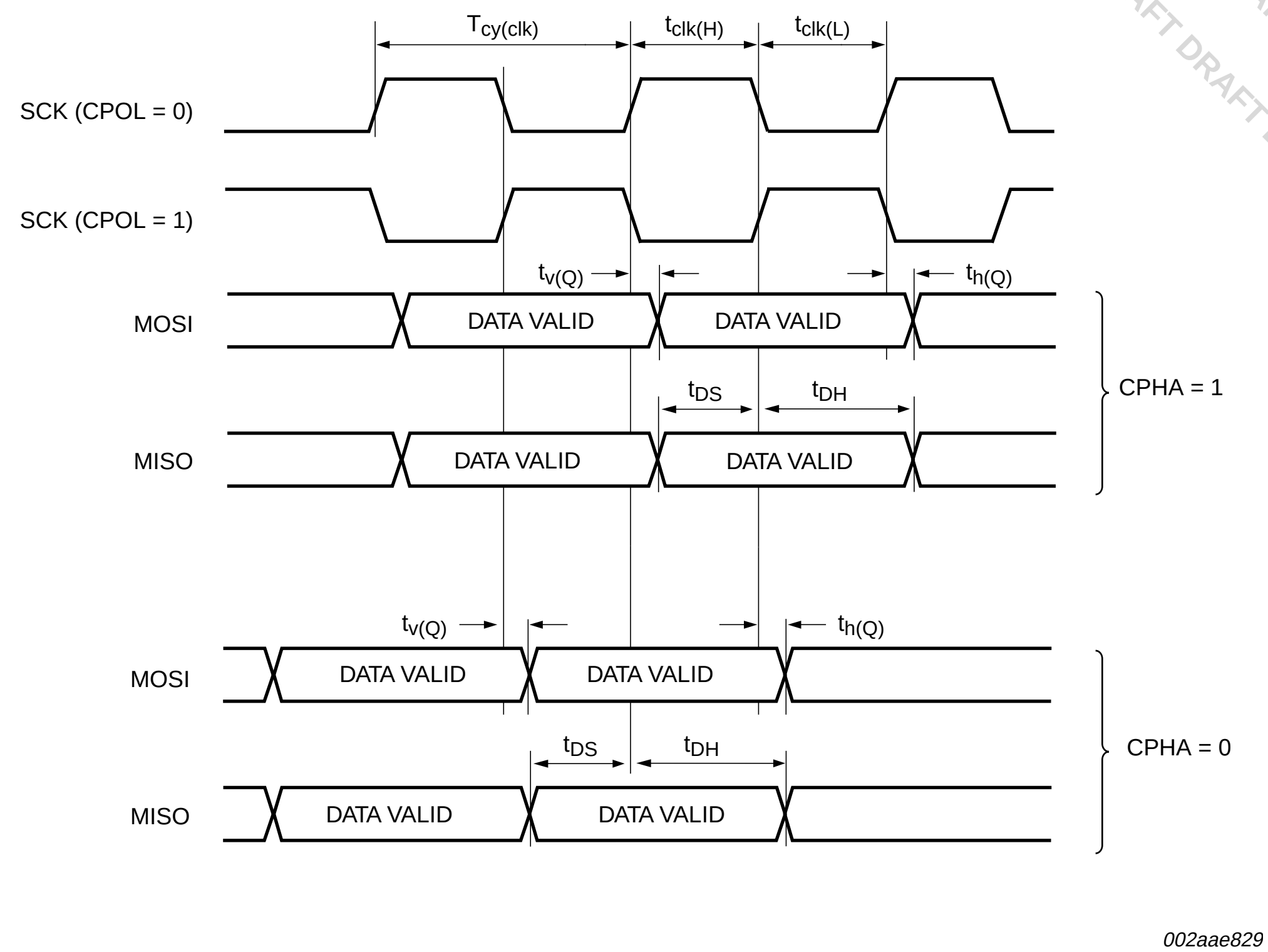


Fig 16. SPI master timing in SPI mode

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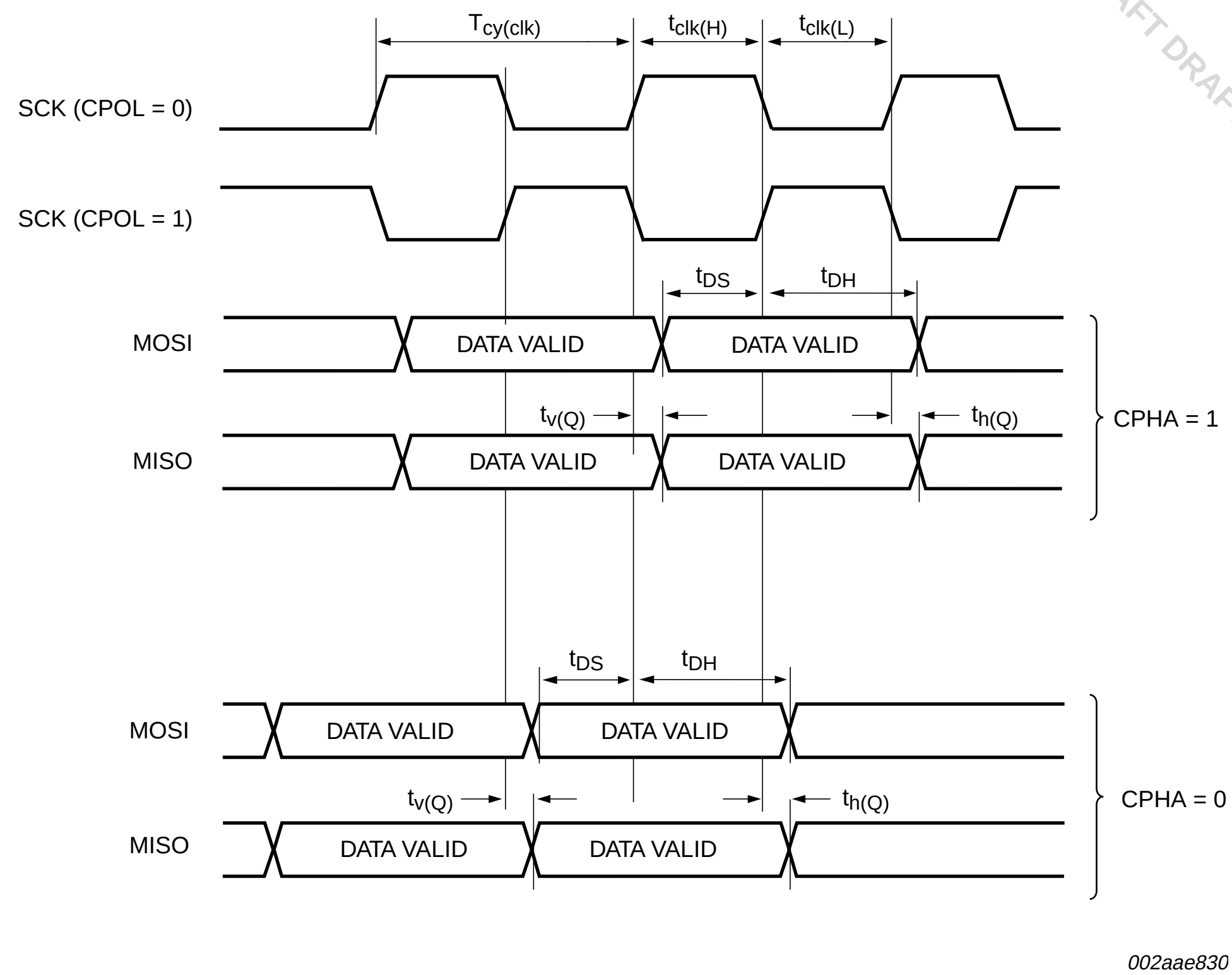


Fig 17. SPI slave timing in SPI mode

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11. Application information

11.1 ADC usage notes

The following guidelines show how to increase the performance of the ADC in a noisy environment beyond the ADC specifications listed in Table 6:

- The ADC input trace must be short and as close as possible to the LPC1102 chip.
- The ADC input traces must be shielded from fast switching digital signals and noisy power supply lines.
- Because the ADC and the digital core share the same power supply, the power supply line must be adequately filtered.
- To improve the ADC performance in a very noisy environment, put the device in Sleep mode during the ADC conversion.

11.2 XTAL input

The input voltage to the on-chip oscillators is limited to 1.8 V. If the oscillator is driven by a clock in slave mode, it is recommended that the input be coupled through a capacitor with C_i = 100 pF. To limit the input voltage to the specified range, choose an additional capacitor to ground C_g which attenuates the input voltage by a factor $C_i/(C_i + C_g)$. In slave mode, a minimum of 200 mV(RMS) is needed.

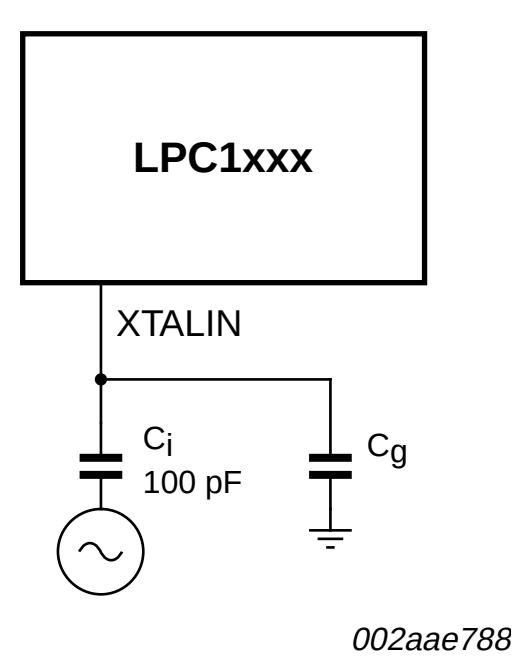


Fig 18. Slave mode operation of the on-chip oscillator

In slave mode the input clock signal should be coupled by means of a capacitor of 100 pF (Figure 18), with an amplitude between 200 mV(RMS) and 1000 mV(RMS). This corresponds to a square wave signal with a signal swing of between 280 mV and 1.4 V.

11.3 Standard I/O pad configuration

Figure 19 shows the possible pin modes for standard I/O pins with analog input function:

- Digital output driver
- Digital input: Pull-up enabled/disabled
- Digital input: Pull-down enabled/disabled
- Digital input: Repeater mode enabled/disabled
- Analog input

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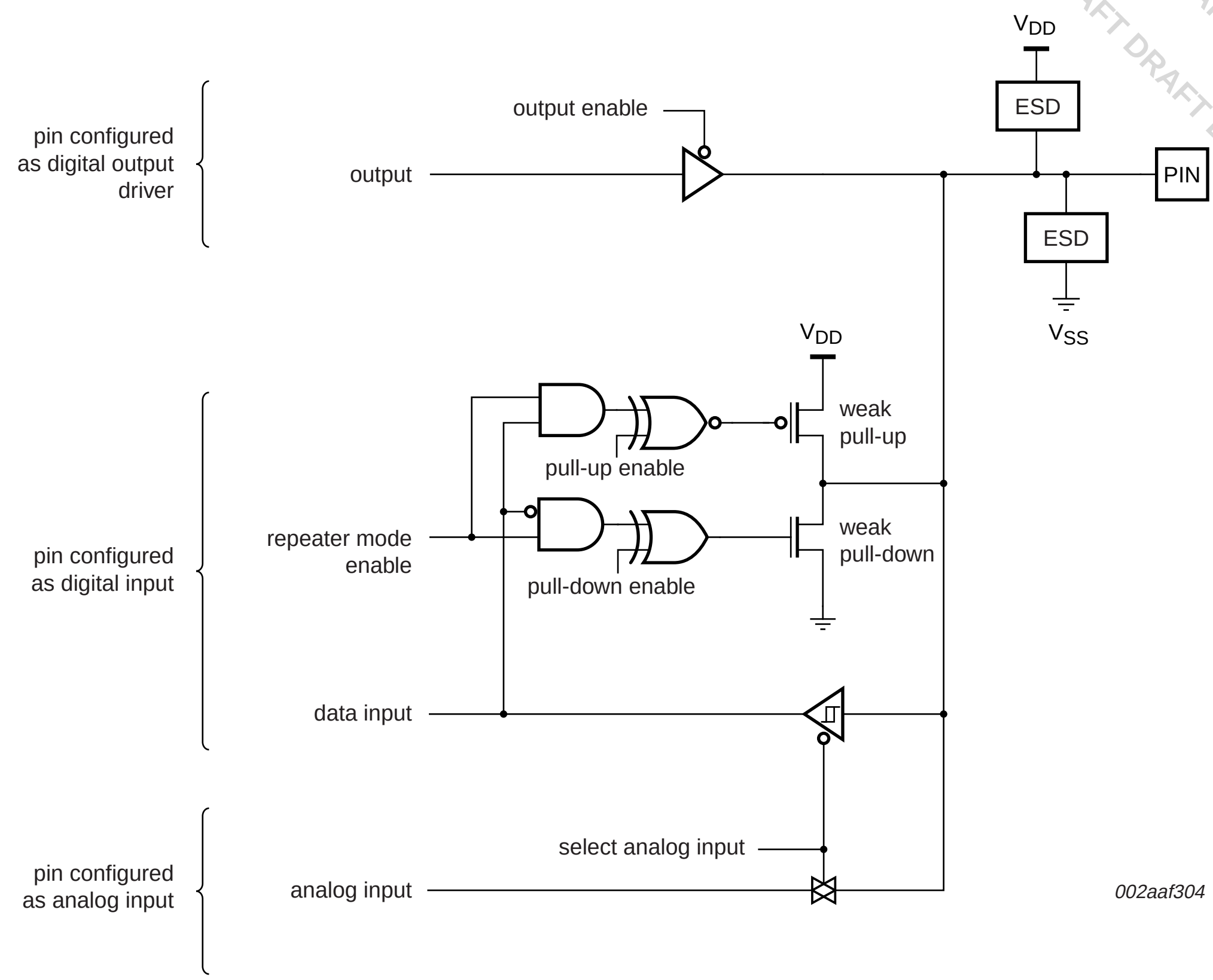


Fig 19. Standard I/O pad configuration

11.4 Reset pad configuration

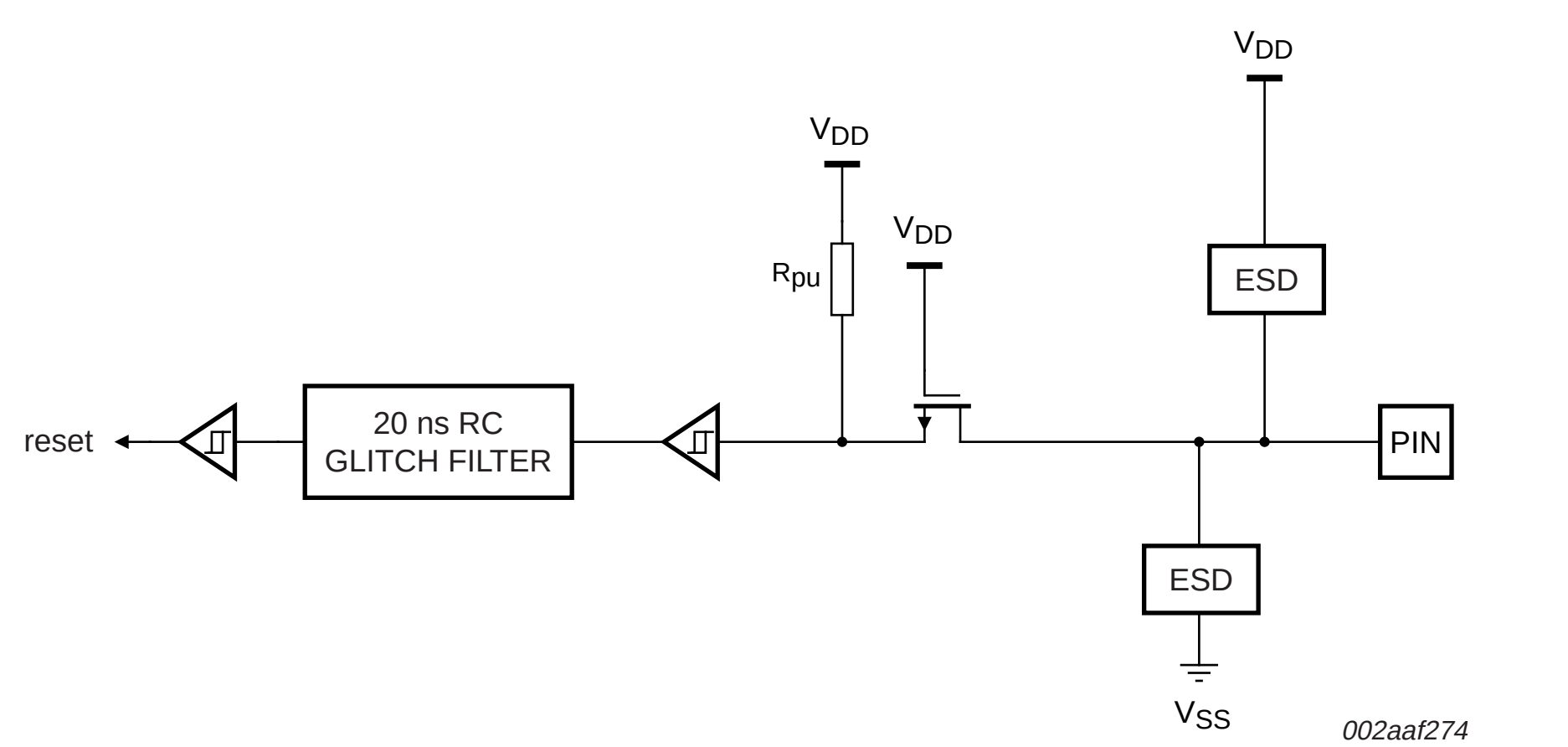


Fig 20. Reset pad configuration

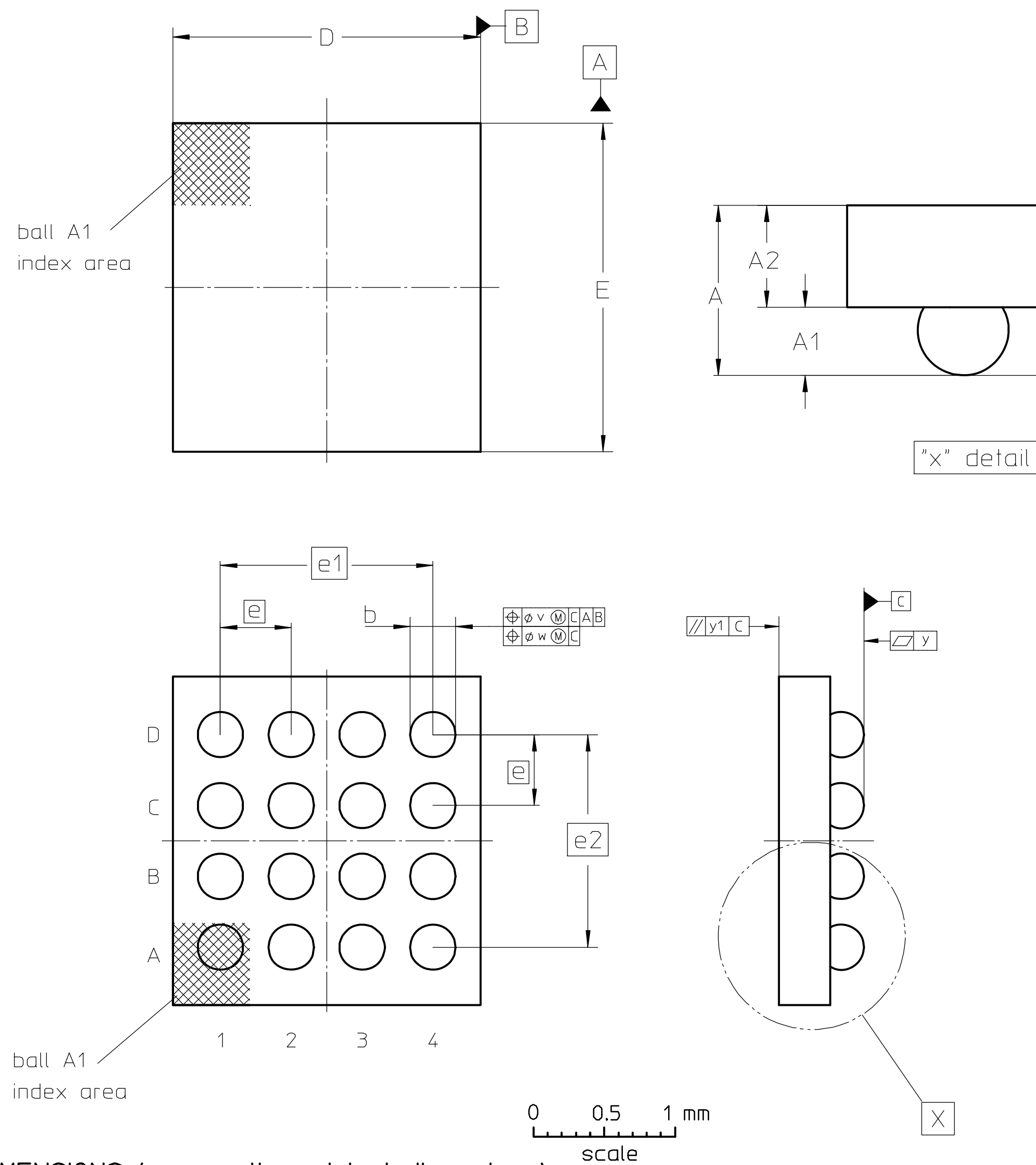
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12. Package outline

WLCSP16: wafer level chip-size package; 16 bumps; 2.17 x 2.32 x 0.6 mm LPC111xL



DIMENSIONS (mm are the original dimensions)

UNIT		A	A_1	A_2	b	D	E	e	e_1	e_2	v	w	y
mm	MAX.	0.65	0.27	0.38	0.35	2.21	2.36	0.5	1.5	2.0	0.15	0.05	0.05
	NOM.	0.60	0.24	0.36	0.32	2.17	2.32						
	MIN.	0.55	0.21	0.34	0.29	2.13	2.28						

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA			
LPC111xL	---	---	---			---

Fig 21. Package outline <tbd> (WLCSP16)

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13. Abbreviations

Table 14. Abbreviations

Acronym	Description
ADC	Analog-to-Digital Converter
AHB	Advanced High-performance Bus
AMBA	Advanced Microcontroller Bus Architecture
APB	Advanced Peripheral Bus
BOD	BrownOut Detection
GPIO	General Purpose Input/Output
PLL	Phase-Locked Loop
RC	Resistor-Capacitor
SPI	Serial Peripheral Interface
SSI	Serial Synchronous Interface
SSP	Synchronous Serial Port
TTL	Transistor-Transistor Logic
UART	Universal Asynchronous Receiver/Transmitter

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14. Revision history

Table 15. Revision history

Document ID	Release date	Data sheet status	Change notice	Supersedes
LPC1102 v. 0.04	<tbd>	Objective data sheet		LPC1102 v. 0.03

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15. Legal information

15.1 Data sheet status

Document status[1][2]	Product status[3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

[1] Please consult the most recently issued document before initiating or completing a design.

[2] The term 'short data sheet' is explained in section "Definitions".

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DRAFT DRAFT DRAFT DRAFT DRAFT

17. Contents

1 General description . . . 1
2 Features and benefits . . . 1
3 Applications . . . 2
4 Ordering information . . . 2
4.1 Ordering options . . . 2
5 Block diagram . . . 3
6 Pinning information . . . 4
6.1 Pinning . . . 4
6.2 Pin description . . . 4
7 Functional description . . . 6
7.1 ARM Cortex-M0 processor . . . 6
7.2 On-chip flash program memory . . . 6
7.3 On-chip SRAM . . . 6
7.4 Memory map . . . 6
7.5 Nested Vectored Interrupt Controller (NVIC) . . 7
7.5.1 Features . . . 7
7.5.2 Interrupt sources . . . 8
7.6 IOCONFIG block . . . 8
7.7 Fast general purpose parallel I/O . . . 8
7.7.1 Features . . . 8
7.8 UART . . . 8
7.8.1 Features . . . 9
7.9 SPI serial I/O controller . . . 9
7.9.1 Features . . . 9
7.10 10-bit ADC . . . 9
7.10.1 Features . . . 9
7.11 General purpose external event counter/timers . . 10
7.11.1 Features . . . 10
7.12 System tick timer . . . 10
7.13 Watchdog timer . . . 10
7.13.1 Features . . . 10
7.14 Clocking and power control . . . 11
7.14.1 Crystal oscillators . . . 11
7.14.1.1 Internal RC oscillator . . . 12
7.14.1.2 Watchdog oscillator . . . 12
7.14.2 System PLL . . . 12
7.14.3 Wake-up process . . . 13
7.14.4 Power control . . . 13
7.14.4.1 Sleep mode . . . 13
7.14.4.2 Deep-sleep mode . . . 13
7.15 System control . . . 14
7.15.1 Reset . . . 14
7.15.2 Brownout detection . . . 14
7.15.3 Code security (Code Read Protection - CRP) 14
7.15.4 APB interface . . . 14
7.15.5 AHBLite . . . 15
7.15.6 External interrupt inputs . . . 15
7.15.7 Memory mapping control . . . 15
7.16 Emulation and debugging . . . 15
8 Limiting values . . . 16
9 Static characteristics . . . 17
9.1 BOD static characteristics . . . 21
9.2 Power consumption . . . 21
9.3 Electrical pin characteristics . . . 24
10 Dynamic characteristics . . . 26
10.1 Flash memory . . . 26
10.2 External clock . . . 26
10.3 Internal oscillators . . . 27
10.4 I/O pins . . . 28
10.5 SPI interfaces . . . 28
11 Application information . . . 31
11.1 ADC usage notes . . . 31
11.2 XTAL input . . . 31
11.3 Standard I/O pad configuration . . . 31
11.4 Reset pad configuration . . . 32
12 Package outline . . . 33
13 Abbreviations . . . 34
14 Revision history . . . 35
15 Legal information . . . 36
15.1 Data sheet status . . . 36
15.2 Definitions . . . 36
15.3 Disclaimers . . . 36
15.4 Trademarks . . . 37
16 Contact information . . . 37
17 Contents . . . 38

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Date of release: 23 June 2010
Document identifier: LPC1102