TLV704 24V、150mA、3.2μA 静态电流、低压降线性稳压器

1 特性

- 输入电压范围：
  - 2.5V 至 24V（仅新芯片最大电压为 30V）
- 可配置的输出电压选项：
  - 固定：1.8V、3V、3.3V、3.6V 和 5V
- 输出电流：高达 150 mA
- 超低 I_Q：100mA 负载电流下为 3.4 μA
- 与 ≥ 0.47 μF 的输出电容器一起工作时可保持稳定
- 过流保护
- 封装：5 引脚 SOT-23 (DBV)
- 工作结温：–40°C 至 +125°C

2 应用

- 家庭和楼宇自动化
- 零售自动化和支付
- 电网基础设施
- 医疗应用
- 照明应用

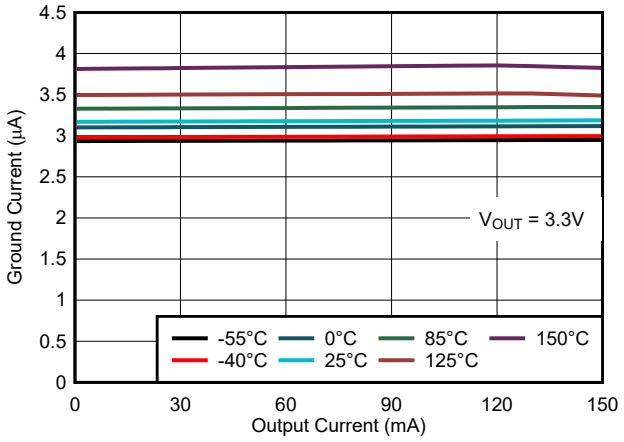


图 3-1. TLV704xx 的静态电流与负载电流（仅限新芯片）

3 说明

TLV704 低压降 (LDO) 线性稳压器是低静态电流器件，可提供采用微型封装、具有宽输入电压范围和实现低功耗运行的优势。因此，TLV704 专为电池供电型应用而设计，可用作低功耗微控制器的电源管理附件。

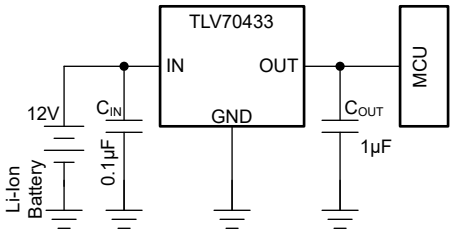
TLV704 LDO 在 100mA 负载电流下支持典型值为 850mV 的低压降。低静态电流（典型值为 3.4μA）在整个输出负载电流（0mA 至 150 mA）范围内都是稳定的。TLV704 还具有内部软启动功能，可降低浪涌电流。内置过流限制保护有助于在发生负载短路或故障时保护稳压器。

TLV704 采用 2.90mm × 1.60mm SOT23-5 封装，对于具有成本效益的电路板很有用。

封装信息(1)

器件型号	封装	封装尺寸（标称值）
TLV704	DBV（SOT-23，5）	2.90mm × 1.60mm

(1) 如需了解所有可用封装，请参阅数据表末尾的可订购产品附录。



典型应用

本文档旨在为方便起见，提供有关 TI 产品中文版本的信息，以确认产品的概要。有关适用的官方英文版本的最新信息，请访问 www.ti.com，其内容始终优先。TI 不保证翻译的准确性和有效性。在实际设计之前，请务必参考最新版本的英文版本。

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4 Revision History

注：以前版本的页码可能与当前版本的页码不同

Changes from Revision D (January 2015) to Revision E (December 2022)	Page
• 更改了文档标题、*特性*、*应用* 和 *说明* 部分，并在文档中添加了 M3 器件信息	1
• Changed *Pin Configuration and Functions* section	4
• Added new chip specific curves to *Typical Characteristics* section	8
• Changed *Overview* section	13
• Changed *Functional Block Diagram* image	13
• Changed *Feature Description* section	13
• Deleted thermal shutdown discussion from *Current Limit* section	14
• Changed *Normal Operation* section	15
• Changed *Dropout Operation* section	15
• Changed *Application Information* section	16
• Added *External Capacitor Requirements*, *Reverse Current*, and *Power Dissipation* sub-sections to *Detailed Design Procedure* section	16
• Changed *Input and Output Capacitor Requirements* section	16
• Added *Reverse Current* section	17
• Changed *Estimating Junction Temperature* section	18
• Added *Best Design Practices* section	18
• Changed *Power Supply Recommendations* section	19
• Changed *Layout Guidelines* section	19
• Changed *Power Dissipation* section: changed title and deleted last sentence from section	19
• Added M3 row to *Available Options* table	20

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Changes from Revision C (August 2011) to Revision D (January 2015) **Page**

- 新增了 *ESD 等级* 表、*特性说明* 部分、*器件功能模式*、*应用和实现* 部分、*电源相关建议* 部分、*布局* 部分、*器件和文档支持* 部分以及*机械、封装和可订购信息* 部分 1
- 更改了“特性”列表中的第四个项目符号 1
- 更改了首页图片；删除了引脚排列 1
- Changed *Pin Configuration and Functions* section; updated table format, renamed pin package to meet new standards 4

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5 Pin Configuration and Functions

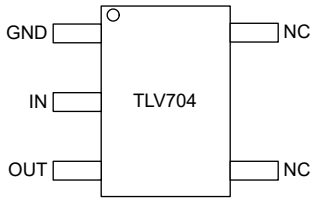

图 5-1. DBV Package, 5-Pin SOT-23 (Top View)

表 5-1. Pin Functions

PIN		TYPE	DESCRIPTION
NAME	DBV		
GND	1	—	Ground pin.
IN	2	I	Input supply pin. A capacitor with a value of 0.1 µF or larger is recommended from this pin to ground. See the *Input and Output Capacitor Requirements* section for more information.
OUT	3	O	Output of the regulator. A capacitor with a value of 1 µF or larger is required from this pin to ground.(1) See the *Input and Output Capacitor Requirements* section for more information.
NC	4, 5	—	Not internally connected. This pin can be left open or tied to ground for improved thermal performance.

(1) The nominal output capacitance must be greater than 0.47 µF. Throughout this document, the nominal derating on these capacitors is 50%. Make sure that the effective capacitance at the pin is greater than 0.47 µF.

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6 Specifications

6.1 Absolute Maximum Ratings

over operating temperature range (unless otherwise noted)(1) (2)

		MIN	MAX	UNIT
Voltage	V_{IN} (for legacy chip only)	–0.3	24	V
	V_{IN} (for new chip only)	–0.3	30	
	V_{OUT} (for legacy chip only)	–0.3	16.5	
	V_{OUT} (for fixed output new chip only)	–0.3	2 X $V_{OUT(typ)}$ or V_{IN} + 0.3V or 5.5V (whichever is lower)	
Current	Peak output current	Internally limited		
Temperature	Junction, T_J	–40	150	°C
	Storage, T_{stg}	–65	150	

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) All voltage values are with respect to network ground terminal.

6.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human body model (HBM), per ANSI/ESDA/JEDEC JS-001, all pins(1)	±2000	V
		Charged device model (CDM), per JEDEC specification JESD22-C101, all pins(2)	±500	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

6.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)(1)

		MIN	NOM	MAX	UNIT
V_{IN}	Input supply voltage	2.5		24	V
V_{OUT}	Output voltage	1.205		15	
I_{OUT}	Output current	0		50	mA
C_{IN}	Input capacitor(2)	0	0.047		μF
C_{OUT}	Output capacitor (for legacy chip only)	0.47	1		
	Output capacitor (for new chip only) (3)	1			
T_J	Operating junction temperature	-40		125	°C

(1) All voltages are with respect to GND.
(2) An input capacitor is not required for LDO stability. However, an input capacitor with an effective value of 0.047 μF is recommended to counteract the effect of source resistance and inductance, which may in some cases cause symptoms of system level instability such as ringing or oscillation, especially in the presence of load transients.
(3) All capacitor values are assumed to derate to 50% of the nominal capacitor value. Maintain an effective output capacitance of 0.47 μF minimum for the stability.

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6.4 Thermal Information

THERMAL METRIC(1)		Legacy Chip DBV (SOT-23) 5 PINS	New Chip DBV (SOT-23) 5 PINS	UNIT
$R_{\theta JA}$	Junction-to-ambient thermal resistance	213.1	170.8	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	110.9	68.7	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	97.4	76.7	°C/W
ψ_{JT}	Junction-to-top characterization parameter	22.0	10.3	°C/W
ψ_{JB}	Junction-to-board characterization parameter	78.4	76.3	°C/W

(1) For more information about traditional and new thermal metrics, see the Semiconductor and IC package thermal metrics application report.

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6.5 Electrical Characteristics

over operating junction temperature range (T_J = –40°C to 125°C), V_{IN} = $V_{OUT(nom)}$ + 1 V, I_{OUT} = 1 mA, and C_{OUT} = 1 µF (unless otherwise noted); typical values are at T_J = 25°C

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
V_{IN}	Input voltage range (1)	T_J = 25°C			24	V
V_{OUT}	Output voltage range (1)	T_J = 25°C	1.2		5	V
V_{OUT}	DC output accuracy(1)	T_J = 25°C	–2		2	%
I_{GND}	Ground pin current (legacy chip) (2)	I_{OUT} = 0 mA, T_J = 25°C		3.2	4.5	µA
		I_{OUT} = 100 mA, T_J = 25°C		3.2	5.5	
	Ground pin current (new chip) (2)	I_{OUT} = 0 mA, T_J = 25°C		3.2	4.1	
		I_{OUT} = 100 mA, T_J = 25°C		3.4	4.5	
ΔV_{OUT} (ΔIOUT)	Load regulation	V_{OUT} < 3.3V, 0 < I_{OUT} < 10 mA , T_J = 25°C		10		mV
		V_{OUT} < 3.3V, 0 < I_{OUT} < 50 mA , T_J = 25°C		25		
		V_{OUT} < 3.3V, 0 < I_{OUT} < 100 mA , T_J = 25°C		33	50	
		V_{OUT} ≥ 3.3 V, 0 < I_{OUT} < 10 mA , T_J = 25°C		7		
		V_{OUT} ≥ 3.3 V, 0 < I_{OUT} < 50 mA , T_J = 25°C		35		
		V_{OUT} ≥ 3.3 V, 0 < I_{OUT} < 100 mA , T_J = 25°C		50	75	
ΔV_{OUT} (ΔVIN)	Line regulation (1)	$V_{OUT(NOM)}$ + 1 V ≤ V_{IN} ≤ 24 V , T_J = 25°C		20	50	mV
I_{CL}	Output current limit (legacy chip)	V_{OUT} = 0 V , T_J = 25°C	160		1000	mA
	Output current limit (new chip)		160		500	
PSRR	Power-supply ripple rejection	f = 100 kHz, C_{OUT} = 10 µF		60		dB
V_{DO}	Dropout voltage	V_{IN} = $V_{OUT(nom)}$ – 0.1 V, I_{OUT} = 10 mA , T_J = 25°C		75		mV
		V_{IN} = $V_{OUT(nom)}$ – 0.1 V, I_{OUT} = 50 mA , T_J = 25°C		400		
		V_{IN} = $V_{OUT(nom)}$ – 0.1 V, I_{OUT} = 100 mA , T_J = 25°C		850	1100	
T_J	Operating junction temperature		–40		125	℃

(1) Minimum V_{IN} = V_{OUT} + V_{DO} or the value shown for *Input voltage* in this table, whichever is greater.
(2) This device employs a leakage null control circuit. This circuit is active only if output current is less than pass FET leakage current. The circuit is typically active when output load is less than 5 µA, V_{IN} is greater than 18 V, and die temperature is greater than 100°C.

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6.6 Typical Characteristics

at operating temperature T_J = 25°C, V_{IN} = $V_{OUT(NOM)}$ + 1.0 V or 2.5 V (whichever is greater), I_{OUT} = 1 mA, C_{IN} = 1 µF, and C_{OUT} = 1 µF (unless otherwise noted)

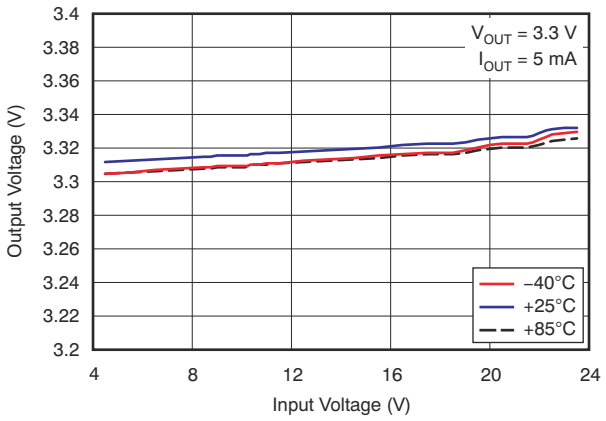

图 6-1. Line Regulation for Legacy Chip

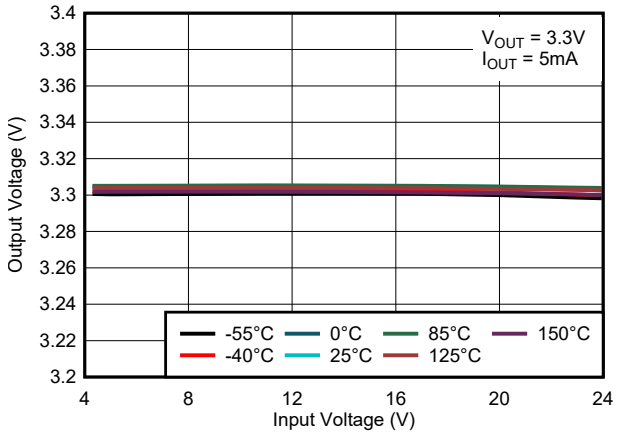

图 6-2. Line Regulation for New Chip

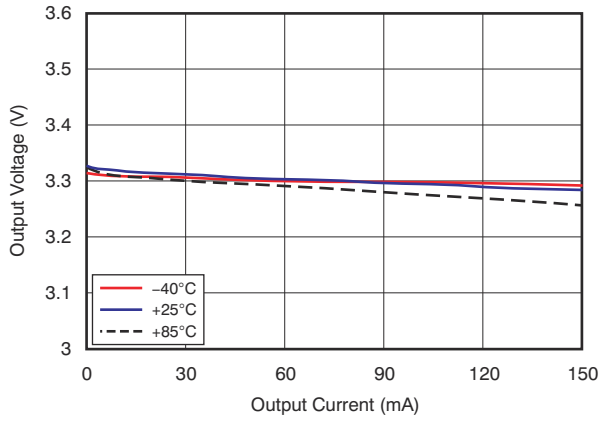

图 6-3. Load Regulation (V_{OUT} = 3.3 V) for Legacy Chip

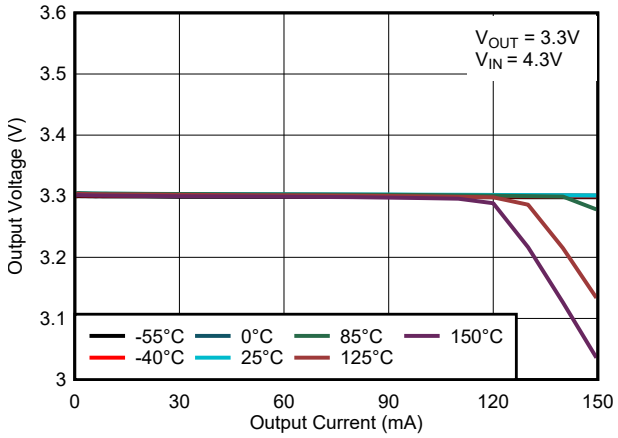

图 6-4. Load Regulation (V_{OUT} = 3.3 V) for New Chip

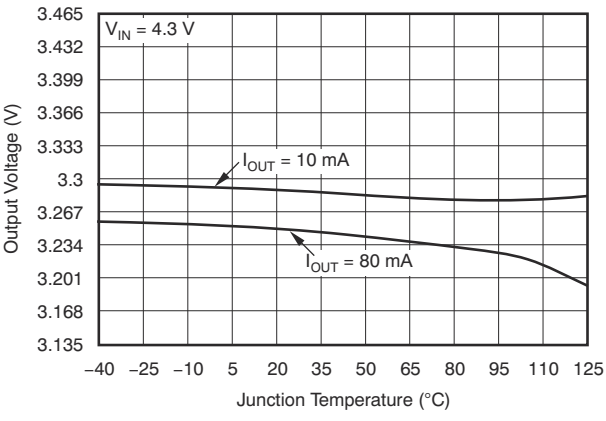

图 6-5. Output Voltage vs Junction Temperature for Legacy Chip

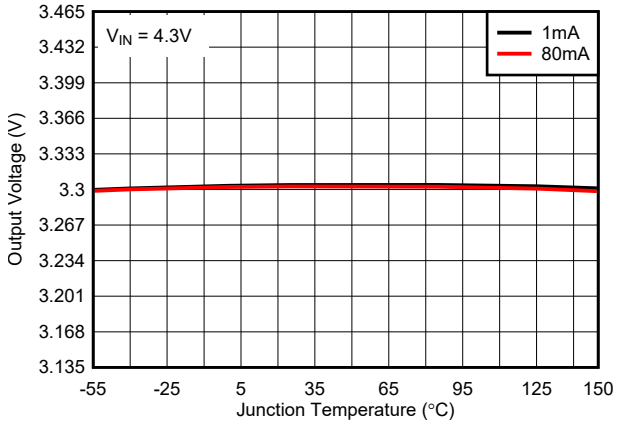

图 6-6. Output Voltage vs Junction Temperature for New Chip

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6.6 Typical Characteristics (continued)

at operating temperature T_J = 25°C, V_{IN} = $V_{OUT(NOM)}$ + 1.0 V or 2.5 V (whichever is greater), I_{OUT} = 1 mA, C_{IN} = 1 µF, and C_{OUT} = 1 µF (unless otherwise noted)

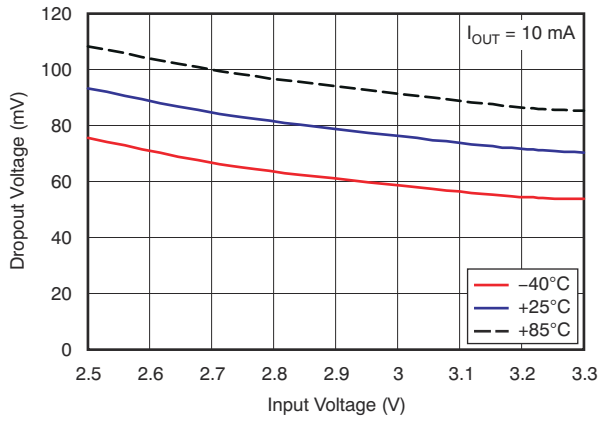

图 6-7. Dropout Voltage vs Input Voltage (TLV70433) for Legacy Chip

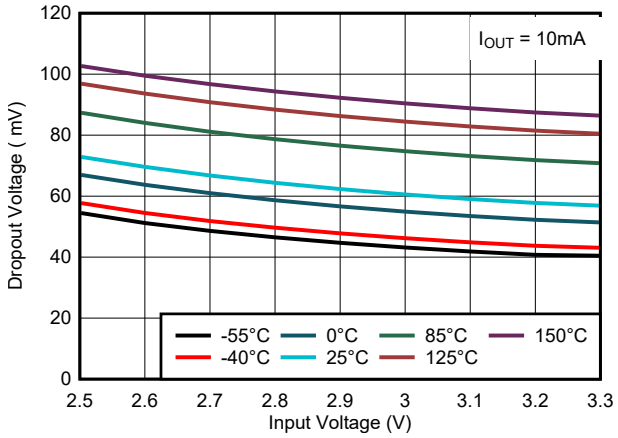

图 6-8. Dropout Voltage vs Input Voltage (TLV70433) for New Chip

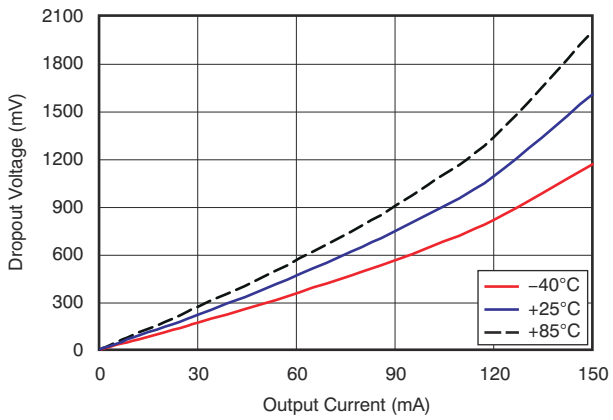

图 6-9. Dropout Voltage vs Output Current for Legacy Chip

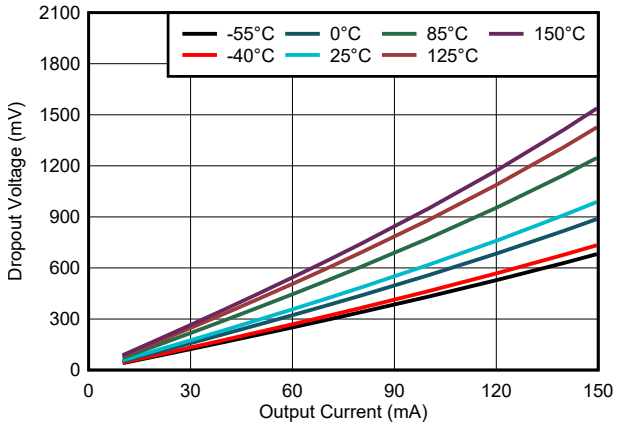

图 6-10. Dropout Voltage vs Output Current for New Chip

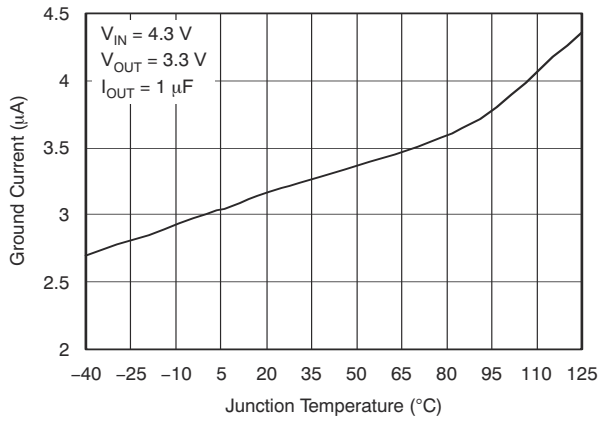

图 6-11. Ground Current vs Junction Temperature for Legacy Chip

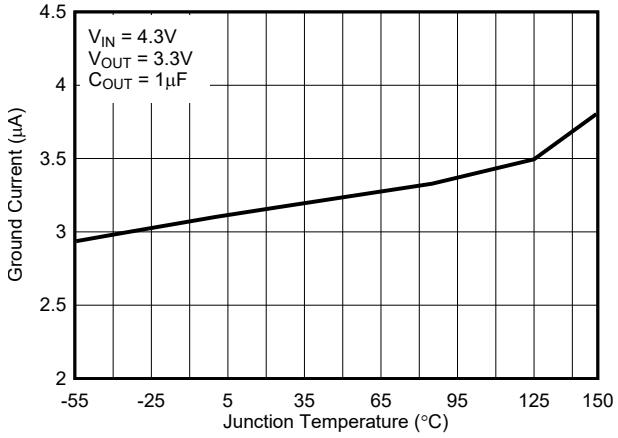

图 6-12. Ground Current vs Junction Temperature for New Chip

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6.6 Typical Characteristics (continued)

at operating temperature T_J = 25°C, V_{IN} = $V_{OUT(NOM)}$ + 1.0 V or 2.5 V (whichever is greater), I_{OUT} = 1 mA, C_{IN} = 1 µF, and C_{OUT} = 1 µF (unless otherwise noted)

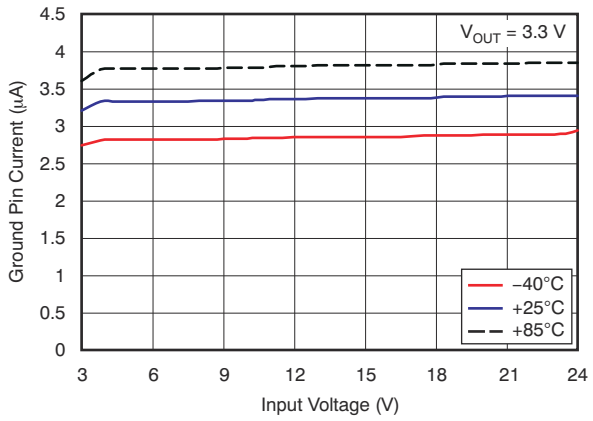

图 6-13. Ground Pin Current vs Input Voltage for Legacy Chip

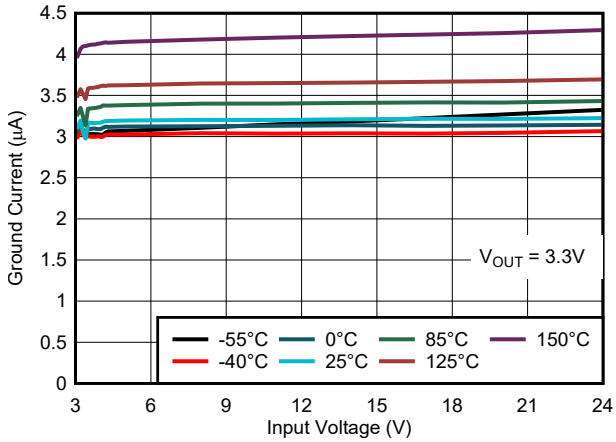

图 6-14. Ground Pin Current vs Input Voltage for New Chip

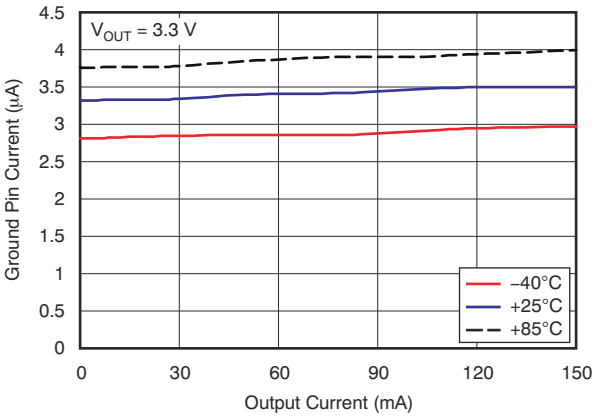

图 6-15. Ground Pin Current vs Load Current for Legacy Chip

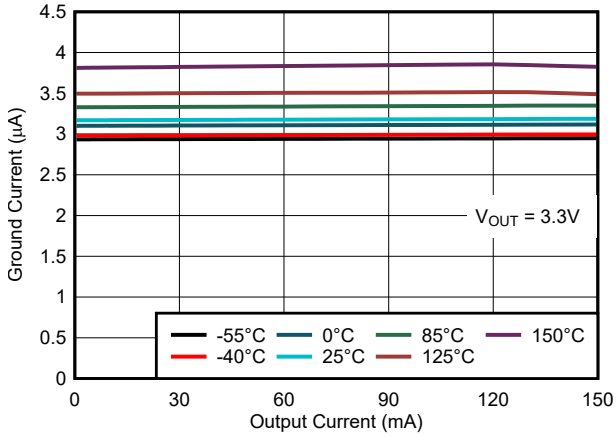

图 6-16. Ground Pin Current vs Load Current for New Chip

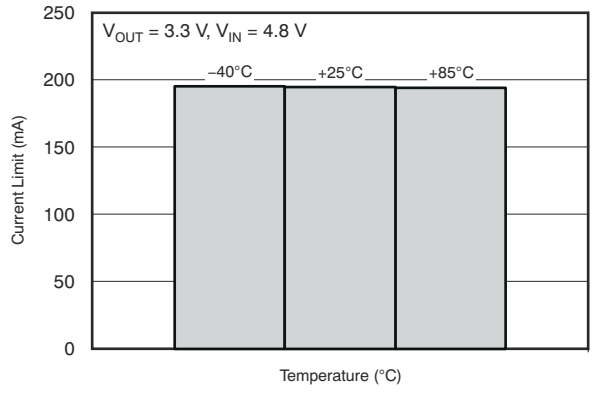

图 6-17. Current Limit vs Junction Temperature for Legacy Chip

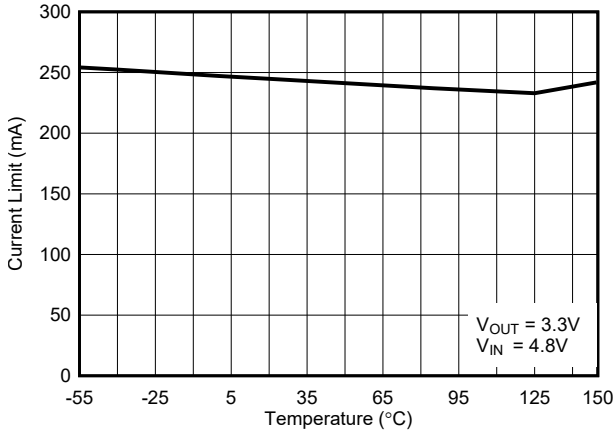

图 6-18. Current Limit vs Junction Temperature for New Chip

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6.6 Typical Characteristics (continued)

at operating temperature T_J = 25°C, V_{IN} = $V_{OUT(NOM)}$ + 1.0 V or 2.5 V (whichever is greater), I_{OUT} = 1 mA, C_{IN} = 1 µF, and C_{OUT} = 1 µF (unless otherwise noted)

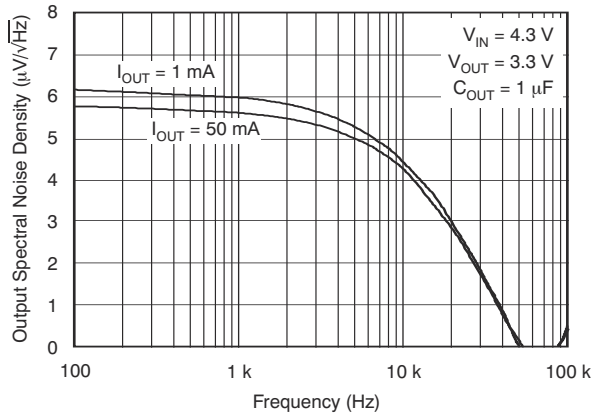

图 6-19. Output Spectral Noise Density vs Frequency for Legacy Chip

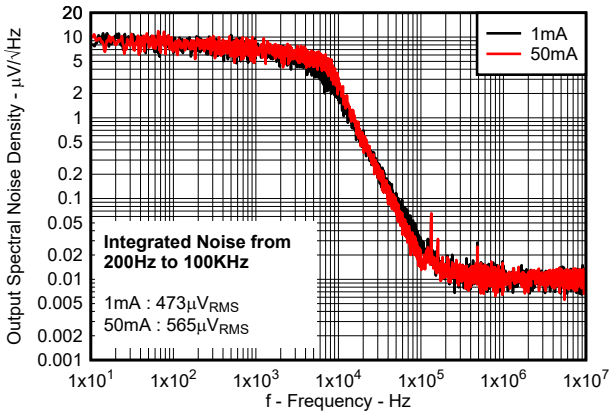

图 6-20. Output Spectral Noise Density vs Frequency for New Chip

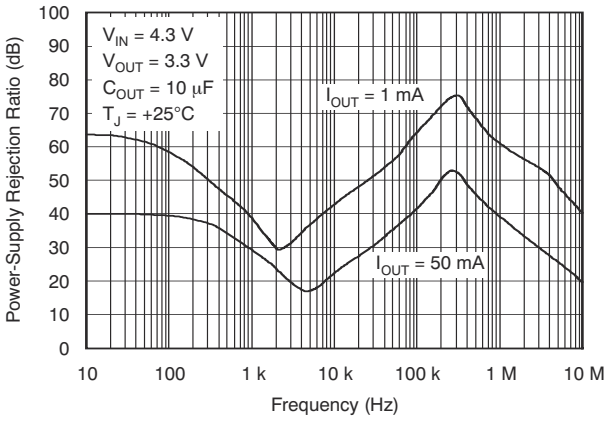

图 6-21. Power-Supply Ripple Rejection vs Frequency for Legacy Chip

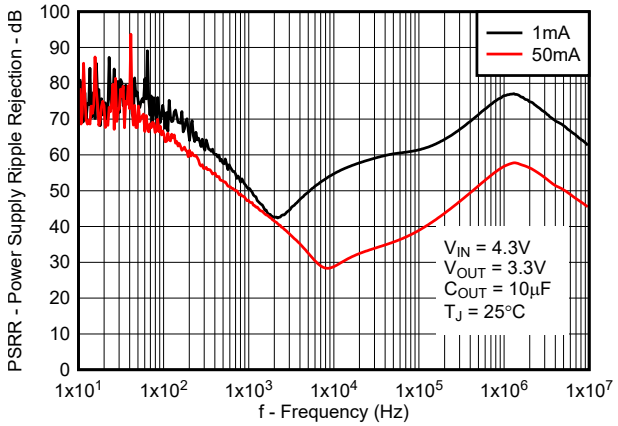

图 6-22. Power-Supply Ripple Rejection vs Frequency for New Chip

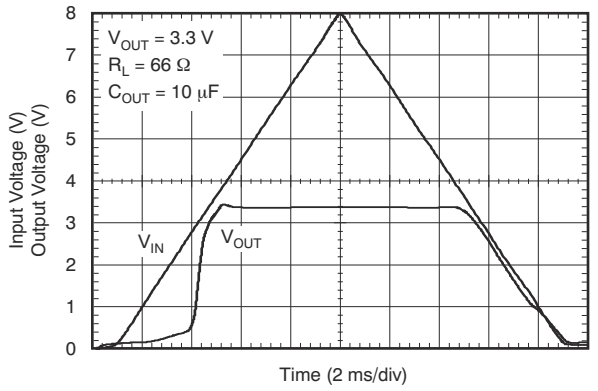

图 6-23. Power Up, Power Down for Legacy Chip

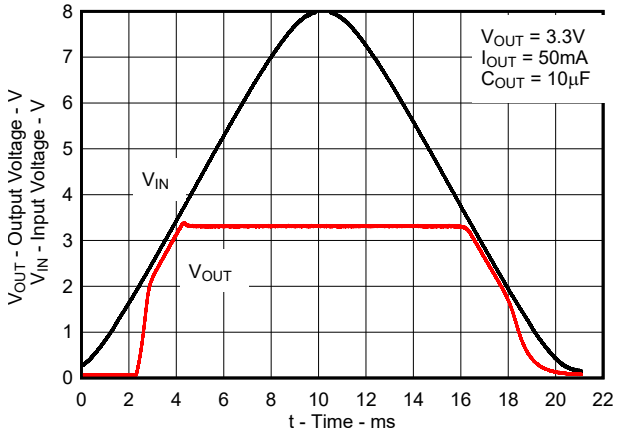

图 6-24. Power Up, Power Down for New Chip

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6.6 Typical Characteristics (continued)

at operating temperature T_J = 25°C, V_{IN} = $V_{OUT(NOM)}$ + 1.0 V or 2.5 V (whichever is greater), I_{OUT} = 1 mA, C_{IN} = 1 µF, and C_{OUT} = 1 µF (unless otherwise noted)

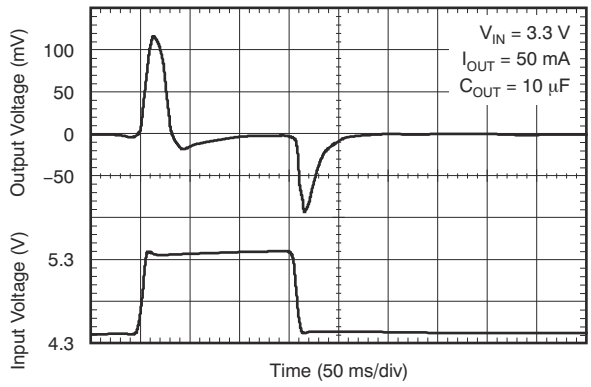

图 6-25. Line Transient Response for Legacy Chip

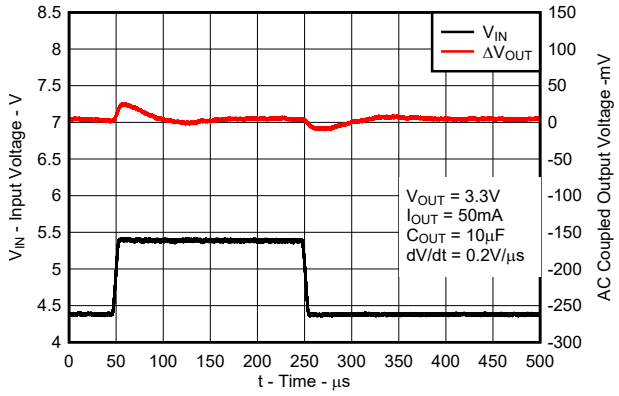

图 6-26. Line Transient Response for New Chip

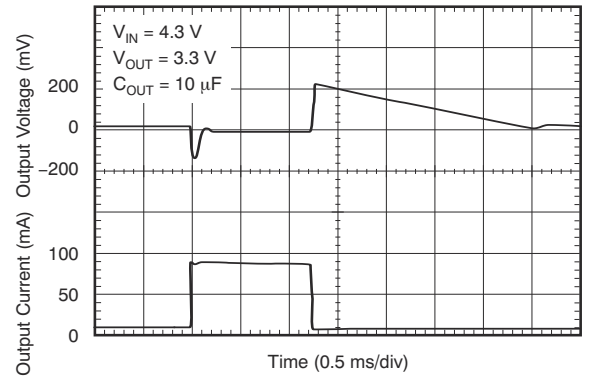

图 6-27. Load Transient Response for Legacy Chip

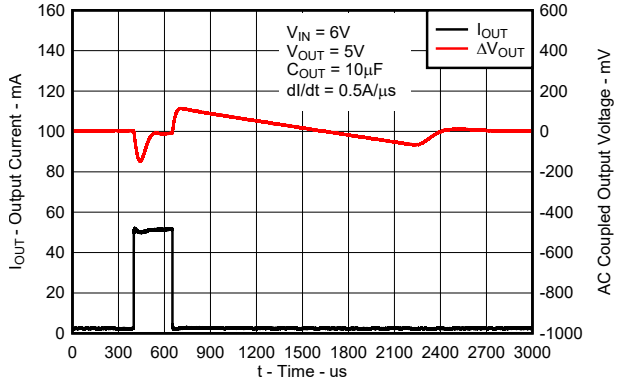

图 6-28. Load Transient Response for New Chip

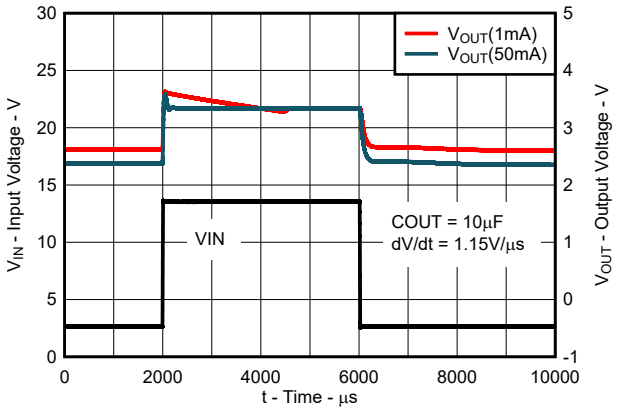

图 6-29. Line Transient Response for New Chip

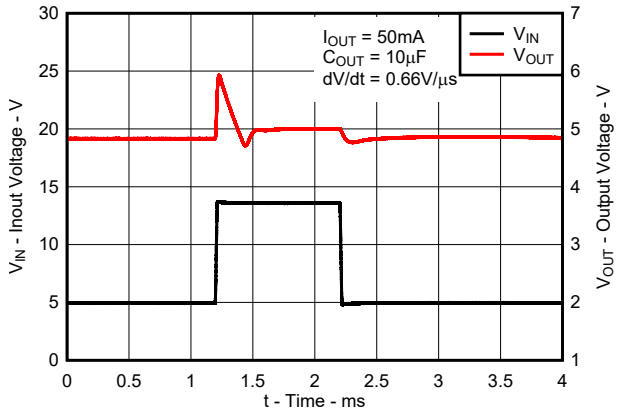

图 6-30. Dropout Exit Transient Response for New Chip

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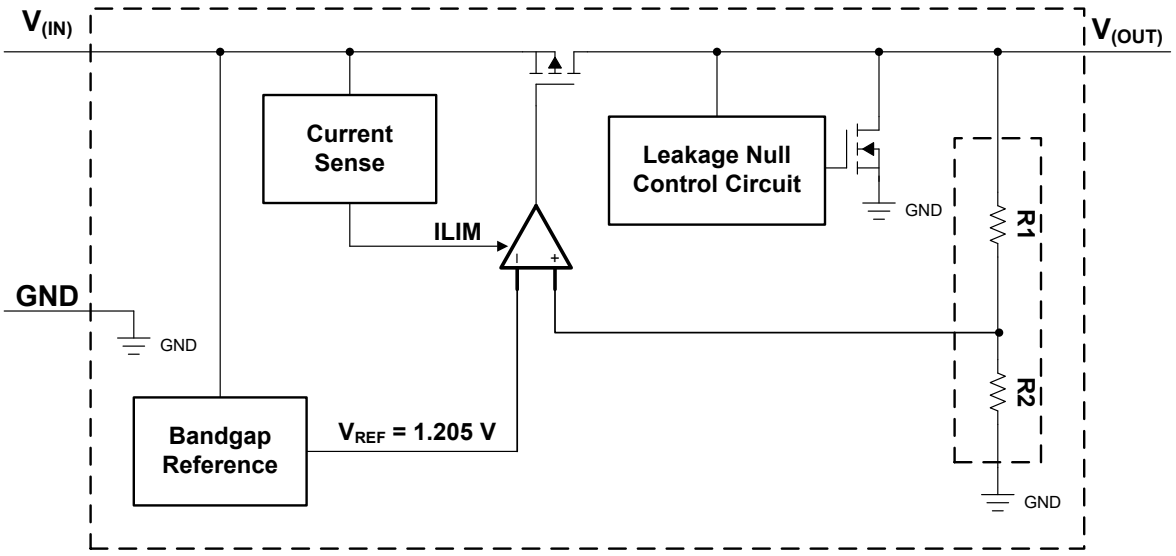
7 Detailed Description

7.1 Overview

The TLV704 low-dropout regulator (LDO) consumes only 3.4 µA of quiescent current across the entire output current range, and offers a wide input voltage range and low-dropout voltage in a small package. The device, which operates over an input range of 2.5 V to 24 V, is stable with any output capacitor greater than or equal to 0.47 µF. The low quiescent current across the complete load current range makes the TLV704 designed for powering battery-operated applications. The TLV704 has internal soft-start to control inrush current into the output capacitor. This LDO also has overcurrent protection during a load-short or fault condition on the output.

7.2 Functional Block Diagram



7.3 Feature Description

7.3.1 Wide Supply Range

This device has an operational input supply range of 2.5 V to 24 V, allowing for a wide range of applications. This wide supply range is designed for applications that have either large transients or high DC voltage supplies.

7.3.2 Low Quiescent Current

This device only requires 3.4 µA (typical) of quiescent current across the complete load current range (0 mA to 150 mA) and has a maximum current consumption of 4.5 µA (for new device only) at –40°C to +125°C.

7.3.3 Dropout Voltage (V_{DO})

Dropout voltage (V_{DO}) is defined as the input voltage minus the output voltage ($V_{IN} - V_{OUT}$) at the rated output current (I_{RATED}), where the pass transistor is fully on. I_{RATED} is the maximum I_{OUT} listed in the *Recommended Operating Conditions* table. In dropout operation, the pass transistor is in the ohmic or triode region of operation, and acts as a switch. The dropout voltage indirectly specifies a minimum input voltage greater than the nominal programmed output voltage at which the output voltage is expected to stay in regulation. If the input voltage falls to less than the value required to maintain output regulation, the output voltage falls as well.

For a CMOS regulator, the dropout voltage is determined by the drain-source, on-state resistance ($R_{DS(ON)}$) of the pass transistor. Therefore, if the linear regulator operates at less than the rated current, the dropout voltage for that current scales accordingly. Use 方程式 1 to calculate the $R_{DS(ON)}$ of the device.

$$R_{DS(ON)} = \frac{V_{DO}}{I_{RATED}} \quad (1)$$

7.3.4 Current Limit

The device has an internal current limit circuit that protects the regulator during transient high-load current faults or shorting events. The current limit is a brick-wall scheme. In a high-load current fault, the brick-wall scheme limits the output current to the current limit (I_{CL}). I_{CL} is listed in the *Electrical Characteristics* table.

The output voltage is not regulated when the device is in current limit. When a current limit event occurs, the device begins to heat up because of the increase in power dissipation. When the device is in brick-wall current limit, the pass transistor dissipates power [(V_{IN} – V_{OUT}) × I_{CL}]. For more information on current limits, see the *Know Your Limits* application note.

图 7-1 shows a diagram of the current limit.

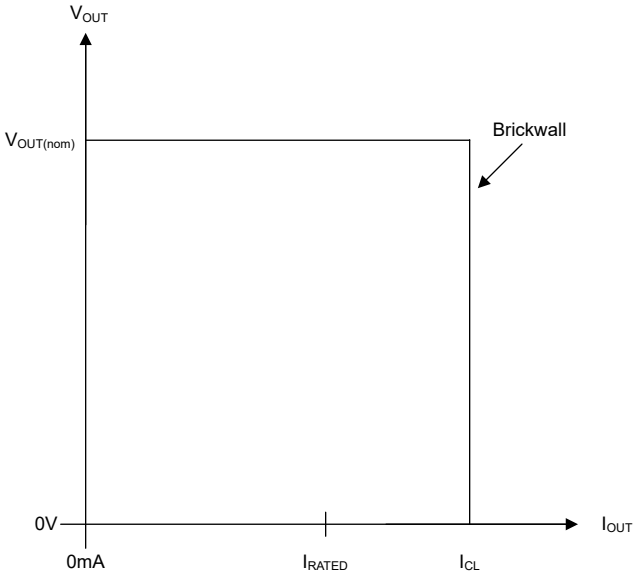


图 7-1. Current Limit

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7.4 Device Functional Modes

表 7-1 provides a quick comparison between the normal, dropout, and disabled modes of operation.

表 7-1. Device Functional Mode Comparison

OPERATING MODE	PARAMETER	
	V_{IN}	I_{OUT}
Normal	$V_{IN} > V_{OUT(nom)} + V_{DO}$	$I_{OUT} < I_{CL}$
Dropout	$V_{IN} < V_{OUT(nom)} + V_{DO}$	$I_{OUT} < I_{CL}$

7.4.1 Normal Operation

The device regulates to the nominal output voltage under the following conditions:

- The input voltage is greater than the nominal output voltage plus the dropout voltage ($V_{OUT(nom)} + V_{DO}$)
- The output current is less than the current limit ($I_{OUT} < I_{CL}$)
- The device junction temperature is greater than –40°C and less than +125°C

7.4.2 Dropout Operation

If the input voltage is lower than the nominal output voltage plus the specified dropout voltage, but all other conditions are met for normal operation, the device operates in dropout mode. In this mode, the output voltage tracks the input voltage. During this mode, the transient performance of the device becomes significantly degraded because the pass transistor is in the ohmic or triode region, and acts as a switch. Line or load transients in dropout can result in large output voltage deviations.

When the device is in a steady dropout state (defined as when the device is in dropout, $V_{IN} < V_{OUT(NOM)} + V_{DO}$, directly after being in a normal regulation state, but *not* during start up), the pass transistor is driven into the ohmic or triode region. When the input voltage returns to a value greater than or equal to the nominal output voltage plus the dropout voltage ($V_{OUT(NOM)} + V_{DO}$), the output voltage can overshoot for a short period of time while the device pulls the pass transistor back into the linear region.

表 7-2 lists the conditions that lead to the different modes of operation.

表 7-2. Device Functional Mode Comparison

OPERATING MODE	PARAMETER	
	V_{IN}	I_{OUT}
Normal mode	$V_{IN} > V_{OUT\ (nom)} + V_{DO}$	$I_{OUT} < I_{CL}$
Dropout mode	$V_{IN} < V_{OUT\ (nom)} + V_{DO}$	$I_{OUT} < I_{CL}$

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8 Application and Implementation

备注

以下应用部分中的信息不属于 TI 器件规格的范围，TI 不担保其准确性和完整性。TI 的客 户应负责确定器件是否适用于其应用。客户应验证并测试其设计，以确保系统功能。

8.1 Application Information

The TLV704 LDO regulator is designed for battery-powered applications and is a good attachment to low-power microcontrollers (such as the MSP430) because of the device low I_Q performance across the entire load current range. The ultra-low supply current of the TLV704 maximizes efficiency at light loads, and the high input voltage range and flexibility of output voltage selection in fixed output levels makes the device applicable for supplies such as unconditioned solar panels.

8.2 Typical Application

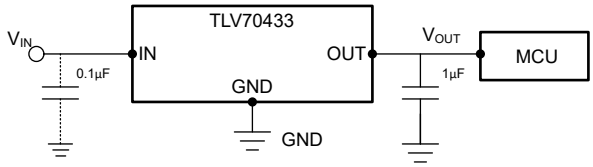

图 8-1. Typical Application

8.2.1 Design Requirements

Select the desired device based on the output voltage.

Provide an input supply with adequate headroom to account for dropout and output current to account for the GND terminal current, and power the load.

8.2.2 Detailed Design Procedure

8.2.2.1 External Capacitor Requirements

The device is designed to be stable using low equivalent series resistance (ESR) ceramic capacitors at the input and output. Multilayer ceramic capacitors have become the industry standard for these types of applications and are recommended, but must be used with good judgment. Ceramic capacitors that employ X7R-, X5R-, and C0G-rated dielectric materials provide relatively good capacitive stability across temperature, whereas the use of Y5V-rated capacitors is discouraged because of large variations in capacitance.

Regardless of the ceramic capacitor type selected, the effective capacitance varies with operating voltage and temperature. Generally, expect the effective capacitance to decrease by as much as 50%. The input and output capacitors recommended in the *Recommended Operating Conditions* table account for an effective capacitance of approximately 50% of the nominal value.

8.2.2.2 Input and Output Capacitor Requirements

Although an input capacitor is not required for stability, good analog design practice is to connect a capacitor from IN to GND. This capacitor counteracts reactive input sources and improves transient response, input ripple, and PSRR. Use an input capacitor if the source impedance is more than 0.5 Ω. A higher value capacitor can be necessary if large, fast rise-time load or line transients are anticipated or if the device is located several inches from the input power source.

Dynamic performance of the device is improved by using a large output capacitor. Use an output capacitor within the range specified in the *Recommended Operating Conditions* table for stability.

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8.2.2.3 Reverse Current

Excessive reverse current can damage this device. Reverse current flows through the intrinsic body diode of the PMOS pass transistor instead of the normal conducting channel. At high magnitudes, this current flow degrades the long-term reliability of the device.

Conditions where reverse current can occur are outlined in this section, all of which can exceed the absolute maximum rating of $V_{OUT} \leqslant V_{IN}$ + 0.3 V. These conditions are:

- If the device has a large C_{OUT} and the input supply collapses with little or no load current
- The output is biased when the input supply is not established
- The output is biased above the input supply

If reverse current flow is expected in the application, external protection is recommended to protect the device. Reverse current is not limited in the device, so external limiting is required if extended reverse voltage operation is anticipated. Limit reverse current to 5% or less of the rated output current of the device in the event this current cannot be avoided.

图 8-2 shows one approach for protecting the device.

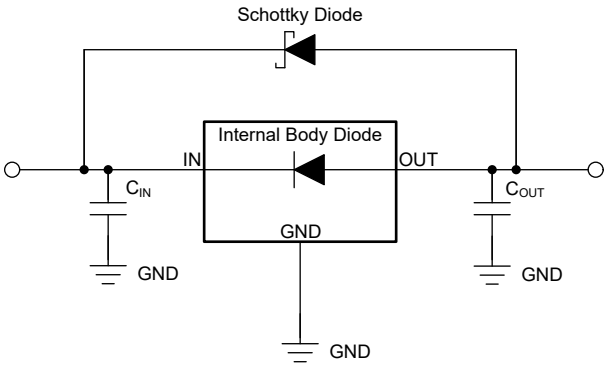

图 8-2. Example Circuit for Reverse Current Protection Using a Schottky Diode

8.2.2.4 Power Dissipation (P_D)

Circuit reliability requires consideration of the device power dissipation, location of the circuit on the printed circuit board (PCB), and correct sizing of the thermal plane. The PCB area around the regulator must have few or no other heat-generating devices that cause added thermal stress.

To first-order approximation, power dissipation in the regulator depends on the input-to-output voltage difference and load conditions. The following equation calculates power dissipation (P_D).

$$P_D = (V_{IN} - V_{OUT}) \times I_{OUT} \quad (2)$$

备注

Power dissipation can be minimized, and therefore greater efficiency can be achieved, by correct selection of the system voltage rails. For the lowest power dissipation, use the minimum input voltage required for correct output regulation.

For devices with a thermal pad, the primary heat conduction path for the device package is through the thermal pad to the PCB. Solder the thermal pad to a copper pad area under the device. This pad area must contain an array of plated vias that conduct heat to additional copper planes for increased heat dissipation.

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The maximum power dissipation determines the maximum allowable ambient temperature (T_A) for the device. According to the following equation, power dissipation and junction temperature are most often related by the junction-to-ambient thermal resistance ($R_{\theta JA}$) of the combined PCB and device package and the temperature of the ambient air (T_A).

$$T_J = T_A + (R_{\theta JA} \times P_D) \quad (3)$$

Thermal resistance ($R_{\theta JA}$) is highly dependent on the heat-spreading capability built into the particular PCB design, and therefore varies according to the total copper area, copper weight, and location of the planes. The junction-to-ambient thermal resistance listed in the *Thermal Information* table is determined by the JEDEC standard PCB and copper-spreading area, and is used as a relative measure of package thermal performance.

8.2.2.5 Estimating Junction Temperature

The JEDEC standard now recommends the use of psi (Ψ) thermal metrics to estimate the junction temperatures of the linear regulator when in-circuit on a typical PCB board application. These metrics are not thermal resistance parameters and instead offer a practical and relative way to estimate junction temperature. These psi metrics are determined to be significantly independent of the copper area available for heat-spreading. The *Thermal Information* table lists the primary thermal metrics, which are the junction-to-top characterization parameter (ψ_{JT}) and junction-to-board characterization parameter (ψ_{JB}). These parameters provide two methods for calculating the junction temperature (T_J), as described in the following equations. Use the junction-to-top characterization parameter (ψ_{JT}) with the temperature at the center-top of device package (T_T) to calculate the junction temperature. Use the junction-to-board characterization parameter (ψ_{JB}) with the PCB surface temperature 1 mm from the device package (T_B) to calculate the junction temperature.

$$T_J = T_T + \psi_{JT} \times P_D \quad (4)$$

where:

- P_D is the dissipated power
- T_T is the temperature at the center-top of the device package

$$T_J = T_B + \psi_{JB} \times P_D \quad (5)$$

where:

- T_B is the PCB surface temperature measured 1 mm from the device package and centered on the package edge

For detailed information on the thermal metrics and how to use them, see the *Semiconductor and IC Package Thermal Metrics* application note.

8.3 Best Design Practices

Place at least one 0.47-µF capacitor as close as possible to the OUT and GND pins of the regulator.

Do not connect the output capacitor to the regulator using a long, thin trace.

Connect an input capacitor as close as possible to the IN and GND pins of the regulator for best performance.

Do not exceed the absolute maximum ratings.

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8.4 Power Supply Recommendations

The TLV704 is designed to operate from an input voltage supply range between 2.5 V and 24 V. The input voltage range must provide adequate headroom for the device to have a regulated output. Inductive impedances between the input supply and the IN pin can create significant voltage excursions at the IN pin during start-up or load transient events. If inductive impedances are unavoidable, use an input capacitor.

8.5 Layout

8.5.1 Layout Guidelines

For best overall performance, place all circuit components on the same side of the printed-circuit-board and as near as practical to the respective LDO pin connections. Place ground return connections for the input and output capacitors as close to the GND pin as possible, using wide, component-side, copper planes. Do not use vias and long traces to create LDO circuit connections to the input capacitor, output capacitor, or the resistor divider because this practice negatively affects system performance. This grounding and layout scheme minimizes inductive parasitics, and thereby reduces load-current transients, minimizes noise, and increases circuit stability. A ground reference plane is also recommended and is either embedded in the PCB or located on the bottom side of the PCB opposite the components. This reference plane serves to assure accuracy of the output voltage and shield the LDO from noise.

8.5.1.1 Power Dissipation

To provide reliable operation, worst-case junction temperature must not exceed 125°C. This restriction limits the power dissipation the regulator can handle in any given application. To make sure the junction temperature is within acceptable limits, calculate the maximum allowable dissipation, $P_{D(max)}$, and the actual dissipation, P_D, which must be less than or equal to $P_{D(max)}$.

The maximum-power-dissipation limit is determined using 方程式 6:

$$P_{D(max)} = \frac{T_J max - T_A}{R_{\theta JA}} \tag{6}$$

where:

- $T_J$max is the maximum allowable junction temperature
- $R_{\theta JA}$ is the thermal resistance junction-to-ambient for the package (see the *Thermal Information* table)
- T_A is the ambient temperature

The regulator dissipation is calculated using 方程式 7:

$$P_D = (V_{IN} - V_{OUT}) \times I_{OUT} \tag{7}$$

8.5.2 Layout Example

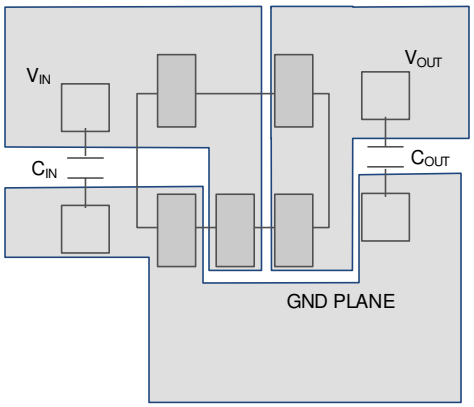

图 8-3. Layout Example for the DBV Package

9 Device and Documentation Support

9.1 Device Support

9.1.1 Development Support

9.1.1.1 Evaluation Module

An evaluation module (EVM) is available to assist in the initial circuit performance evaluation using the TLV704. The TLV70433DBVEVM-712 evaluation module (and related user guide) can be requested at the Texas Instruments website through the product folders or purchased directly from the TI eStore.

9.1.2 Device Nomenclature

表 9-1. Available Options(1)

PRODUCT	V_{OUT}
TLV704**xxyyyz** Legacy chip	**xx** is the nominal output voltage (for example 33 = 3.3 V). **yyy** is the package designator. **z** is the package quantity.
TLV704**xxyyyzM3** New chip	**xx** is the nominal output voltage (for example 33 = 3.3 V). **yyy** is the package designator. **z** is the package quantity. **M3** is a suffix designator for newer chip redesigns, fabricated on the latest TI process technology.

(1) For the most current package and ordering information, see the Package Option Addendum at the end of this document, or visit the device product folder at www.ti.com.

9.2 Documentation Support

9.2.1 Related Documentation

For related documentation see the following:

- Texas Instruments, *TLV70433DBVEVM-712, TLV70433PKEVM-712 Evaluation Modules* user guide

9.3 接收文档更新通知

要接收文档更新通知，请导航至 ti.com 上的器件产品文件夹。点击 *订阅更新* 进行注册，即可每周接收产品信息更改摘要。有关更改的详细信息，请查看任何已修订文档中包含的修订历史记录。

9.4 支持资源

TI E2E™ 支持论坛是工程师的重要参考资料，可直接从专家获得快速、经过验证的解答和设计帮助。搜索现有解答或提出自己的问题可获得所需的快速设计帮助。

链接的内容由各个贡献者“按原样”提供。这些内容并不构成 TI 技术规范，并且不一定反映 TI 的观点；请参阅 TI 的《使用条款》。

9.5 Trademarks

TI E2E™ is a trademark of Texas Instruments.
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9.6 Electrostatic Discharge Caution

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

9.7 术语表

TI 术语表　　本术语表列出并解释了术语、首字母缩略词和定义。

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10 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

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PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
PTLV70450DBVRM3	ACTIVE	SOT-23	DBV	5	3000	TBD	Call TI	Call TI	-40 to 125		Samples
TLV70418DBVR	ACTIVE	SOT-23	DBV	5	3000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	1NG	Samples
TLV70430DBVR	ACTIVE	SOT-23	DBV	5	3000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	QUQ	Samples
TLV70430DBVT	ACTIVE	SOT-23	DBV	5	250	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	QUQ	Samples
TLV70433DBVR	ACTIVE	SOT-23	DBV	5	3000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	PAO	Samples
TLV70433DBVT	ACTIVE	SOT-23	DBV	5	250	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	PAO	Samples
TLV704345DBVR	ACTIVE	SOT-23	DBV	5	3000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	13T	Samples
TLV704345DBVT	ACTIVE	SOT-23	DBV	5	250	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	13T	Samples
TLV70436DBVR	ACTIVE	SOT-23	DBV	5	3000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	PAW	Samples
TLV70436DBVT	ACTIVE	SOT-23	DBV	5	250	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	PAW	Samples
TLV70450DBVR	ACTIVE	SOT-23	DBV	5	3000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	PAX	Samples
TLV70450DBVT	ACTIVE	SOT-23	DBV	5	250	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	PAX	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

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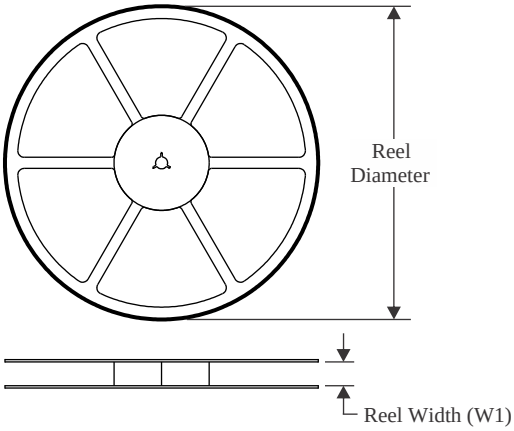
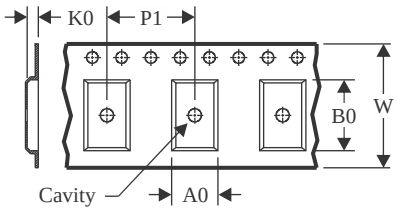
TAPE AND REEL INFORMATION

REEL DIMENSIONS

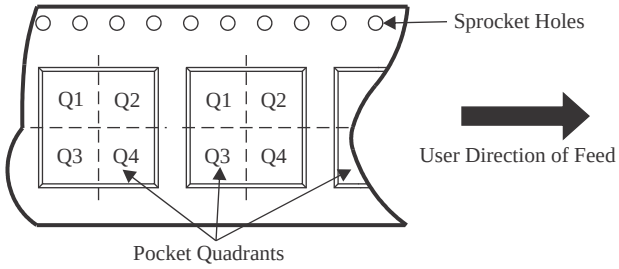


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

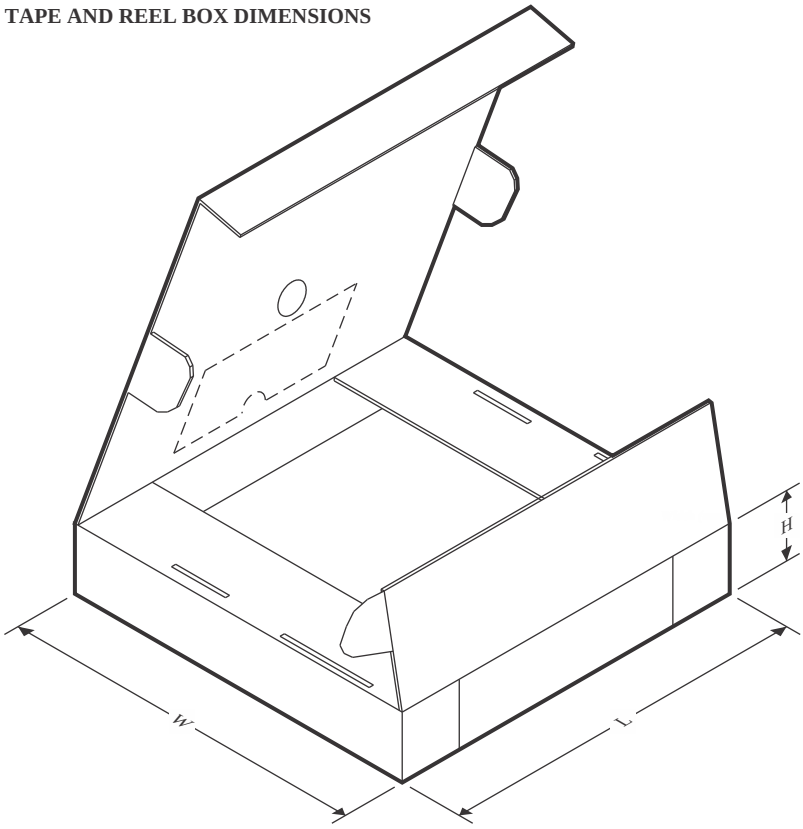
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TLV70418DBVR	SOT-23	DBV	5	3000	180.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
TLV70430DBVR	SOT-23	DBV	5	3000	178.0	9.0	3.23	3.17	1.37	4.0	8.0	Q3
TLV70430DBVT	SOT-23	DBV	5	250	178.0	8.4	3.23	3.17	1.37	4.0	8.0	Q3
TLV70433DBVR	SOT-23	DBV	5	3000	178.0	9.0	3.23	3.17	1.37	4.0	8.0	Q3
TLV70433DBVT	SOT-23	DBV	5	250	178.0	8.4	3.23	3.17	1.37	4.0	8.0	Q3
TLV704345DBVR	SOT-23	DBV	5	3000	178.0	9.0	3.23	3.17	1.37	4.0	8.0	Q3
TLV704345DBVT	SOT-23	DBV	5	250	178.0	8.4	3.23	3.17	1.37	4.0	8.0	Q3
TLV70436DBVR	SOT-23	DBV	5	3000	178.0	9.0	3.23	3.17	1.37	4.0	8.0	Q3
TLV70436DBVT	SOT-23	DBV	5	250	178.0	8.4	3.23	3.17	1.37	4.0	8.0	Q3
TLV70450DBVR	SOT-23	DBV	5	3000	178.0	9.0	3.23	3.17	1.37	4.0	8.0	Q3
TLV70450DBVT	SOT-23	DBV	5	250	178.0	8.4	3.3	3.2	1.4	4.0	8.0	Q3

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

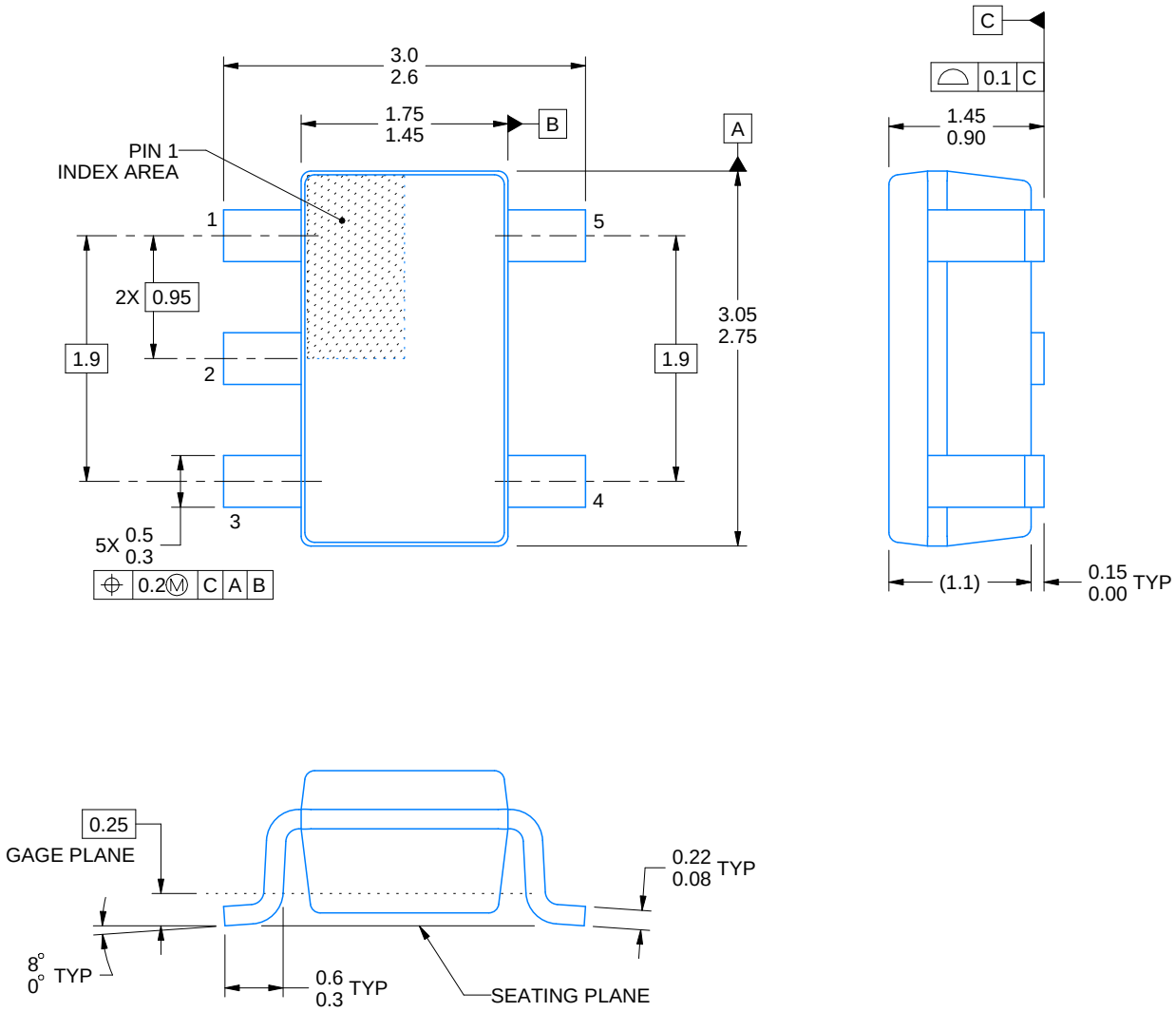
Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TLV70418DBVR	SOT-23	DBV	5	3000	210.0	185.0	35.0
TLV70430DBVR	SOT-23	DBV	5	3000	180.0	180.0	18.0
TLV70430DBVT	SOT-23	DBV	5	250	180.0	180.0	18.0
TLV70433DBVR	SOT-23	DBV	5	3000	180.0	180.0	18.0
TLV70433DBVT	SOT-23	DBV	5	250	180.0	180.0	18.0
TLV704345DBVR	SOT-23	DBV	5	3000	180.0	180.0	18.0
TLV704345DBVT	SOT-23	DBV	5	250	180.0	180.0	18.0
TLV70436DBVR	SOT-23	DBV	5	3000	180.0	180.0	18.0
TLV70436DBVT	SOT-23	DBV	5	250	180.0	180.0	18.0
TLV70450DBVR	SOT-23	DBV	5	3000	180.0	180.0	18.0
TLV70450DBVT	SOT-23	DBV	5	250	180.0	180.0	18.0

PACKAGE OUTLINE

DBV0005A

SOT-23 - 1.45 mm max height

SMALL OUTLINE TRANSISTOR



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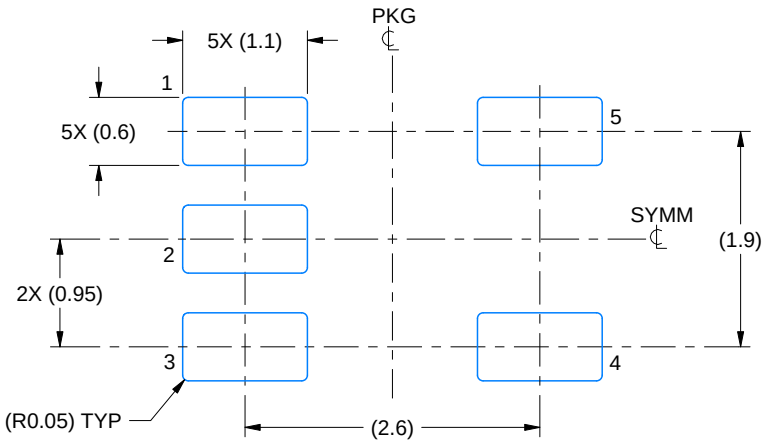
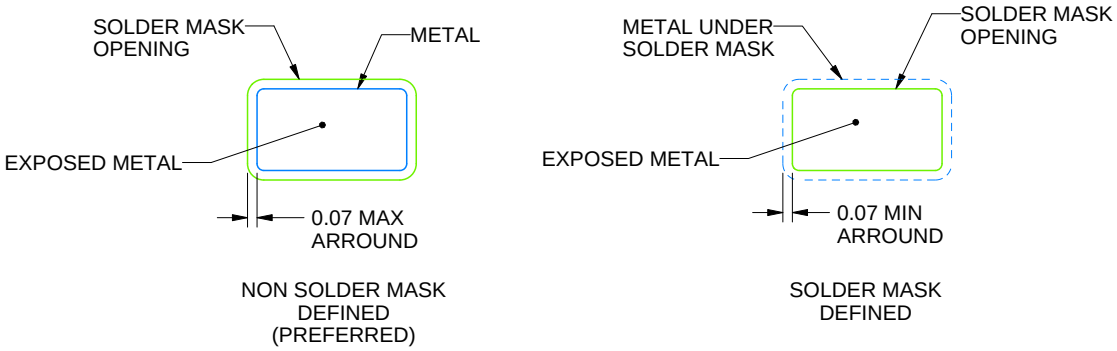
NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. Refernce JEDEC MO-178.
4. Body dimensions do not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.25 mm per side.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:15X



SOLDER MASK DETAILS

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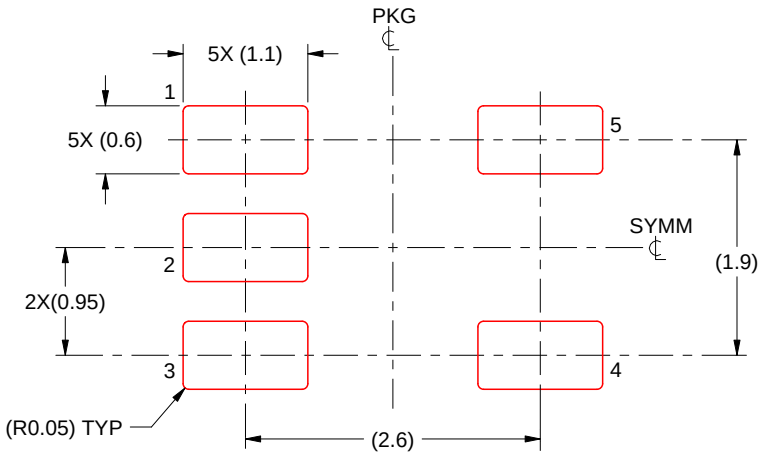
NOTES: (continued)

5. Publication IPC-7351 may have alternate designs.
6. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:15X

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NOTES: (continued)

7. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
8. Board assembly site may have different recommendations for stencil design.

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