BENCHMARQ

bq4832Y

RTC Module With 32Kx8 NVSRAM

Features

- Integrated SRAM, real-time clock, CPU supervisor, crystal, power-fail circuit, and battery
- Real-Time Clock counts hundredths of seconds through years in BCD format
- RAM-like clock access
- Compatible with industry-standard 32K x 8 SRAMs
- Unlimited write cycles
- 10-year minimum data retention and clock operation in the absence of power
- Automatic power-fail chip deselect and write-protection
- Watchdog timer, power-on reset, alarm/periodic interrupt, power-fail and battery-low warning
- Software clock calibration for greater than ±1 minute per month accuracy

General Description

The bq4832Y RTC Module is a nonvolatile 262,144-bit SRAM organized as 32,768 words by 8 bits with an integral real-time clock and CPU supervisor. The CPU supervisor provides a programmable watchdog timer and a microprocessor reset. Other features include alarm, power-fail, and periodic interrupts, and a battery-low warning.

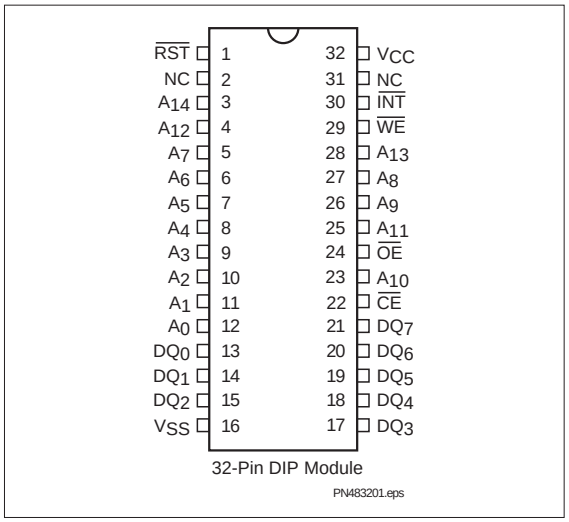
The device combines an internal lithium battery, quartz crystal, clock and power-fail chip, and a full CMOS SRAM in a plastic 32-pin DIP module. The RTC Module directly replaces industry-standard SRAMs and also fits into many EPROM and EEPROM sockets without any requirement for special write timing or limitations on the number of write cycles.

Registers for the real-time clock, alarm and other special functions are located in registers 7FF0h–7FFFh of the memory array.

The clock and alarm registers are dual-port read/write SRAM locations that are updated once per second by a clock control circuit from the internal clock counters. The dual-port registers allow clock updates to occur without interrupting normal access to the rest of the SRAM array.

The bq4832Y also contains a power-fail-detect circuit. The circuit deselects the device whenever V_{CC} falls below tolerance, providing a high degree of data security. The battery is electrically isolated when shipped from the factory to provide maximum battery capacity. The battery remains disconnected until the first application of V_{CC}.

Pin Connections



32-Pin DIP Module

PN483201.eps

Pin Names

A_0–A_{14}	Address input
$\overline{CE}$	Chip enable
$\overline{RST}$	Microprocessor reset
$\overline{WE}$	Write enable
$\overline{OE}$	Output enable
DQ_0–DQ_7	Data in/data out
$\overline{INT}$	Programmable interrupt
V_{CC}	+5 volts
V_{SS}	Ground

Sept. 1996 C

Functional Description

Figure 1 is a block diagram of the bq4832Y. The following sections describe the bq4832Y functional operation, including memory and clock interface, data-retention modes, power-on reset timing, watchdog timer activation, and interrupt generation.

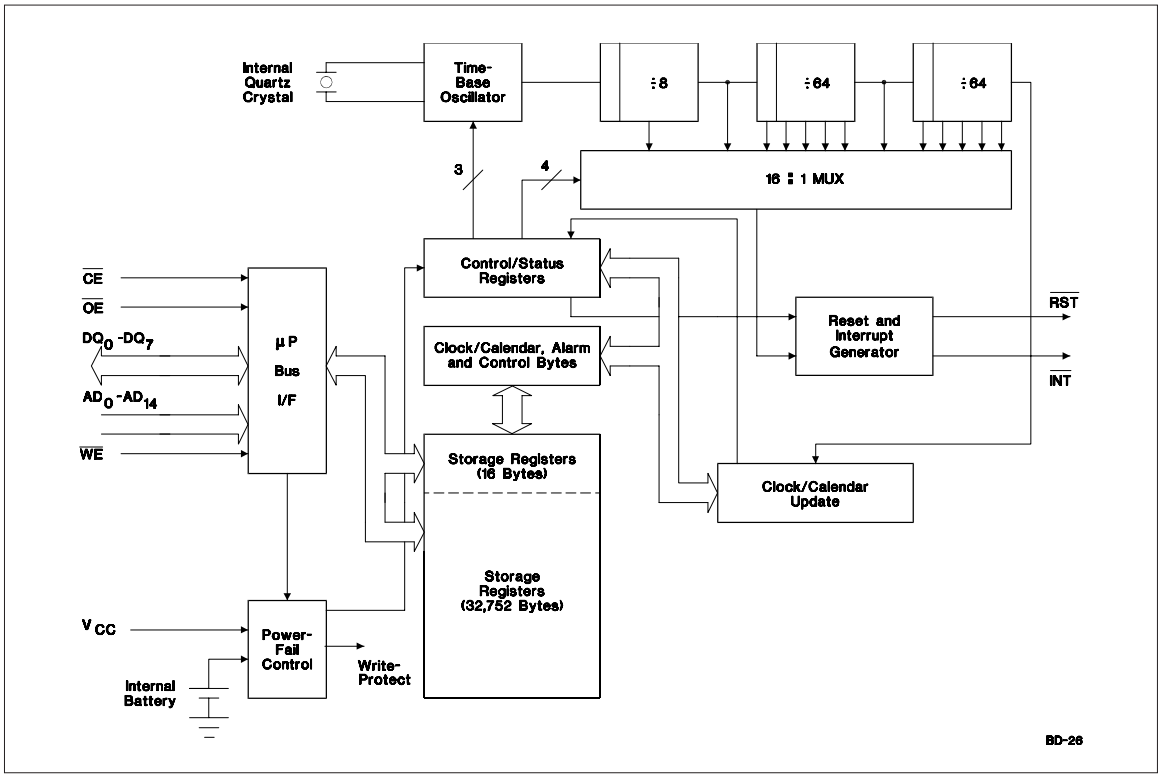


Figure 1. Block Diagram

Truth Table

V_{CC}	$\overline{CE}$	$\overline{OE}$	$\overline{WE}$	Mode	DQ	Power
< V_{CC} (max.)	V_{IH}	X	X	Deselect	High Z	Standby
> V_{CC} (min.)	V_{IL}	X	V_{IL}	Write	D_{IN}	Active
	V_{IL}	V_{IL}	V_{IH}	Read	D_{OUT}	Active
	V_{IL}	V_{IH}	V_{IH}	Read	High Z	Active
< V_{PFD} (min.) > V_{SO}	X	X	X	Deselect	High Z	CMOS standby
≤ V_{SO}	X	X	X	Deselect	High Z	Battery-backup mode

Address Map

The bq4832Y provides 16 bytes of clock and control status registers and 32,752 bytes of storage RAM.

Figure 2 illustrates the address map for the bq4832Y. Table 1 is a map of the bq4832Y registers, and Table 2 describes the register bits.

Memory Interface

Read Mode

The bq4832Y is in read mode whenever $\overline{OE}$ (output enable) is low and $\overline{CE}$ (chip enable) is low. The device architecture allows ripple-through access of data from eight of 262,144 locations in the static storage array. Thus, the unique address specified by the 15 address inputs defines which one of the 32,768 bytes of data is to be accessed. Valid data is available at the data I/O pins within t_{AA} (address access time) after the last address input signal is stable, providing that the $\overline{CE}$ and $\overline{OE}$ (output enable) access times are also satisfied. If the $\overline{CE}$ and $\overline{OE}$ access times are not met, valid data is available after the latter of chip enable access time (t_{ACE}) or output enable access time (t_{OE}).

$\overline{CE}$ and $\overline{OE}$ control the state of the eight three-state data I/O signals. If the outputs are activated before t_{AA}, the data lines are driven to an indeterminate state until t_{AA}. If the address inputs are changed while $\overline{CE}$ and $\overline{OE}$ remain low, output data remains valid for t_{OH} (output data hold time), but goes indeterminate until the next address access.

Write Mode

The bq4832Y is in write mode whenever $\overline{WE}$ and $\overline{CE}$ are active. The start of a write is referenced from the latter-occurring falling edge of $\overline{WE}$ or $\overline{CE}$. A write is terminated by the earlier rising edge of $\overline{WE}$ or $\overline{CE}$. The addresses must be held valid throughout the cycle. $\overline{CE}$ or $\overline{WE}$ must return high for a minimum of t_{WR2} from $\overline{CE}$ or t_{WR1} from $\overline{WE}$ prior to the initiation of another read or write cycle.

Data-in must be valid t_{DW} prior to the end of write and remain valid for t_{DH1} or t_{DH2} afterward. $\overline{OE}$ should be kept high during write cycles to avoid bus contention; although, if the output bus has been activated by a low on $\overline{CE}$ and $\overline{OE}$, a low on $\overline{WE}$ disables the outputs t_{WZ} after $\overline{WE}$ falls.

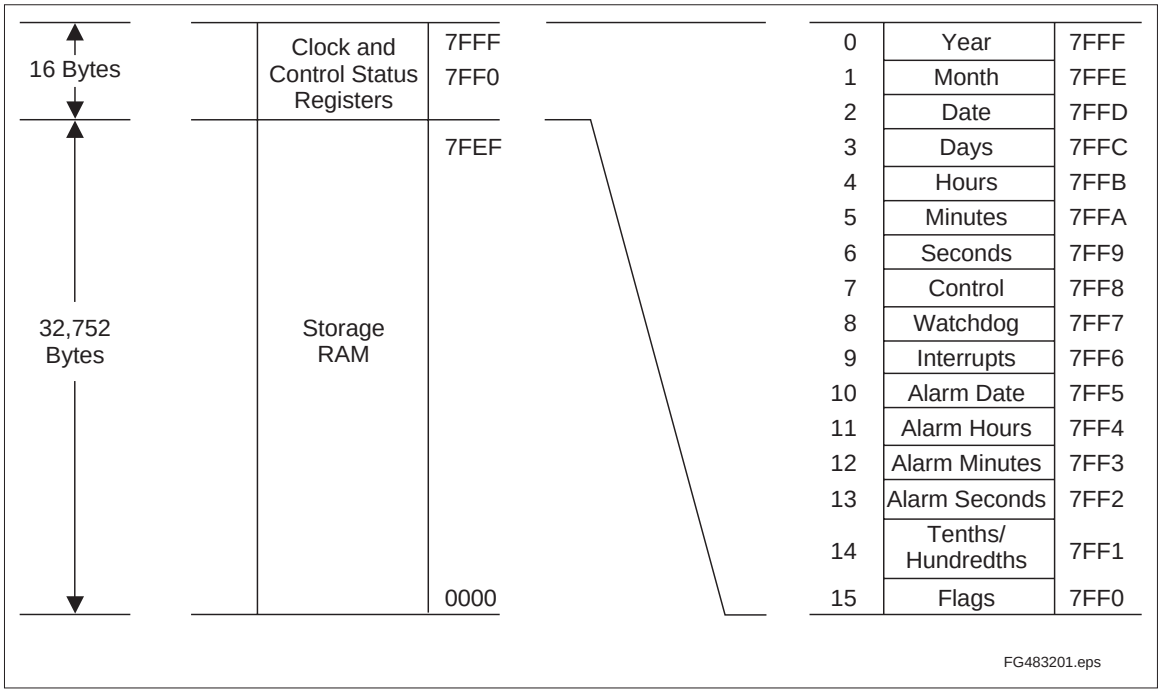


Figure 2. Address Map

Data-Retention Mode

With valid V_{CC} applied, the bq4832Y operates as a conventional static RAM. Should the supply voltage decay, the RAM automatically power-fail deselects, write-protecting itself t_{WPT} after V_{CC} falls below V_{PFD}. All outputs become high impedance, and all inputs are treated as "don't care."

If power-fail detection occurs during a valid access, the memory cycle continues to completion. If the memory cycle fails to terminate within time t_{WPT}, write-protection takes place. When V_{CC} drops below V_{SO}, the control circuit switches power to the internal energy source, which preserves data.

The internal coin cell maintains data in the bq4832Y after the initial application of V_{CC} for an accumulated period of at least 10 years when V_{CC} is less than V_{SO}. As system power returns and Vcc rises above V_{SO}, the battery is disconnected, and the power supply is switched to external V_{CC}. Write-protection continues for t_{CER} after V_{CC} reaches V_{PFD} to allow for processor stabilization. After t_{CER}, normal RAM operation can resume.

Clock Interface

Reading the Clock

The interface to the clock and control registers of the bq4832Y is the same as that for the general-purpose storage memory. Once every second, the user-accessible clock/calendar locations are updated simultaneously from the internal real time counters. To prevent reading data in transition, updates to the bq4832Y clock registers should be halted. Updating is halted by setting the read bit D6 of the control register to 1. As long as the read bit is 1, updates to user-accessible clock locations are inhibited. Once the frozen clock information is retrieved by reading the appropriate clock memory locations, the read bit should be reset to 0 in order to allow updates to occur from the internal counters. Because the internal counters are not halted by setting the read bit, reading the clock locations has no effect on clock accuracy. Once the read bit is reset to 0, within one second the internal registers update the user-accessible registers with the correct time. A halt command issued during a clock update allows the update to occur before freezing the data.

Table 1. bq4832Y Clock and Control Register Map

Address	D7	D6	D5	D4	D3	D2	D1	D0	Range (h)	Register
7FFF	10 Years				Year				00–99	Year
7FFE	X	X	X	10 Month	Month				01–12	Month
7FFD	X	X	10 Date		Date				01–31	Date
7FFC	X	FTE	X	X	X	Day			01–07	Days
7FFB	X	X	10 Hours		Hours				00–23	Hours
7FFA	X	10 Minutes			Minutes				00–59	Minutes
7FF9	OSC	10 Seconds			Seconds				00–59	Seconds
7FF8	W	R	S	Calibration					00–31	Control
7FF7	WDS	BM4	BM3	BM2	BM1	BM0	WD1	WD0		Watchdog
7FF6	AIE	PWRIE	ABE	PIE	RS3	RS2	RS1	RS0		Interrupts
7FF5	ALM3	X	10-date alarm		Alarm date				01–31	Alarm date
7FF4	ALM2	X	10-hour alarm		Alarm hours				00–23	Alarm hours
7FF3	ALM1	Alarm 10 minutes			Alarm minutes				00–59	Alarm minutes
7FF2	ALM0	Alarm 10 seconds			Alarm seconds				00–59	Alarm seconds
7FF1	0.1 seconds				0.01 seconds				00–99	0.1/0.01 seconds
7FF0	WDF	AF	PWRF	BLF	PF	X	X	X		Flags

Notes: X = Unused bits; can be written and read.
Clock/Calendar data in 24-hour BCD format.
BLF = 1 for low battery.
OSC = 1 stops the clock oscillator.
Interrupt enables are cleared on power-up.

Table 2. Clock and Control Register Bits

Bits	Description
ABE	Alarm interrupt enable in battery-backup mode
AF	Alarm interrupt flag
AIE	Alarm interrupt enable
ALM0–ALM3	Alarm repeat rate
BLF	Battery-low flag
BM0–BM4	Watchdog multiplier
FTE	Frequency test mode enable
OSC	Oscillator stop
PF	Periodic interrupt flag
PIE	Periodic interrupt enable
PWRF	Power-fail interrupt flag
PWRIE	Power-fail interrupt enable
R	Read clock enable
RS0–RS3	Periodic interrupt rate
S	Calibration sign
W	Write clock enable
WD0–WD1	Watchdog resolution
WDF	Watchdog flag
WDS	Watchdog steering

Setting the Clock

Bit D7 of the control register is the write bit. Like the read bit, the write bit when set to a 1 halts updates to the clock/calendar memory locations. Once frozen, the locations can be written with the desired information in 24-hour BCD format. Resetting the write bit to 0 causes the written values to be transferred to the internal clock counters and allows updates to the user-accessible registers to resume within one second. Use the write bit, D7, only when updating the time registers (7FFF-7FF9).

Stopping and Starting the Clock Oscillator

The OSC bit in the seconds register turns the clock on or off. If the bq4832Y is to spend a significant period of time in storage, the clock oscillator can be turned off to preserve battery capacity. OSC set to 1 stops the clock oscillator. When OSC is reset to 0, the clock oscillator is turned on and clock updates to user-accessible memory locations occur within one second.

The OSC bit is set to 1 when shipped from the Benchmarq factory.

Calibrating the Clock

The bq4832Y real-time clock is driven by a quartz controlled oscillator with a nominal frequency of 32,768 Hz. The quartz crystal is contained within the bq4832Y package along with the battery. The clock accuracy of the bq4832Y module is tested to be within 20ppm or about 1 minute per month at 25°C. The oscillation rates of crystals change with temperature as Figure 3 shows. To compensate for the frequency shift, the bq4832Y offers onboard software clock calibration. The user can adjust the calibration based on the typical operating temperature of individual applications.

The software calibration bits are located in the control register. Bits D0–D4 control the magnitude of correction, and bit D5 the direction (positive or negative) of correction. Assuming that the oscillator is running at exactly 32,786 Hz, each calibration step of D0–D4 adjusts the clock rate by +4.068 ppm (+10.7 seconds per month) or -2.034 ppm (-5.35 seconds per month) depending on the value of the sign bit D5. When the sign bit is 1, positive adjustment occurs; a 0 activates negative adjustment. The total range of clock calibration is +5.5 or -2.75 minutes per month.

Two methods can be used to ascertain how much calibration a given bq4832Y may require in a system. The first involves simply setting the clock, letting it run for a month, and then comparing the time to an accurate known reference like WWV radio broadcasts. Based on the variation to the standard, the end user can adjust the clock to match the system's environment even after the product is packaged in a non-serviceable enclosure. The only requirement is a utility that allows the end user to access the calibration bits in the control register.

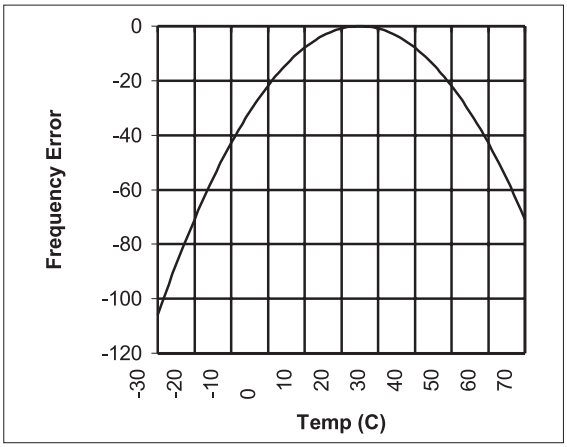


Figure 3. Frequency Error

The second approach uses a bq4832Y test mode. When the frequency test mode enable bit FTE in the days register is set to a 1, and the oscillator is running at exactly 32,768 Hz, the LSB of the seconds register toggles at 512 Hz. Any deviation from 512 Hz indicates the degree and direction of oscillator frequency shift at the test temperature. For example, a reading of 512.01024 Hz indicates a (1E6∗0.01024)/512 or +20 ppm oscillator frequency error, requiring ten steps of negative calibration (10∗-2.034 or -20.34) or 001010 to be loaded into the calibration byte for correction. To read the test frequency, the bq4832Y must be selected and held in an extended read of the seconds register, location 7FF9, without having the read bit set. The frequency appears on DQ0. The FTE bit must be set using the write bit control. The FTE bit must be reset to 0 for normal clock operation to resume.

Power-On Reset

The bq4832Y provides a power-on reset, which pulls the $\overline{RST}$ pin low on power-down and remains low on power-up for t_{CER} after V_{CC} passes V_{PFD}.

Watchdog Timer

The watchdog circuit monitors the microprocessor's activity. If the processor does not reset the watchdog timer within the programmed time-out period, the circuit asserts the $\overline{INT}$ or $\overline{RST}$ pin. The watchdog timer is activated by writing the desired time-out period into the eight-bit watchdog register described in Table 3 (device address 7FF7). The five bits (BM4–BM0) store a binary multiplier, and the two lower-order bits (WD1–WD0) select the resolution, where 00 = 1/16 second, 01 = ¼ second, 10 = 1 second, and 11 = 4 seconds.

The time-out period is the multiplication of the five-bit multiplier with the two-bit resolution. For example, writing 00011 in BM4–BM0 and 10 in WD1–WD0 results in a total time-out setting of 3 x 1 or 3 seconds. A multiplier of zero disables the watchdog circuit. Bit 7 of the watchdog register (WDS) is the watchdog steering bit. When WDS is set to a 1 and a time-out occurs, the watchdog asserts a reset pulse for t_{CER} on the $\overline{RST}$ pin. During the reset pulse, the watchdog register is cleared to all zeros disabling the watchdog. When WDS is set to a 0, the watchdog asserts the $\overline{INT}$ pin on a time-out. The $\overline{INT}$ pin remains low until the watchdog is reset by the microprocessor or a power failure occurs. Additionally, when the watchdog times out, the watchdog flag bit (WDF) in the flags register, location 7FF0, is set.

To reset the watchdog timer, the microprocessor must write to the watchdog register. After being reset by a write, the watchdog time-out period starts over. As a precaution, the watchdog circuit is disabled on a power failure. The user must, therefore, set the watchdog at boot-up for activation.

Interrupts

The bq4832Y allows four individually selected interrupt events to generate an interrupt request on the $\overline{INT}$ pin. These four interrupt events are:

- The watchdog timer interrupt, programmable to occur according to the time-out period and conditions described in the watchdog timer section.
- The periodic interrupt, programmable to occur once every 122µs to 500ms.
- The alarm interrupt, programmable to occur once per second to once per month.
- The power-fail interrupt, which can be enabled to be asserted when the bq4832Y detects a power failure.

The periodic, alarm, and power-fail interrupts are enabled by an individual interrupt-enable bit in register 7FF6, the interrupts register. When an event occurs, its event flag bit in the flags register, location 7FF0, is set. If the corresponding event enable bit is also set, then an interrupt request is generated. Reading the flags register clears all flag bits and makes $\overline{INT}$ high impedance. To reset the flag register, the bq4832Y addresses must be held stable at location 7FF0 for at least 50ns to avoid inadvertent resets.

Periodic Interrupt

Bits RS3–RS0 in the interrupts register program the rate for the periodic interrupt. The user can interpret the interrupt in two ways: either by polling the flags register for PF assertion or by setting PIE so that $\overline{INT}$ goes active when the bq4832Y sets the periodic flag. Reading the flags register resets the PF bit and returns $\overline{INT}$ to the high-impedance state. Table 4 shows the periodic rates.

Table 3. Watchdog Register Bits

MSB			Bits				LSB
7	6	5	4	3	2	1	0
WDS	BM4	BM3	BM2	BM1	BM0	WD1	WD0

Table 4. Periodic Rates

RS3	RS2	RS1	RS0	Interrupt Rate
0	0	0	0	None
0	0	0	1	10ms
0	0	1	0	100ms
0	0	1	1	122.07µs
0	1	0	0	244.14µs
0	1	0	1	488.281µs
0	1	1	0	976.5625
0	1	1	1	1.953125ms
1	0	0	0	3.90625ms
1	0	0	1	7.8125ms
1	0	1	0	15.625ms
1	0	1	1	31.25ms
1	1	0	0	62.5ms
1	1	0	1	125ms
1	1	1	0	250ms
1	1	1	1	500ms

Alarm Interrupt

Registers 7FF5–7FF2 program the real-time clock alarm. During each update cycle, the bq4832Y compares the date, hours, minutes, and seconds in the clock registers with the corresponding alarm registers. If a match between all the corresponding bytes is found, the alarm flag AF in the flags register is set. If the alarm interrupt is enabled with AIE, an interrupt request is generated on $\overline{INT}$. The alarm condition is cleared by a read to the flags register. ALM3–ALM0 puts the alarm into a periodic mode of operation. Table 5 describes the selectable rates.

Table 5. Alarm Frequency (Alarm Bits DQ7 of Alarm Registers)

ALM3	ALM2	ALM1	ALM0	Alarm Frequency
1	1	1	1	Once per second
1	1	1	0	Once per minute when seconds match
1	1	0	0	Once per hour when minutes, and seconds match
1	0	0	0	Once per day when hours, minutes, and seconds match
0	0	0	0	When date, hours, minutes, and seconds match

The alarm interrupt can be made active while the bq4832Y is in the battery-backup mode by setting ABE in the interrupts register. Normally, the $\overline{INT}$ pin tristates during battery backup. With ABE set, however, $\overline{INT}$ is driven low if an alarm condition occurs and the AIE bit is set. Because the AIE bit is reset during power-on reset, an alarm generated during power-on reset updates only the flags register. The user can read the flags register during boot-up to determine if an alarm was generated during power-on reset.

Power-Fail Interrupt

When V_{CC} falls to the power-fail-detect point, the power-fail flag PWRF is set. If the power-fail interrupt enable bit (PWRIE) is also set, then $\overline{INT}$ is asserted low. The power-fail interrupt occurs t_{WPT} before the bq4832Y generates a reset and deselects. The PWRIE bit is cleared on power-up.

Battery-Low Warning

The bq4832Y checks the internal battery on power-up. If the battery voltage is below 2.2V, the battery-low flag BLF in the flags register is set to a 1 indicating that clock and RAM data may be invalid.

Absolute Maximum Ratings

Symbol	Parameter	Value	Unit	Conditions
V_{CC}	DC voltage applied on V_{CC} relative to V_{SS}	-0.3 to 7.0	V	
V_T	DC voltage applied on any pin excluding V_{CC} relative to V_{SS}	-0.3 to 7.0	V	$V_T \le V_{CC} + 0.3$
T_{OPR}	Operating temperature	0 to +70	°C	
T_{STG}	Storage temperature (V_{CC} off; oscillator off)	-40 to +70	°C	
T_{BIAS}	Temperature under bias	-10 to +70	°C	
T_{SOLDER}	Soldering temperature	+260	°C	For 10 seconds

Note: Permanent device damage may occur if **Absolute Maximum Ratings** are exceeded. Functional operation should be limited to the Recommended DC Operating Conditions detailed in this data sheet. Exposure to conditions beyond the operational limits for extended periods of time may affect device reliability.

Recommended DC Operating Conditions ($T_A = T_{OPR}$)

Symbol	Parameter	Minimum	Typical	Maximum	Unit	Notes
V_{CC}	Supply voltage	4.5	5.0	5.5	V	
V_{SS}	Supply voltage	0	0	0	V	
V_{IL}	Input low voltage	-0.3	-	0.8	V	
V_{IH}	Input high voltage	2.2	-	V_{CC} + 0.3	V	

Note: Typical values indicate operation at T_A = 25°C.

DC Electrical Characteristics ($T_A = T_{OPR}$, $V_{CCmin} \le V_{CC} \le V_{CCmax}$)

Symbol	Parameter	Minimum	Typical	Maximum	Unit	Conditions/Notes
I_{LI}	Input leakage current	-	-	± 1	µA	$V_{IN} = V_{SS}$ to V_{CC}
I_{LO}	Output leakage current	-	-	± 1	µA	$\overline{CE} = V_{IH}$ or $\overline{OE} = V_{IH}$ or $\overline{WE} = V_{IL}$
V_{OH}	Output high voltage	2.4	-	-	V	I_{OH} = -1.0 mA
V_{OL}	Output low voltage	-	-	0.4	V	I_{OL} = 2.1 mA
I_{OD}	$\overline{RST}$, $\overline{INT}$ sink current	10	-	-	mA	V_{OL} = 0.4V
I_{SB1}	Standby supply current	-	3	6	mA	$\overline{CE} = V_{IH}$
I_{SB2}	Standby supply current	-	2	4	mA	$\overline{CE} \ge V_{CC}$ - 0.2V, 0V ≤ V_{IN} ≤ 0.2V, or $V_{IN} \ge V_{CC}$ - 0.2V
I_{CC}	Operating supply current	-	55	75	mA	Min. cycle, duty = 100%, $\overline{CE} = V_{IL}$, $I_{I/O}$ = 0mA
V_{PFD}	Power-fail-detect voltage	4.30	4.37	4.50	V	
V_{SO}	Supply switch-over voltage	-	3	-	V	

Notes: Typical values indicate operation at T_A = 25°C, V_{CC} = 5V.
$\overline{RST}$ and $\overline{INT}$ are open-drain outputs.

Capacitance (T_A = 25°C, F = 1MHz, V_{CC} = 5.0V)

Symbol	Parameter	Minimum	Typical	Maximum	Unit	Conditions
$C_{I/O}$	Input/output capacitance	-	-	10	pF	Output voltage = 0V
C_{IN}	Input capacitance	-	-	10	pF	Input voltage = 0V

Note: These parameters are sampled and not 100% tested.

AC Test Conditions

Parameter	Test Conditions
Input pulse levels	0V to 3.0V
Input rise and fall times	5 ns
Input and output timing reference levels	1.5 V (unless otherwise specified)
Output load (including scope and jig)	See Figures 4 and 5

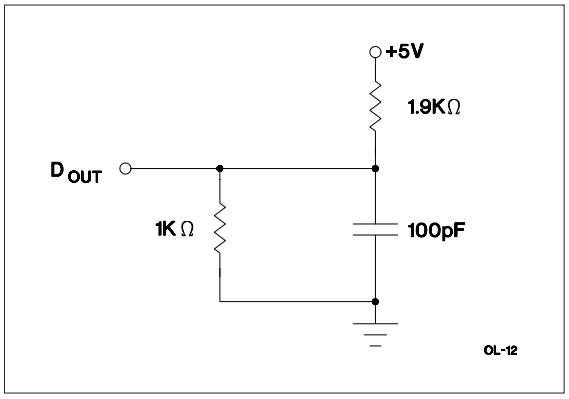


Figure 4. Output Load A

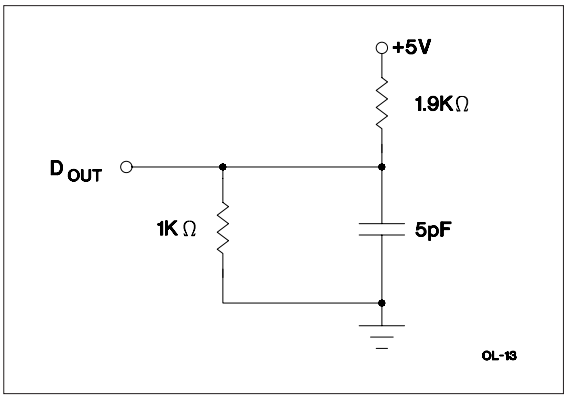
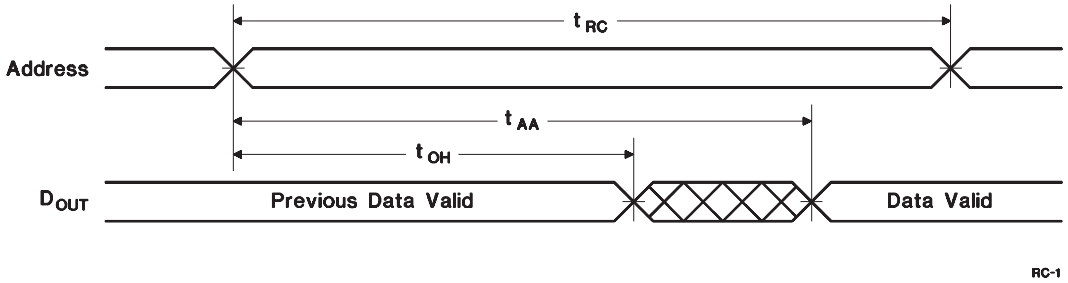


Figure 5. Output Load B

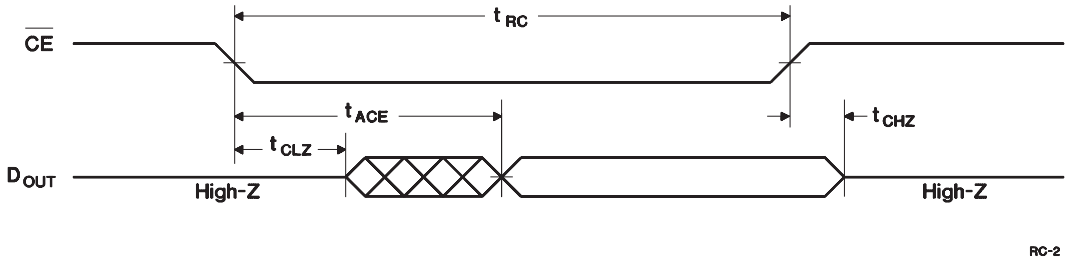
Read Cycle ($T_A = T_{OPR}$, $V_{CCmin} \le V_{CC} \le V_{CCmax}$)

Symbol	Parameter	–85		Unit	Conditions
		Min.	Max.		
t_{RC}	Read cycle time	85	-	ns	
t_{AA}	Address access time	-	85	ns	Output load A
t_{ACE}	Chip enable access time	-	85	ns	Output load A
t_{OE}	Output enable to output valid	-	45	ns	Output load A
t_{CLZ}	Chip enable to output in low Z	5	-	ns	Output load B
t_{OLZ}	Output enable to output in low Z	0	-	ns	Output load B
t_{CHZ}	Chip disable to output in high Z	0	35	ns	Output load B
t_{OHZ}	Output disable to output in high Z	0	25	ns	Output load B
t_{OH}	Output hold from address change	10	-	ns	Output load A

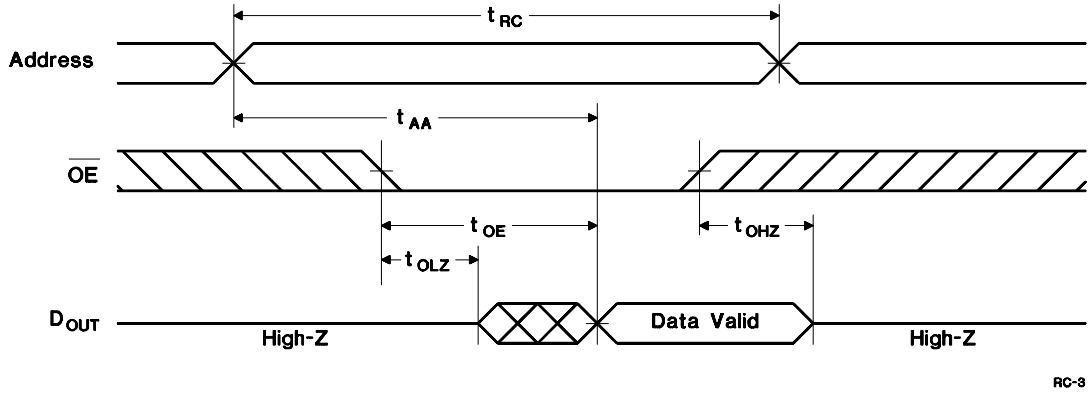
Read Cycle No. 1 (Address Access) [1,2]



Read Cycle No. 2 (CE Access) [1,3,4]



Read Cycle No. 3 (OE Access) [1,5]



Notes:
1. $\overline{WE}$ is held high for a read cycle.
2. Device is continuously selected: $\overline{CE} = \overline{OE} = V_{IL}$.
3. Address is valid prior to or coincident with $\overline{CE}$ transition low.
4. $\overline{OE} = V_{IL}$.
5. Device is continuously selected: $\overline{CE} = V_{IL}$.

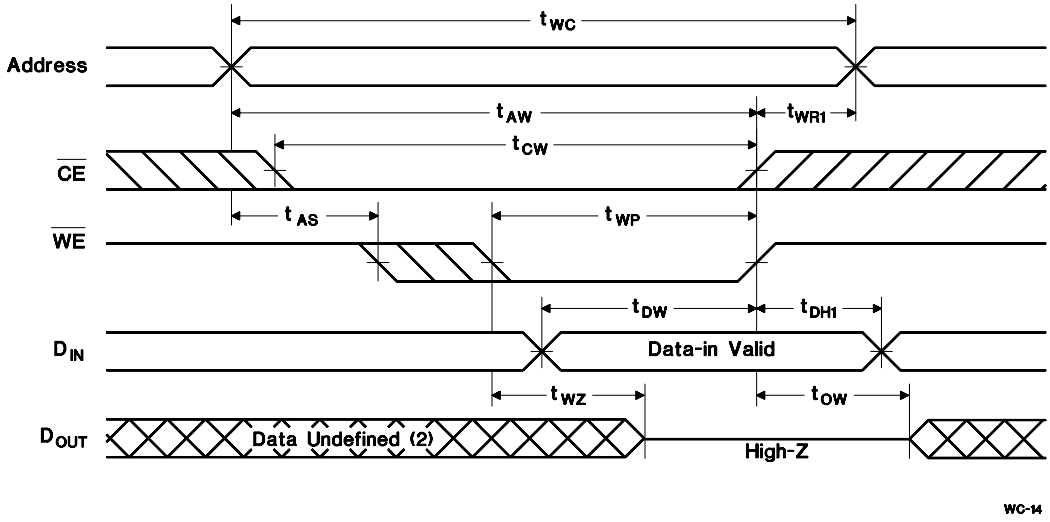
Write Cycle ($T_A = T_{OPR}$, $V_{CCmin} \le V_{CC} \le V_{CCmax}$)

Symbol	Parameter	–85		Units	Conditions/Notes
		Min.	Max.		
t_{WC}	Write cycle time	85	-	ns	
t_{CW}	Chip enable to end of write	75	-	ns	(1)
t_{AW}	Address valid to end of write	75	-	ns	(1)
t_{AS}	Address setup time	0	-	ns	Measured from address valid to beginning of write. (2)
t_{WP}	Write pulse width	65	-	ns	Measured from beginning of write to end of write. (1)
t_{WR1}	Write recovery time (write cycle 1)	5	-	ns	Measured from $\overline{WE}$ going high to end of write cycle. (3)
t_{WR2}	Write recovery time (write cycle 2)	15	-	ns	Measured from $\overline{CE}$ going high to end of write cycle. (3)
t_{DW}	Data valid to end of write	35	-	ns	Measured to first low-to-high transition of either $\overline{CE}$ or $\overline{WE}$.
t_{DH1}	Data hold time (write cycle 1)	0	-	ns	Measured from $\overline{WE}$ going high to end of write cycle. (4)
t_{DH2}	Data hold time (write cycle 2)	10	-	ns	Measured from $\overline{CE}$ going high to end of write cycle. (4)
t_{WZ}	Write enabled to output in high Z	0	30	ns	I/O pins are in output state. (5)
t_{OW}	Output active from end of write	0	-	ns	I/O pins are in output state. (5)

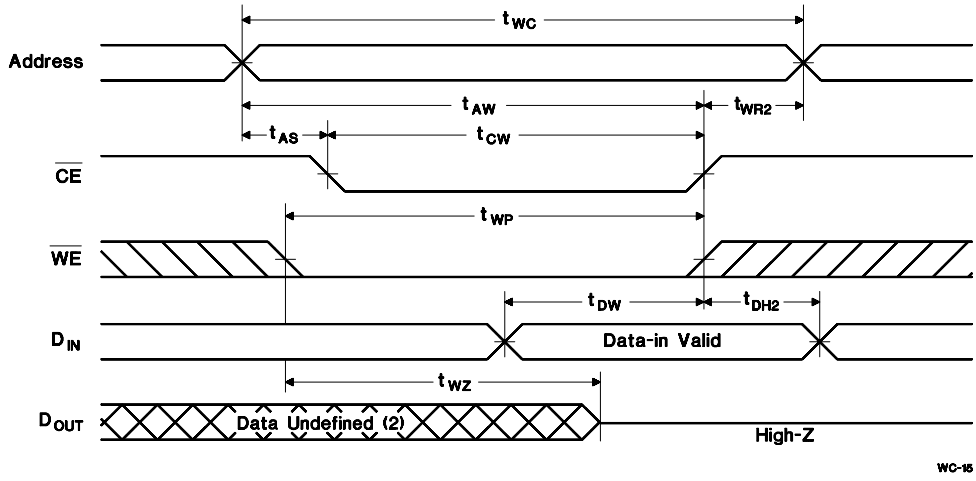
Notes:

1. A write ends at the earlier transition of $\overline{CE}$ going high and $\overline{WE}$ going high.
2. A write occurs during the overlap of a low $\overline{CE}$ and a low $\overline{WE}$. A write begins at the later transition of $\overline{CE}$ going low and $\overline{WE}$ going low.
3. Either t_{WR1} or t_{WR2} must be met.
4. Either t_{DH1} or t_{DH2} must be met.
5. If $\overline{CE}$ goes low simultaneously with $\overline{WE}$ going low or after $\overline{WE}$ going low, the outputs remain in high-impedance state.

Write Cycle No. 1 (WE-Controlled) [1,2,3]



Write Cycle No. 2 (CE-Controlled) [1,2,3,4,5]



Notes:

1. $\overline{CE}$ or $\overline{WE}$ must be high during address transition.
2. Because I/O may be active ($\overline{OE}$ low) during this period, data input signals of opposite polarity to the outputs must not be applied.
3. If $\overline{OE}$ is high, the I/O pins remain in a state of high impedance.
4. Either t_{WR1} or t_{WR2} must be met.
5. Either t_{DH1} or t_{DH2} must be met.

Power-Down/Power-Up Cycle ($T_A = T_{OPR}$)

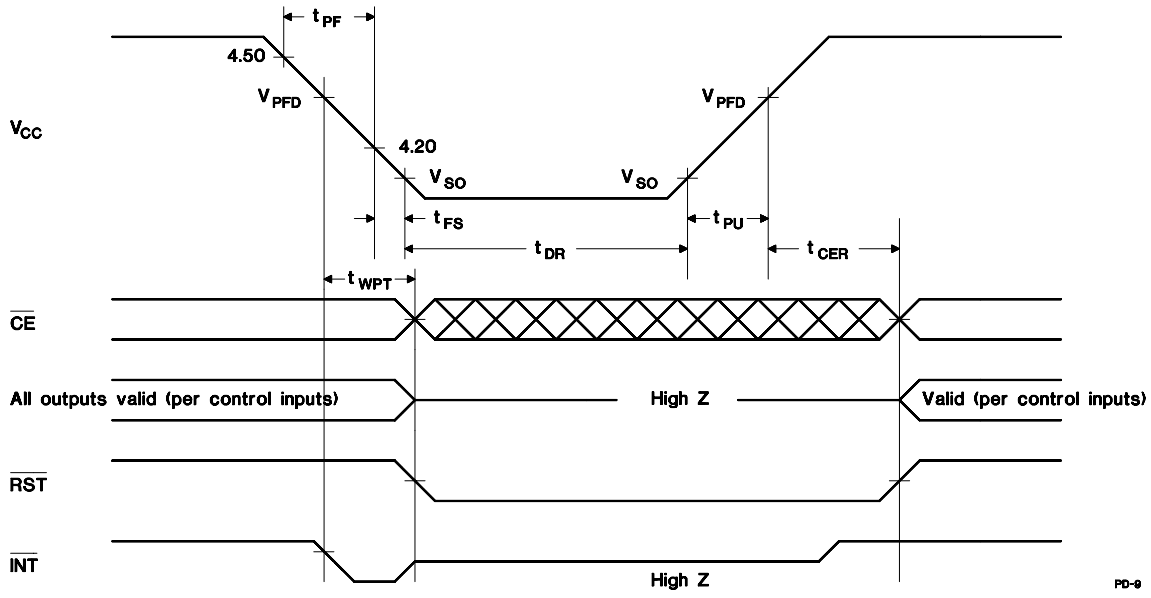
Symbol	Parameter	Minimum	Typical	Maximum	Unit	Conditions
t_{PF}	V_{CC} slew, 4.50 to 4.20 V	300	-	-	µs	
t_{FS}	V_{CC} slew, 4.20 to V_{SO}	10	-	-	µs	
t_{PU}	V_{CC} slew, V_{SO} to V_{PFD} (max.)	0	-	-	µs	
t_{CER}	Chip enable recovery time	40	100	200	ms	Time during which SRAM is write-protected after V_{CC} passes V_{FPD} on power-up.
t_{DR}	Data-retention time in absence of V_{CC}	10	-	-	years	T_A = 25°C. (2)
t_{WPT}	Write-protect time	40	100	160	µs	Delay after V_{CC} slews down past V_{PFD} before SRAM is write-protected.

Notes: 1. Typical values indicate operation at T_A = 25°C, V_{CC} = 5V.

2. Battery is disconnected from circuit until after V_{CC} is applied for the first time. t_{DR} is the accumulated time in absence of power beginning when power is first applied to the device.

Caution: Negative undershoots below the absolute maximum rating of -0.3V in battery-backup mode may affect data integrity.

Power-Down/Power-Up Timing



Notes: 1. PWRIE is set to "1" to enable power fail interrupt.

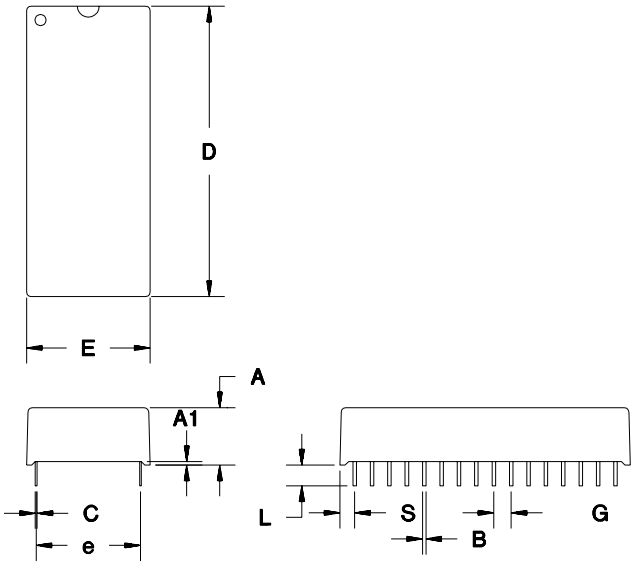
2. $\overline{RST}$ and $\overline{INT}$ are open drain and require an external pull-up resistor.

Data Sheet Revision History

Change No.	Page No.	Description
1	4	Corrected the locations of bits D6 and D4 of the Interrupts Register and the corresponding bits D5 and D3 of the Flags Register (these were reversed).
2	4	Corrected the alarm date register (7FF5) to allow for 01-31 days in a month instead of 01-07 days.
2	9	Lowered I_{SB1} from 4, 7mA to 3, 6mA; lowered I_{SB2} typical from 2.5mA to 2mA.

Notes: Change 1 = Mar. 1996 B changes from Oct. 1995 A.
Change 2 = Sept. 1996 C changes from Mar. 1996 B.

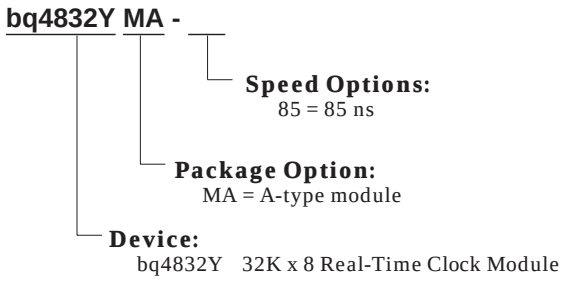
MA: 32-Pin A-Type Module



32-Pin MA (A-Type Module)

Dimension	Inches		Millimeters	
	Min.	Max.	Min.	Max.
A	0.365	0.375	9.27	9.53
A1	0.015	-	0.38	-
B	0.017	0.023	0.43	0.58
C	0.008	0.013	0.20	0.33
D	1.670	1.700	42.42	43.18
E	0.710	0.740	18.03	18.80
e	0.590	0.630	14.99	16.00
G	0.090	0.110	2.29	2.79
L	0.120	0.150	3.05	3.81
S	0.075	0.110	1.91	2.79

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