

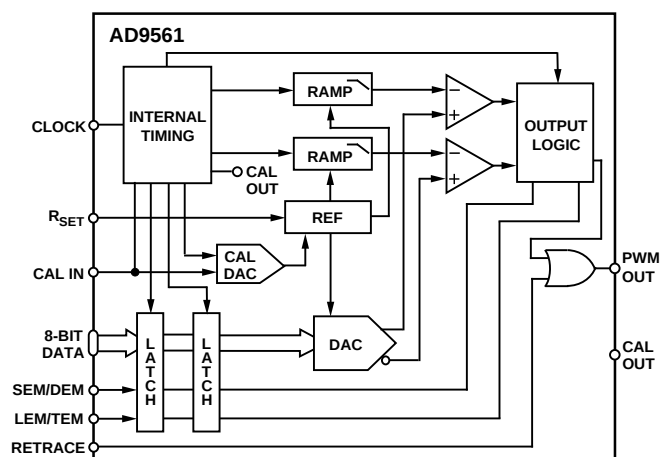
FEATURES

60 MHz Pulse Rate
8-Bit Resolution
Center, Left or Right Justify
Low Power: 700 mW typical
Minimum Pulse Width: <5 ns
Maximum PW: 100 % Full-scale

APPLICATIONS

Laser Printers
Digital Copiers
Color Copiers

FUNCTIONAL BLOCK DIAGRAM



GENERAL DESCRIPTION

The AD9561 is a second generation high speed, digitally programmable pulse width modulator (PWM). Output pulse width is proportional to an 8-bit DATA input value. Two additional control inputs determine if the pulse is placed at the beginning, middle or end of the clock period. Pulse width and placement can be changed every clock cycle up to 60 MHz.

Pulse width modulation is a well proven method for controlling gray scale and resolution enhancement in scanning laser print engines. Modulating pulse width provides the most cost effective method for continuous tone reproduction and resolution enhancement in low-to-moderate cost scanning electro-photographic systems.

The AD9561 uses precision analog circuits to control dot size so that near-photographic quality images are practical without the high frequency clock signals required by all digital approaches.

The AD9561 has improved features and performance over its predecessor, the AD9560. An improved ramp topology enables control of pulse width through 100% of the dot clock period as opposed to 95% for the AD9560. This enables smooth transition across dot boundaries for line screen applications.

Additionally, input data setup and hold time are symmetrical at 2 ns each, simplifying interface to the system bus.

Finally, chip design and pinout are optimized to decrease sensitivity of analog circuits to digital coupling. (See layout section for detailed recommendations for optimum results.)

Inputs are TTL or CMOS compatible, and outputs are CMOS compatible. The AD9561JR is packaged in a 28-lead plastic SOIC. It is rated over the commercial temperature range, 0°C to +70°C.

HIGHLIGHTS

1. 60 MHz native printer clock rate.
2. Single +5 V power supply.
3. On-chip Autocalibration.
4. Pulse placement flexibility.
5. High resolution: 256 pulse widths.

REV. 0

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AD9561—SPECIFICATIONS (+V_S = +5 V; R_{SET} = 715 Ω , CLOCK = 20 MHz unless otherwise noted)

Parameter	Temp	Min	AD9561JR Typ	Max	Units
RESOLUTION		8			Bits
ACCURACY (@ 20 MHz)					
Differential Nonlinearity	+25°C		± 0.5	± 2	LSB
Integral Linearity ¹	+25°C		± 1.5	± 4	LSB
Odd/Even Pulse Mismatch ²	+25°C		± 0.75		LSB
DIGITAL INPUTS					
Logic “1” Voltage	Full	2.0			V
Logic “0” Voltage	Full			0.8	V
Input Current	Full			± 1	μ A
Input Capacitance	+25°C		5		pF
Data Setup Time	Full	2.0	0.3		ns
Data Hold Time	Full	2.0	0.3		ns
Minimum Clock Pulse Width (HIGH)	Full		6		ns
DYNAMIC PERFORMANCE					
Maximum Trigger Rate	Full	60			MHz
Minimum Propagation Delay (t _{PD}) ³	+25°C	12	20	28	ns
Minimum Propagation Delay TC	Full		60		ps/°C
Output Pulse Width @ Code 25 ⁴	Full		5		ns
Output Pulse Width @ Code 255	Full		100		% Clock
Output Rise Time ^{5, 6}	Full		1.8	3	ns
Output Fall Time ^{5, 6}	Full		1.8	3	ns
RETRACE Propagation Delay	Full		6		ns
PWM OUTPUT					
Logic “1” Voltage ^{5, 6}	Full	4.6			V
Logic “0” Voltage ^{5, 6}	Full			0.4	V
CAL OUT					
Logic “1” Voltage	Full	4.6			V
Logic “0” Voltage	Full			0.4	V
POWER SUPPLY ⁷					
Positive Supply Current (+5.0 V)	Full		140	170	mA
Power Dissipation	Full		700	850	mW
Power Reduce Current	Full		70	85	mA
Power Reduce Dissipation	Full		350	425	mW
Power Supply Rejection Ratio					
Propagation Delay Sensitivity (TEM) ⁸	+25°C		1.5		ns/V

NOTES

¹Best Fit between codes 25 and 230. INL is very layout sensitive.

²Due to linearity mismatch in dual ramps.

³Measured from rising edge of clock to transition of Codes 0 to 255.

⁴Minimum pulse width (at 20 MHz) limited by rise time. Pulse width for Code 25 will be greater when CLOCK < 20 MHz.

⁵Output load = 10 pF and 2 mA source/sink.

⁶Load conditions to test output drive capability. Linearity will degrade with either capacitive or current loading. Best linearity obtained driving a single CMOS input.

⁷All performance specifications valid when supply maintained at +5 V, $\pm 5\%$.

⁸Tested from +4.75 V to +5.25 V.

Specification subject to change without notice.

ABSOLUTE MAXIMUM RATINGS¹

Positive Supply Voltage	+7 V
Digital Input Voltage Range	-0.5 V to V_{DD}
Minimum R_{SET}	120 Ω
Digital Output Current (Sourcing) ²	10 mA
Digital Output Current (Sinking) ²	10 mA
Operating Temperature Range ³	0°C to +70°C
Storage Temperature Range	-65°C to +150°C
Junction Temperature	+150°C
Lead Soldering Temperature (10 sec) ⁴	+300°C

NOTES

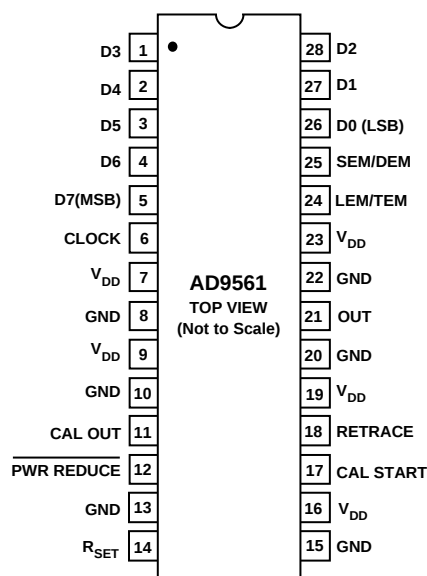
¹Absolute maximum ratings are limiting values, to be applied individually, and beyond which serviceability may be impaired. Functional operation under any of these conditions is not necessarily implied.

²CAL OUT should drive a single TTL or CMOS input.

³Typical Thermal Impedance:

28-lead SOIC (plastic) $\theta_{JA} = 71.4^\circ\text{C/W}$; $\theta_{JC} = 23^\circ\text{C/W}$.

⁴When soldering surface mount packages in vapor phase equipment, temperature should not exceed 220°C for more than one minute.

PIN CONFIGURATION**ORDERING GUIDE**

Model	Temperature Range	Package Description	Package Option
AD9561JR	0°C to +70°C	28-Lead SOIC	R-28
AD9561JR-REEL*	0°C to +70°C	28-Lead SOIC	R-28

*Tape and Reel ordered in multiples of 1000 ICs.

PIN DESCRIPTIONS

Pin	Name	Description
1–5	D3–D7	Digital Data Bits, D7 Is MSB
6	CLOCK	Clock Input
7	V_{DD}	+5 V Supply
8	GND	Ground Return
9	V_{DD}	+5 V Supply
10	GND	Ground Return
11	CAL OUT	Calibration Complete Output
12	POWER REDUCE	Place AD9561 in Sleep Mode
13	GND	Ground Return
14	R_{SET}	Ramp Current Set Resistor
15	GND	Ground Return
16	V_{DD}	+5 V Supply
17	CAL START	Initiates Calibration Cycle
18	RETRACE	Force Output High
19	V_{DD}	+5 V Supply
20	GND	Ground Return
21	OUT	Modulated Pulse Out
22	GND	Ground Return
23	V_{DD}	+5 V Supply
24	LEM/TEM	Controls Leading (1) or Trailing (0) Edge Modulation
25	SEM/DEM	Controls Single (1) or Dual (0) Edge Modulation
26–28	D0–D2	Digital Data Bits, D0 is LSB

CAUTION

ESD (electrostatic discharge) sensitive device. Electrostatic charges as high as 4000 V readily accumulate on the human body and test equipment and can discharge without detection. Although the AD9561 features proprietary ESD protection circuitry, permanent damage may occur on devices subjected to high energy electrostatic discharges. Therefore, proper ESD precautions are recommended to avoid performance degradation or loss of functionality.



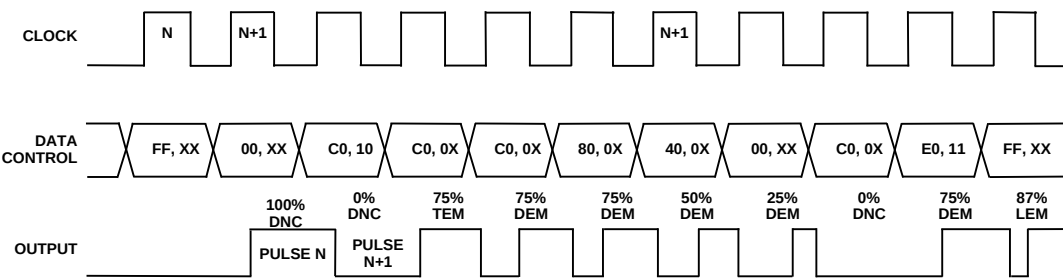


Figure 1. Pulse Pattern Example

THEORY OF OPERATION

General

The AD9561 is a mixed signal IC designed to provide high-speed pulse width modulation in laser printers and copiers. It uses high performance analog circuits to achieve high resolution pulse control without requiring the excessively high clock rates of an all digital solution.

Because of the sensitivity of analog circuits to digital crosstalk, PCB layout is critical for achieving optimum results. Please read the layout section at the end of this data sheet and follow suggestions completely for best performance.

The AD9561 was designed to facilitate either higher effective resolution or photo-realistic image reproduction on low cost laser print platforms. Its 8-bit pulse width resolution and pulse positioning capabilities combine to offer the highest level of gray shading and resolution enhancement flexibility available. It also includes an autocalibration circuit to minimize external components, and eliminates an extra burden on the system microprocessor.

The Functional Block Diagram illustrates the analog content, comprising ramp generators, DACs and comparators that generate a series of pulses. These pulses are combined in the output logic to form PWM OUT pulses whose width is proportional to the 8-bit DATA and whose position is determined by the SEM/DEM and LEM/TEM inputs.

The AD9561 employs a proprietary ramp topology that eliminates the loss of dynamic range at the ends of the ramp. The Functional Block Diagram is shown for illustration purposes only and does not represent the actual implementation.

Modulation Modes

Positioning the width controlled pulses at the beginning, middle or end of the CLOCK period, as shown in Figure 2, adds significantly to the flexibility of the AD9561. This is accomplished through control bit SEM/DEM and LEM/TEM. These acronyms represent Single-Edge Modulation/Dual-Edge Modulation and Leading-Edge Modulation/Trailing-Edge Modulation. SEM/DEM and LEM/TEM are collectively identified as CONTROL.

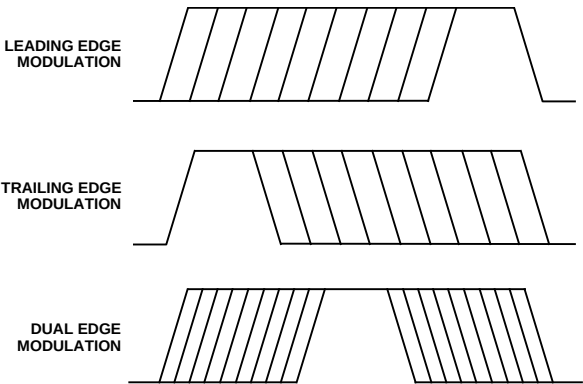


Figure 2. Modulation Modes

Pulse positioning within the CLOCK period is defined by the following table:

Table I. Truth Table

SEM/DEM	LEM/TEM	Alignment
1	1	LEM
1	0	TEM
0	X	DEM

Single-Edge Modulation offers two options in which one edge is modulated while the other remains fixed relative to the CLOCK. For Leading-Edge Modulation, the rising edge of the pulse is delayed from the leading edge of the CLOCK proportional to DATA, and the falling edge remains fixed at the end of the CLOCK period. This may also be called “right-hand justified.”

Similarly, Trailing-Edge Modulation has the rising edge fixed on the beginning of the CLOCK period and the falling edge delayed proportional to DATA. This can be called “left-hand justified.”

Dual-Edge Modulation is often called “center justified” because the delay of both edges varies relative to the CLOCK. With increasing values for DATA, pulse width increases with its center remaining constant proportional to the CLOCK.

Like DATA, modulation control inputs SEM/DEM, and LEM/TEM can be updated at the CLOCK rate up to 60 MHz.

Pulse Pattern Example

Figure 1 at the top of the previous page illustrates the PWM OUT of the AD9561 with various DATA and CONTROL inputs. The DATA format is Binary. In the Pulse Pattern Example, the Hexadecimal format is used, i.e., FF_H represents decimal 255.

The top line shows the CLOCK; the second shows DATA and CONTROL inputs, which are latched on the rising edge of CLOCK. The third line shows the resulting pulse.

The AD9561 DATA and CONTROL inputs are double latched. The OUTPUT pulse labeled "Pulse N" results from DATA and CONTROL values latched in by the first CLOCK, illustrating the one CLOCK period timing delay.

The CONTROL value number for pulse one is shown as xx. This means the value is not important because a 100% pulse will be output for any CONTROL value for DATA value 255 or FF_H. Likewise, OUTPUT Pulse N is noted as 100% DNC (do not care), also noting that CONTROL value is unimportant.

The fourth DATA/CONTROL value is C0/0X. This indicates that the level for LEM/TEM is unimportant when SEM/DEM is logic Level "0".

Selecting R_{SET}

Because the AD9561 must provide full range coverage of the CLOCK pulse period, the ramp time must be matched to the CLOCK period. All components for the ramp generators, except R_{SET}, are integrated in the AD9561.

R_{SET} is selected by the user to set the ramp time close to the CLOCK period. The ramps are generated by constant current sources charging on-chip capacitors.

R_{SET} can be chosen in the range from 226 Ω for 60 MHz operation to 16.5 kΩ for 1 MHz. Because the absolute value of the on-chip capacitor can vary by ±20%, the autocalibration circuit is included to fine tune the matching of the ramp time to the CLOCK period.

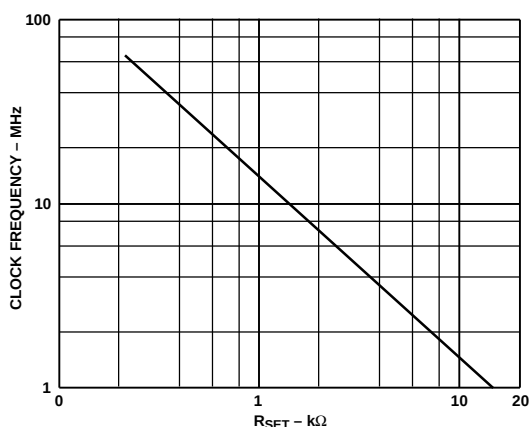


Figure 3. R_{SET} Values vs. CLOCK Frequency

Figure 3 shows approximate values for R_{SET} over the operating frequency range. The following equation should be used to determine R_{SET}:

$$R = \frac{30.2068 \times 10^9}{F^{1.04414}}$$

where F is the CLOCK frequency in Hz. The resistor value determined by the equation will generate a current near center-range of the autocalibration circuit.

Autocalibration

The AD9561 should be calibrated when power is applied to the system or after a power reduce cycle.

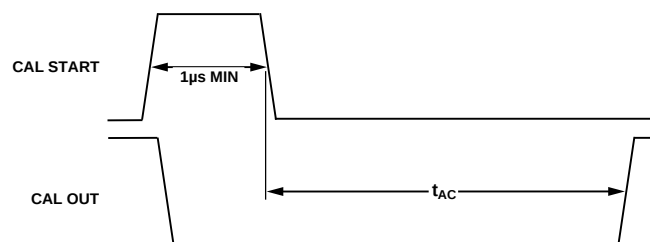


Figure 4. Autocalibration Timing

Autocalibration is initiated by applying a pulse of 1 μs minimum duration to Pin 17, CAL START. The CLOCK pulse should be applied continuously during calibration. As Figure 4 shows, the initial state of CAL OUT is not known.

During the CAL IN pulse, all internal logic is initialized for calibration and proper synchronization once calibration is complete; the falling edge of CAL IN initiates the Auto-CAL cycle.

Auto-CAL is not affected by the code applied to the DATA or CONTROL inputs. However, to assure that no pulses are generated during calibration, it is suggested that all digital inputs be held at Logic "0".

On the falling edge of CAL IN, the ramp's slope is set as slow as possible for the current R_{SET}. Figure 4 shows the RAMP slope increasing as autocalibration adds small incremental currents, until it crosses the internal REF LO before the end of the CLOCK period.

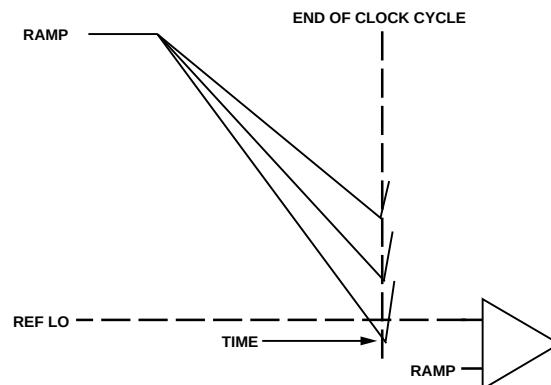


Figure 5. Autocalibration Conceptual

The calibration current is incremented on each 32nd CLOCK pulse until the full-scale ramp time is equal to the period of the CLOCK. Cal Complete is detected and CAL OUT goes high when the ramp crosses REF LO before it is reset by the next CLOCK. With a maximum of 64 incremental increases, the maximum autocalibration time, t_{AC} , can be calculated by the equation:

$$t_{AC} = \frac{32 \times 64}{F_C}$$

where: F_C = CLOCK frequency in Hertz

AD9561

This yields the maximum time from the trailing edge of CAL IN to the rising edge of CAL OUT. As an example, the maximum time required for auto-calibration for a system with clock frequency of 20 MHz is 102.4 ns plus the width of the CAL IN pulse.

Power Reduce

The POWER REDUCE function permits the user to power down all nonessential circuits when the printer is not active. Applying a Logic “0” to POWER REDUCE decreases the power supply requirement by approximately half.

APPLICATIONS

DATA Timing

Input DATA to the AD9561 is double latched. As a result of the internal timing, the OUTPUT is delayed more than one clock period from its corresponding DATA word. Figure 6 illustrates timing of DATA and CONTROL inputs relative to the CLOCK.

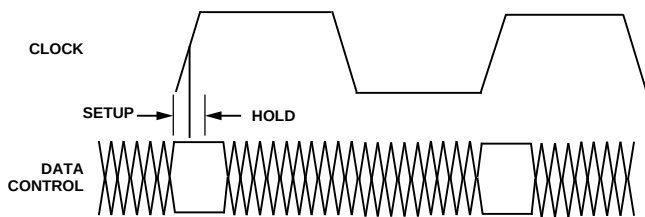


Figure 6. DATA and CONTROL Timing

The DATA and CONTROL inputs to the AD9561 are standard master-slave latches. Inputs are latched in on the rising edge of the CLOCK with 2 ns Set-Up time and 2 ns Hold time. This is a design improvement over the AD9560 meant to simplify interfacing the AD9561 to digital processing circuits.

A propagation delay exists between the CLOCK and OUTPUT pulses. The minimum propagation delay can be observed when alternating between codes 0 (00_H hexadecimal) and 255 (FF_H hexadecimal). This delay is due in part to normal circuit propagation; the remainder is due to time required to implement the proprietary ramp function. OUTPUT pulse transitions will typically occur 22 ns after the rising edge of CLOCK. It may vary from 10 ns–35 ns over temperature.

Transfer Function

Output pulse width increases with increasing DATA values. As the heavy line of Figure 7 shows, the transfer function of the AD9561 is slightly nonideal.

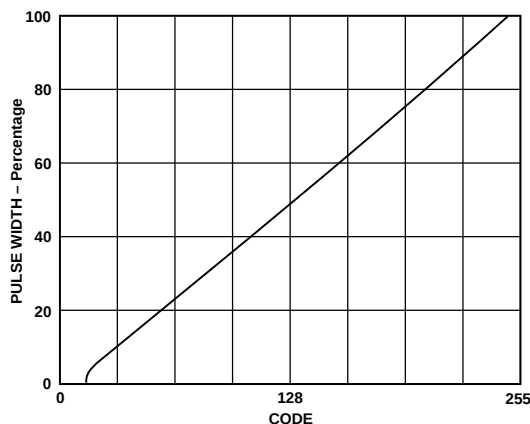


Figure 7. Pulse Width Transfer Function

An ideal transfer would give 0% (or 0 ns) pulse width for a Code 0. As the code is incremented in steps of one, the pulse width would increase by 0.39% until it reached 100% for Code 255.

When operating at high clock rates, several of the most narrow pulses do not reach valid logic Level “1” because of finite rise time. For example, at 20 MHz, a 1.95% pulse (code 5 or 05_H) would have an expected pulse width of 1 ns. Because the rise time is typically 1.5 ns, this pulse will not reach a full output level. Therefore, depending on the clock rate, the lowest set of codes produces a series of triangle waves increasing in width and amplitude until a pulse of approximately 3 ns–5 ns reaches a proper logic level. Thus, the transfer is flat until about 3 ns–5 ns pulse width (number of codes varies as a function of CLOCK frequency).

Because of the new ramp topology in the AD9561, the transfer function extends slightly greater than 100% (typically 102%) of the clock period. This has the effect of creating smooth transitions at the CLOCK period boundaries instead of the discontinuities produced by the AD9560.

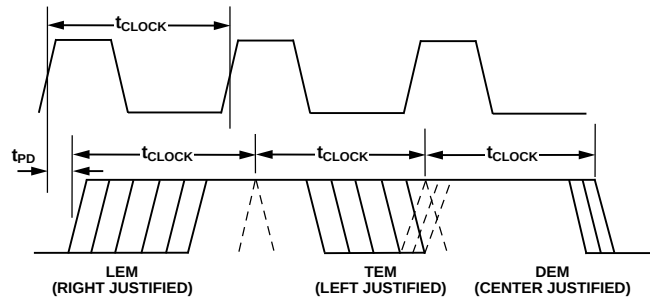


Figure 8. Dot Clock Period Transitions

As shown in Figure 8, a Leading Edge Modulated pulse followed by a Trailing Edge Modulated pulse will stay high from the rising edge of the first pulse to the falling edge of the second. This is due to Code 255 being designed to be typically 102% of the CLOCK period. (Dashed lines indicate where transitions would occur if the code for the following or preceding period were 0.) Likewise, no gap occurs for maximum width Trailing Edge Modulation to max pulse width for Dual Edge Modulation. Because the ending and starting characteristics of all modes are symmetrical, any combination of pulses that ends at the boundary of the first period and starts at the boundary of the second period will produce a continuous pulse across the boundary.

For the purposes of printing text, or any time absolute white or black is required, 0 is decoded and a 100% LOW is output in the next CLOCK cycle. Similarly, 255 is detected and the next pulse is 100% HIGH.

Retrace

The RETRACE function permits driving the output to a constant Logic High. For laser printer applications, applying a logic “1” to RETRACE holds the laser on during the retrace period so end of scan can be detected. Returning it to Logic Low gives control back to the input data bits D0–D7.

Grounding and Bypassing

Because the AD9561 uses analog circuits to achieve its superb gray scale resolution, caution must be exercised when incorporating it into the mostly digital controller card for a printer. Achieving the accuracy designed into the AD9561 requires that interference due to improper grounding, power supply noise and digital coupling be minimized by following good layout practices. It is strongly urged that all following recommendations be followed.

Factory characterization proves that a single ground plane dedicated to the AD9561 is most effective. This is atypical of many mixed signal circuits that use separate analog and digital grounds. Due to the operating speed of the AD9561, separate grounds result in erratic performance, which is eliminated by using a single isolated ground plane. This is because the DATA "low" value can be different from the ground value of the AD9561. All pins on the AD9561 labeled GROUND should be connected to the single dedicated ground plane. For best results, it is suggested that this plane be in the first interior layer under the IC. To assure logic level compatibility from the drive circuits to the AD9561, a single connection to the board's main ground is necessary.

The connection between the dedicated ground plane and the board's main ground should be parallel to the path of the digital signals interfacing to the AD9561. High frequency return current seeks the path most parallel to the signal current. Whenever a parallel path does not exist, ground bounce results.

CLOCK, DATA and CONTROL signal traces should run from the drive logic to the AD9561 in a group parallel to the connection between the system ground and the AD9561 ground. Using more than one signal plane will permit these traces to be as close to the ground interconnection as possible. This results in lowest impedance ground return and minimum ground interference due to digital switching.

Attention to subtle layout characteristics can yield significant improvement in performance of high speed mixed signal ICs. The AD9561 pinouts were chosen for maximum isolation of sensitive pins such as R_{SET} . The Pin 1 end of the IC should be oriented toward the source of the high speed digital inputs. This will help assure that these signal runs are short, with essentially the same length, thus having equal propagation delays. Most importantly, it will facilitate orienting traces to minimize coupling.

High speed digital traces including DATA, CLOCK, SEM/DEM, LEM/TEM and the OUTPUT should not pass under the body of the IC. The CLOCK, in particular, should enter perpendicular to the IC.

For best results, the OUTPUT trace should exit perpendicular to the IC and pass through a via to a signal layer under the ground plane. This trace or any resistor or other component of the output circuit should not be parallel to R_{SET} as electro-magnetic coupling can occur, causing the ramp current reference to be noisy and linearity to deteriorate.

Optimally, R_{SET} should be a chip resistor located on the same side of the board as the AD9561. It should be located close to Pin 14, without being close to the other IC pins. R_{SET} should be on the top of the board with the AD9561 with no vias to add stray reactance and additional coupling paths.

To reiterate the key layout considerations, high speed digital traces should not be located near the R_{SET} pin or under the center of the IC body.

A final interface consideration relates to rise/fall time of the high speed signals. Some logic families have rise and fall times as fast as 2 V/ns. This can result in on-chip parasitic coupling of these signals into the analog section. The undesirable effect can be eliminated by inserting series resistors in the DATA, SEM/DEM and LEM/TEM connections. These resistors, in conjunction with the capacitance of the input pin and bond pad, will form a low pass filter to limit slew rate of the signals. The value of these resistors should be chosen based on trading off slower rise and fall time to possible interference to set up and hold times for faster clock rates.

Power supply noise can also disrupt the linear circuits of the AD9561. Since switching power supplies are becoming the norm in most systems, caution should be exercised to minimize switching noise reaching the AD9561. The IC is designed for maximum power supply rejection. However, frequency content of switching supply noise often exceeds the frequency range of highest rejection. The preferred method would be to use a linear regulator from a higher supply voltage. If this is not practical, insert a ferrite bead in series with the supply connection. If possible, a V_{DD} plane or a substantial width trace should connect V_{DD} to Pin 7 first and then connect to each of the other V_{DD} pins with wide traces. Thorough decoupling will complete a low pass filter for the supply.

All V_{DD} connections should be connected together. 0.1 μ F chip capacitors should be connected as closely as possible to each V_{DD} pin to the dedicated ground plane. Laboratory results indicate that performance is maximized when these chip capacitors are mounted on the same side of the PC card as the AD9561. If mounting chip components on the same side as the AD9561 is not a preferred manufacturing method, due consideration is encouraged to make an exception, at least in the case of R_{SET} and as many decoupling capacitors as practical. Additionally, a 10 μ F tantalum capacitor should decouple the supply on the AD9561 side of the regulator or ferrite bead, also to the dedicated ground plane.

For a recommended layout, see the AD9561/PCB data sheet. A copy can be obtained by calling Applications Support at 1-800-ANALOGD.

OUTLINE DIMENSIONS
Dimensions shown in inches and (mm).

28-Lead SOIC
(R-28)

