PROCESS CP219

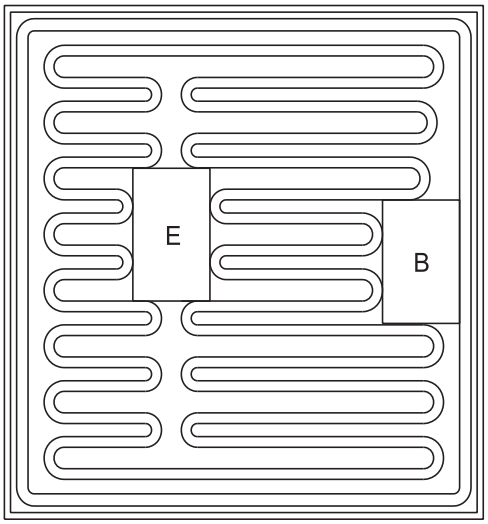
Power Transistor

NPN - High Current Transistor Chip

PROCESS DETAILS

Process	EPITAXIAL PLANAR
Die Size	83 x 83 MILS
Die Thickness	11 MILS
Base Bonding Pad Area	13.2 x 19.7 MILS
Emitter Bonding Pad Area	13.2 x 21.2 MILS
Top Side Metalization	Al - 30,000Å
Back Side Metalization	Au - 12,000Å

GEOMETRY



BACKSIDE COLLECTOR

R0

GROSS DIE PER 4 INCH WAFER

1,670

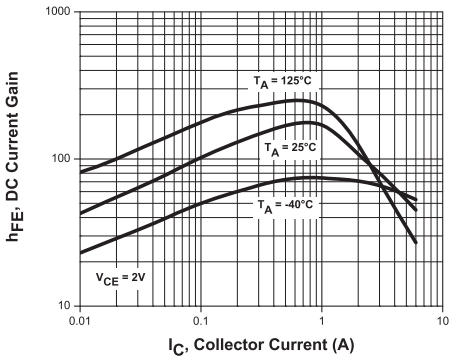
PRINCIPAL DEVICE TYPES

2N5336
2N5337
2N5338
2N5339
2N5427
2N5428
2N5429
2N5430
D44H11
CJD44H11

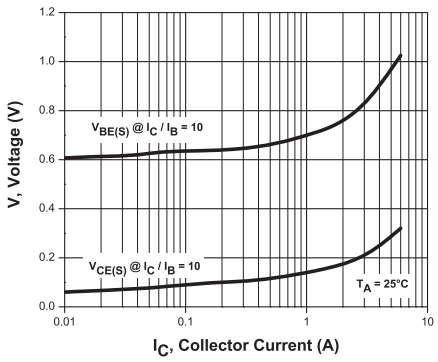
PROCESS CP219

Typical Electrical Characteristics

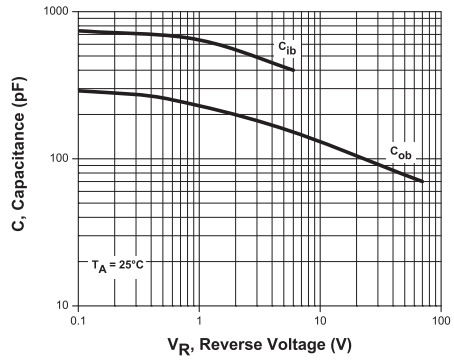
DC Current Gain



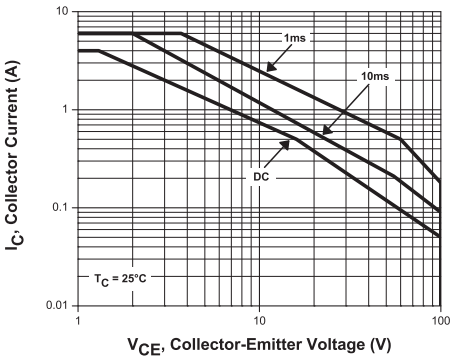
"ON" Voltage



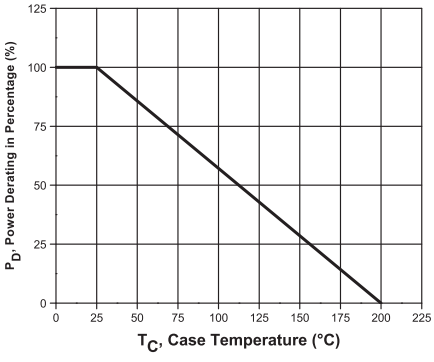
Capacitance



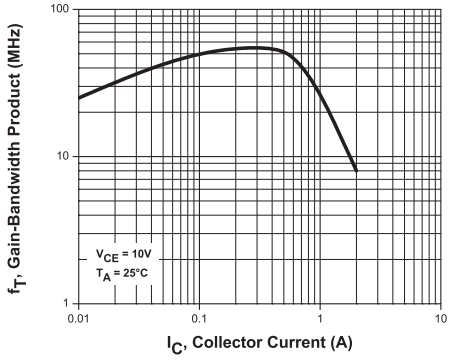
Safe Operating Area



Normalized Power Derating



Current Gain-Bandwidth Product



R3 (22-March 2010)