128MB- 16Mx64 DDR SDRAM UNBUFFERED W/PLL

FEATURES

- Double-data-rate architecture
- Speed of 100MHz, 133MHz and 166MHz
- Bi-directional data strobes (DQS)
- Differential clock inputs (CK & CK#)
- Programmable Read Latency 2,2,5 (clock)
- Programmable Burst Length (2,4,8)
- Programmable Burst type (sequential & interleave)
- Edge aligned data output, center aligned data input
- Auto and self refresh
- Serial presence detect
- JEDEC standard 200 pin SO-DIMM package
- Power Supply: 2.5V ± 0.25V

DESCRIPTION

The WED3DG6418S is a 16Mx64 Double Data Rate SDRAM memory module based on 128Mb DDR SDRAM component. The module consists of eight 16Mx8 DDR SDRAMs in 66 pin TSOP package mounted on a 200 Pin FR4 substrate.

Synchronous design allows precise cycle control with the use of system clock. Data I/O transactions are possible on both edges and Burst Lenths allow the same device to be useful for a variety of high bandwidth, high performance memory system applications.

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PIN CONFIGURATIONS

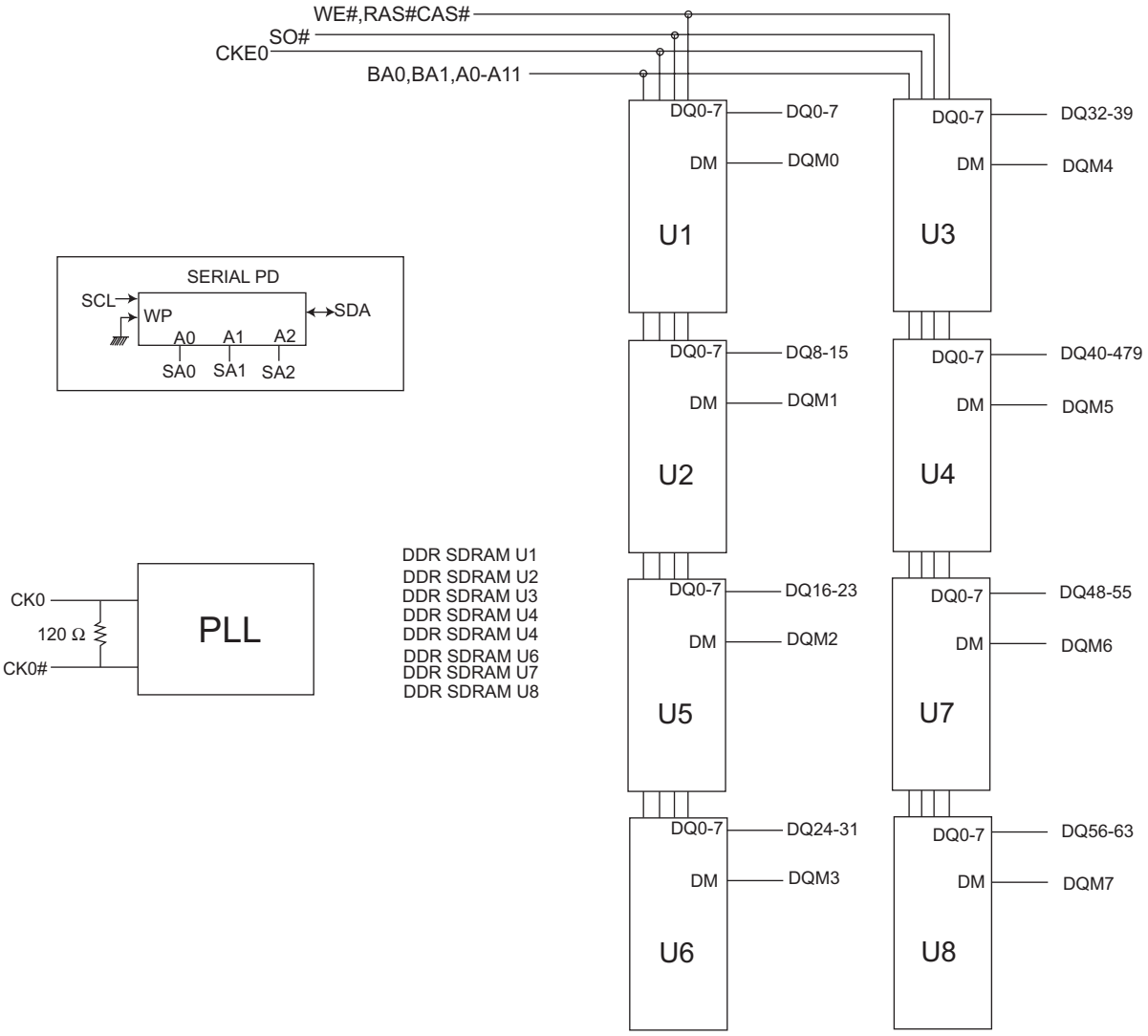
Pin	Symbol	Pin	Symbol	Pin	Symbol	Pin	Symbol
1	V_{REF}	51	V_{SS}	101	A9	151	DQ42
2	V_{REF}	52	V_{SS}	102	A8	152	DQ46
3	V_{SS}	53	DQ19	103	V_{SS}	153	DQ43
4	V_{SS}	54	DQ23	104	V_{SS}	154	DQ47
5	DQ0	55	DQ24	105	A7	155	V_{CC}
6	DQ4	56	DQ28	106	A6	156	V_{CC}
7	DQ1	57	V_{CC}	107	A5	157	V_{CC}
8	DQ5	58	V_{CC}	108	A4	158	NC
9	V_{CC}	59	DQ25	109	A3	159	V_{SS}
10	V_{CC}	60	DQ29	110	A2	160	NC
11	DQS0	61	DQS3	111	A1	161	V_{SS}
12	DM0	62	DM3	112	A0	162	V_{SS}
13	DQ2	63	V_{SS}	113	V_{CC}	163	DQ48
14	DQ6	64	V_{SS}	114	V_{CC}	164	DQ52
15	V_{SS}	65	DQ26	115	A10/AP	165	DQ49
16	V_{SS}	66	DQ30	116	BA1	166	DQ53
17	DQ3	67	DQ27	117	BA0	167	V_{CC}
18	DQ7	68	DQ31	118	RAS#	168	V_{CC}
19	DQ8	69	V_{CC}	119	WE#	169	DQS6
20	DQ12	70	V_{CC}	120	CAS#	170	DM6
21	V_{CC}	71	NC	121	CSO	171	DQ50
22	V_{CC}	72	NC	122	NC	172	DQ54
23	DQ9	73	NC	123	NC	173	V_{SS}
24	DQ13	74	NC	124	NC	174	V_{SS}
25	DQS1	75	V_{SS}	125	V_{SS}	175	DQ51
26	DM1	76	V_{SS}	126	V_{SS}	176	DQ55
27	V_{SS}	77	DQS8	127	DQ32	177	DQ56
28	V_{SS}	78	DM8	128	DQ36	178	DQ60
29	DQ10	79	NC	129	DQ33	179	V_{CC}
30	DQ14	80	NC	130	DQ37	180	V_{CC}
31	DQ11	81	V_{CC}	131	V_{CC}	181	DQ57
32	DQ15	82	V_{CC}	132	V_{CC}	182	DQ61
33	V_{CC}	83	NC	133	DQS4	183	DQS7
34	V_{CC}	84	NC	134	DM4	184	DM7
35	CK0	85	NC	135	DQ34	185	V_{SS}
36	V_{CC}	86	NC	136	DQ38	186	V_{SS}
37	CK0#	87	V_{SS}	137	V_{SS}	187	DQ58
38	V_{SS}	88	V_{SS}	138	V_{SS}	188	DQ62
39	V_{SS}	89	NC	139	DQ35	189	DQ59
40	V_{SS}	90	V_{SS}	140	DQ39	190	DQ63
41	DQ16	91	NC	141	DQ40	191	V_{CC}
42	DQ20	92	V_{CC}	142	DQ44	192	V_{CC}
43	DQ17	93	V_{CC}	143	V_{CC}	193	SDA
44	DQ21	94	V_{CC}	144	V_{CC}	194	SA0
45	V_{CC}	95	NC	145	DQ41	195	SCL
46	V_{CC}	96	CKE0	146	DQ45	196	SA1
47	DQS2	97	NC	147	DQS5	197	V_{CCSPD}
48	DM2	98	NC	148	DM5	198	SA2
49	DQ18	99	NC	149	V_{SS}	199	V_{CCID}
50	DQ22	100	A11	150	V_{SS}	200	NC

PIN NAMES

A0 – A11	Address input (Multiplexed)
BA0-BA1	Bank Select Address
DQ0-DQ63	Data Input/Output
DQS0-DQS8	Data Strobe Input/Output
CK0	Clock input
CK0#	Clock input
CKE0	Clock Enable Input
CS0#	Chip select Input
RAS#	Row Address Strobe
CAS#	Column Address Strobe
WE#	Write Enable
DQM0-DQM8	Data-In Mask
V_{CC}	Power Supply (2.5V)
V_{CCQ}	Power Supply for DQS (2.5V)
V_{SS}	Ground
V_{REF}	Power Supply for Reference
V_{CCSPD}	Serial EEPROM Power Supply (2.3V to 3.6V)
SDA	Serial data I/O
SCL	Serial clock
SA0-SA2	Address in EEPROM
V_{CCID}	V_{CC} Identification Flag
NC	No Connect

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FUNCTIONAL BLOCK DIAGRAM



Absolute Maximum Ratings

Parameter	Symbol	Value	Units
Voltage on any pin relative to V_{SS}	V_{IN}, V_{OUT}	-0.5 ~ 3.6	V
Voltage on V_{CC} supply relative to V_{SS}	V_{CC}, V_{CCQ}	-1.0 ~ 3.6	V
Storage Temperature	T_{STG}	-55 ~ +150	°C
Power Dissipation	P_D	8	W
Short Circuit Current	I_{OS}	50	mA

Note:

Permanent device damage may occur if "ABSOLUTE MAXIMUM RATINGS" are exceeded.
Functional operation should be restricted to recommended operating condition.
Exposure to higher than recommended voltage for extended periods of time could affect device reliability.

DC CHARACTERISTICS

(t_A = 0 to 70°C, V_{CC} = 2.5V ± 0.2V)

Parameter	Symbol	Min	Max	Unit
Supply Voltage	V_{CC}	2.3	2.7	V
Supply Voltage	V_{CCQ}	2.3	2.7	V
Reference Voltage	V_{REF}	V_{CCQ}/2-50mV	V_{CCQ}/2+50mV	V
Termination Voltage	V_{TT}	V_{REF}-0.04	V_{REF}+0.04	V
Input High Voltage	V_{IH}	V_{REF}+0.15	V_{CCQ}+0.3	V
Input Low Voltage	V_{IL}	-0.3	V_{REF}+0.15	V
Output High Voltage	V_{OH}	V_{TT}+0.76	—	V
Output Low Voltage	V_{OL}	—	V_{TT}-0.76	V

CAPACITANCE

(t_A = 23°C, f = 1MHz, V_{CC} = 3.3V, V_{REF}=1.4V ± 200mV)

Parameter	Symbol	Min	Max	Unit
Input Capacitance (A0-A12)	$C_{IN}1$	-	34	pF
Input Capacitance (RAS#,CAS#,WE#)	$C_{IN}2$	-	34	pF
Input Capacitance (CKE0)	$C_{IN}3$	-	34	pF
Input Capacitance (CK0, CK0#)	$C_{IN}4$	-	30	pF
Input Capacitance (CS0#)	$C_{IN}5$	-	30	pF
Input Capacitance (DQM0-DQM8)	$C_{IN}6$	-	10	pF
Input Capacitance (BA0-BA1)	$C_{IN}7$	-	45	pF
Data input/output capacitance (DQ0-DQ63)(DQS)	C_{OUT}	-	10	pF

I_{DD} SPECIFICATIONS AND TEST CONDITIONS

(Recommended operating conditions, t_A = 0 to 70°C, V_{CCQ} = 2.5V ± 0.2V, V_{CC} = 2.5V ± 0.2V)

Parameter	Symbol	Conditions	DDR333@CL=2.5 Max	DDR266@CL=2, 2.5 Max	DDR200@CL=2 Max	Units
Operating Current	I_{DD0}	One device bank; Active = Precharge; t_{RC}=t_{RC}(MIN); t_{CK}=t_{CK} (MIN); DQ, DM and DQS inputs changing once per clock cycle; Address and control inputs changing once every two cycles.	840	760	680	mA
Operating Current	I_{DD1}	One device banks; Active-Read-Precharge; Burst = 2; t_{RC}=t_{RC}(MIN); t_{CK}=t_{CK} (MIN); I_{OUT}=0mA; Address and control inputs changing once per clock cycle.	1040	960	880	mA
Precharge Power-Down Standby Current	I_{DD2P}	All device bank idle; Power-down mode; t_{CK}=t_{CK}(MIN); CKE=(low)	24	24	24	mA
Idle Standby Current	I_{DD2F}	CS# = High; All device banks idle; t_{CK}=t_{CK}(MIN); CKE = high; Address and other control inputs changing once per clock cycle. V_{IN} = V_{REF} for DQ, DQS and DM.	200	180	160	mA
Active Power-Down Standby Current	I_{DD3P}	One device bank active; Power-down mode; t_{CK}(MIN); CKE=(low)	280	280	225	mA
Active Standby Current	I_{DD3N}	CS# = High; CKE = High; One device bank; Active-Precharge; t_{RC}=t_{RAS}(MAX); t_{CK}=t_{CK}(MIN); DQ, DM and DQS inputs changing twice per clock cycle; Address and other control inputs changing once per clock cycle	495	440	360	mA
Operating Current	I_{DD4R}	Burst = 2; Reads; Continous burst; Once device bank active; Address and control inputs changing once per clock cycle; t_{CK}=t_{CK}(MIN); I_{OUT}=0mA	1280	1140	960	mA
Operating Current	I_{DD4W}	Burst=2; Writes; Continous burst; Once device bank active; Address and control inputs changing once per clock cycle; t_{CK}=t_{CK}(MIN); DQ,DM and DQS inputs changing twice per clock cycle.	1216	1040	815	mA
Auto Refresh Current	I_{DD5}	t_{RC}=t_{RC}(MIN)	1520	1440	1315	mA
Self Refresh Current	I_{DD6}	CKE £ 0.2V	16	16	16	mA
Operating Current	I_{DD7A}	Four bank interleaving Reads (BL=4) with auto precharge with t_{RC}=t_{RC}(MIN); t_{CK}=t_{CK}(MIN); Address and control input change only during Active Read or Write commands.	2640	2400	1920	mA

* Module I_{DD} was calculated on the basis of component I_{DD} and can be different measured according to DQ loading cap.

DETAILED TEST CONDITIONS FOR DDR SDRAM I_{DD1} & I_{DD7A}

I_{DD1} : OPERATING CURRENT: ONE BANK

1. Typical Case : V_{CC} = 2.5V, T = 25°C
2. Worst Case : V_{CC} = 2.7V, T = 10°C
3. Only one bank is accessed with t_{RC} (min), Burst Mode, Address and Control inputs on NOP edge are changing once per clock cycle.
I_{OUT} = 0mA
4. Timing patterns
   -DDR200 (100Mhz, CL = 2) : t_{CK} = 10ns, CL2, BL = 4, t_{RCD} = 2*t_{CK}, t_{RAS} = 5*t_{CK}
   Read : A0 N R0 N N P0 N A0 N - repeat the same timing with random address changing; 50% of data changing at every burst

   -DDR266B (133Mhz, CL = 2.5): t_{CK} = 7.5ns, CL = 2.5, BL = 4, t_{RCD} = 3*t_{CK}, t_{RC} = 9*t_{CK}, t_{RAS} = 5*t_{CK}
   Read : A0 N N R0 N P0 N N N A0 N - repeat the same timing with random address changing; 50% of data changing at every burst

   -DDR266A (133Mhz, CL = 2) : t_{CK} = 7.5ns, CL = 2, BL = 4, t_{RCD} = 3*t_{CK}, t_{RC} = 9*t_{CK}, t_{RAS} = 5*t_{CK}
   Read : A0 N N R0 N P0 N N N A0 N - repeat the same timing with random address changing; 50% of data changing at every burst

   -DDR333 (166MHz, CL = 2.5) : t_{CK} = 6ns, CL = 2.5, BL = 4, t_{RCD} = 10*t_{CK}, t_{RAS} = 7*t_{CK}
   Read " A0 N N R0 N P0 N N N A0 N - repeat the same timing with random address changing; 50% of data changing at every burst.

I_{DD7A} : OPERATING CURRENT : FOUR BANK OPERATION

1. Typical Case : V_{cc} = 2.5V, T = 25°C
2. Worst Case : V_{cc} = 2.7V, T = 10°C
3. Four banks are being interleaved with t_{RC} (min), Burst Mode, Address and Control inputs on NOP edge are not changing.
I_{OUT} = 0mA
4. Timing patterns
   - DDR200 (100Mhz, CL = 2) : t_{CK} = 10ns, CL2, BL = 4, t_{RRD} = 2*t_{CK}, t_{RCD} = 3*t_{CK}, Read with autoprecharge
   Read : A0 N A1 R0 A2 R1 A3 R2 A0 R3 A1 R0 - repeat the same timing with random address changing; 100% of data changing at every burst

   -DDR266B (133Mhz, CL = 2.5) : t_{CK} = 7.5ns, CL = 2.5, BL = 4, t_{RRD} = 2*t_{CK}, t_{RCD} = 3*t_{CK}
   Read with autoprecharge
   Read : A0 N A1 R0 A2 R1 A3 R2 N R3 A0 N A1 R0 - repeat the same timing with random address changing; 100% of data changing at every burst

   -DDR266A (133Mhz, CL = 2) : t_{CK} = 7.5ns, CL2 = 2, BL = 4, t_{RRD} = 2*t_{CK}, t_{RCD} = 3*t_{CK}
   Read : A0 N A1 R0 A2 R1 A3 R2 N R3 A0 N A1 R0 - repeat the same timing with random address changing; 100% of data changing at every burst

   -DDR333 (166MHz, CL = 2.5) : t_{CK} = 6ns, CL = 2.5, BL = 4, t_{RRD} = 2*t_{CK}, t_{RCD} = 3*t_{CK}, Read with autoprecharge
   Read : A0 N A1 R0 A2 R1 A3 R2 N R3 A0 N A1 R0 - repeat the same timing with random address changing; 100% of data changing at every burst

Legend : A = Activate, R = Read, W = Write, P = Precharge, N = NOP

ORDER INFORMATION

Part Number	Speed	CAS Latency
WED3EG6418S335D4	166MHz/333Mbps	CL=2.5
WED3EG6418S262D4	133MHz/266Mbps	CL=2
WED3EG6418S265D4	133MHz/266Mbps	CL=2.5
WED3EG6418S202D4	100MHz/200Mbps	CL=2

PACKAGE DIMENSIONS

ALL DIMENSIONS ARE IN INCHES

