TEXAS INSTRUMENTS

SN74LVC1G07-Q1 - 具有开漏输出的单路缓冲器/驱动器

1 特性

- 符合汽车类 应用要求
- 具有符合 AEC-Q100 标准的下列特性：
  - 器件温度等级 1：–40°C 至 +125°C 的环境工作温度范围
  - 2000V 器件人体放电模型 (HBM) ESD 分类等级 2
  - 1000V 器件充电器件模型 (CDM) ESD 分类等级 C5
- 支持 5V V_{CC} 运行
- 输入与开漏输出支持最高 5.5V 的电压
- 电压为 3.3V 时，t_{pd} 最大值为 5.7ns
- 低功耗，I_{CC} 最大值为 10μA
- 电压为 3.3V 时，输出驱动为 ±24mA
- I_{off} 支持局部断电模式运行

2 应用

- 汽车信息娱乐系统
- 汽车 ADAS 摄像头和融合系统
- 汽车车身控制模块 AV 接收器
- 汽车 HEV/动力总成
- 蓝光播放器与家庭影院
- DVD 录像机和播放器
- 台式机或笔记本电脑
- 数字音频广播或互联网广播播放器
- 数码摄像机 (DVC)
- 嵌入式 PC
- GPS：个人导航设备
- 移动互联网设备
- 网络投影仪前端
- 便携式媒体播放器
- 专业音频混合器
- 烟雾探测器
- 固态硬盘 (SSD)：企业级
- 高清 (HDTV)
- 平板电脑：企业级
- 音频接口盒：便携式
- DLP 正投影系统
- DVR 和 DVS
- 数码相框 (DPF)
- 数码相机

3 说明

SN74LVC1G07-Q1 是一款单通道开漏缓冲器/驱动器，适用于汽车 应用。的高速串行链路的稳定性。按照设计，该器件可在 1.65V 至 5.5V V_{CC} 电压下运行。

SN74LVC1G07-Q1 器件的输出为漏极开路，可连接其它开漏输出，以实施低电平有效的连线 OR 或高电平有效的连线 AND 功能。最大灌电流为 32mA。

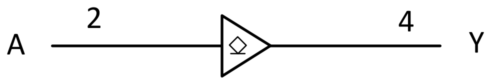
该器件完全 适用于 I_{off} 为了部分断电的应用。I_{off} 电路会禁用输出，从而在器件掉电时防止电流回流损坏器件。

器件信息[1]

器件型号	封装（引脚）	封装尺寸（标称值）
SN74LVC1G07-Q1	SOT-23 (5)	2.90mm × 1.60mm
	SC70 (5)	2.00mm × 1.25mm
	SON (6)	1.45mm × 1.00mm

(1) 如需了解所有可用封装，请参阅数据表末尾的可订购产品附录。

逻辑图（正逻辑）



目录

4 修订历史记录

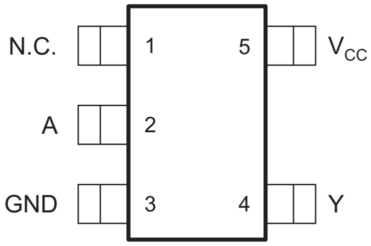
注：之前版本的页码可能与当前版本有所不同。

Changes from Revision A (February 2017) to Revision B	Page
• 已添加 向 器件信息表添加了 DRY 封装选项	1
• Added DRY package as Product Preview device option to Pin Configuration and Functions	3
• Added DRY package to Thermal Information table	4

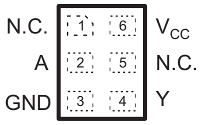
Changes from Original (March 2011) to Revision A	Page
• 已添加 *应用，器件信息表、ESD 额定值表、典型特性、功能 说明部分、器件功能模式、应用和实施部分、电源相关建议部分、布局部分、器件和文档支持部分以及机械、封装和可订购信息* 部分。	1
• Changed $R_{\theta JA}$ value for DBV (SOT-23) package from: 206 to: 269.3	4

5 Pin Configuration and Functions

DBV or DCK Package
5-Pin SOT-23 or SC70
Top View



DRY Package
6-Pin SON
Transparent Top View



N.C. – No internal connection

See mechanical drawings for dimensions.

Pin Functions

PIN			DESCRIPTION
NAME	DBV, DCK	DRY	
N.C.	1	1, 5	Not connected
A	2	2	Input
GND	3	3	Ground
Y	4	4	Output
V_{CC}	5	6	Power Pin

6 Specifications

6.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)(1)

			MIN	MAX	UNIT
V_{CC}	Supply voltage		–0.5	6.5	V
V_I	Input voltage(2)		–0.5	6.5	V
V_O	Voltage range applied to any output in the high-impedance or power-off state(2)		–0.5	6.5	V
V_O	Voltage range applied to any output in the high or low state(2)(3)		–0.5	6.5	V
I_{IK}	Input clamp current	$V_I < 0$		–50	mA
I_{OK}	Output clamp current	$V_O < 0$		–50	mA
I_O	Continuous output current			±50	mA
	Continuous current through V_{CC} or GND			±100	mA
T_J	Operating junction temperature			150	°C
T_{stg}	Storage temperature		–65	150	°C

(1) Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) The input and output negative-voltage ratings may be exceeded if the input and output current ratings are observed.
(3) The value of V_{CC} is provided in the recommended operating conditions table.

6.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human-body model (HBM), per AEC Q100-002(1)	±2000	V
		Charged-device model (CDM), per AEC Q100-011	±1000	

(1) AEC Q100-002 indicates that HBM stressing shall be in accordance with the ANSI/ESDA/JEDEC JS-001 specification.

6.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)(1)

			MIN	MAX	UNIT
V_{CC}	Supply voltage	Operating	1.65	5.5	V
		Data retention only	1.5		
V_{IH}	High-level input voltage	V_{CC} = 1.65 V to 1.95 V	0.65 × V_{CC}		V
		V_{CC} = 2.3 V to 2.7 V	1.7		
		V_{CC} = 3 V to 3.6 V	2		
		V_{CC} = 4.5 V to 5.5 V	0.7 × V_{CC}		
V_{IL}	Low-level input voltage	V_{CC} = 1.65 V to 1.95 V		0.35 × V_{CC}	V
		V_{CC} = 2.3 V to 2.7 V		0.7	
		V_{CC} = 3 V to 3.6 V		0.8	
		V_{CC} = 4.5 V to 5.5 V		0.3 × V_{CC}	
V_I	Input voltage		0	5.5	V
V_O	Output voltage		0	5.5	V
I_{OL}	Low-level output current	V_{CC} = 1.65 V		4	mA
		V_{CC} = 2.3 V		8	
		V_{CC} = 3 V		16	
				24	
		V_{CC} = 4.5 V		32	
Δt/Δv	Input transition rise or fall rate	V_{CC} = 1.8 V ±0.15 V, 2.5 V ± 0.2 V		20	ns/V
		V_{CC} = 3.3 V ± 0.3 V		10	
		V_{CC} = 5 V ± 0.5 V		5	
T_A	Operating free-air temperature		–40	125	°C

(1) All unused inputs of the device must be held at V_{CC} or GND to ensure proper device operation. Refer to the TI application report, *Implications of Slow or Floating CMOS Inputs*, SCBA004.

6.4 Thermal Information

THERMAL METRIC(1)		SN74LVC1G07-Q1			UNIT
		DBV (SOT-23)	DCK (SC70)	DRY (SON)	
		5 PINS	5 PINS	6 PINS	
$R_{\theta JA}$	Junction-to-ambient thermal resistance	269.3	301.2	439	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	175.2	186.5	277	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	104.9	111.8	271	°C/W
ψ_{JT}	Junction-to-top characterization parameter	73.4	78.3	84	°C/W
ψ_{JB}	Junction-to-board characterization parameter	104.5	110.6	271	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	–	–	–	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report.

6.5 Electrical Characteristics

over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	V_{CC}	MIN	TYP(1)	MAX	UNIT
V_{OL}		I_{OL} = 100 µA	1.65 V to 5.5 V			0.1	V
		I_{OL} = 4 mA	1.65 V			0.45	
		I_{OL} = 8 mA	2.3 V			0.3	
		I_{OL} = 16 mA	3 V			0.4	
		I_{OL} = 24 mA				0.55	
		I_{OL} = 32 mA	4.5 V			0.55	
I_I	A input	V_I = 5.5 V or GND	0 to 5.5 V			±5	µA
I_{off}		V_I or V_O = 5.5 V	0			±10	µA
I_{CC}		V_I = 5.5 V or GND, I_O = 0	1.65 V to 5.5 V			10	µA
ΔI_{CC}		One input at V_{CC} – 0.6 V, Other inputs at V_{CC} or GND	3 V to 5.5 V			500	µA
C_i		V_I = V_{CC} or GND	3.3 V		4		pF
C_o		V_O = V_{CC} or GND	3.3 V		5		pF

(1) All typical values are at V_{CC} = 3.3 V, T_A = 25°C.

6.6 Switching Characteristics

over recommended operating free-air temperature range (unless otherwise noted) (see Figure 3)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC} = 1.8 V ± 0.15 V		V_{CC} = 2.5 V ± 0.2 V		V_{CC} = 3.3 V ± 0.3 V		V_{CC} = 5 V ± 0.5 V		UNIT
			MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	
t_{pd}	A	Y	2.4	9.8	1	7.0	1.5	5.7	1	4.9	ns

6.7 Operating Characteristics

T_A = 25°C

PARAMETER		TEST CONDITIONS	V_{CC} = 1.8 V	V_{CC} = 2.5 V	V_{CC} = 3.3 V	V_{CC} = 5 V	UNIT
			TYP	TYP	TYP	TYP	
C_{pd}	Power dissipation capacitance	f = 10 MHz	3	3	4	6	pF

6.8 Typical Characteristics

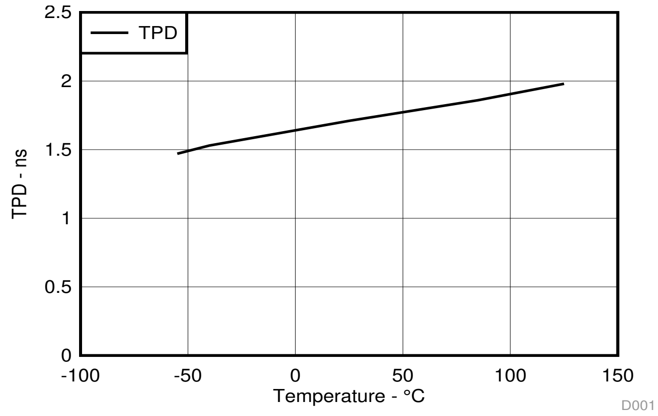


Figure 1. TPD Across Temperature at 3.3V Vcc

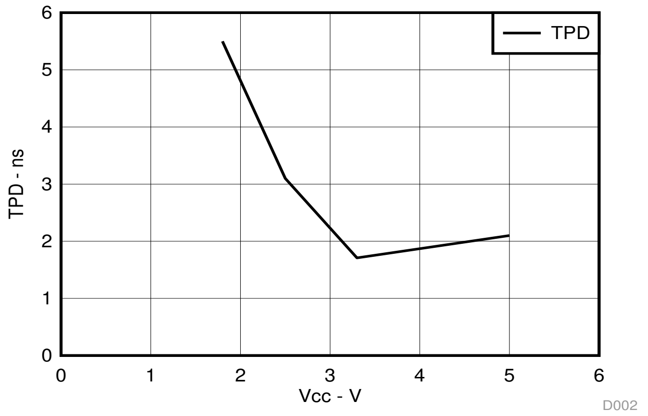
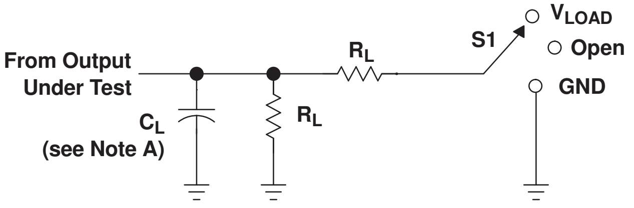


Figure 2. TPD Across Vcc at 25°C

7 Parameter Measurement Information (Open Drain)

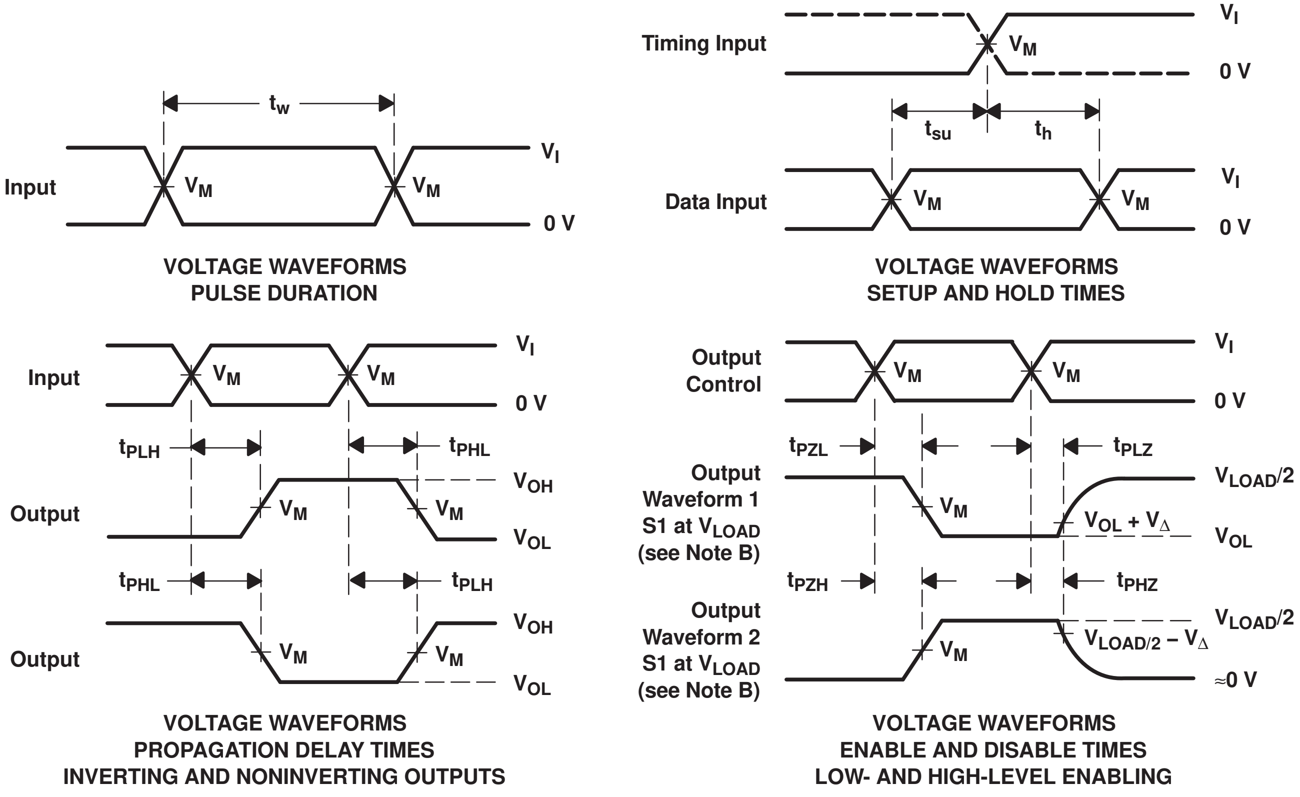
7.1 PMI



LOAD CIRCUIT

TEST	S1
t_{PZL} (see Notes E and F)	V_{LOAD}
t_{PLZ} (see Notes E and G)	V_{LOAD}
t_{PHZ}/t_{PZH}	V_{LOAD}

V_{CC}	INPUT		V_M	V_{LOAD}	C_L	R_L	V_Δ
	V_I	t_r/t_f					
1.8 V ± 0.15 V	V_{CC}	≤ 2 ns	$V_{CC}/2$	2 × V_{CC}	30 pF	1 kΩ	0.15 V
2.5 V ± 0.2 V	V_{CC}	≤ 2 ns	$V_{CC}/2$	2 × V_{CC}	30 pF	500 Ω	0.15 V
3.3 V ± 0.3 V	3 V	≤ 2.5 ns	1.5 V	6 V	50 pF	500 Ω	0.3 V
5 V ± 0.5 V	V_{CC}	≤ 2.5 ns	$V_{CC}/2$	2 × V_{CC}	50 pF	500 Ω	0.3 V



NOTES:
- A. C_L includes probe and jig capacitance.
- B. Waveform 1 is for an output with internal conditions such that the output is low, except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high, except when disabled by the output control.
- C. All input pulses are supplied by generators having the following characteristics: PRR ≤ 10 MHz, Z_O = 50 Ω.
- D. The outputs are measured one at a time, with one transition per measurement.
- E. Since this device has open-drain outputs, t_{PLZ} and t_{PZL} are the same as t_{pd}.
- F. t_{PZL} is measured at V_M.
- G. t_{PLZ} is measured at $V_{OL} + V_\Delta$.
- H. All parameters and waveforms are not applicable to all devices.

Figure 3. Load Circuit And Voltage Waveforms

8 Detailed Description

8.1 Overview

The SN74LVC1G07-Q1 device contains one open-drain buffer with a maximum sink current of 32 mA. This device is fully specified for partial-power-down applications using I_{off}. The I_{off} circuitry disables the outputs, preventing damaging current backflow through the device when it is powered down.

8.2 Functional Block Diagram

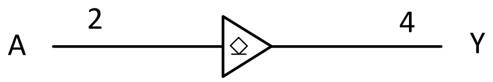


Figure 4. Logic Diagram (Positive Logic)

8.3 Feature Description

- Wide operating voltage range.
  - Operates from 1.65 V to 5.5 V.
- Allows down-voltage translation.
- Inputs and outputs accept voltages to 5.5 V.
- I_{off} feature allows voltages on the inputs and outputs, when V_{CC} is 0 V.

8.4 Device Functional Modes

Table 1 lists the functional modes of SN74LVC1G07-Q1.

Table 1. Function Table

INPUT A	OUTPUT Y
L	L
H	Z

9 Application and Implementation

NOTE

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

9.1 Application Information

The SN74LVC1G07-Q1 is a high drive CMOS device that can be used to implement a high output drive buffer, such as an LED application. It can sink 32 mA of current at 4.5 V making it ideal for high drive and wired-OR/AND functions. It is good for high speed applications up to 100 MHz. The inputs are 5.5 V tolerant allowing it to translate up/down to V_{CC}.

9.2 Typical Application

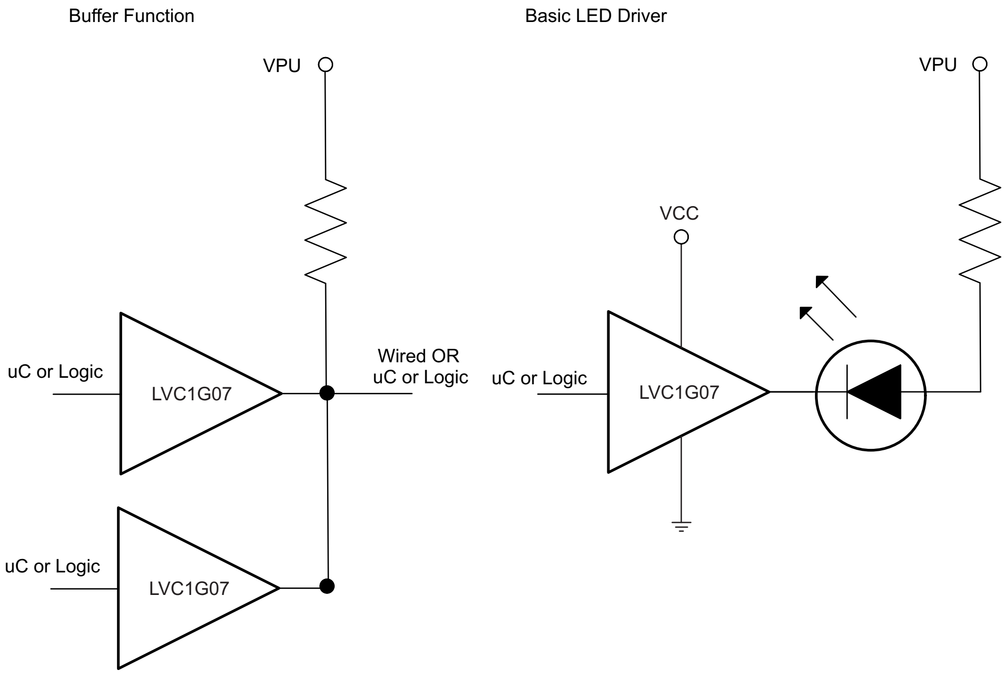


Figure 5. Typical Application-SN74LVC1G07-Q1

9.2.1 Design Requirements

This device uses CMOS technology and has high-output drive. Care should be taken to avoid bus contention because it may drive currents that would exceed maximum limits. The high drive also creates fast edges into light loads; so, routing and load conditions should be considered to prevent ringing.

9.2.2 Detailed Design Procedure

1. Recommended Input Conditions
   - Rise time and fall time specs. See ($\Delta t/\Delta V$) in the *Recommended Operating Conditions* table.
   - Specified high and low levels. See (V_{IH} and V_{IL}) in the *Recommended Operating Conditions* table.
   - Inputs are over-voltage tolerant allowing them to go as high as (V_I max) in the *Recommended Operating Conditions* table at any valid V_{CC}.
2. Recommended Output Conditions
   - Load currents should not exceed (I_O max) per output and should not exceed (Continuous current through V_{CC} or GND) total current for the part. These limits are located in the *Absolute Maximum Ratings* table.

Typical Application (continued)

– Outputs should not be pulled above 5.5 V.

9.2.3 Application Curve

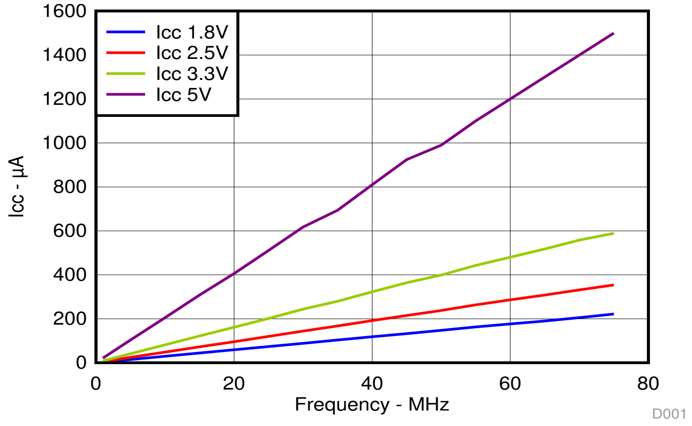


Figure 6. Icc vs Frequency

10 Power Supply Recommendations

The power supply can be any voltage between the min and max supply voltage rating located in the *Recommended Operating Conditions* table.

Each V_{CC} pin should have a good bypass capacitor to prevent power disturbance. A 0.1-µF capacitor is recommended for devices with a single supply. If there are multiple V_{CC} pins then a 0.01-µF or 0.022-µF capacitor is recommended for each power pin. It is acceptable to parallel multiple bypass caps to reject different frequencies of noise. 0.1-µF and 1-µF capacitors are commonly used in parallel. The bypass capacitor should be installed as close to the power pin as possible for best results.

11 Layout

11.1 Layout Guidelines

When using multiple bit logic devices inputs should not ever float. In many cases, functions or parts of functions of digital logic devices are unused; for example, when only two inputs of a triple-input AND gate are used or only 3 of the 4 buffer gates are used. Such input pins should not be left unconnected because the undefined voltages at the outside connections result in undefined operational states. Specified below are the rules that must be observed under all circumstances. All unused inputs of digital logic devices must be connected to a high or low bias to prevent them from floating. The logic level that should be applied to any particular unused input depends on the function of the device. Generally, they are tied to GND or V_{CC}, whichever is more convenient.

11.2 Layout Example

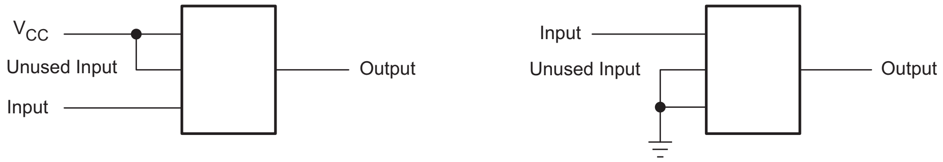


Figure 7. Layout Example

12 器件和文档支持

12.1 接收文档更新通知

要接收文档更新通知，请导航至 ti.com. 上的器件产品文件夹。单击右上角的*通知我*进行注册，即可每周接收产品信息更改摘要。有关更改的详细信息，请查看任何已修订文档中包含的修订历史记录。

12.2 社区资源

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12.4 静电放电警告

ESD 可能会损坏该集成电路。德州仪器 (TI) 建议通过适当的预防措施处理所有集成电路。如果不遵守正确的处理措施和安装程序，可能会损坏集成电路。

ESD 的损坏小至导致微小的性能降级，大至整个器件故障。 精密的集成电路可能更容易受到损坏，这是因为非常细微的参数更改都可能会导致器件与其发布的规格不相符。

12.5 Glossary

SLYZ022 — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

13 机械、封装和可订购信息

以下页面包含机械、封装和可订购信息。这些信息是指定器件的最新可用数据。数据如有变更，恕不另行通知，且不会对此文档进行修订。如需获取此数据表的浏览器版本，请查阅左侧的导航栏。

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
SN74LVC1G07QDBVRQ1	ACTIVE	SOT-23	DBV	5	3000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	CCQO	Samples
SN74LVC1G07QDCKRQ1	ACTIVE	SC70	DCK	5	3000	RoHS & Green	SN	Level-2-260C-1 YEAR	-40 to 125	16J	Samples
SN74LVC1G07QDCKTQ1	ACTIVE	SC70	DCK	5	250	RoHS & Green	SN	Level-2-260C-1 YEAR	-40 to 125	16J	Samples
SN74LVC1G07QDRYRQ1	ACTIVE	SON	DRY	6	5000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	HL	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

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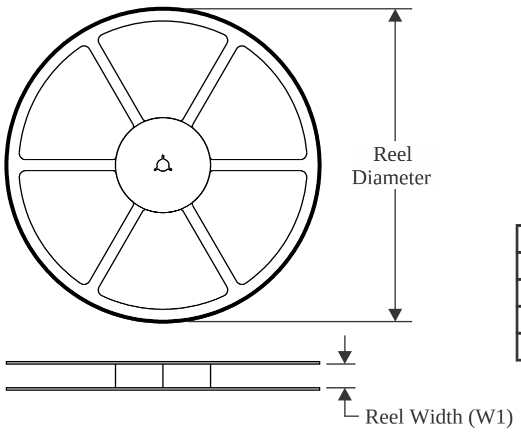
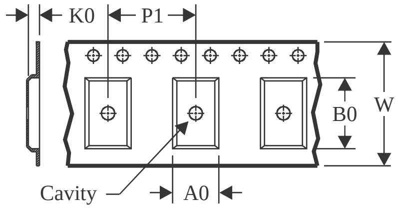
TAPE AND REEL INFORMATION

REEL DIMENSIONS

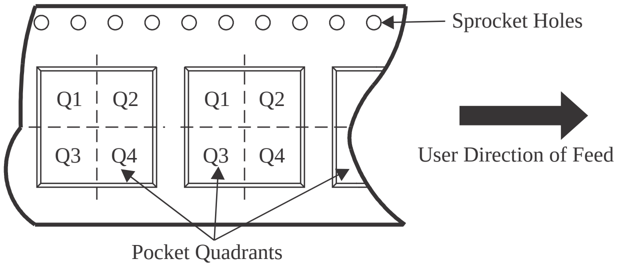


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

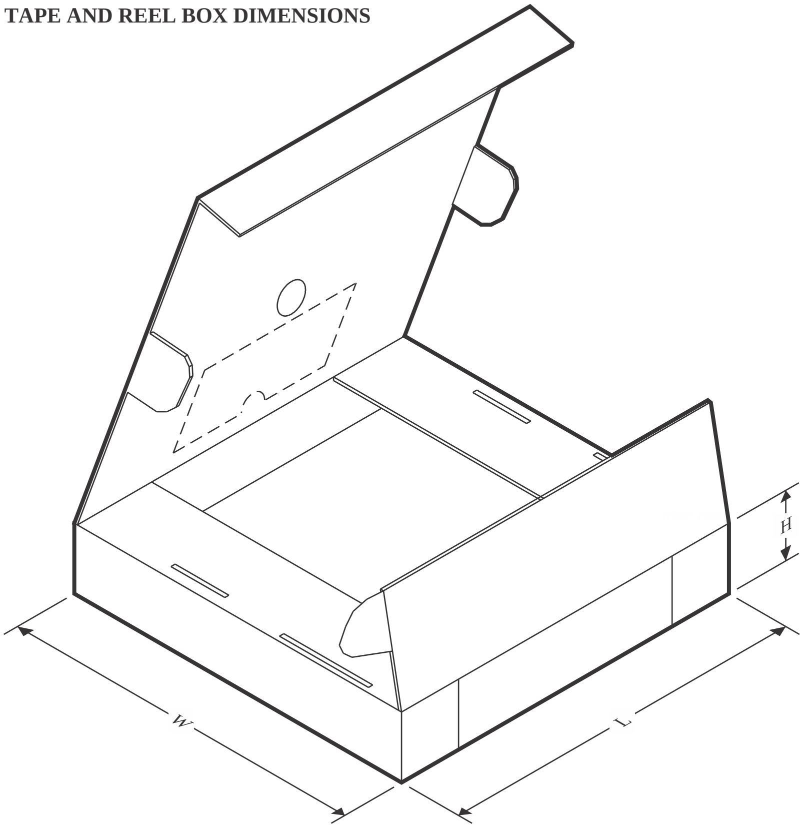
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
SN74LVC1G07QDBVRQ1	SOT-23	DBV	5	3000	179.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
SN74LVC1G07QDCKRQ1	SC70	DCK	5	3000	178.0	9.0	2.4	2.5	1.2	4.0	8.0	Q3
SN74LVC1G07QDCKTQ1	SC70	DCK	5	250	178.0	9.0	2.4	2.5	1.2	4.0	8.0	Q3
SN74LVC1G07QDRYRQ1	SON	DRY	6	5000	180.0	9.5	1.2	1.65	0.7	4.0	8.0	Q1

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

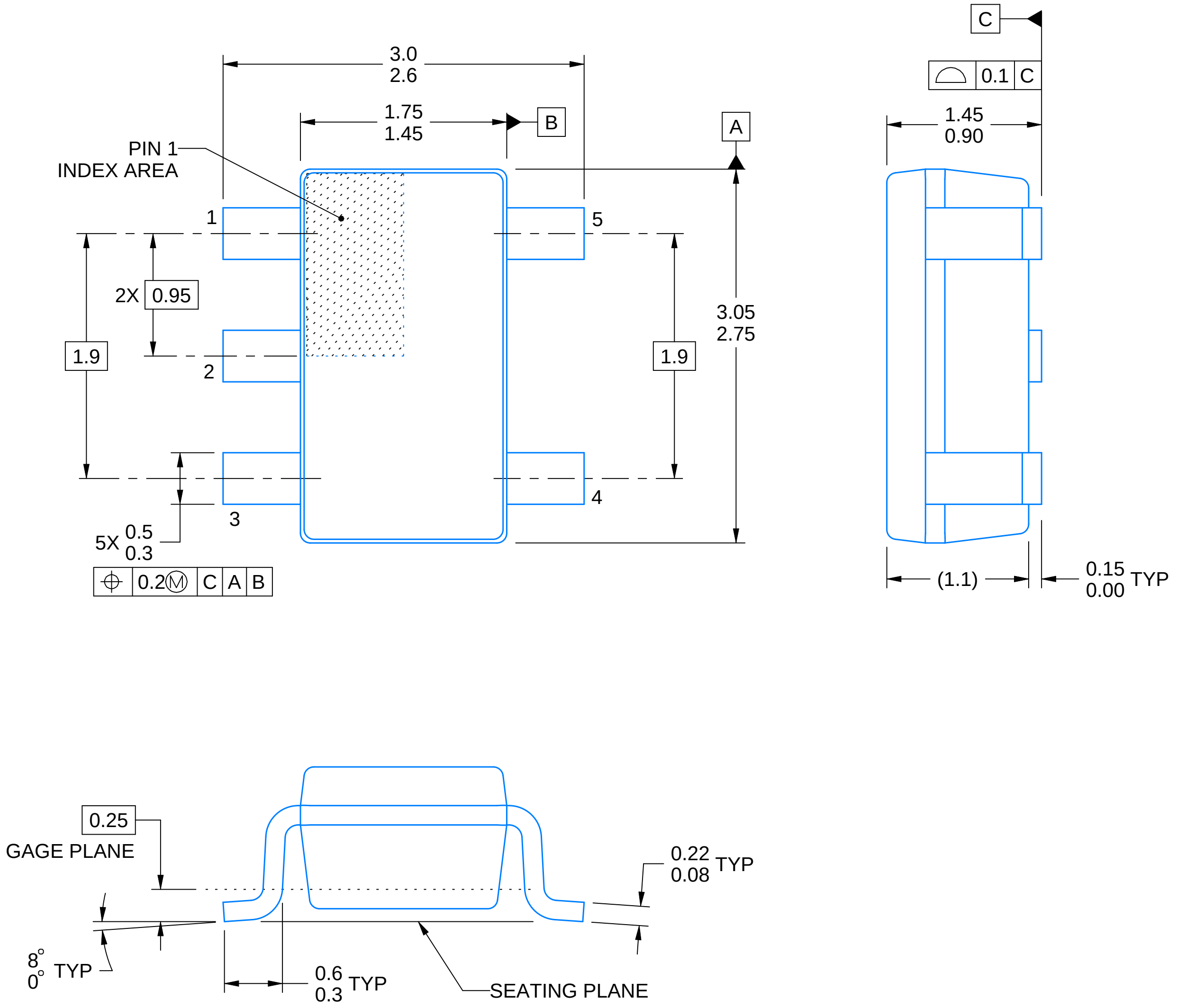
Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
SN74LVC1G07QDBVRQ1	SOT-23	DBV	5	3000	200.0	183.0	25.0
SN74LVC1G07QDCKRQ1	SC70	DCK	5	3000	190.0	190.0	30.0
SN74LVC1G07QDCKTQ1	SC70	DCK	5	250	180.0	180.0	18.0
SN74LVC1G07QDRYRQ1	SON	DRY	6	5000	189.0	185.0	36.0

PACKAGE OUTLINE

DBV0005A

SOT-23 - 1.45 mm max height

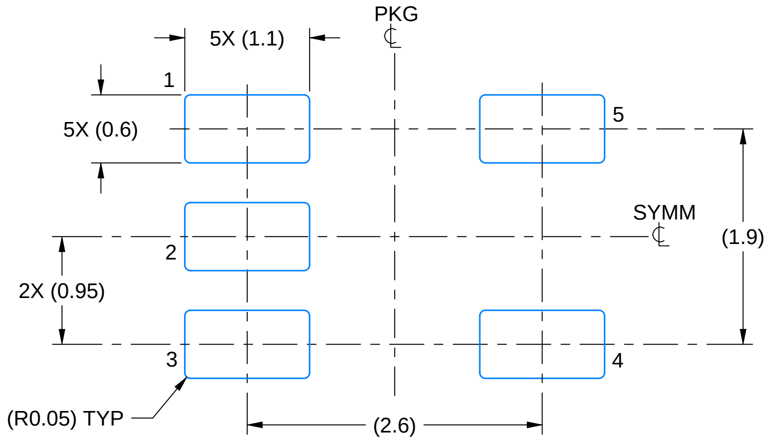
SMALL OUTLINE TRANSISTOR



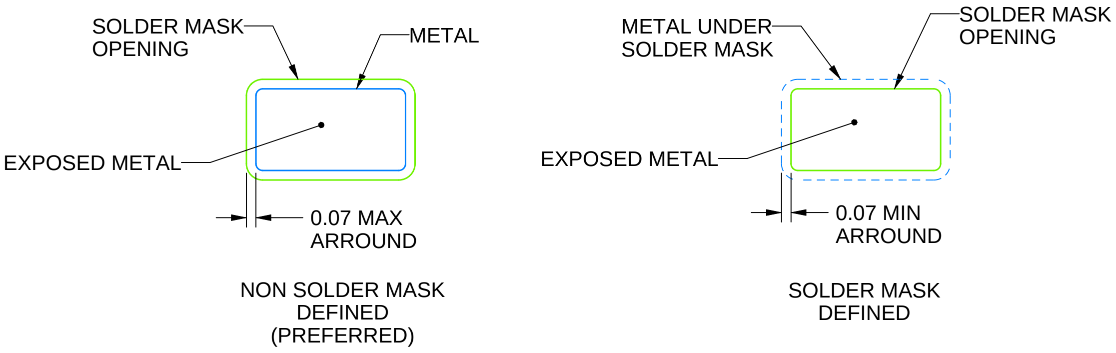
4214839/F 06/2021

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. Refernce JEDEC MO-178.
4. Body dimensions do not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.25 mm per side.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:15X



SOLDER MASK DETAILS

4214839/F 06/2021

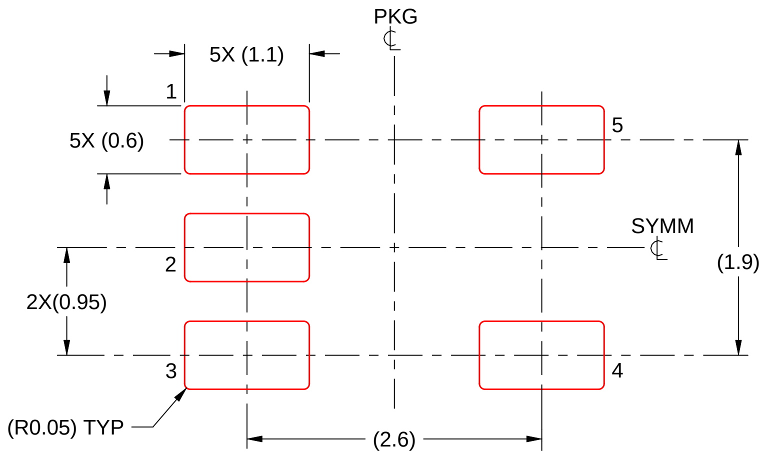
NOTES: (continued)

5. Publication IPC-7351 may have alternate designs.
6. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

EXAMPLE STENCIL DESIGN

SOT-23 - 1.45 mm max height

SMALL OUTLINE TRANSISTOR



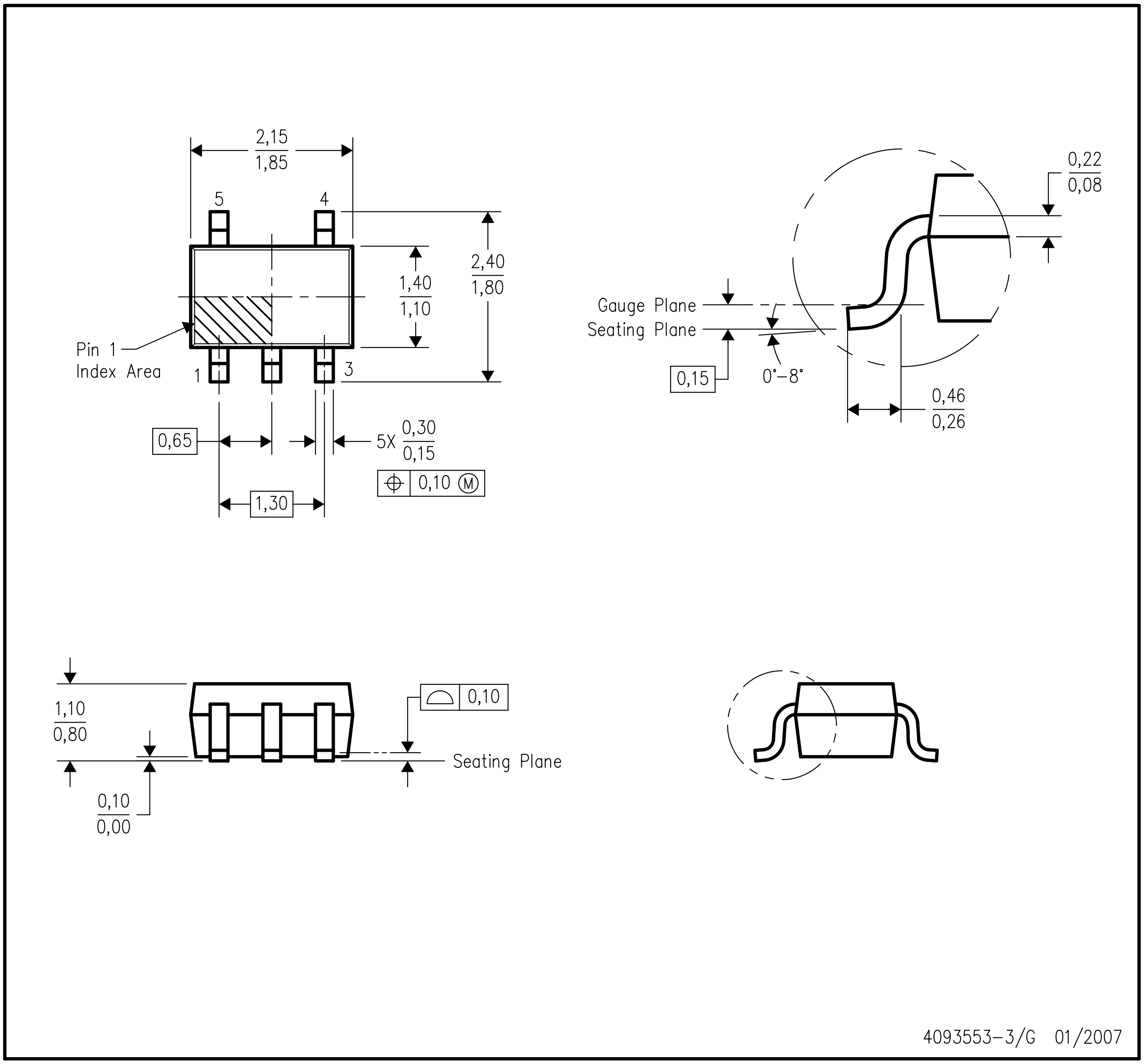
SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:15X

4214839/F 06/2021

NOTES: (continued)

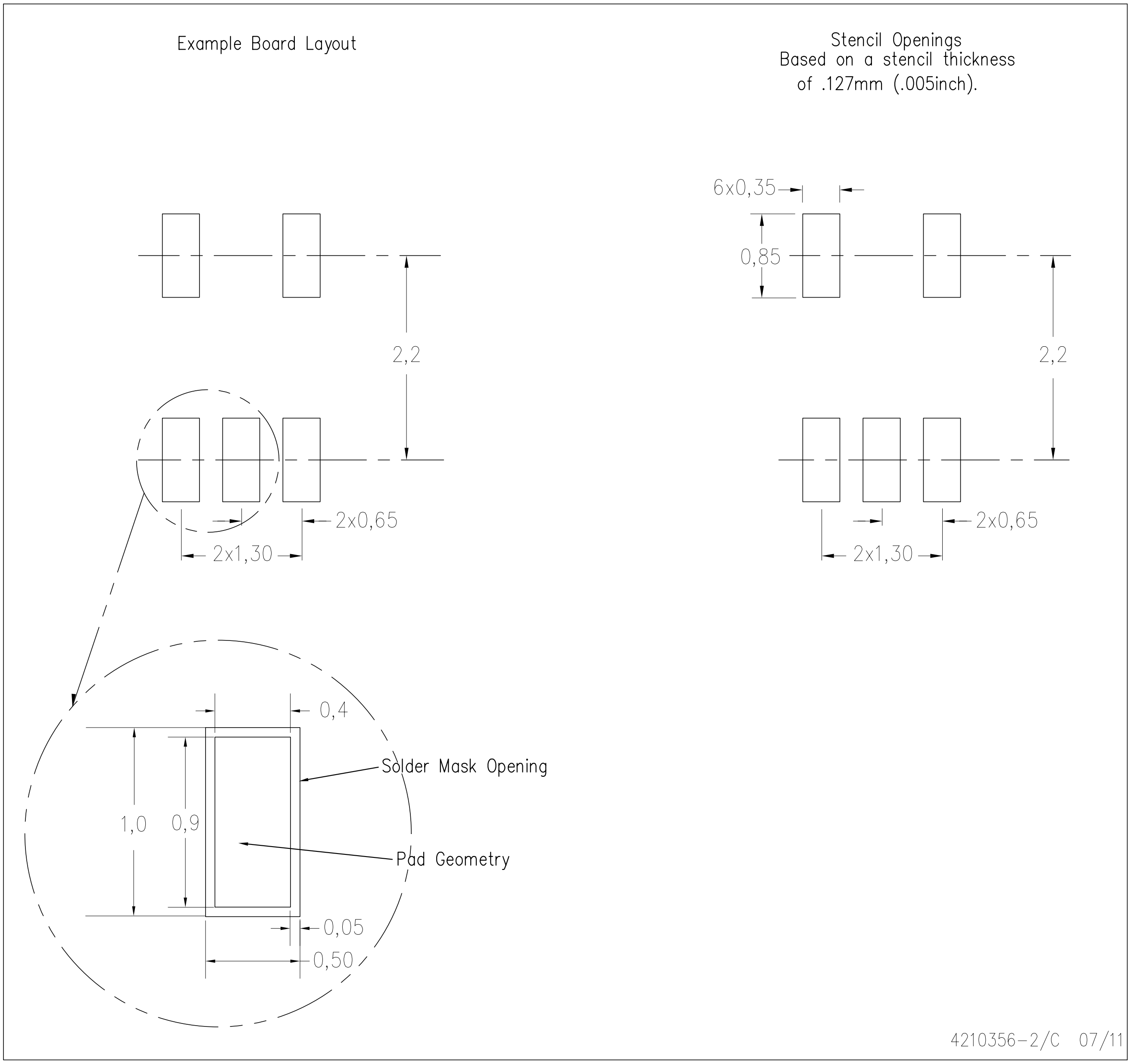
7. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
8. Board assembly site may have different recommendations for stencil design.

DCK (R–PDSO–G5) PLASTIC SMALL–OUTLINE PACKAGE



NOTES:
- A. All linear dimensions are in millimeters.
- B. This drawing is subject to change without notice.
- C. Body dimensions do not include mold flash or protrusion. Mold flash and protrusion shall not exceed 0.15 per side.
- D. Falls within JEDEC MO–203 variation AA.

DCK (R–PDSO–G5) PLASTIC SMALL OUTLINE



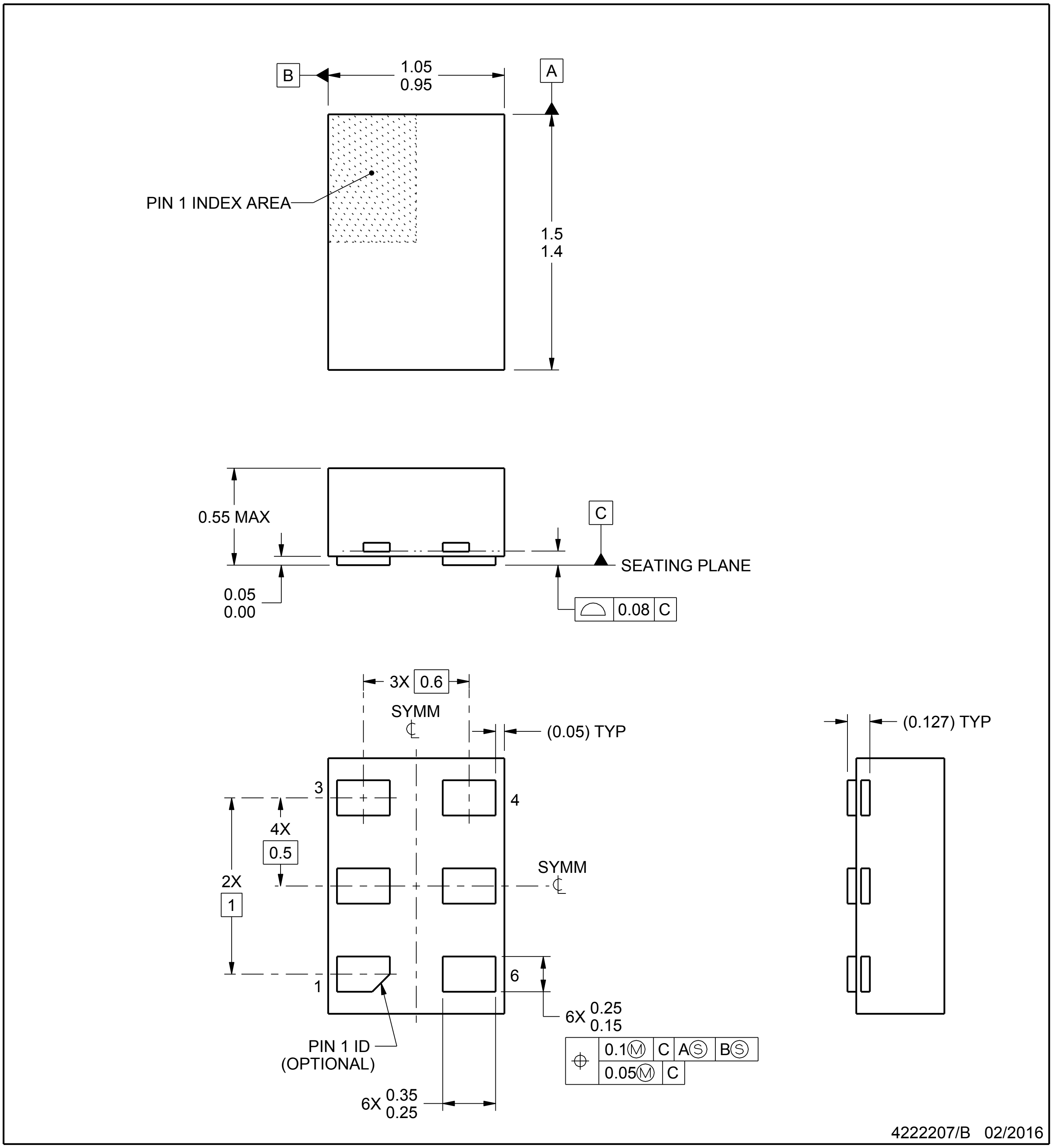
NOTES:
- A. All linear dimensions are in millimeters.
- B. This drawing is subject to change without notice.
- C. Customers should place a note on the circuit board fabrication drawing not to alter the center solder mask defined pad.
- D. Publication IPC–7351 is recommended for alternate designs.
- E. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Example stencil design based on a 50% volumetric metal load solder paste. Refer to IPC–7525 for other stencil recommendations.

DRY 6

USON - 0.6 mm max height

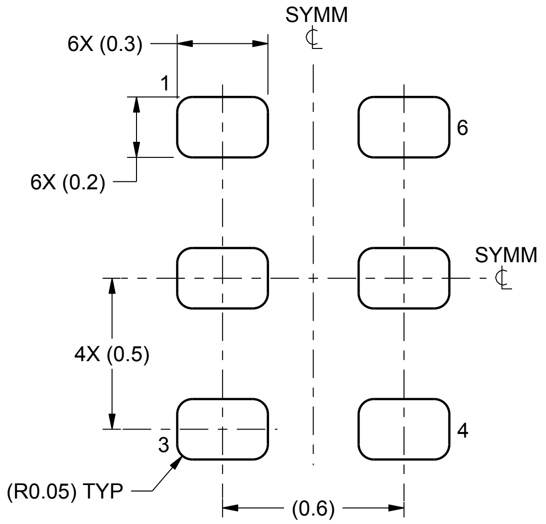
PLASTIC SMALL OUTLINE - NO LEAD

Images above are just a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.

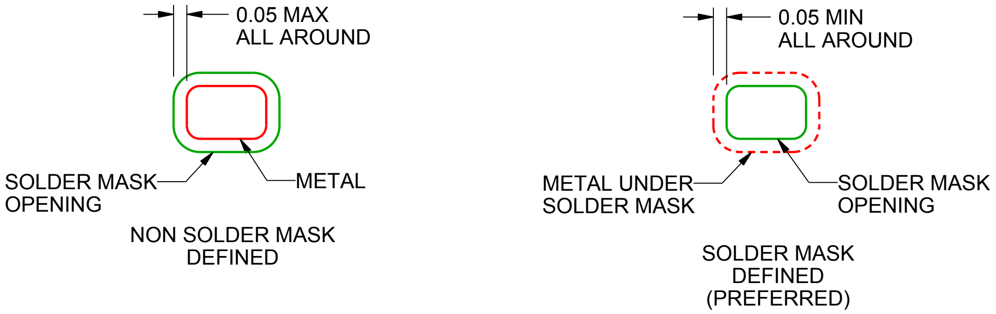


NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.



LAND PATTERN EXAMPLE
1:1 RATIO WITH PKG SOLDER PADS
SCALE:40X

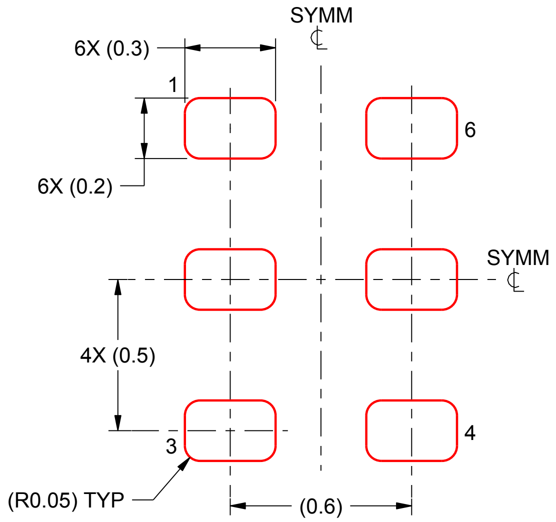


SOLDER MASK DETAILS

4222207/B 02/2016

NOTES: (continued)

3. For more information, see QFN/SON PCB application report in literature No. SLUA271 (www.ti.com/lit/slua271).



SOLDER PASTE EXAMPLE
BASED ON 0.075 - 0.1 mm THICK STENCIL
SCALE:40X

4222207/B 02/2016

NOTES: (continued)

4. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

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