ON Semiconductor®

VGA Port Companion Circuit

PACVGA201

Features

- Seven channels of ESD protection for all VGA port connector pins
- Meets IEC-61000-4-2 Level-4 ESD requirements (±8kV contact discharge)
- Very low loading capacitance from ESD protection diodes on VIDEO lines, 4pF typical
- TTL to CMOS level-translating buffers with power down mode for HSYNC and VSYNC lines
- Three power supplies for design flexibility
- Compact 16-pin QSOP package
- RoHS compliant (lead-free) finishing

Applications

- ESD protection and termination resistors for VGA (video) port interfaces
- Desktop PCs
- Notebook computers
- LCD monitors

Product Description

The PACVGA201 provides seven channels of ESD protection for all signal lines commonly found in a VGA port. ESD protection is implemented with current-steering diodes designed to safely handle the high surge currents encountered with IEC-61000-4-2 Level-4 ESD Protection (±8kV contact discharge). When a channel is subjected to an electrostatic discharge, the ESD current pulse is diverted via the protection diodes into the positive supply rail or ground where it may be safely dissipated.

Separate positive supply rails are provided for the VIDEO, DDC_OUT and SYNC channels to facilitate interfacing with low-voltage video controller ICs and to provide design flexibility in multiple-supply-voltage environments.

An internal diode (D_1, in schematic below) is provided such that V_{CC2} is derived from V_{CC3} (V_{CC2} does not require an external power supply input). In applications where V_{CC3} may be powered down, diode D_1 blocks any DC current path from the DDC_OUT pins back to the powered down V_{CC3} rail via the upper ESD protection diodes.

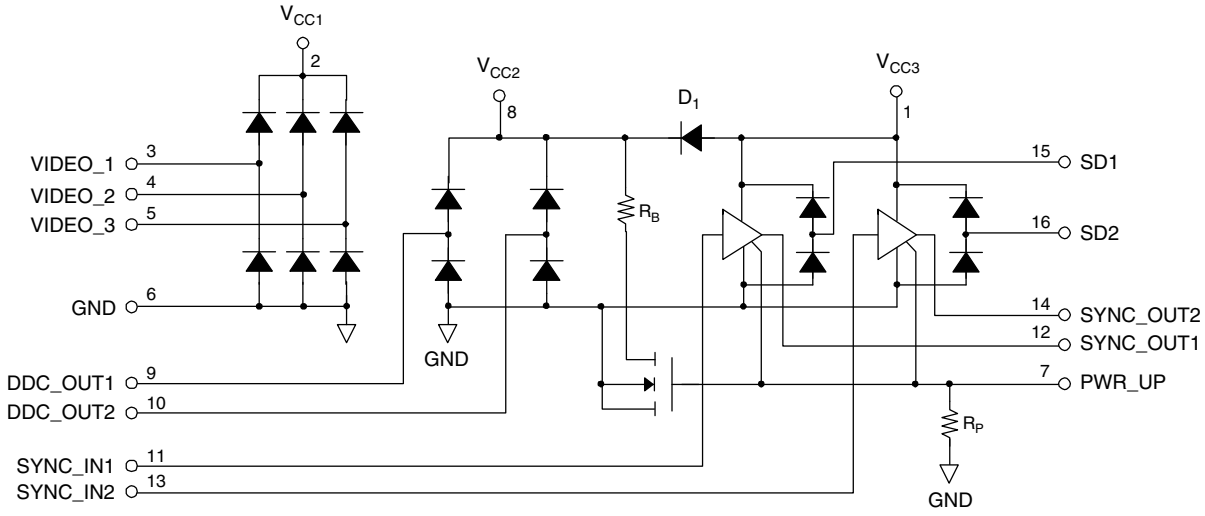
Two non-inverting drivers provide buffering for the HSYNC and VSYNC signals from the Video Controller IC (SYNC_IN1, SYNC_IN2). These buffers accept TTL input levels and convert them to CMOS output levels that swing between Ground and V_{CC3}.

When the PWR_UP input is driven LOW, the SYNC outputs are driven LOW and the SYNC inputs can float: no current will be drawn from the VCC3 supply.
The PACVGA201 is housed in a 16-pin QSOP package with RoHS compliant lead-free finishing.

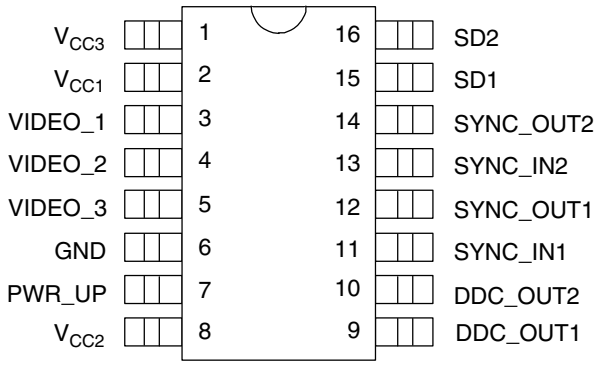
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Publication Order Number:
PACVGA201/D

Simplified Electrical Schematic



Top View



16-Pin QSOP

Note: This drawing is not to scale.

Ordering Information

PART NUMBERING INFORMATION			
Pins	**Package**	**Ordering Part Number[1]**	**Part Marking**
16	QSOP	PACVGA201QR	PACVGA 201QR

Note 1: Parts are shipped in Tape & Reel form unless otherwise specified.

PIN DESCRIPTIONS		
Pins(s)	**NAME**	**DESCRIPTION**
1	V_{CC3}	V_{CC3} supply pin. This is an isolated supply input for the two sync buffers and SD1 and SD2 ESD protection circuits.
2	V_{CC1}	V_{CC1} supply pin. This is an isolated supply pin for the VIDEO_1, VIDEO_2 and VIDEO_3 ESD protection circuits.
3	VIDEO_1	Video signal ESD protection channel. This pin is typically tied one of the video lines between the VGA controller device and the video connector.
4	VIDEO_2	Video signal ESD protection channel. This pin is typically tied one of the video lines between the VGA controller device and the video connector.
5	VIDEO_3	Video signal ESD protection channel. This pin is typically tied one of the video lines between the VGA controller device and the video connector.
6	GND	Ground reference supply pin.
7	PWR_UP	Enables the sync buffers when high. When PWR_UP is low the sync outputs are forced low and the inputs can be floated.
8	V_{CC2}	V_{CC2} supply pin. This is an isolated supply pin for the DDC_OUT1 and DDC_OUT2 ESD protection circuits. Internally, V_{CC2} is derived from the V_{CC3} input if the V_{CC2} input is not connected to a supply voltage.
9	DDC_OUT1	DDC_OUT1 ESD protection channel.
10	DDC_OUT2	DDC_OUT2 ESD protection channel
11	SYNC_IN1	Sync signal buffer input. Connects to the VGA Controller side of one of the sync lines.
12	SYNC_OUT1	Sync signal buffer output. Connects to the video connector side of one of the sync lines.
13	SYNC_IN2	Sync signal buffer input. Connects to the VGA Controller side of one of the sync lines.
14	SYNC_OUT2	Sync signal buffer output. Connects to the video connector side of one of the sync lines.
15	SD1	ESD protection channel input.
16	SD2	ESD protection channel input.

Specifications

ABSOLUTE MAXIMUM RATINGS		
PARAMETER	**RATING**	**UNITS**
V_{CC1},V_{CC2} and V_{CC3} Supply Voltage Inputs	[GND - 0.5] to +6.0	V
Diode Forward Current (one diode conducting at a time)	20	mA
DC Voltage at Inputs VIDEO_1, VIDEO_2, VIDEO_3 DDC_OUT1, DDC_OUT2 SYNC_IN1, SYNC_IN2	 [GND - 0.5] to [V_{CC1} + 0.5] [GND - 0.5] to [V_{CC2} + 0.5] [GND - 0.5] to [V_{CC3} + 0.5]	 V V V
Operating Temperature Range	0 to +70	°C
Storage Temperature Range	-65 to +150	°C
Package Power Rating	750	mW

ELECTRICAL OPERATING CHARACTERISTICS (SEE NOTE 1)

SYMBOL	PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
I_{CC1}	V_{CC1} Supply Current	V_{CC1} = 5.0V			10	μA
I_{CC3}	V_{CC3} Supply Current	V_{CC3} = 5V; SYNC inputs at GND or V_{CC3}; PWR_UP pin at V_{CC3}; SYNC ouputs unloaded		10		μA
		V_{CC3} = 5V; SYNC inputs at 3.0V; PWR_UP pin at V_{CC3}; SYNC ouputs unloaded		200		μA
		V_{CC3} = 5V; PWR_UP input at GND; SYNC ouputs unloaded			10	μA
V_{CC2}	V_{CC2} Pin Open Circuit Voltage	V_{CC2} voltage internally derived from V_{CC3} via diode D1; no external current drawn		[V_{CC3} - 0.80]		V
V_{IH}	Logic High Input Voltage	V_{CC3} = 5V; Note 2	2.0			V
V_{IL}	Logic Low Input Voltage	V_{CC3} = 5V; Note 2			0.8	V
V_{OH}	Logic High Output Voltage	I_{OH} = -4mA, V_{CC3} = 5.0V; Note 3	4.4			V
V_{OL}	Logic Low Output Voltage	I_{OL} = 4mA, V_{CC3} = 5.0V; Note 3			0.4	V
R_B, R_P	Resistor Value	PWR_UP = V_{CC3} = 5.0V	0.5	1	2	MΩ
I_{IN}	Input Current VIDEO_x pins HSYNC, VSYNC pins	 V_{CC1} = 5.0V; V_{IN} = V_{CC1} or GND V_{CC3} = 5.0V; V_{IN} = V_{CC3} or GND			 ±1 ±1	 μA μA
C_{IN}	Input Capacitance on VIDEO_1, VIDEO_2 and VIDEO_3 pins	V_{CC1} = 5.0V; V_{IN} = 2.5V; measured at 1MHz V_{CC1} = 2.5V; V_{IN} = 1.25V; measured at 1MHz		4 4.5		pF pF
t_{PLH}	SYNC Buffer L => H Propagation Delay	C_L = 50pF; V_{CC3} = 5.0V; Input t_R and $t_F \leq$ 5ns		8	12	ns
t_{PHL}	SYNC Buffer H => L Propagation Delay	C_L = 50pF; V_{CC3} = 5.0V; Input t_R and $t_F \leq$ 5ns		8	12	ns
t_R, t_F	SYNC Buffer Output Rise & Fall Times	C_L = 50pF; V_{CC3} = 5.0V; Input t_R and $t_F \leq$ 5ns		7.0		ns
V_{ESD}	ESD Withstand Voltage	V_{CC1} = V_{CC2} = V_{CC3} = 5V; Note 4	±8			kV

Note 1: All parameters specified over standard operating conditions unless otherwise noted.
Note 2: These parameters apply only to SYNC_IN1, SYNC_IN2 and PWR_UP.
Note 3: These parameters apply only to SYNC_OUT1 and SYNC_OUT2.
Note 4: Per the IEC-61000-4-2 International ESD Standard, Level 4 contact discharge method. V_{CC1}, V_{CC2} and V_{CC3} must be bypassed to GND via a low impedance ground plane with a 0.2uF or greater, low inductance, chip ceramic capacitor at each supply pin. ESD pulse is applied between the applicable pins and GND. ESD pulse can be positive or negative with respect to GND. Applicable pins are: VIDEO_1, VIDEO_2, VIDEO_3, SYNC_OUT1, SD1, SYNC_OUT2, SD2, DDC_OUT1 and DDC_OUT2. All other pins are ESD protected to the industry standard 2kV per the Human Body model (MIL-STD-883, Method 3015).

Application Information

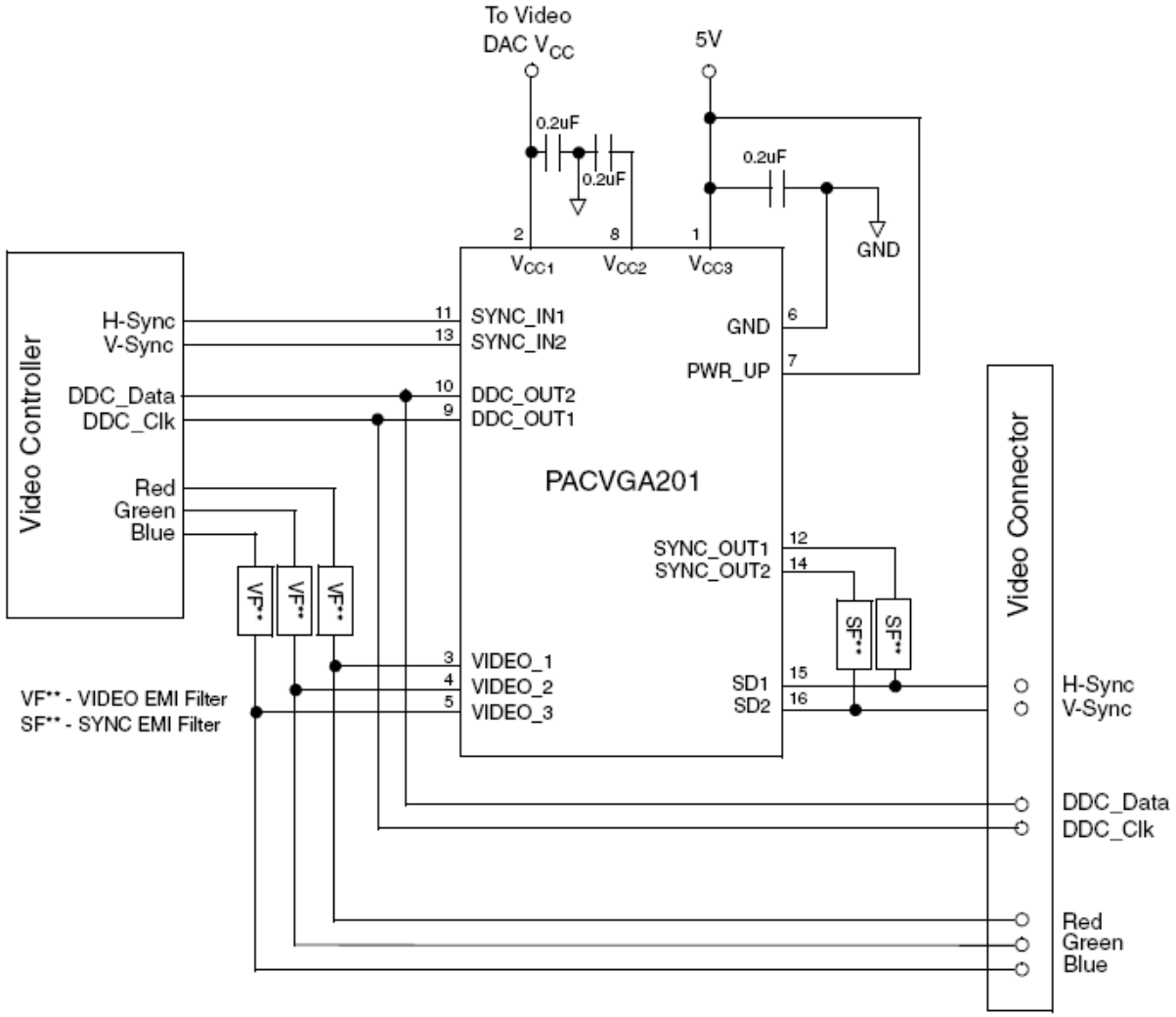


Figure 1. Typical Connection Diagram

A resistor may be necessary between the V_{CC2} pin and ground if protection against a stream of ESD pulses is required while the PACVGA201 is in the power-down state. The value of this resistor should be chosen such that the extra charge deposited into the V_{CC2} bypass capacitor by each ESD pulse will be discharged before the next ESD pulse occurs. The maximum ESD repetition rate specified by the IEC-61000-4-2 standard is one pulse per second. When the PACVGA201 is in the power-up state, an internal discharge resistor is connected to ground via a FET switch for this purpose.

For the same reason, V_{CC1} and V_{CC3} may also require bypass capacitor discharging resistors to ground if there are no other components in the system to provide a discharge path to ground.

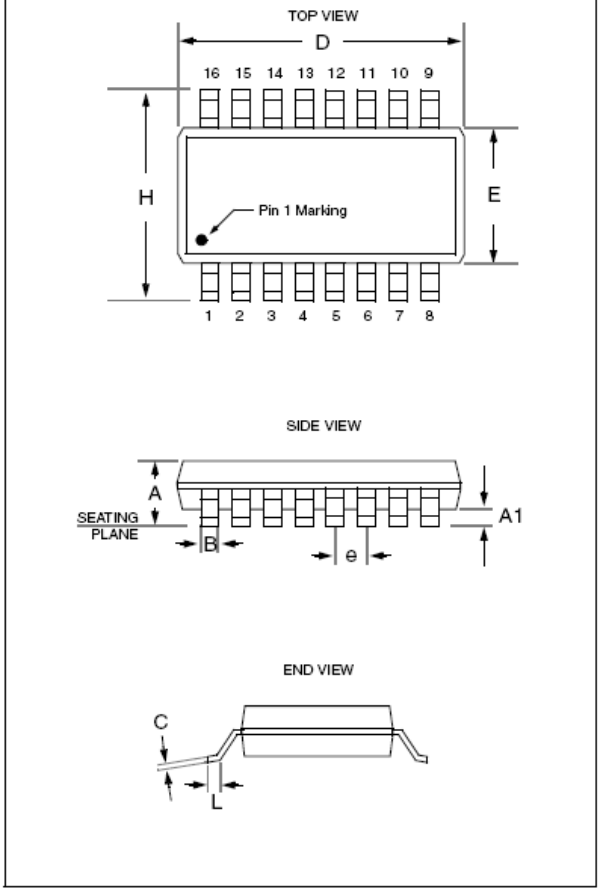
Mechanical Details

QSOP Mechanical Specifications

PACVGA201 devices are supplied in 16-pin QSOP packages. Dimensions are presented below. For complete information on the QSOP-16, see the California Micro Devices QSOP Package Information document.

PACKAGE DIMENSIONS				
Package	QSOP (JEDEC name is SSOP)			
Pins	16			
Dimensions	**Millimeters**		**Inches**	
	Min	**Max**	**Min**	**Max**
A	1.35	1.75	0.053	0.069
A1	0.10	0.25	0.004	0.010
B	0.20	0.30	0.008	0.012
C	0.18	0.25	0.007	0.010
D	4.80	5.00	0.189	0.197
E	3.81	3.98	0.150	0.157
e	0.64 BSC		0.025 BSC	
H	5.79	6.19	0.228	0.244
L	0.40	1.27	0.016	0.050
# per tube	100 pcs*			
# per tape and reel	2500 pcs			
Controlling dimension: inches				

Mechanical Package Diagrams



Package Dimensions for QSOP-16

* This is an approximate number which may vary.

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