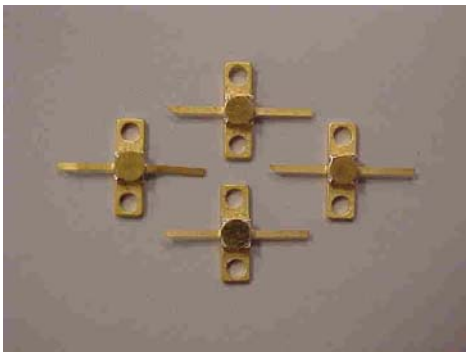
- FEATURES
  - 26.5 dBm Linear Output Power
  - 18.5 dB Power Gain at 2 GHz
  - 11.5 dB Maximum Stable Gain at 10 GHz
  - 36 dBm Output IP3
  - 45% Power-Added Efficiency at 2 GHz



- DESCRIPTION AND APPLICATIONS

The FPD750P100 is a packaged AlGaAs/InGaAs pseudomorphic High Electron Mobility Transistor (PHEMT), featuring a 0.25 µm by 750 µm Schottky barrier gate, defined by high-resolution stepper-based photolithography. The recessed and offset Gate structure minimizes parasitics to optimize performance. The epitaxial structure and processing have been optimized for reliable high-power applications. The FPD750P100 also features Si_3N_4 passivation and is also available in die form and in the low cost plastic SOT89, SOT343, and DFN plastic packages.

Typical applications include commercial and other narrowband and broadband high-performance amplifiers, including SATCOM uplink transmitters, PCS/Cellular low-voltage high-efficiency output amplifiers, and medium-haul digital radio transmitters.

- ELECTRICAL SPECIFICATIONS AT 22°C

Parameter	Symbol	Test Conditions	Min	Typ	Max	Units
UNLESS OTHERWISE NOTED, RF SPECIFICATIONS MEASURED AT f = 2 GHz USING CW SIGNAL						
Power at 1dB Gain Compression	P_{1dB}	V_{DS} = 8 V; I_{DS} = 50% I_{DSS}	25.0	26.5		dBm
Power Gain at P_{1dB}	G_{1dB}	V_{DS} = 8 V; I_{DS} = 50% I_{DSS}	18.0	18.5		dB
Maximum Stable Gain (S_{21}/S_{12})	SSG	V_{DS} = 8 V; I_{DS} = 50% I_{DSS}				
		f = 2 GHz	22.0	23.0		dB
		f = 10 GHz	10.5	11.5		dB
Power-Added Efficiency	PAE	V_{DS} = 8 V; I_{DS} = 50% I_{DSS}; P_{OUT} = P_{1dB}		45		%
Output Third-Order Intercept Point	IP3	V_{DS} = 8V; I_{DS} = 50% I_{DSS}				
(from 15 to 5 dB below P_{1dB})		Matched for optimal power		36		dBm
Saturated Drain-Source Current	I_{DSS}	V_{DS} = 1.3 V; V_{GS} = 0 V	185	230	280	mA
Maximum Drain-Source Current	I_{MAX}	V_{DS} = 1.3 V; V_{GS} ≅ +1 V		375		mA
Transconductance	G_M	V_{DS} = 1.3 V; V_{GS} = 0 V		200		mS
Gate-Source Leakage Current	I_{GSO}	V_{GS} = -5 V		1	15	µA
Pinch-Off Voltage	$\|V_P\|$	V_{DS} = 1.3 V; I_{DS} = 0.75 mA	0.7	1.0	1.3	V
Gate-Drain Breakdown Voltage	$\|V_{BDGD}\|$	I_{GD} = 0.75 mA	14.5	16.0		V
Thermal Resistivity (see Notes)	θ_{JC}	V_{DS} > 6V		48		°C/W

- RECOMMENDED BIAS CONDITIONS:

  Drain-Source Voltage: 5V to 8V Drain-Source Current: 33% to 50% I_{DSS}

- ABSOLUTE MAXIMUM RATINGS[1]

Parameter	Symbol	Test Conditions	Min	Max	Units
Drain-Source Voltage	V_{DS}	$-3V < V_{GS} < +0V$		9	V
Gate-Source Voltage	V_{GS}	$0V < V_{DS} < +8V$		-3	V
Drain-Source Current	I_{DS}	For $V_{DS} > 2V$		I_{DSS}	mA
Gate Current	I_G	Forward or reverse current		7.5	mA
RF Input Power[2]	P_{IN}	Under any acceptable bias state		175	mW
Channel Operating Temperature	T_{CH}	Under any acceptable bias state		175	ºC
Storage Temperature	T_{STG}	Non-Operating Storage	-40	150	ºC
Total Power Dissipation	P_{TOT}	See De-Rating Note below		2.3	W
Gain Compression	Comp.	Under any bias conditions		5	dB
Simultaneous Combination of Limits[3]		2 or more Max. Limits		80	%

[1] $T_{Ambient}$ = 22°C unless otherwise noted [2] Max. RF Input Limit must be further limited if input VSWR > 2.5:1
[3] Users should avoid exceeding 80% of 2 or more Limits simultaneously

Notes:

- Operating conditions that exceed the Absolute Maximum Ratings could result in permanent damage to the device.
- Thermal Resitivity specification assumes a Au/Sn eutectic die attach onto a Au-plated copper heatsink or rib.
- Power Dissipation defined as: $P_{TOT} \equiv (P_{DC} + P_{IN}) - P_{OUT}$, where
  P_{DC}: DC Bias Power
  P_{IN}: RF Input Power
  P_{OUT}: RF Output Power
- Absolute Maximum Power Dissipation to be de-rated as follows above 22°C:
  $P_{TOT} = 2.3W - (0.0147W/°C) \times T_{HS}$
  where T_{HS} = heatsink or ambient temperature above 22°C

Example: For a 85°C heatsink temperature: $P_{TOT} = 2.3W - (0.0147 \times (85 - 22)) = 1.37W$

- HANDLING PRECAUTIONS

  To avoid damage to the devices care should be exercised during handling. Proper Electrostatic Discharge (ESD) precautions should be observed at all stages of storage, handling, assembly, and testing. These devices should be treated as Class 0 (< 250V) per JESD22-A114-B, Human Body Model, and Class A (< 200V) per JESD22-A115-A, Machine Model.

- APPLICATIONS NOTES & DESIGN DATA

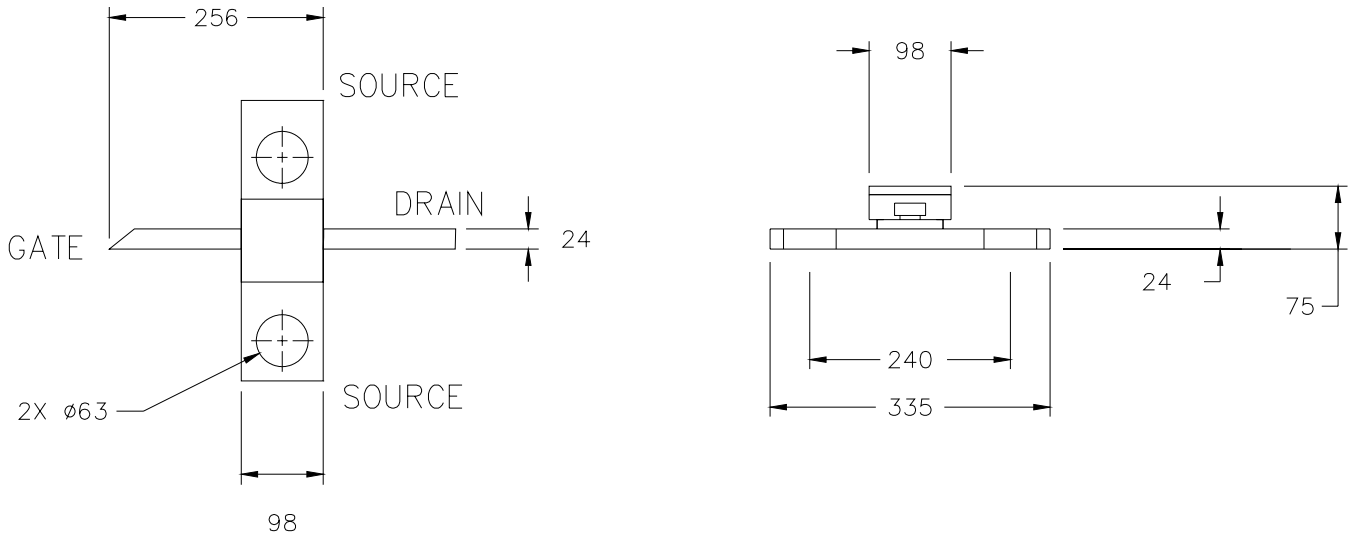
  Applications Notes are available from your local Filtronic Sales Representative or directly from the factory. Complete design data, including S-parameters, noise data, and large-signal models are available on the Filtronic web site.

- RECOMMENDED BIASING GUIDELINES:

  For most applications, a dual-bias circuit is required due to the amount of quiescent current drawn by the FPD3000P100. The Source of the discrete pHEMT device is wire-bonded to the package flange, and therefore self-biasing (using a bypassed Source resistor to set the Gate-Source voltage) is not practical. A dual-bias circuit will require a regulated and filtered negative Gate supply as well as a positive Drain supply. Typical Gate bias voltages will be about -0.4V. Active bias circuits can be employed if the dissipation by a Drain current sense resistor is acceptable, and in these cases the bias voltages must be sequenced so that the negative Gate voltage is established at its final value before the Drain voltage is reached, to prevent device self-oscillation.

PACKAGE OUTLINE

dimensions in mils, tolerance = ± 3 mils



All information and specifications are subject to change without notice.