National Semiconductor

July 24, 2000

ADC08B200 / ADC08B200Q

8-Bit, 200 MSPS A/D Converter with Capture Buffer

General Description

The ADC08B200 is a high speed analog-to-digital converter (ADC) with an integrated capture buffer. The 8-bit, 200 MSPS A/D core is based upon the proven ADC08200 with integrated track-and-hold and is optimized for low power consumption. This device contains a selectable size capture buffer of up to 1,024 bytes that allows fast capture of an input signal with a slower readout rate. An on-chip clock PLL circuit provides the option of on-chip clock rate multiplication to provide the high speed sampling clock.

The ADC08B200 is resistant to latch-up and the outputs are short-circuit proof. The top and bottom of the ADC08B200's reference ladder are available for connections, enabling a wide range of input possibilities. The digital outputs are TTL/CMOS compatible with a separate output power supply pin to support interfacing with 2.7V to 3.3V logic. The digital inputs and outputs are low voltage TTL/CMOS compatible and the output data format is straight binary.

The ADC08B200Q runs on an Automotive Grade Flow and is AEC-Q100 Grade 2 Qualified.

The ADC08B200 is offered in a 48-pin plastic package (TQFP) and is specified over the extended industrial temperature range of −40°C to +105°C. An evaluation board is available to assist in the easy evaluation of the ADC08B200.

Features

- Single-ended input
- Selectable capture buffer size
- PLL for clock multiplication
- Reference Ladder Top and Bottom accessible
- Linear power scaling with sample rate
- FPGA training pattern
- AEC-Q100 Grade 2 Qualified
- Power-down feature

Key Specifications

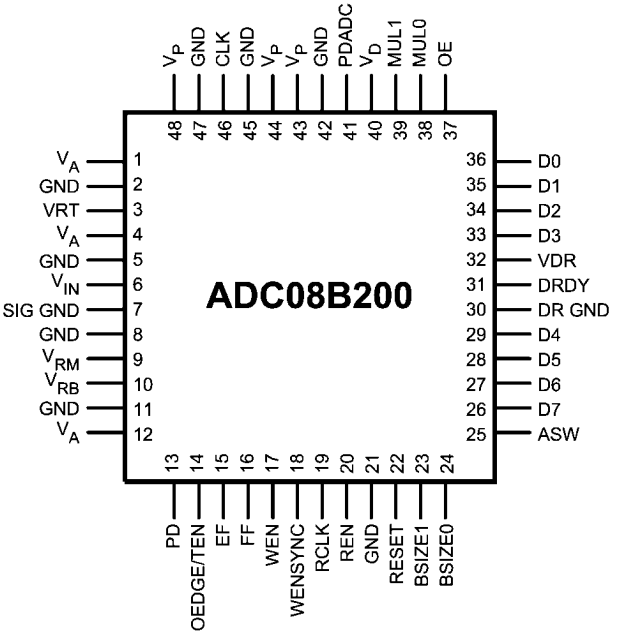
(PLL Bypassed)

■ Resolution	8 Bits
■ Maximum sampling frequency	200 MSPS (min)
■ DNL	±0.4 LSB (typ)
■ ENOB (f_{IN}= 49 MHz)	7.2 bits (typ)
■ THD (f_{IN}= 49 MHz)	−53 dBc (typ)
■ Power Consumption	
— Operating, 50 MHz Input	2 mW / Msps (typ)
— Power Down	2.15 mW (typ)

Applications

- Laser Ranging
- RADAR
- Pulse Capturing

Pin Configuration



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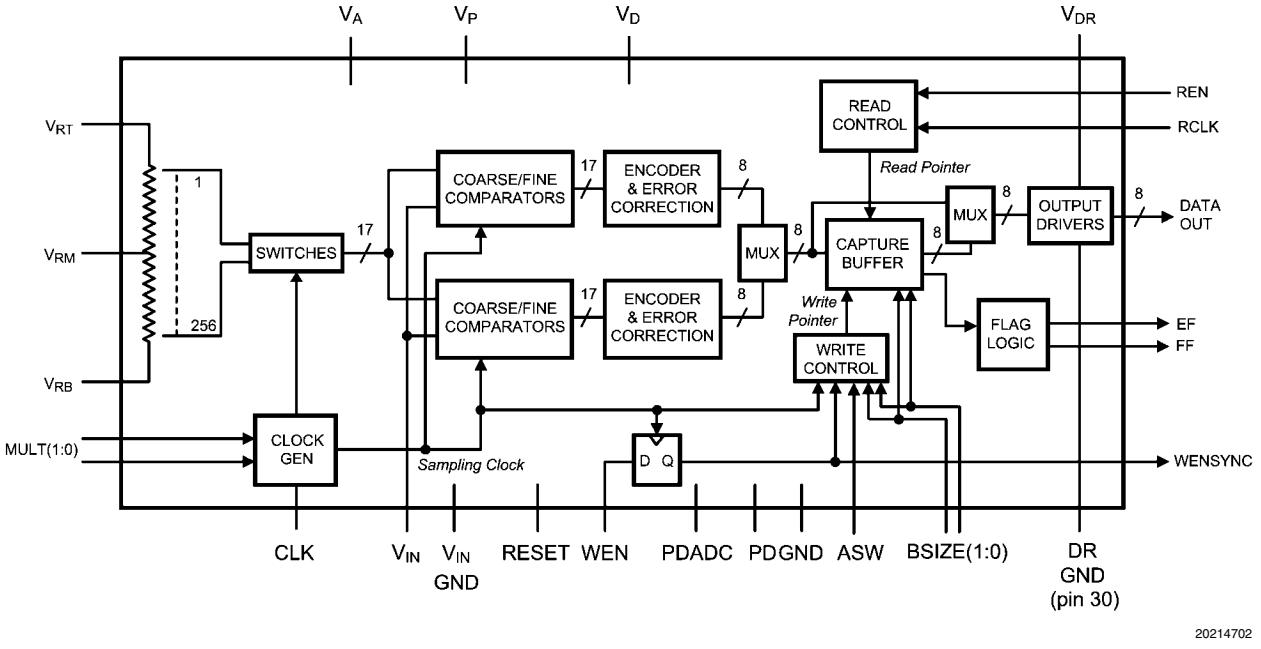
Ordering Information

Order Number	Temperature Range	Package	Features
ADC08B200CIVS	$-40°C \le T_A \le +105°C$	48-pin TQFP	
ADC08B200QCIVS	$-40°C \le T_A \le +105°C$	48-pin TQFP	AEC-Q100 Grade 2 Qualified. Automotive Grade Production Flow
ADC08B200EB		Evaluation Board	

Block Diagram



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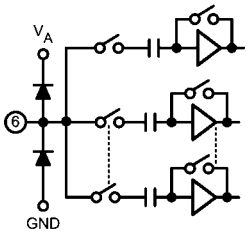
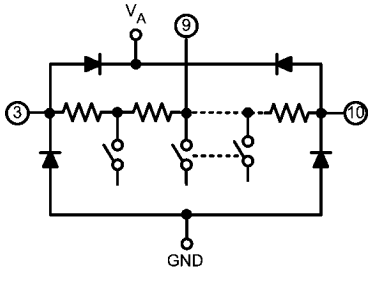
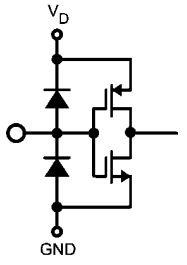
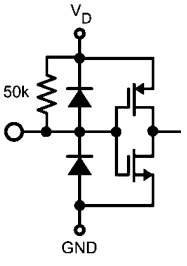
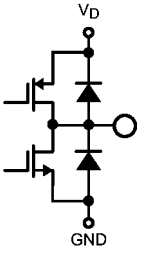
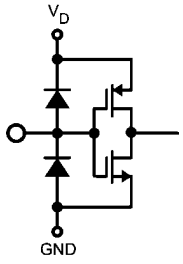
Pin Descriptions and Equivalent Circuits

Pin No.	Symbol	Equivalent Circuit	Description
6	V_{IN}		Analog signal input. Conversion range is V_{RB} to V_{RT}.
3	V_{RT}		Analog Input that is the high (top) side of the reference ladder of the ADC. Voltage on V_{RT} and V_{RB} inputs define the V_{IN} conversion range. V_{RT} should be more positive than V_{RB}. Bypass well.
9	V_{RM}		Analog input that is the mid-point of the reference ladder. This pin should be bypassed to a quiet point in the ground plane with a 0.1 µF capacitor. DO NOT LOAD this pin.
10	V_{RB}		Analog Input that is the low side (bottom) of the reference ladder of the ADC. The voltages on V_{RT} and V_{RB} inputs define the V_{IN} conversion range. Bypass well.

Pin No.	Symbol	Equivalent Circuit	Description
13	PD		Chip Power Down input. When this pin is high, the entire chip is in the Power Down mode. Any data in the capture buffer is lost and the output pins hold the last byte that was output.
41	PDADC		ADC Power Down Input. When this pin is high, the ADC is powered down. The capture buffer is active and the data within it may be clocked out.
46	CLK		CMOS/TTL compatible digital clock Input. When the PLL is bypassed, the clock signal at this pin is the ADC sampling clock and V_{IN} is sampled on the rising edge of this clock input. When the PLL is enabled, the signal at this input is the reference clock, which is multiplied to provide a higher frequency sample clock.
19	RCLK		Buffer Read Clock input. When the capture buffer is enabled, this input signal is used to read the data from the internal buffer. The data output and the buffer empty flag (EF) transition with the rise of this clock.
17	WEN		Write Enable input. A high level at this input causes a byte of data to be written into the capture buffer with the rise of each sample clock.
20	REN		Read Enable input. A high level at this input causes a byte of data to be read from the capture buffer with the rise of each RCLK input. This rise of the REN input should be synchronous with the RCLK input and should not be high while the WEN input is high.
22	RESET		Device Reset Input. A high level at this input resets all control logic on the chip.
37	OE		Output Enable input. A high level at this input enables the output buffers. A low level at this input puts the digital data output pins into a high impedance state.
14	OEDGE/TEN		Output Edge Select or Test Mode Enable input. If this input is high, the data outputs transition with the rising edge of the DRDY output. If this input is low, the data outputs transition with the falling edge of the DRDY output. Forcing a potential of $V_A/2$ at this input enables the Test Mode.
18	WENSYNC		Synchronized WEN output. The WEN control input is synchronized on-chip with the internal sample clock and is provided at this output.
31	DRDY		Data Ready output. This signal transitions with the transition of the digital data outputs and indicates that the output data is ready.
26 thru 29 and 33 thru 36	D0–D7		Digital data digital Outputs. D0 is the LSB, D7 is the MSB.
16	FF		Buffer Full Flag. This output is high when the capture buffer is full.
15	EF		Buffer Empty Flag. This output is high when the capture buffer is empty.

Pin No.	Symbol	Equivalent Circuit	Description
25	ASW		Auto-Stop Write input. This pin has a dual function. With the buffer enabled, this pin acts as the ASW input. When this input is high, writing to the buffer is halted when the capture buffer is full (FF high). When the buffer is disabled, this pin is ignored. When the device is in Test Mode, this pin acts as the Output Edge Select signal, functioning in accordance with the description of the OEDGE/TEN pin.
23,24	BSIZE(1:0)		Buffer Size input. These inputs determine the size of the buffer, as described in the Functional Description.
38, 39	MULT(1:0)		Clock Multiply Factor input. These inputs determine the internal clock PLL's multiplication factor.
1, 4, 12	V_A		Positive analog supply pin. Connect to a voltage source of +3.3V.
43, 44, 48	V_P		PLL supply pin. Connect to a voltage source of +3.3V.
40	V_D		Digital core supply pin. Connect to a voltage source of +3.3V.
32	V_{DR}		Power supply for the output drivers. Connect to a voltage source of 2.7V to V_D.
2, 5, 8, 11, 21, 42, 45, 47	GND		The ground return for the chip core.
7	SIG GND		Analog input signal ground.
30	DR GND		The ground return for the output drivers.

Absolute Maximum Ratings

(Notes 1, 2)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/ Distributors for availability and specifications.

Supply Voltage (V_A, V_P, V_D, V_{DR})	-0.3V to 3.8V
Driver Supply Voltage (V_{DR})	-0.3V to V_A +0.3V
Voltage on Any Input or Output Pin	−0.3V to V_A
Reference Voltage (V_{RT}, V_{RB})	GND to V_A
Input Current, Data Outputs	±1 mA
Input Current all other pins (Note 3)	±25 mA
Package Input Current (Note 3)	±50 mA
Power Dissipation at T_A = 25°C	See (Note 4)
ESD Susceptibility (Note 5)	
Human Body Model	2500V
Machine Model	200V
Charged Device Model	1000V
Soldering Temperature, Infrared, 10 seconds (Note 6)	235°C
Storage Temperature	−65°C to +150°C

Operating Ratings (Notes 1, 2)

Operating Temperature Range	$-40°C \le T_A \le +105°C$
Supply Voltage (V_A)	+3.0V to +3.6V
Driver Supply Voltage (V_{DR})	+2.7V to (V_A + 0.3V)
Maximum Supply Voltage	
V_D, V_P	V_A + 0.3V
CLK Frequency	
PLL Bypassed	1 to 210 MHz
PLL used	15 to 105 MHz
RCLK Frequency (Note 12)	2 - 210 MHz
RCLK Duty Cycle	35% to 65%
Ground Difference |GND - DR GND|	0V to 300 mV
Upper Reference Voltage (V_{RT})	0.5V to (V_A − 0.3V)
Lower Reference Voltage (V_{RB})	0V to (V_{RT} − 0.5V)
Reference Delta (V_{RT} − V_{RB})	0.5V to 2.3V
V_{IN} Voltage Range	V_{RB} to V_{RT}

Package Thermal Resistance

Package	θ_{JA}
48-Lead TQFP	76 °C/W

Converter Electrical Characteristics

The following specifications apply for V_A = V_D = V_P = V_{DR} = +3.3V_{DC}, V_{RT} = +1.9V, V_{RB} = 0.3V, C_L = 10 pF, f_{CLK} = 200 MHz at 50% duty cycle, OEDGE/TEN = 1, Buffer and PLL bypassed. **Boldface limits apply for T_J = T_{MIN} to T_{MAX}**: all other limits T_J = 25°C (Notes 7, 8)

Symbol	Parameter	Conditions		Typical (Note 9)	Limits (Note 9)	Units (Limits)
DC ACCURACY						
INL	Integral Non-Linearity			±0.55	**±1.3**	LSB (max)
DNL	Differential Non-Linearity			±0.40	**±0.9**	LSB (max)
	Missing Codes				**0**	(max)
FSE	Full Scale Error			−39	**−80** **0**	mV (min) mV (max)
V_{OFF}	Zero Scale Offset Error			55	**70**	mV (max)
ANALOG INPUT AND REFERENCE CHARACTERISTICS						
V_{IN}	Input Voltage			1.6	**V_{RB}** **V_{RT}**	V (min) V (max)
C_{IN}	V_{IN} Input Capacitance	V_{IN} = 0.75V +0.5 Vrms	(CLK LOW)	3		pF
			(CLK HIGH)	4		pF
R_{IN}	Analog Input Resistance			>1		MΩ
FPBW	Full Power Bandwidth			500		MHz
V_{RT}	Top Reference Voltage			1.9	**V_A** **0.5**	V (max) V (min)
V_{RB}	Bottom Reference Voltage			0.3	**V_{RT} − 0.5** **0**	V (max) V (min)
V_{RT} - V_{RB}	Reference Voltage Delta			1.6	**0.5** **2.3**	V (min) V (max)
R_{REF}	Reference Ladder Resistance	V_{RT} to V_{RB}		160	**145** **200**	Ω (min) Ω (max)

Symbol	Parameter	Conditions		Typical (Note 9)	Limits (Note 9)	Units (Limits)
DIGITAL INPUT CHARACTERISTICS						
V_{IH}	Logic High Input Voltage		OEDGE/TEN	2.2	**2.7**	V (min)
			Others	1.6	**2.1**	V (min)
V_{IL}	Logic Low Input Voltage		OEDGE/TEN	0.9	**0.5**	V (max)
			Others	1.3	**0.7**	V (max)
I_{IH}	Logic High Input Current	$V_{IH} = V_{DR} = V_A = 3.6V$	OEDGE/TEN Operational Test Mode	 10 70		 µA µA
			Others	10		nA
I_{IL}	Logic Low Input Current	$V_{IL} = 0V$, $V_{DR} = V_A = 3.0V$	OEDGE/TEN Operational Test Mode	 –10 –600		 µA µA
			Others	–50		nA
C_{IN}	Logic Input Capacitance			3		pF
DIGITAL OUTPUT CHARACTERISTICS						
V_{OH}	High Level Output Voltage	$V_A = V_{DR} = 3.0V$, $I_{OH} = –5$ mA		3.0	**2.4**	V (min)
V_{OL}	Low Level Output Voltage	$V_A = V_{DR} = 3.0V$, $I_{OL} = 5$ mA		0.25	**0.5**	V (max)
C_{OUT}	Digital Output Capacitance			2		pF
DYNAMIC PERFORMANCE						
ENOB	Effective Number of Bits	$f_{IN} = 10$ MHz, $V_{IN} = FS – 0.25$ dB		7.4		Bits
		$f_{IN} = 49$ MHz, $V_{IN} = FS – 0.25$ dB		7.2	**6.8**	Bits (min)
		$f_{IN} = 49$ MHz, $V_{IN} = FS – 0.25$ dB, PLL x8		7.2		Bits
		$f_{IN} = 100$ MHz, $V_{IN} = FS – 0.25$ dB		7.0		Bits
		$f_{IN} = 100$ MHz, $V_{IN} = FS – 0.25$ dB, PLL x4		6.9		Bits
SINAD	Signal-to-Noise & Distortion	$f_{IN} = 10$ MHz, $V_{IN} = FS – 0.25$ dB		46		dBc
		$f_{IN} = 49$ MHz, $V_{IN} = FS – 0.25$ dB		45	**42.7**	dBc (min)
		$f_{IN} = 49$ MHz, $V_{IN} = FS – 0.25$ dB, PLL x8		45		dBc
		$f_{IN} = 100$ MHz, $V_{IN} = FS – 0.25$ dB		44		dBc
		$f_{IN} = 100$ MHz, $V_{IN} = FS – 0.25$ dB, PLL x4		43.4		dBc
SNR	Signal-to-Noise Ratio	$f_{IN} = 10$ MHz, $V_{IN} = FS – 0.25$ dB		47		dBc
		$f_{IN} = 49$ MHz, $V_{IN} = FS – 0.25$ dB		46.3	**43.7**	dBc (min)
		$f_{IN} = 49$ MHz, $V_{IN} = FS – 0.25$ dB, PLL x8		45.8		dBc
		$f_{IN} = 100$ MHz, $V_{IN} = FS – 0.25$ dB		45.6		dBc
		$f_{IN} = 100$ MHz, $V_{IN} = FS – 0.25$ dB, PLL x4		45.6		\dBc
SFDR	Spurious Free Dynamic Range	$f_{IN} = 10$ MHz, $V_{IN} = FS – 0.25$ dB		56		dBc
		$f_{IN} = 49$ MHz, $V_{IN} = FS – 0.25$ dB		56		dBc
		$f_{IN} = 49$ MHz, $V_{IN} = FS – 0.25$ dB, PLL x8		56		dBc
		$f_{IN} = 100$ MHz, $V_{IN} = FS – 0.25$ dB		50		dBc
		$f_{IN} = 100$ MHz, $V_{IN} = FS – 0.25$ dB, PLL x4		49.7		dBc
THD	Total Harmonic Distortion	$f_{IN} = 10$ MHz, $V_{IN} = FS – 0.25$ dB		–55		dBc
		$f_{IN} = 49$ MHz, $V_{IN} = FS – 0.25$ dB		–53		dBc
		$f_{IN} = 49$ MHz, $V_{IN} = FS – 0.25$ dB, PLL x8		–53		dBc
		$f_{IN} = 100$ MHz, $V_{IN} = FS – 0.25$ dB		–49		dBc
		$f_{IN} = 100$ MHz, $V_{IN} = FS – 0.25$ dB, PLL x4		-47.5		dBc

Symbol	Parameter	Conditions	Typical (Note 9)	Limits (Note 9)	Units (Limits)
HD2	2nd Harmonic Distortion	f_{IN} = 10 MHz, V_{IN} = FS – 0.25 dB	–57		dBc
		f_{IN} = 49 MHz, V_{IN} = FS – 0.25 dB	–55		dBc
		f_{IN} = 49 MHz, V_{IN} = FS – 0.25 dB, PLL x8	–55		dBc
		f_{IN} = 100 MHz, V_{IN} = FS – 0.25 dB	–50		dBc
		f_{IN} = 100 MHz, V_{IN} = FS – 0.25 dB, PLL x4	–49.9		dBc
HD3	3rd Harmonic Distortion	f_{IN} = 10 MHz, V_{IN} = FS – 0.25 dB	–62		dBc
		f_{IN} = 49 MHz, V_{IN} = FS – 0.25 dB	–63		dBc
		f_{IN} = 49 MHz, V_{IN} = FS – 0.25 dB, PLL x8	–62		dBc
		f_{IN} = 100 MHz, V_{IN} = FS – 0.25 dB	–56		dBc
		f_{IN} = 100 MHz, V_{IN} = FS – 0.25 dB, PLL x4	–54.6		dBc
IMD	Intermodulation Distortion	f_1 = 11 MHz, V_{IN} = FS – 6.25 dB f_2 = 12 MHz, V_{IN} = FS – 6.25 dB	-50		dBc
POWER SUPPLY CHARACTERISTICS					
I_A	Analog Supply Current	DC Input	72.5		mA
		f_{IN} = 50 MHz	76.8	**88.3**	mA (max)
		PD High	0.3		mA
I_D	Digital Core Supply Current	DC Input, Buffer bypassed	1.2		mA
		f_{IN} = 50 MHz, Buffer bypassed	1.6	**2.1**	mA (max)
		f_{IN} = 50 MHz, 1k writing to Buffer (Note 10)	38	**42.4**	mA
		PDADC High, reading Buffer (Note 10)	1.1		mA
		PD High	0.3		mA
I_P	PLL Supply Current	PLL x2	8.8	**10.1**	mA (max)
		PLL disabled	3.6	**4.3**	mA (max)
		PD High	60		µA
I_{DR}	Output Driver Supply Current	DC Input	7		mA
		f_{IN} = 50 MHz	41	**57**	mA (max)
		PD High	25		µA
$I_A + I_D + I_P + I_{DR}$	Total Operating Current	DC Input, Buffer bypassed, PLL x2 (Note 10)	97.5		mA
		50 MHz Input, writing to Buffer, PLL X2 (Note 10)	164.6	**198**	mA (max)
		PDADC = Hi, reading Buffer, RCLK = 200 MHz, D.C. input	20		mA
		PD High	0.65		mA
PC	Power Consumption	DC Input, Buffer & PLL bypassed	306		mW
		50 MHz Input, writing to Buffer, PLL X2 (Note 10)	543	**653**	mW (max)
		PDADC High, reading Buffer, PLL disabled (Note 10)	66		mW
		PD High	2.15		mW
$PSRR_1$	D.C. Power Supply Rejection Ratio	FSE change with 3.0V to 3.6V change in V_A	48		dB
$PSRR_2$	A.C. Power Supply Rejection Ratio	SNR reduction with 200 mV at 10MHz on supply	TBD		dB

Converter Timing Characteristics

The following specifications apply for $V_A = V_{DR} = +3.3V_{DC}$, $V_{RT} = +1.9V$, $V_{RB} = 0.3V$, $C_L = 50$ pF, $f_{CLK} = 200$ MHz at 50% duty cycle, OEDGE/TEN = 1, Buffer and PLL bypassed. **Boldface limits apply for $T_J = T_{MIN}$ to T_{MAX}**: all other limits $T_J = 25°C$ (Notes 7, 8)

Symbol	Parameter	Conditions	Typical (Note 9)	Limits (Note 9)	Units (Limits)
f_{C1}	Maximum Input Clock Rate	PLL Disabled	210	**200**	MHz (min)
		Using PLL	15	**105**	MHz (min)
f_{C2}	Minimum Input Clock Rate	PLL Disabled	1		MHz
		Using PLL	15		MHz
t_{CL}	Minimum CLK Low Time	(Note 11)		**1.7**	ns (min)
t_{CH}	Minimum CLK High Time	(Note 11)		**1.7**	ns (min)
f_{RC1}	Maximum RCLK Rate	(Note 12)	210	**200**	MHz (min)
f_{RC2}	Minimum RCLK Rate	(Note 12)	2		MHz
t_{RCL}	Minimum RCLK Low Time	(Note 11)		**2.0**	ns (min)
t_{RCH}	Minimum RCLK High Time	(Note 11)		**2.0**	ns (min)
ΔDC	DRDY to RCLK Duty Cycle Delta		0.3	**±3**	%
t_{SU}	REN to RCLK Set-Up Time		−0.4	**−0.8** **4.0**	ns (min) ns (max)
t_{RR}	RCLK Rising Edge to DRDY Rising Edge		3.8	**2.4** **5.9**	ns (min) ns (max)
t_{RF}	RCLK Falling Edge to DRDY Falling Edge		3.5		ns
t_{SKDR}	Skew of DRDY Rising Edge to DATA		160		ps
t_{SKR}	RCLK Falling Edge to First DATA Byte		2.3	**1.8** **7.4**	ns (min) ns (max)
t_{SKEF}	Skew of DRDY Rising Edge to EF Rising Edge		36		ps
t_{CFF}	CLK Rising Edge to FF Rising Edge		4.2		ns
t_{FFW}	FF Rising Edge to WENSYNC Falling Edge	ASW pin high	4.2		ns
t_{CW}	CLK Rising Edge to WENSYNC Rising Edge	PLL Disabled	3.5	**2.4** **5.5**	ns (min) ns (max)
t_{RST}	RESET Pulse Width	(Note 11)		**4**	Write Clock Cycles (min)
t_r	Output Data Rise Time (0.4V to 2.5V)	$C_L = 10$ pF	0.9		ns
		$C_L = 20$ pF	2		ns
t_f	Output Data Fall Time (2.4V to 0.4V)	$C_L = 10$ pF	1.4		ns
		$C_L = 20$ pF	3.2		ns
t_{ODF}	RCLK Rising Edge to Data Output Fall to 0.4V	Reading Buffer	7.0	**4.0** **11.7**	ns (min) ns (max)
		Buffer bypassed, PLL disabled	5.5		ns
t_{ODR}	RCLK Rising Edge to Data Output Rise to 2.5V	Reading Buffer	6.5	**2.3** **13.1**	ns (min) ns (max)
		Buffer bypassed, PLL disabled	5.5		ns
t_{OHF}	RCLK Rising Edge to Data Output Fall to 2.5V	Reading Buffer	3.8	**2.4** **5.5**	ns (min) ns (max)
t_{OHR}	RCLK Rising Edge to Data Output Rise to 0.4V	Reading Buffer	4.5	**2.6** **6.9**	ns (min) ns (max)
t_{SLEW}	Output Slew Rate	Output Falling (2.4V to 0.4V)	1.5		V / ns
		Output Rising (0.4V to 2.5V)	2.3		V / ns

Symbol	Parameter	Conditions		Typical (Note 9)	Limits (Note 9)	Units (Limits)
t_{DRDY1}	PD Low to Device Active	PLL Enabled		20		µs
		PLL Bypassed		2		µs
t_{DRDY2}	PDADC Low to Device Active			2		µs
	Pipeline Delay (Latency)			6		Clock Cycles
t_{AD}	Sampling (Aperture) Delay	CLK Rise to Acquisition of Data	PLL on	3.4		ns
			PLL off	3.9		ns
t_{AJ}	Aperture Jitter	PLL Bypassed		2		ps rms
		PLL Enabled in x8 mode (Note 13)		7		ps rms

Note 1: Absolute Maximum Ratings indicate limits beyond which damage to the device may occur. Operating Ratings indicate conditions for which the device is functional, but do not guarantee specific performance limits. For guaranteed specifications and test conditions, see the Electrical Characteristics. The guaranteed specifications apply only for the test conditions listed. Some performance characteristics may degrade when the device is not operated under the listed test conditions.

Note 2: All voltages are measured with respect to GND = DR GND = 0V, unless otherwise specified.

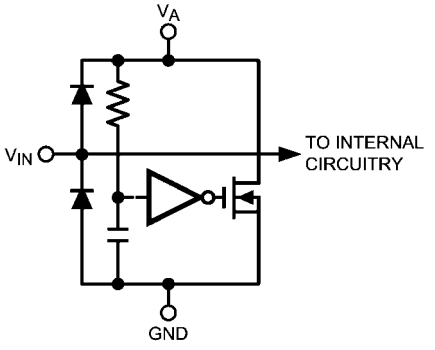
Note 3: When the input voltage at any pin exceeds the power supplies (that is, less than GND or DR GND, or greater than V_A, V_P, V_D or V_{DR}), the current at that pin should be limited to 25 mA. The 50 mA maximum package input current rating limits the number of pins that can safely exceed the power supplies with an input current of 25 mA to two.

Note 4: The absolute maximum junction temperature ($T_J$max) for this device is 150°C. The maximum allowable power dissipation is dictated by $T_J$max, the junction-to-ambient thermal resistance (θ_{JA}), and the ambient temperature (T_A), and can be calculated using the formula $P_D MAX = (T_J max - T_A) / \theta_{JA}$.

Note 5: Human body model is 100 pF capacitor discharged through a 1.5 kΩ resistor. Machine model is 220 pF discharged through ZERO Ohms.

Note 6: See AN-450, "Surface Mounting Methods and Their Effect on Product Reliability".

Note 7: The analog inputs are protected as shown below. Input voltage magnitudes up to V_A + 300 mV or to 300 mV below GND will not damage this device. However, errors in the A/D conversion can occur if the input goes above V_A or below GND by more than 100 mV. For example, if V_A is $3.3V_{DC}$ the input voltage must be $\leq 3.4V_{DC}$ to ensure accurate conversions.



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Note 8: To guarantee accuracy, it is required that V_A, V_D, V_P and V_{DR} be well bypassed. Each supply pin should be decoupled with separate bypass capacitors.

Note 9: Typical figures are at T_J = 25°C, and represent most likely parametric norms. Test limits are guaranteed to National's AOQL (Average Outgoing Quality Level).

Note 10: This current or power is used only during the short time that the buffer is being written to or read from, depending upon the specification.

Note 11: This parameter is guaranteed by design and/or characterization and is not production tested.

Note 12: RCLK should be stopped with the buffer is not being read.

Note 13: Jitter with the PLL enabled is measured with 32k samples and the PLL in the x8 multiplication mode.

Specification Definitions

APERTURE (SAMPLING) DELAY is that time delay after the rise of the sample clock until the input signal is sampled within the ADC.

APERTURE JITTER is the variation in aperture delay from sample to sample. Aperture jitter shows up as input noise.

CLOCK DUTY CYCLE is the ratio of the time that the clock waveform is at a logic high to the total time of one clock period.

DIFFERENTIAL NON-LINEARITY (DNL) is the measure of the maximum deviation from the ideal step size of 1 LSB. Measured at 200 MSPS with a ramp input.

EFFECTIVE NUMBER OF BITS (ENOB, or EFFECTIVE BITS) is another method of specifying Signal-to-Noise and Distortion Ratio, or SINAD. ENOB is defined as (SINAD – 1.76) / 6.02 and says that the converter is equivalent to a perfect ADC of this (ENOB) number of bits.

FULL POWER BANDWIDTH is a measure of the frequency at which the reconstructed output fundamental drops 3 dB below its low frequency value for a full scale input.

FULL-SCALE ERROR is a measure of how far the last code transition is from the ideal 1½ LSB below V_{RT} and is defined as:

$$FSE = V_{max} + 1.5\ LSB - V_{RT}$$

where V_{max} is the voltage at which the transition to the maximum (full scale) code occurs.

INTEGRAL NON-LINEARITY (INL) is a measure of the deviation of each individual code from a line drawn from zero scale (½ LSB below the first code transition) through positive full scale (½ LSB above the last code transition). The deviation of any given code from this straight line is measured from the center of that code value. The end point test method is used. Measured at 200 MSPS with a ramp input.

INTERMODULATION DISTORTION (IMD) is the creation of additional spectral components as a result of two sinusoidal frequencies being applied to the ADC input at the same time. it is defined as the ratio of the power in the second and third order intermodulation products to the power in one of the original frequencies. IMD is usually expressed in dBFS.

MISSING CODES are those output codes that are skipped and will never appear at the ADC outputs. These codes cannot be reached with any input value.

OFFSET ERROR is the error in the input voltage required to cause the first code transition. It is defined as the difference between the voltage required to cause the first code transition and the ideal voltage (1/2 LSB) to cause that transition.

$$V_{OFF} = V_{ZT} - 1/2\ LSB = V_{ZT} - (V_{RT} - V_{RB}) / 512$$

where V_{ZT} is the first code transition input voltage.

OUTPUT DELAY is the time delay after the rising edge of the RCLK input before the data update is present at the output pins.

OUTPUT HOLD TIME is the length of time that the output data is valid after the rise of CLK or RCLK output.

PIPELINE DELAY (LATENCY) is the number of clock cycles between initiation of conversion and when that data is presented to the output driver stage. New data is available at every clock cycle, but the data lags the conversion by the Pipeline Delay plus the Output Delay.

POWER SUPPLY REJECTION RATIO (PSRR) is a measure of how well the ADC rejects a change in the power supply voltage. For the ADC08B200, PSRR1 is the ratio of the change in Full-Scale Error that results from a change in the DC power supply voltage, expressed in dB. PSRR2 is a measure of how well an a.c. signal riding upon the power supply is rejected at the output.

SIGNAL TO NOISE RATIO (SNR) is the ratio, expressed in dB, of the rms value of the input signal at the output to the rms value of the sum of all other spectral components below one-half the sampling frequency, not including harmonics or d.c.

SIGNAL TO NOISE PLUS DISTORTION (S/(N+D) or SINAD) is the ratio, expressed in dB, of the rms value of the input signal at the output to the rms value of all of the other spectral components below half the clock frequency, including harmonics but excluding d.c.

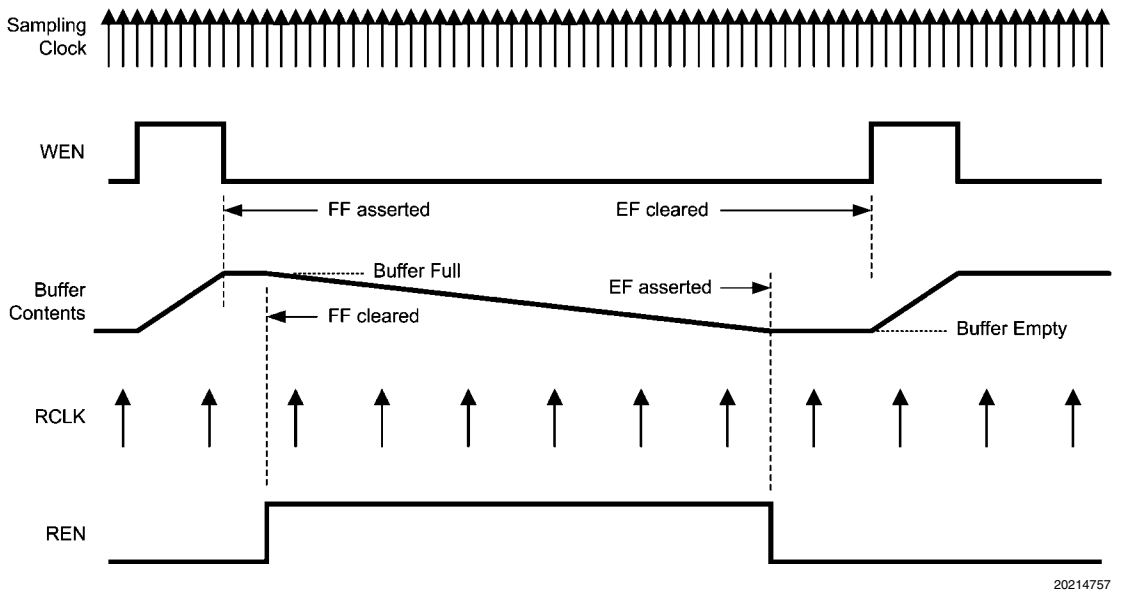
SPURIOUS FREE DYNAMIC RANGE (SFDR) is the difference, expressed in dB, between the rms values of the input signal at the output and the peak spurious signal, where a spurious signal is any signal present in the output spectrum that is not present at the input.

TOTAL HARMONIC DISTORTION (THD) is the ratio expressed in dB, of the rms total of the first nine harmonic levels at the output to the level of the fundamental at the output. THD is calculated as

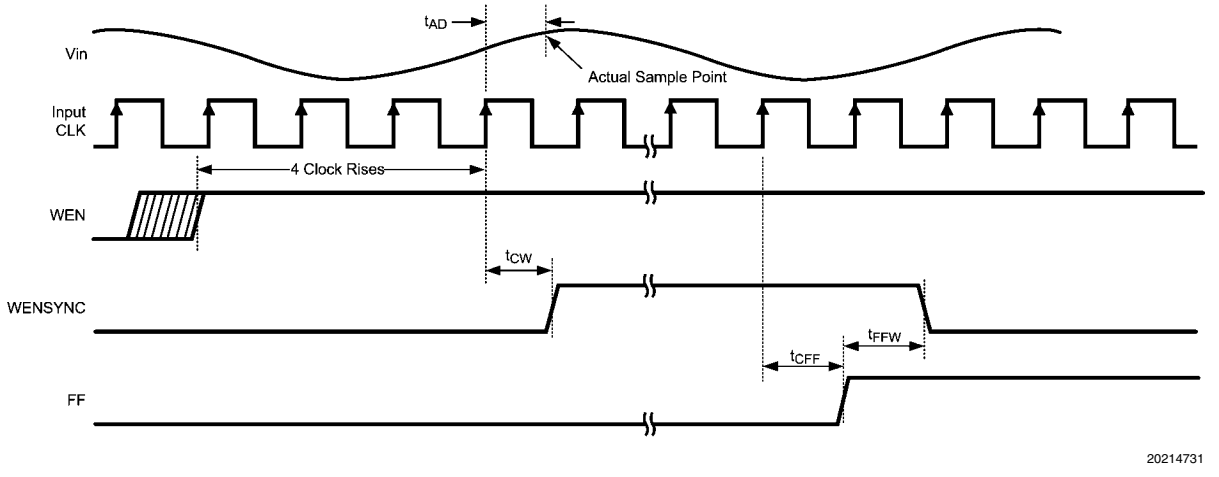
$$THD = 20 \times \log \sqrt{\frac{A_{f2}^2 + \ldots + A_{f10}^2}{A_{f1}^2}}$$

where A_{f1} is the RMS power of the fundamental (output) frequency and A_{f2} through A_{f10} are the RMS power of the first 9 harmonic frequencies in the output spectrum

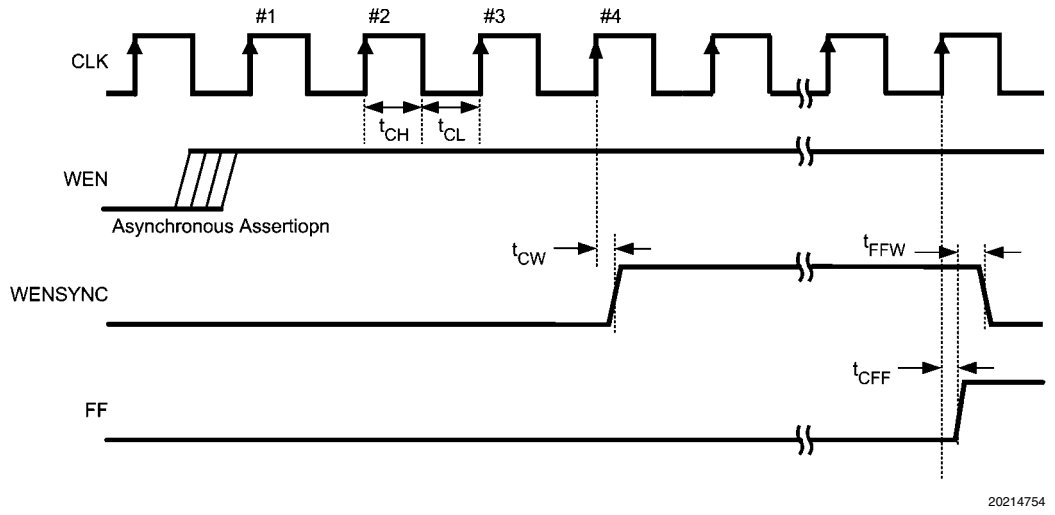
Timing Diagrams (PLL Bypassed)



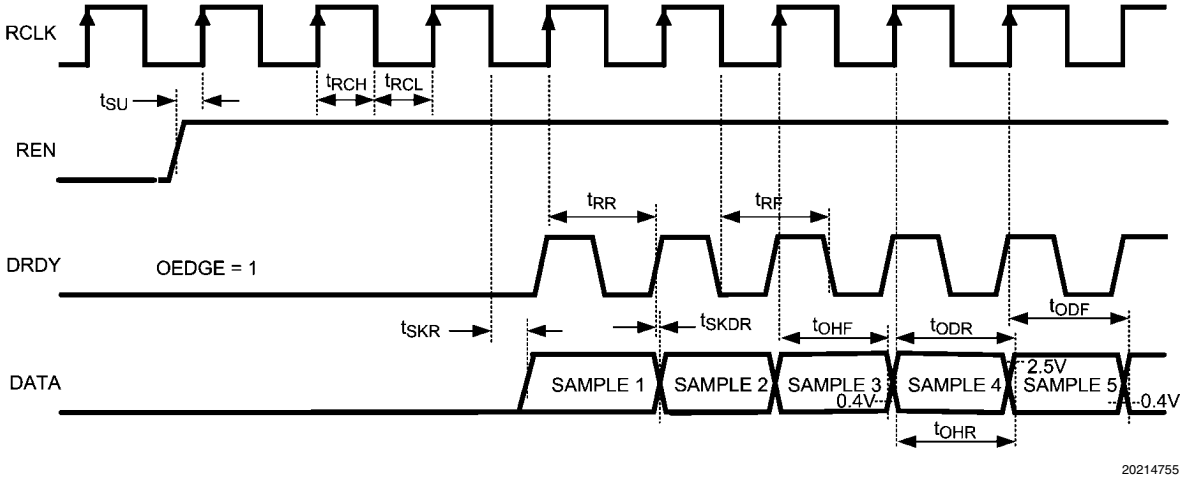
ADC08B200 Data Capture and Read Operation



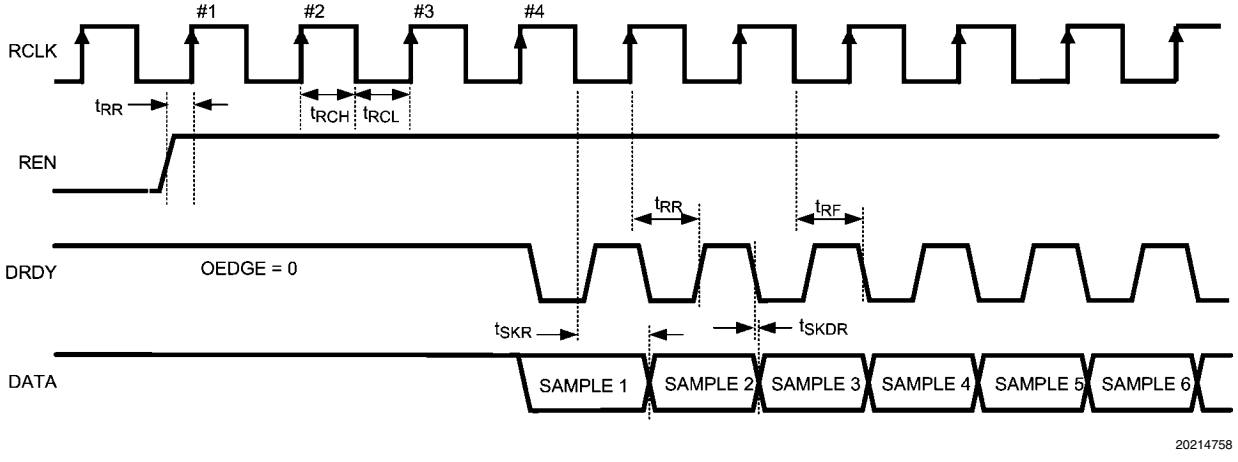
ADC08B200 Capture and Write Enable Timing



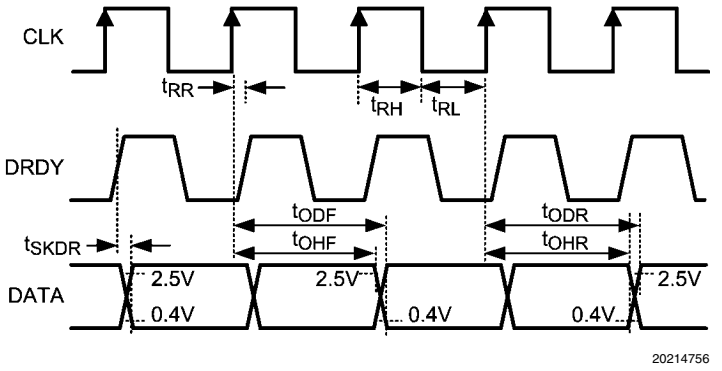
ADC08B200 Buffer Write Timing



ADC08B200 Buffer Read Timing (OEDGE/TEN = 1)



ADC08B200 Buffer Read Timing (OEDGE/TEN = 0)

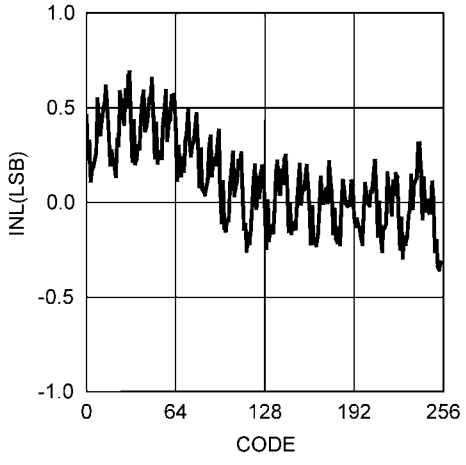


ADC08B200 Buffer Bypassed Timing

Typical Performance Characteristics

$V_A = V_D = V_P = V_{DR} = 3.3V$, $f_{CLK} = 200$ MHz, $f_{IN} = 50$ MHz, PLL & Buffer bypassed, $T_A = 25°C$, unless otherwise stated

INL



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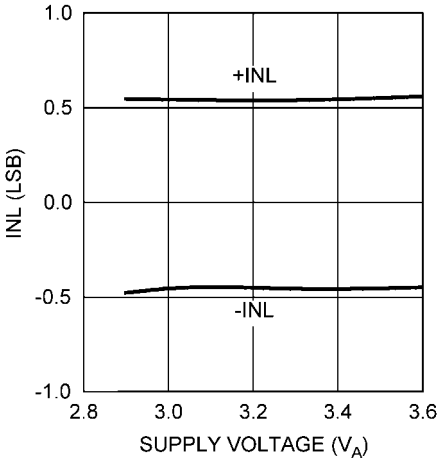
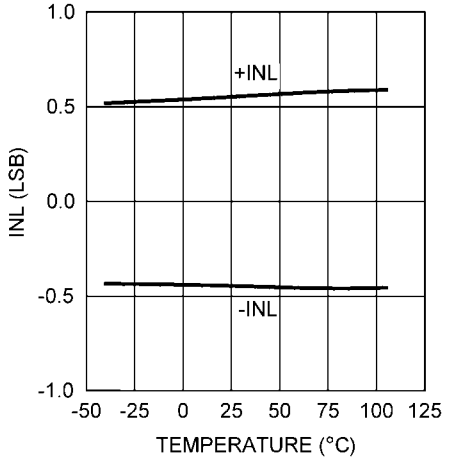
INL vs. Supply Voltage



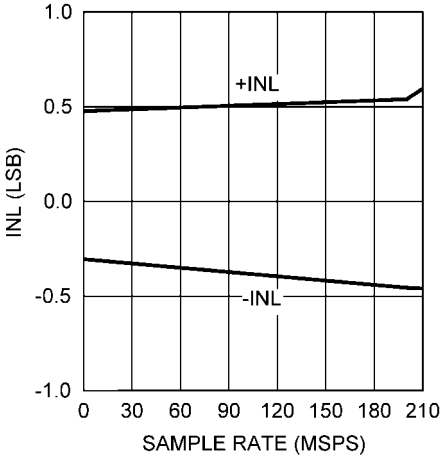
20214715

INL vs. Temperature



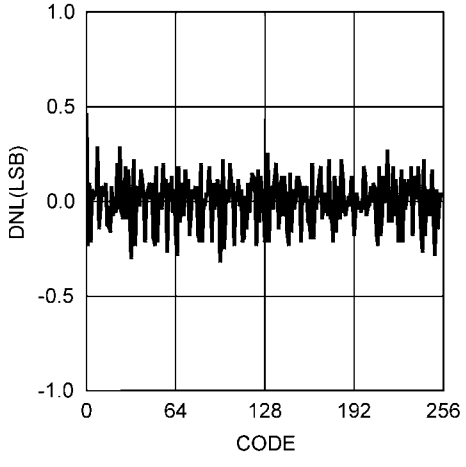
20214714

INL vs. Sample Rate



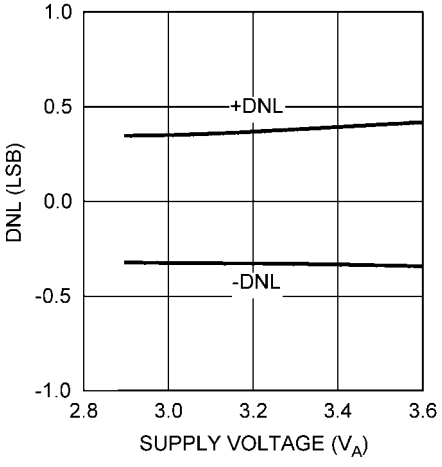
20214710

DNL



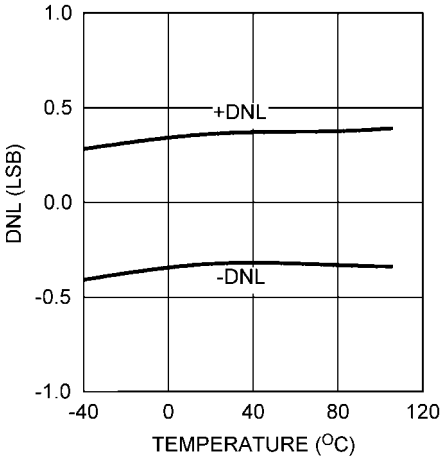
20214709

DNL vs. Supply Voltage



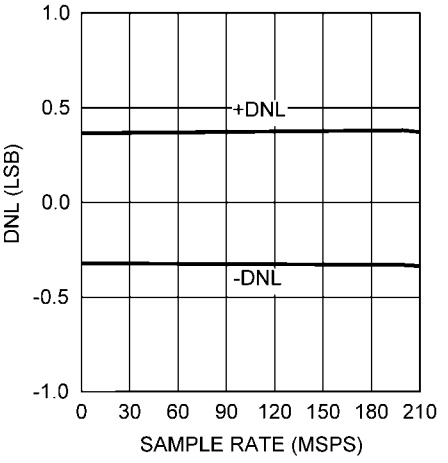
20214718

DNL vs. Temperature



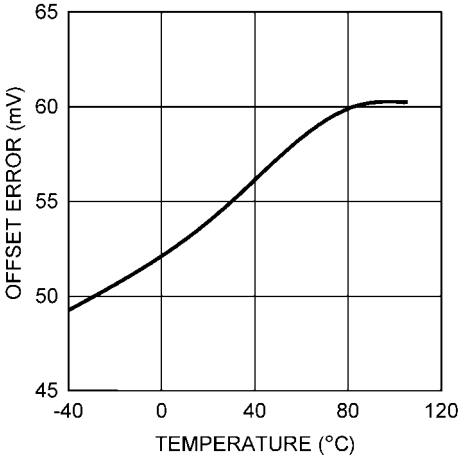
20214717

DNL vs. Sample Rate



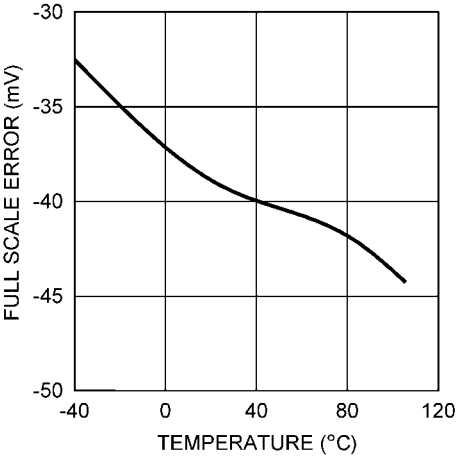
20214711

Offset Error vs. Temperature



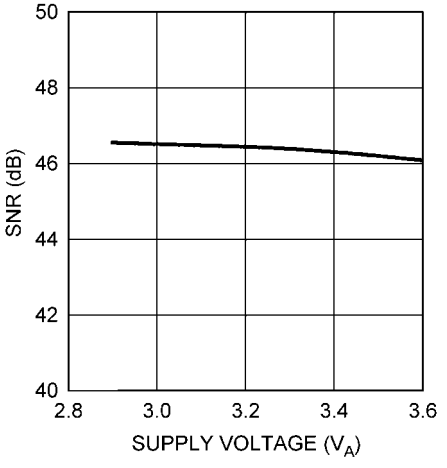
20214761

Full Scale Error vs. Temperature



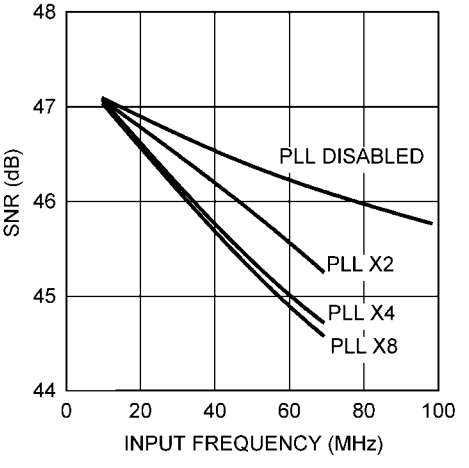
20214762

SNR vs. Supply Voltage



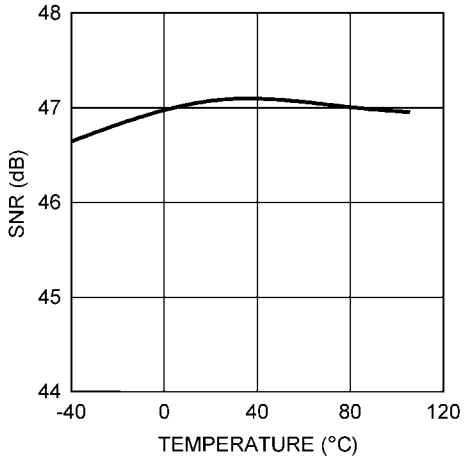
20214721

SNR vs. Input Frequency



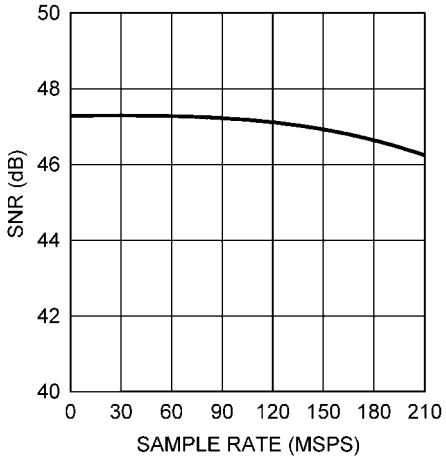
20214723

SNR vs. Temperature



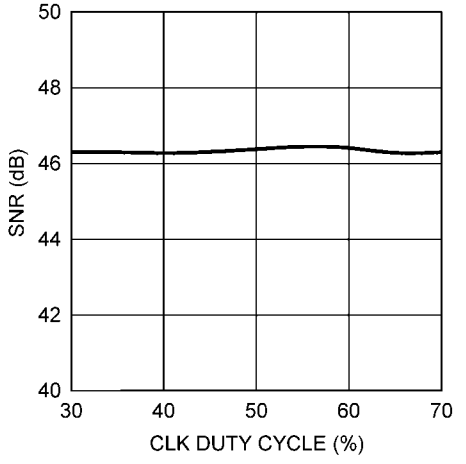
20214720

SNR vs. Sample Rate



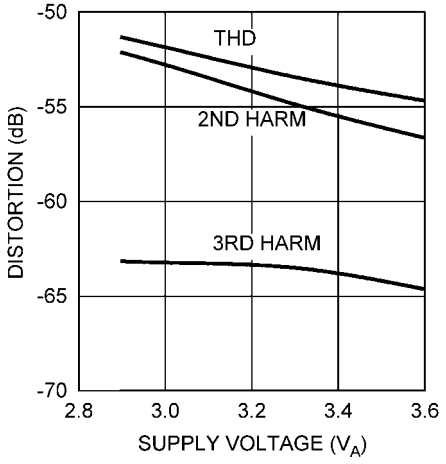
20214712

SNR vs. Clock Duty Cycle



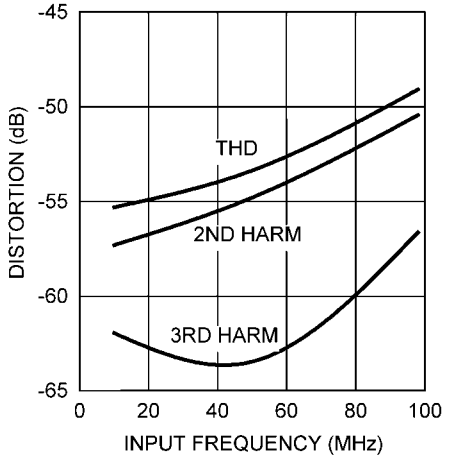
20214724

Distortion vs. Supply Voltage



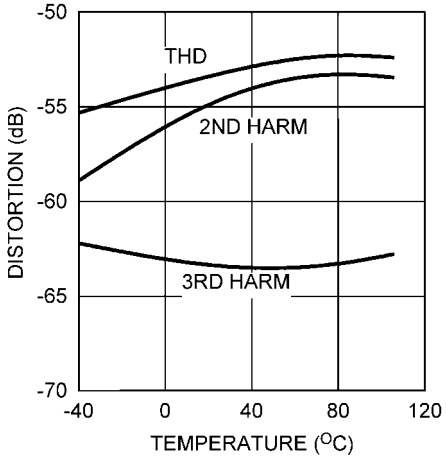
20214726

Distortion vs. Input Frequency



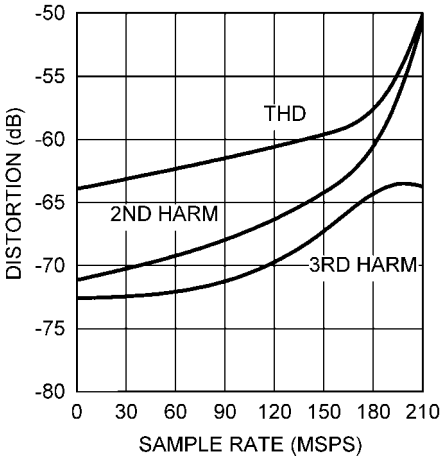
20214728

Distortion vs. Temperature



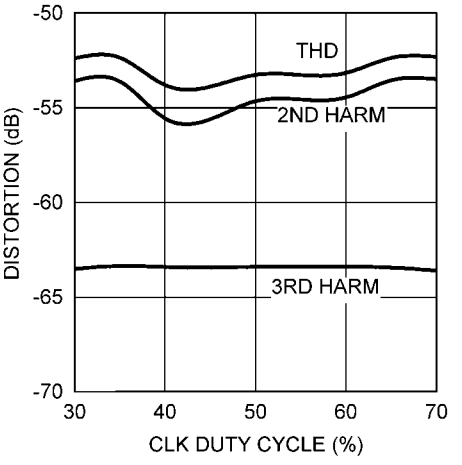
20214725

Distortion vs. Sample Rate



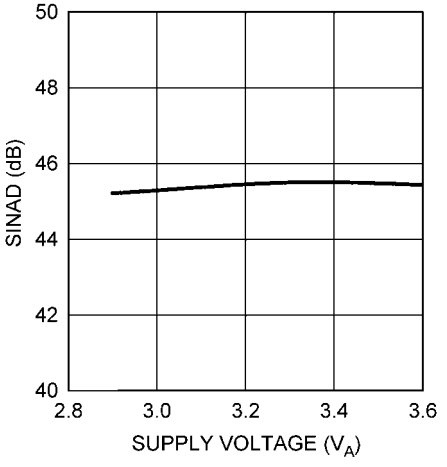
20214713

Distortion vs. Clock Duty Cycle



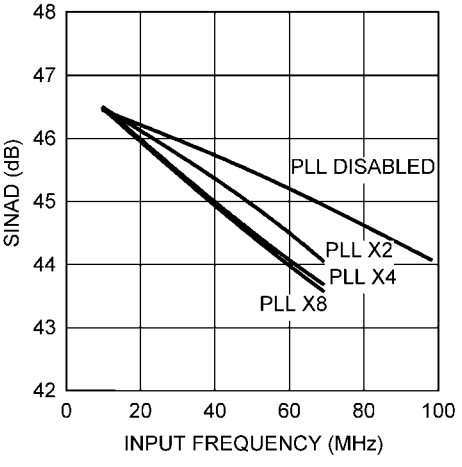
20214729

SINAD vs. Supply Voltage



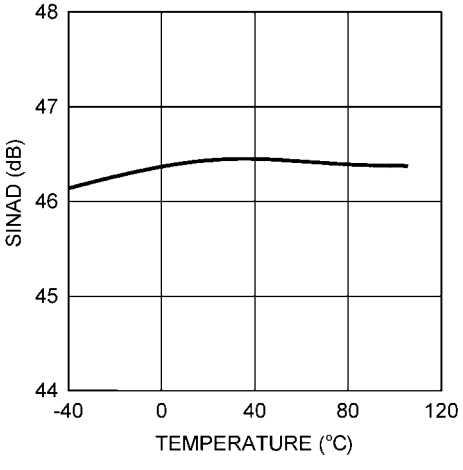
20214738

SINAD vs. Input Frequency



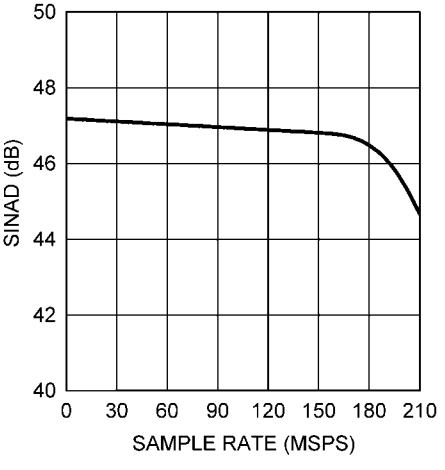
20214739

SINAD vs. Temperature



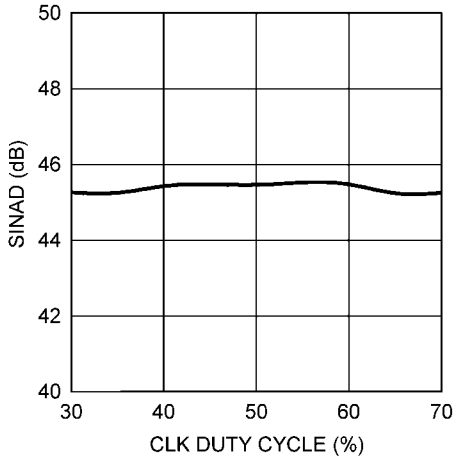
20214730

SINAD vs. Sample Rate



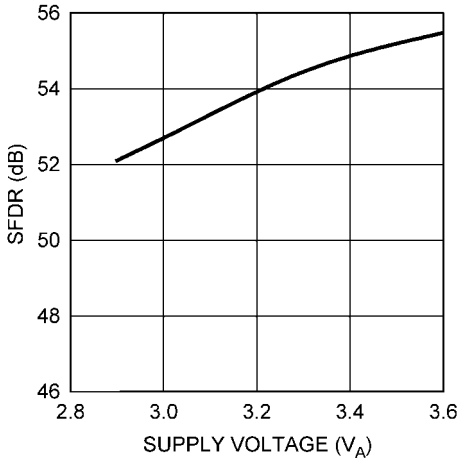
20214716

SINAD vs. CLK Duty Cycle



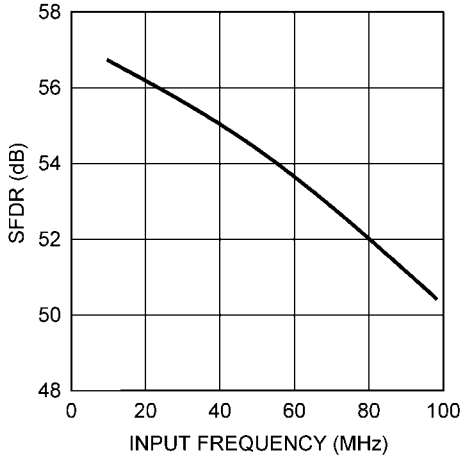
20214740

SFDR vs. Supply Voltage



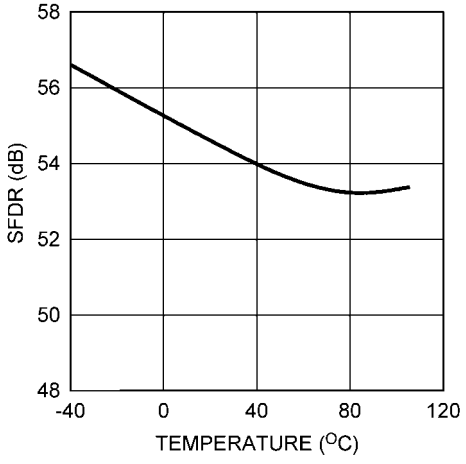
20214727

SFDR vs. Input Frequency



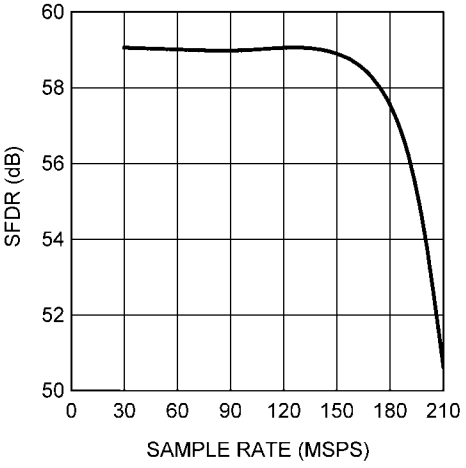
20214741

SFDR vs. Temperature



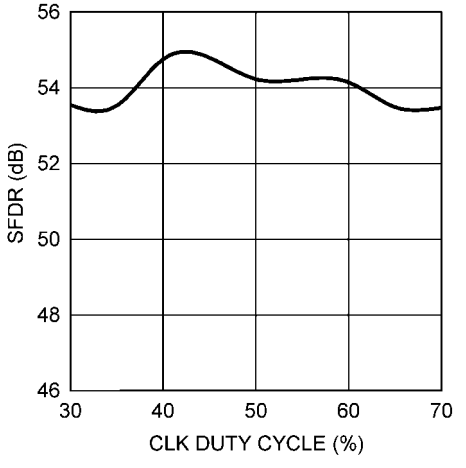
20214742

SFDR vs. Sample Rate



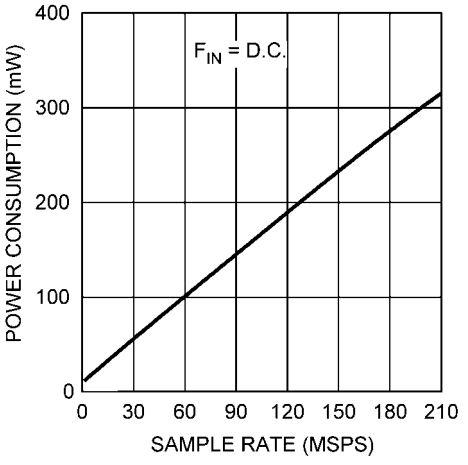
20214744

SFDR vs. Clock Duty Cycle



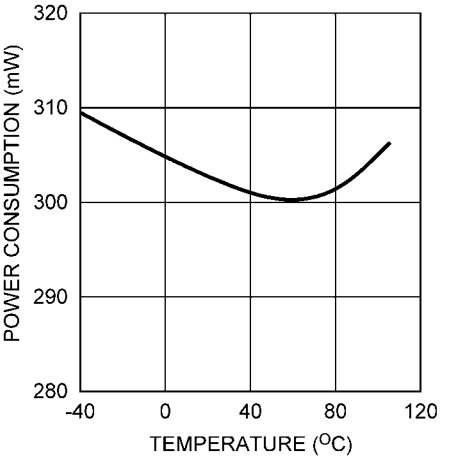
20214745

Power Consumption vs. Sample Rate



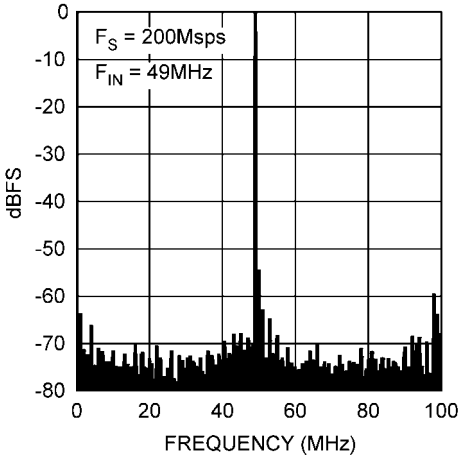
20214719

Power Consumption vs. Temperature



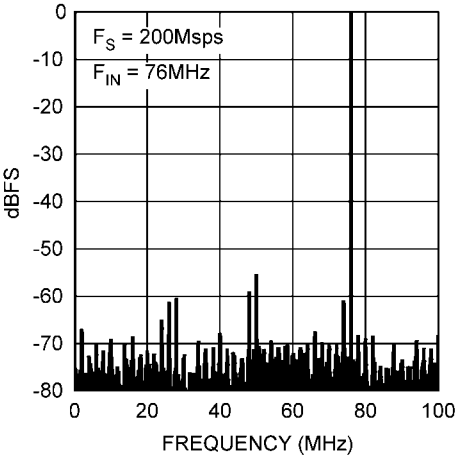
20214760

Spectral Response @ f_{IN} = 49 MHz



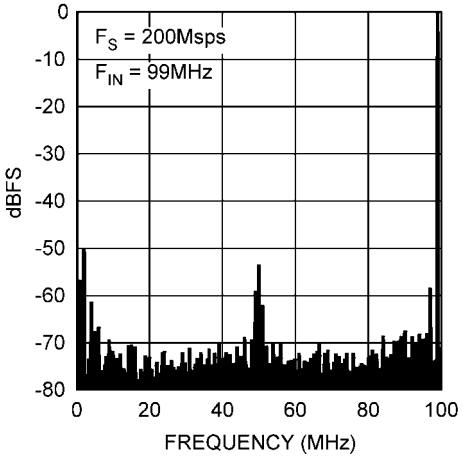
20214746

Spectral Response @ f_{IN} = 76 MHz



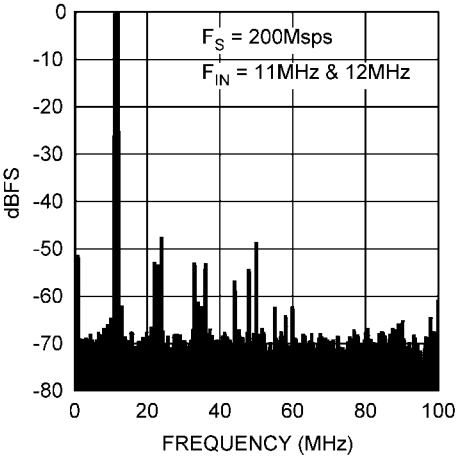
20214747

Spectral Response @ f_{IN} = 99 MHz



20214748

Intermodulation Distortion



20214743

Functional Description

The ADC08B200 integrates an 8-bit, high speed ADC and a configurable capture buffer of up to 1 kilobyte, allowing the sampling and processing tasks to be independent of each other. This functionality is intended for those applications that need to sample an input signal at a high rate and then read the collected samples at a slower rate. The Timing Diagrams illustrate the operation of the ADC08B200.

The analog input signal that is within the voltage range set by V_{RT} and V_{RB} is digitized to eight bits. Input voltages below V_{RB} will cause the output word to consist of all zeroes. Input voltages above V_{RT} will cause the output word to consist of all ones.

The ADC08B200 exhibits a power consumption that is proportional to frequency, limiting power consumption to what is needed at the clock rate that is used. This, its excellent performance over a wide range of clock frequencies and the incorporation of a capture buffer make ADC08B200 an ideal choice for many 8-bit ADC applications.

Data is acquired at the rising edge of the sample clock and, in the buffer bypass mode, the digital equivalent of that data is available at the digital outputs 6 clock cycles plus t_{OD} later. When the Buffer is enabled, the converted data is written to the buffer with each internal conversion clock cycle and can be read out with the RCLK signal. The ADC08B200 will convert as long as a CLK signal is present, but when using the buffer no writing to the buffer will occur when that buffer is full. The output coding is straight binary.

The entire device is in the active state when the Power Down pin (PD) is low. When the PD pin is high, the entire device is in the power down mode, consuming very little power. Holding the clock input low after raising the Power Down pin will further reduce the power consumption in the power down mode.

When the PDADC pin is high, only the A/D converter itself is in the power down mode. The rest of the chip is left powered up so that the capture buffer may be read. If both the PD and PDADC pins are high, the PD pin dominates and the entire device is powered down.

The A/D converter sample clock can be either the clock signal at the CLK input pin or a multiplied version of that clock. The clock multiplier can be 2, 4 or 8. In any case, the sample clock is also used to write the converter data into the capture buffer when that buffer is used.

As long as the chip is not in a power down state and there is a clock signal present, the A/D converter is converting the input signal. However, the data is stored into the capture buffer, when the buffer is used, only while the Write Enable (WEN) input is high. The data is read from the capture buffer with the RCLK signal, which can be a free running clock, while the Read Enable (REN) signal is high.

Note that the capture buffer on this chip must be entirely filled to its configured size before reading its contents can begin. It is not possible to write to and read from the buffer at the same time and the WEN and REN inputs should not be high at the same time. If they are high at the same time, the REN input is ignored. This is true even if the REN input is high first and a read operation is progressing normally when the WEN input goes high. Asserting the WEN input while REN is high will cause the read operation to be aborted, an internal buffer reset to be issued (resetting the pointers) and a capture operation to begin. Although this device is intended for fast capture and slower read out applications, it is possible for the RCLK to operate at the same rate or faster than the sample clock.

Two status flags are provided to manage the capture buffer. As the name suggests, the Full Flag (FF) goes high when the buffer is full. The next sample clock rise after the assertion of FF will begin writing over the oldest data because the write pointer will "wrap around". This is called an "over run" condition. Similarly, the Empty Flag (EF) indicates that the last of the data has been read and the buffer is empty. When EF goes high, the DRDY and Data outputs stop switching and both DRDY and the Data lines remain low if OEDGE=1. Both remain high if OEDGE=0.

The user has the option to stop writing to the buffer automatically upon a buffer full condition with the use of the ASW (Auto Stop Write) input. If the ASW input is low, the buffer will be continually written to, resulting in the possibility of the write pointer "wrapping around" and the data continually being overwritten as long as there is a clock and the WEN input is high. If the ASW input is high, the write operation stops upon reaching the "full" condition.

FF goes low upon device reset and when the "full" condition is removed by starting a transfer operation with the assertion of REN. The EF output goes low when the "empty" condition is removed by starting a capture operation with the raising of WEN. The EF output goes high upon device reset because resetting empties the buffer.

The RESET signal resets the read and write pointers and the EF and FF flags. The RESET signal also stops the read operation early (before the EF flag goes high). Consequently, only a partial read is performed if the RESET input goes high while a buffer read out is under way. This allows the buffer pointers to be reset so a new capture operation can begin. The RESET signal has no effect upon the A/D converter, which has its own internal Power-On Reset circuit.

Note that the RCLK input does not need to be as noise (jitter) free as does the CLK signal. The reason for this is that RCLK is only used to read the Capture Buffer, while the CLK signal is either the ADC sample clock or is the reference for the internal PLL that generates the sample clock for the ADC. Consequently, CLK jitter directly affects the ADC's SNR performance. There is no requirement for the RCLK to have any fixed relationship with CLK in terms of phase or frequency.

Applications Information

1.0 REFERENCE INPUTS

The reference inputs V_{RT} and V_{RB} are the top and bottom of the reference ladder, respectively. Input signals between these two voltages will be digitized to 8 bits. External voltages applied to the reference input pins should be within the range specified in the Operating Ratings and the Electrical Characteristics table. Any device used to drive the reference pins should be able to source sufficient current into the V_{RT} pin and sink sufficient current from the V_{RB} pin to maintain the desired voltages.

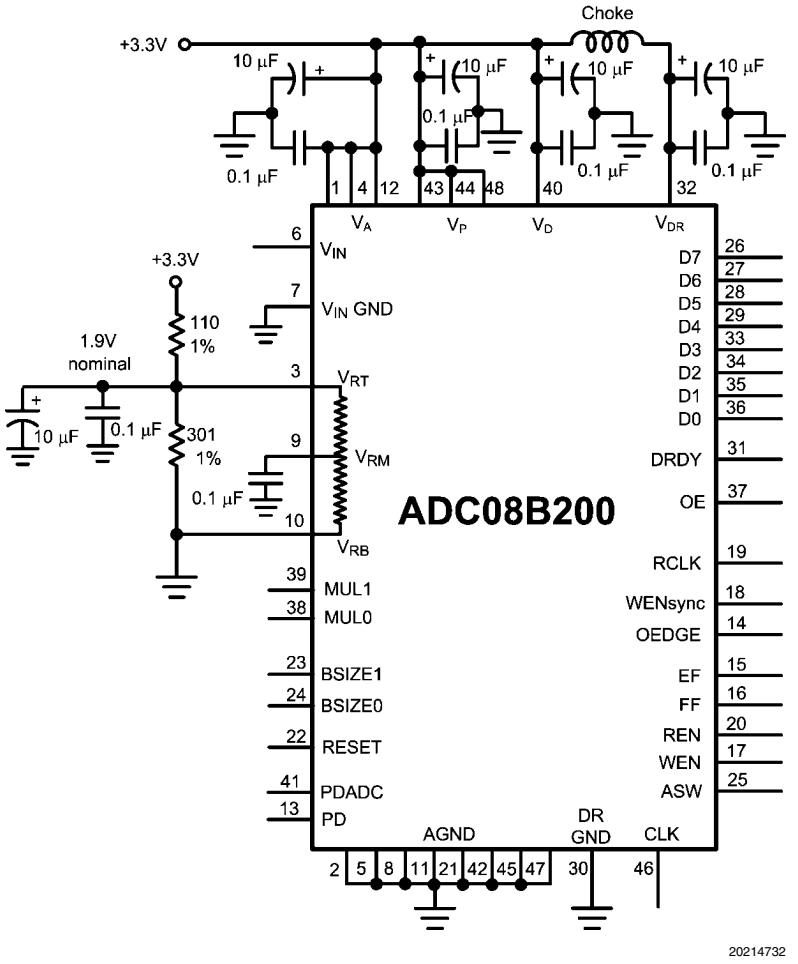


FIGURE 1. Simple, low component count reference biasing. Because of the ladder and external resistor tolerances, the reference voltage of this circuit can vary too much for some applications.

The reference bias circuit of *Figure 1* is very simple and the performance is adequate for many applications. However, circuit tolerances will lead to a wide reference voltage range. Better reference tolerance can be achieved by driving the reference pins with low impedance sources.

The circuit of *Figure 2* will allow a more accurate setting of the reference voltages, with upper and lower reference accuracies of about 16 mV, or about 2 1/2 LSB. The upper amplifier must be able to source the reference current as determined by the value of the reference resistor and the value of (V_{RT} – V_{RB}). The lower amplifier must be able to sink this reference current. Both amplifiers should be stable with a capacitive load.

The *LM8272* was chosen because of its rail-to-rail input and output capability, its high output current capability and its ability to drive large capacitive loads.

The divider resistors at the inputs to the amplifiers could be changed to suit the application reference voltage needs, or the divider can be replaced with potentiometers or DACs for precise settings. The bottom of the ladder (V_{RB}) may be returned to ground if the minimum input signal excursion is 0V.

V_{RT} should always be at least 0.5V more positive than V_{RB}. While V_{RT} may be as high as the V_A supply voltage and V_{RB} may be as low as ground, the difference between these two voltages (V_{RT} – V_{RB} should not exceed 2.3V to prevent a slight waveform distortion.

The V_{RM} pin is the center of the reference ladder and should be bypassed to a quiet point in the ground plane with a 0.1 µF capacitor. DO NOT leave this pin open and DO NOT load this pin with more than 10µA.

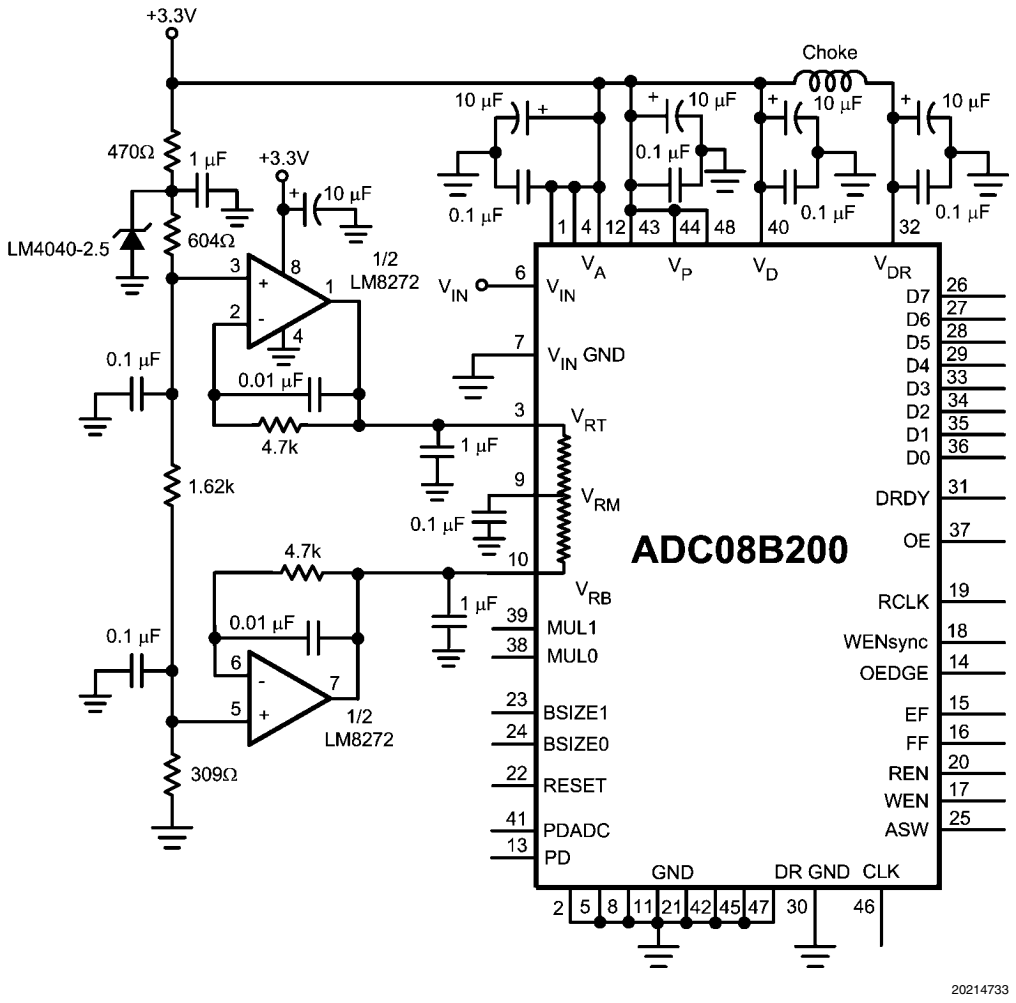


FIGURE 2. Driving the reference to force desired values requires driving with a low impedance source.

2.0 THE ANALOG INPUT

The analog input of the ADC08B200 is a switch followed by an integrator. The input capacitance changes with the clock level, appearing as 3 pF when the clock is low, and 4 pF when the clock is high. The sampling nature of the analog input causes current spikes at the input that result in voltage spikes there. These spikes are normal and need not be eliminated. However, any amplifier used to drive the analog input must be able to settle within the clock high time. Using a single pole RC filter between the amplifier and the ADC input will minimize the effects of these transients on the driving amplifier. The cutoff frequency of this filter should be approximately the same as the ADC sample rate for Nyquist applications. Choose a capacitor value of 33 pF to 51 pF and a resistor value according to the formula

$$R = \frac{1}{2 \cdot \pi \cdot (C + 6\ pF) \cdot f_S}$$

where f_S is the converter sample rate. The added 6 pF in the formula above allows for the ADC input capacitance and a small board capacitance. For undersampling applications, eliminate the capacitor and chose a pole frequency of about 2 to 3 times the maximum input frequency, using the ADC input capacitance when the the clock is high, plus trace capacitance, for the filter capacitor. The optimum time constant for this circuit depends not only upon the amplifier and ADC, but also upon the circuit layout and board material. The LMH6702 and the LMH6628 have been found to be good amplifiers to drive the ADC08B200.

Figure 3 shows an example of an input circuit using the LMH6702 at the ADC08B200 input. The input amplifier should incorporate some gain as most operational amplifiers exhibit better phase margin and transient response with gains above 2 or 3 than with unity gain. If an overall gain of less than 3 is required, attenuate the input and operate the amplifier at a higher gain, as indicated in *Figure 3*.

This will provide optimum SNR performance for Nyquist applications. Best THD performance is realized when the capacitor and resistor values are both zero, but this would compromise SNR and SINAD performance. Generally, the capacitor should not be added for undersampling applications.

The circuit of *Figure 3* has both gain and offset adjustments. If you eliminate these adjustments normal circuit tolerances may result in signal clipping unless care is exercised in the worst case analysis of component tolerances and the input signal excursion is appropriately limited to account for the worst case conditions.

Full scale and offset adjustments may also be made by adjusting V_{RT} and V_{RB}, perhaps with the aid of a pair of a DACs or a dual DAC. Of course, this circuit may be implemented without provision for offset and gain adjustments, but component tolerances would require the planned use of less than the full dynamic range of the ADC.

One advantage of having access to the bottom of the reference ladder (V_{RB}) is that the voltage at the analog input does not have to come to 0V to cause an output code of zero. If V_{RB} is set high enough, the negative supply on the amplifier driving the analog input may be at ground. How high V_{RB} needs to be set to allow this will depend upon the amplifier type and how close to its negative supply (or ground) the output can go while maintaining linearity. This might be 100mV to 150mV for a rail-to-rail output amplifier or 1 Volt for other amplifiers.

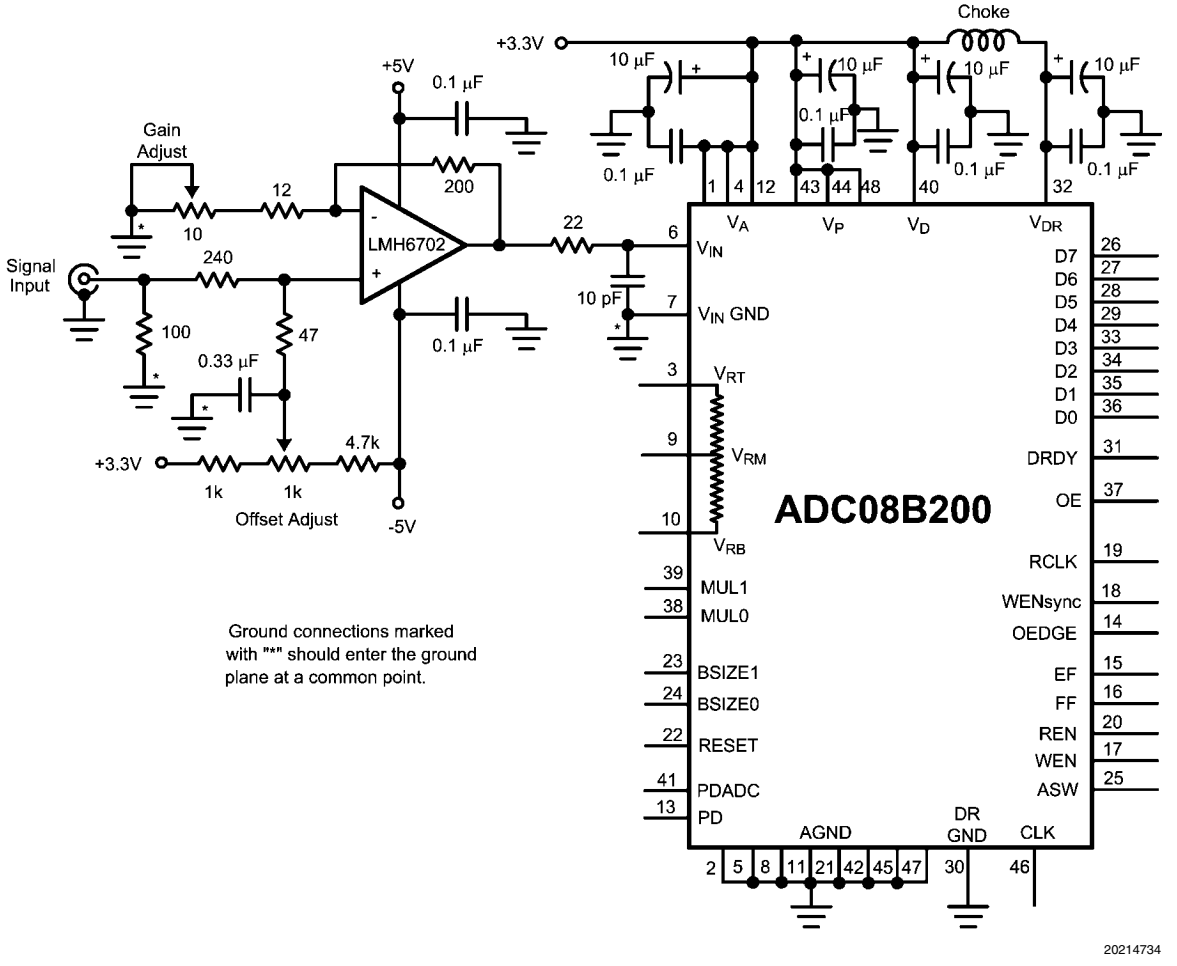


FIGURE 3. The input amplifier should incorporate some gain for best performance (see text).

3.0 POWER SUPPLY CONSIDERATIONS

A/D converters draw sufficient transient current to corrupt their own power supplies if not adequately bypassed. Generally, a 10 µF tantalum or aluminum electrolytic capacitor should be provided for each of the four supplies and a 0.1 µF ceramic chip capacitor placed within one centimeter of each converter power supply pin.

To further lower the inductance in series with the capacitors, mount the 0.1 µF capacitors on the same side of the board as the ADC and use 2 to 4 closely spaced through holes to connect the ground side of the capacitors to the ground plane. The through holes used to ground one side of these capacitors should not be used to connect anything else to ground. Leadless chip capacitors are preferred because they have low lead inductance.

While a single voltage source is recommended for the V_A, V_D and V_P supplies of the ADC08B200, the V_A supply pins should be well isolated from the other supply pins to prevent any digital noise from being coupled into the analog portions of the ADC. A choke is recommended between the V_{DR} supply pin and the other supply pins with adequate bypass capacitors close to each supply pin, as shown in *Figure 1*, *Figure 2* and *Figure 3*.

As is the case with all high speed converters, the ADC08B200 should be assumed to have little power supply rejection. None of the supplies for the converter should be the supply that is used for other digital circuitry in any system with a lot of digital power being consumed. The ADC supplies should be the same supply used for other analog circuitry.

No pin should ever have a voltage on it that is in excess of the supply voltage or below ground by more than 300 mV, not even on a transient basis. This can be a problem upon application of power and power shut-down. Be sure that the supplies to circuits driving any of the input pins, analog or digital, do not come up any faster than does the voltage at the ADC08B200 power pins.

4.0 THE DIGITAL INPUT PINS

The ADC08B200 has 14 digital input pins, 6 of which are used for buffer control and 2 of which are used for PLL control.

4.1 The PD Pin

The Power Down (PD) pin, when high, puts the ADC08B200 into a low power mode where power consumption is significantly reduced below its operating power. Stopping the clock after raising the PD input will reduce power consumption even more. The ADC is active and will perform normally about 2 microseconds after the PD pin is brought low. However, the PLL, if used, requires 20 microseconds to stabilize after the PD pin is brought low.

The digital output pins retain the last conversion output code when either the clock is stopped or the PD pin is high. The buffer contents are lost when PD is brought high.

4.2 The PDADC Pin

When the PDADC pin is high the ADC is powered down. The capture buffer is active and the data within it may be clocked out.

This is helpful for reduction of average power consumption as the ADC can be powered down while data is being read from the buffer. As with the PD pin, the ADC is active and will perform normally about 2 microseconds after the PDADC pin is brought low. Again the PLL, if used, requires 20 microseconds to stabilize after the PD pin is brought low.

The PLL remains active when the PDADC input is high to allow for faster initiation of data capture after PDADC is lowered. Stopping the input clock when PDADC is invoked can result in a loss of PLL lock and a longer than normal recovery time from PDADC.

4.3 The Master CLK Pin

Although the ADC08B200 is tested and its performance is guaranteed with a 200 MHz clock, it typically will function well with clock frequencies as indicated in the Electrical Characteristics table.

The low and high times of the clock signal can affect the performance of any A/D Converter. Because achieving a precise duty cycle is difficult, the ADC08B200 is designed to maintain performance over a range of duty cycles. While it is specified and performance is guaranteed with a 50% clock duty cycle and 200 Msps, ADC08B200 performance is typically maintained with clock high and low times and a clock frequency range as indicated in the electrical table. Note that clock minimum low and high times may not be simultaneously imposed.

The ADC Clock input line should be series terminated at the clock source in the characteristic impedance of that line if the clock line is longer than

$$\frac{t_r}{6 \times t_{prop}}$$

where t_r is the clock rise time and t_{prop} is the propagation rate of the signal along the trace. Typical t_{prop} is about 150 ps/inch (59 ps/cm) on FR-4 board material.

It is always best and advisable that one clock source pin drive a single destination pin for best signal integrity. However, if the clock source is used to drive more than just one destination, the CLK pin should be a.c. terminated with a series RC to ground such that the resistor value is equal to the characteristic impedance of the clock line and the capacitor value is

$$C \geq \frac{4 \times t_{prop} \times L}{Z_o}$$

where t_{PROP} is the signal propagation rate down the clock line, "L" is the line length and Z_O is the characteristic impedance of the clock line. The units of "L" must be compatible with the units of t_{PROP}. This termination should be located as close as possible to, but within one centimeter of, the ADC08B200 clock pin. Furthermore, this termination should be beyond the receiving pin as seen from the clock source. For FR-4 board material, the value of C becomes

$$C \geq \frac{6 \times 10^{-10} \times L}{Z_o}$$

Where L is the length of the clock line in inches.

4.4 The RESET Pin

A high level at this Reset input resets all control logic on the chip, including the buffer's read and write counters. The FF output is reset low and the EF flag is reset high upon a device reset. Invoking a reset during the WRITE phase can cause buffer data to be corrupted. A reset during the READ phase will stop the READ phase before it is completed.

The RESET signal is asynchronous and should be at least 4 sample clock cycles wide. If no RESET is provided, the chip generates its own internal reset signal at the beginning of the buffer write phase.

4.5 The OEDGE/TEN Pin

If this Output Edge Select input is high, the data outputs transition with the rising edge of the DRDY output. If this input is low, the data outputs transition with the falling edge of the DRDY. Forcing a potential of $V_A/2$ at this input enables the Test Mode. There is an on-chip pull-up resistor at this pin, so the device interprets a floating input at this pin to be a logic high. See *Section 10.0 TEST PATTERN OUTPUT* for the output test pattern.

4.6 The OE Pin

A high level at this Output Enable input enables the output buffers. A low level at this input puts the digital data output pins, including the DRDY output, into a high impedance state. The only exception is in the Test Pattern Mode, where the OE input is ignored and the the DRDY and data output pins are active regardless of the OE pin status.

Caution: Although this device has a TRI-STATE output, maintaining optimum noise performance requires keeping the capacitance on the data output pins as low as possible. Therefore, it is never a good idea to connect the output pins to a bus. Each output pin should be connected to a single input with lines as short as possible.

4.7 Buffer-Associated Pins

The on-chip buffer is 1 kilobyte (1,024 bytes) in size and is controlled through six (6) TTL-CMOS compatible digital input pins.

4.7.1 THE RCLK PIN

When the capture buffer is enabled, the RCLK input is used to read the data from the buffer. The data output and the EF flag transition with the rise of RCLK.

It is best to halt the RCLK when not reading the buffer to minimize its impact upon noise performance. RCLK may be stopped in either the high or the low state.

4.7.2 THE WEN PIN

A high level at this Write Enable input causes data to be written into the capture buffer. One byte is written with the rise of each sample clock. This input may go high asynchronously.

4.7.3 THE REN PIN

A high level at this Read Enable input causes data to be read from the capture buffer. One byte is read with the rise of each RCLK input. This signal should go high synchronous with the RCLK input and should not be high while the WEN input is high. If this input is high while the WEN input is high, the WEN input has priority and the REN input is ignored, regardless of which of these two inputs is high first. It is not possible to read from the buffer while a write to the buffer is in progress.

4.7.4 THE ASW PIN

This Auto-Stop Write input has a dual function. With writing to the buffer enabled and this ASW high, this pin acts as the ASW (Auto-Stop Write) input, which causes writing to the buffer to halt once the buffer is full (FF high). This prevents write "wrap around" and the over-writing of older data. When writing to the buffer is disabled, this pin is ignored. When the device is in Test Mode, this pin acts as the Output Edge Select input and functions as described for the OEDGE/TEN input.

4.7.5 THE BSIZE PINS

The two Buffer Size input pins (BSIZE0 and BSIZE1) are used to select the required buffer size for the application or to bypass the buffer altogether. Refer to *Section 8.0 USING THE DATA BUFFER* for use of these pins

5.0 PLL CONTROL: THE MULT PINS

The two MULT input pins (MULT0 and MULT1) are used to select the CLK Multiplier for the internal PLL, or to bypass the PLL. Refer to *Section 7.0 CLOCK OPTIONS* for more information.

6.0 DIGITAL OUTPUT PINS

The ADC08B200 has 12 digital output pins: 8 Digital Data Output pins, DRDY, WENSYNC, EF and FF

6.1 Digital Data Outputs

This 8-bit bus is LVTTL/LVCMOS compatible, with a Straight Binary output format. Data is clocked out on this bus in one of two ways. When the internal buffer is bypassed, data is clocked out at the sample clock rate. When the internal buffer is used, data is clocked out at the RCLK rate. In either case, data is clocked out on the rising edge of the appropriate clock. Refer to *Section 7.0 CLOCK OPTIONS* for information on sample rate determination.

When the Capture Buffer is bypassed, data is read directly from the converter at the sample clock rate.

When the capture buffer is used, data is read from the capture buffer and presented at these pins when the REN input is high. If OEDGE/TEN is high, the digital data output and DRDY are held low when no valid data is being sent out. If OEDGE/TEN is low, the digital data and DRDY are held high when no valid data is being sent out. These pins source data at the converter sample rate when the buffer is disabled.

Whether the buffer is enabled or not, the output data is provided synchronous with DRDY. That is, the data transition occurs with the edge of DRDY defined by OEDGE/TEN such that the data transitions on the rise of DRDY if OEDGE/TEN is high or on the fall of DRDY if OEDGE/TEN is low.

The data output drivers are capable of sourcing and sinking a relatively high current to enable rapid charging and discharging of the output capacitance, thereby allowing fast output rise and fall times. The data outputs should be as lightly loaded as possible to minimize on-chip noise and the resulting loss of SNR performance. Note the specified load capacitance at the heading of the Electrical Characteristics Table.

6.2 The DRDY Pin

This output is intended for use to latch output data into a receiving device and transitions with the transition of the digital data outputs. The synchronizing edge of the DRDY signal can be selected with the OEDGE input. When the buffer is not used, DRDY is active as long as the ADC is functioning. When the buffer is enabled, DRDY is active only while data is being sent out. When no valid data is being sent out, the DRDY output sense is the opposite of the OEDGE input. When OE is low and the device is NOT in the Test Pattern Mode (OEDGE floating or at V_A / 2), the DRDY output is in the high impedance state, as are the data outputs. However, in Test Pattern Mode the OE input is ignored and all output drivers (data and DRDY) are in the active state. When the buffer is used, DRDY is held low at all times except during the buffer read phase, where it switches in synchronism with the data output pins.

The DRDY output should be have a load that is identical to the load of the digital data outputs to ensure that the DRDY output edge transitions at the same time as does the data.

6.3 The WENSYNC Pin

This output is synchronous with the internal sample clock and is provided as an indication as to when sampling takes place. The actual point in time when sampling takes place is as indicated in the *"Capture and Write Enable"* Timing Diagram.

6.4 The EF Pin

This Empty Flag goes high, synchronous with the internal sample clock, when the Capture Buffer is empty, either by the buffer having been completely read or upon RESET of the device. This output goes low when one or more bytes is written to the buffer. When EF goes high, the DRDY and Data outputs stop switching and both DRDY and the Data lines remain low if OEDGE=1, or high if OEDGE=0.

6.5 The FF Pin

The Full Flag output indicates that the buffer is full and goes high, synchronous with the internal sample clock, when the capture buffer is full. If the WEN input remains high, the rise of the next sample clock after the FF output goes high will cause the buffer pointer to "wrap around" and start writing over the previous data unless the ASW input is high. The FF signal goes low when the REN signal goes high and the full condition no longer exists. This signal also goes low upon a RESET of the device.

7.0 CLOCK OPTIONS

The ADC08B200 incorporates a PLL to facilitate clocking. The PLL, like any PLL or DLL, can add phase noise to the clock signal and so to the conversion process. The effect of this phase noise increases with higher analog signal input frequencies. If a stable clock source at the desired sample rate is available, it is preferable to use that clock as the sample clock for the ADC08B200, bypassing the PLL. If such a source is not available, the internal PLL may be used to multiply the input clock frequency by 2, 4 or 8 to obtain the desired sample rate from a lower frequency clock source.

Bypassing the PLL or setting the CLK frequency multiplier is accomplished through the use of the two MULT pins as indicated in *Table 1*. Expected noise performance with and with-

out the use of the PLL is indicated in the Typical Performance Characteristics of this data sheet.

TABLE 1. MULT Pin Function

MULT1	MULT0	CLK Frequency Multiplier	CLK Freq. Range (MHz)
0	0	1	1 - 210
0	1	2	15 - 105
1	0	4	15 - 50
1	1	8	15 - 25

The internal sampling clock frequency is the input clock frequency at the CLK pin multiplied by the multiplier in *Table 1*. When the PLL is bypassed, the input clock at the CLK pin is used as the sample clock and the PLL is disabled.

8.0 USING THE DATA BUFFER

The Data Buffer has read and write pointers and the first word written to it is the first word read from it. The Data Buffer is configurable to 256-, 512-, or 1024- bytes, and must be completely filled to the configured number of bytes before it can be read. The "FF" flag goes high once the configured number of bytes is in the buffer are read. Once the data buffer contents are completely read, indicated by the "EF" flag going high, the same data cannot be read again. It is possible to read back only part of the buffer contents. Asserting the WEN high input, even while a valid read operation is under way, will cause a resetting of the read and write pointers and initiation of a write operation.

The WEN (Write Enable) input is used to enable writing to the buffer, while the REN (Read Enable) input is used to enable reading from the buffer. If both of these are high, the WEN input dominates and the REN input is ineffective until WEN goes low. If the WEN pin remains high after the buffer is full, the previous contents are over-written. The ASW (Auto-Stop Write) pin may be used to automatically stop writing to the buffer when it is full to the configured number of bytes. See *Sections 4.7.2 THE WEN PIN*, *4.7.3 THE REN PIN* and *4.7.4 THE ASW PIN* for information on these inputs.

The BSIZE inputs are used to configure the Data Buffer size (described in *Table 2*). The user has a choice of using the buffer or bypassing it.

When the buffer is used and its contents have been read, the DRDY and the Data Outputs maintain the opposite sense of the OEDGE input. When the buffer is bypassed, it is not used and the data is presented at the ADC data output pins at the same rate as the sample clock. *Table 2* indicates the choices available and the BSIZE pin settings to achieve each.

When the buffer is bypassed (both BSIZE pins low), the ADC output is sent directly to the output port at the sample clock rate without going through the buffer. In this mode all buffer control inputs (WEN, REN, ASW and RCLK) are ignored and the EF and FF outputs are held low. The DRDY output may be used to capture the data at the output port.

TABLE 2. BSIZE Pin Function

BSIZE1	BSIZE0	Buffer Size
0	0	Buffer is bypassed
0	1	256 bytes
1	0	512 bytes
1	1	1024 bytes

8.1 Reading the Buffer

There are two options for reading the contents of the ADC08B200 buffer. Since the DRDY output is source-synchronous with the data output, it may be used to read the buffer data into the receiving device. This buffer read method works well at any read rate for which the device is capable and is the preferred method of reading the buffer at read rates greater than about 70 to 80 MHz. When using this method it is important that the DRDY line electrical length and load are matched with those of the data lines in order to minimize DRDY to data output skew.

The other read option is to ignore the DRDY signal and use the RCLK signal to read the ADC08B200 buffer. This method may be easier to implement than is the use of DRDY when using a DSP or processor to read the buffer. However, because RCLK is not source-synchronous with the data lines, this method is not recommenced for buffer read (RCLK) rates above about 60 to 70 MHz. Specifications for $t_{OHF} + t_F / 2$and $t_{OHR} + t_R / 2$ provide the necessary timing information of output data relative to RCLK. Keep in mind that the device timing specifications apply at the device pins. Additional system delays must be taken into account to determine the RCLK to Data timing relationship at the receiving device.

Regardless of which method is used, RCLK is needed to clock the captured data from the buffer. The buffer can not be read without RCLK. Likewise reading the test pattern also requires the use of RCLK.

RCLK may be stopped when not reading the buffer and may be stopped in either the high state or the low state.

9.0 MODES OF OPERATION

The ADC08B200 has several modes of operation. These modes are detailed in *Table 3*.

The buffer function is controlled by the BSIZE pins, BSIZE0 and BSIZE1, as indicated in *Table 4*. The buffer can be bypassed and data read directly from the ADC by setting both of the BSIZE pins low.

TABLE 3. Modes of Operation

PD	PDADC	WEN	REN	Power State	Operational State
1	x	x	x	Shutdown	Shutdown, non-operational
0	1	0	0	Buffer Active, ADC Shutdown	ADC powered down, no data can be captured. Buffer may be read.
0	x	0	1	Active	Data is being read from buffer with RCLK
0	0	0	0	Active	If buffer is bypassed, data is present at output bus. If buffer is used, the chip is ready to capture data to the buffer.
0	0	1	x	Active	The ADC's digital output is being captured to the buffer. The REN input is ignored.
0	1	1	x	Buffer Active, ADC Shutdown	*PROHIBITED.* WEN input is ignored.

TABLE 4. Buffer Write/Read

BSIZE1	BSIZE0	WEN	REN	Buffer Function
0	0	x	x	Buffer bypassed
0	1	1	x	Write to 256 byte buffer
1	0	1	x	Write to 512 byte buffer
1	1	1	x	Write to 1k byte buffer
0	1	0	1	Read from 256 byte buffer
1	0	0	1	Read from 512 byte buffer
1	1	0	1	Read from 1k byte buffer

10.0 TEST PATTERN OUTPUT

The ADC08B200 has a test mode whereby the data outputs have a test pattern which may be used to "train" a receiving device, such as a PLD. The Test Mode is invoked by forcing a potential of $V_A/2$ at the OEDGE/TEN input. There is an on-chip pull-up resistor at this pin, so the device interprets a floating input at this pin to be a logic high. This pattern is used to test the integrity of the buffer, so the RCLK (Read Clock) input must be used to get the output pattern.

The test pattern that is put out is a continuously repeated pattern of output codes 00h - FFh - 00h - FFh - 00h. Note that this pattern repeats as long as the test mode is invoked and RCLK is running, so that every second time a logic low appears it will be present for two bit times.

11.0 APPLICATION EXAMPLE

Figure 4 shows an example of a typical application. The analog input and reference circuits are as described in *Figure 2* and *Figure 3*, except the input amplifier is shown without any gain and offset adjustments. The overall nominal gain of the input amplifier circuit is 1.98 and the nominal –3 dB input bandwidth is about 195 MHz. Note that this circuit does not show an anti-aliasing filter.

A 50 MHz clock oscillator is used for the input clock source. The MULT0 input grounded and the MULT1 input high means (from *Table 1*) that this 50 MHz input clock is multiplied by the internal PLL by 4 to provide a 200 Msps capture rate.

Since the BSIZE0 and BSIZE1 pins are both high, the internal capture buffer size is set to 1,024 bytes (see *Table 2*). Data writing to the internal buffer will automatically stop when the buffer is full because the ASW input is high. The FF (Full Flag) will go high when the buffer is full and data is ready to be read.

The OEDGE pin is high, meaning the output data will transition at the rise of the DRDY output. Since the PD pin is grounded and the OE pin is high, the device will never be completely powered down and the outputs are always enabled. Since the PDADC pin is driven from the controlling device, the ADC may be powered down, leaving the output buffer active, when the device buffer is being read, or when the device is not in use.

The digital lines between the ADC08B200 and the receiving device have 33 Ohms at the signal source end as source terminators, assuming output impedances of about 20 Ohms and 50-Ohm lines. The RESET and PDADC lines are not terminated because these are basically d.c. lines and it is assumed that they do not toggle frequently.

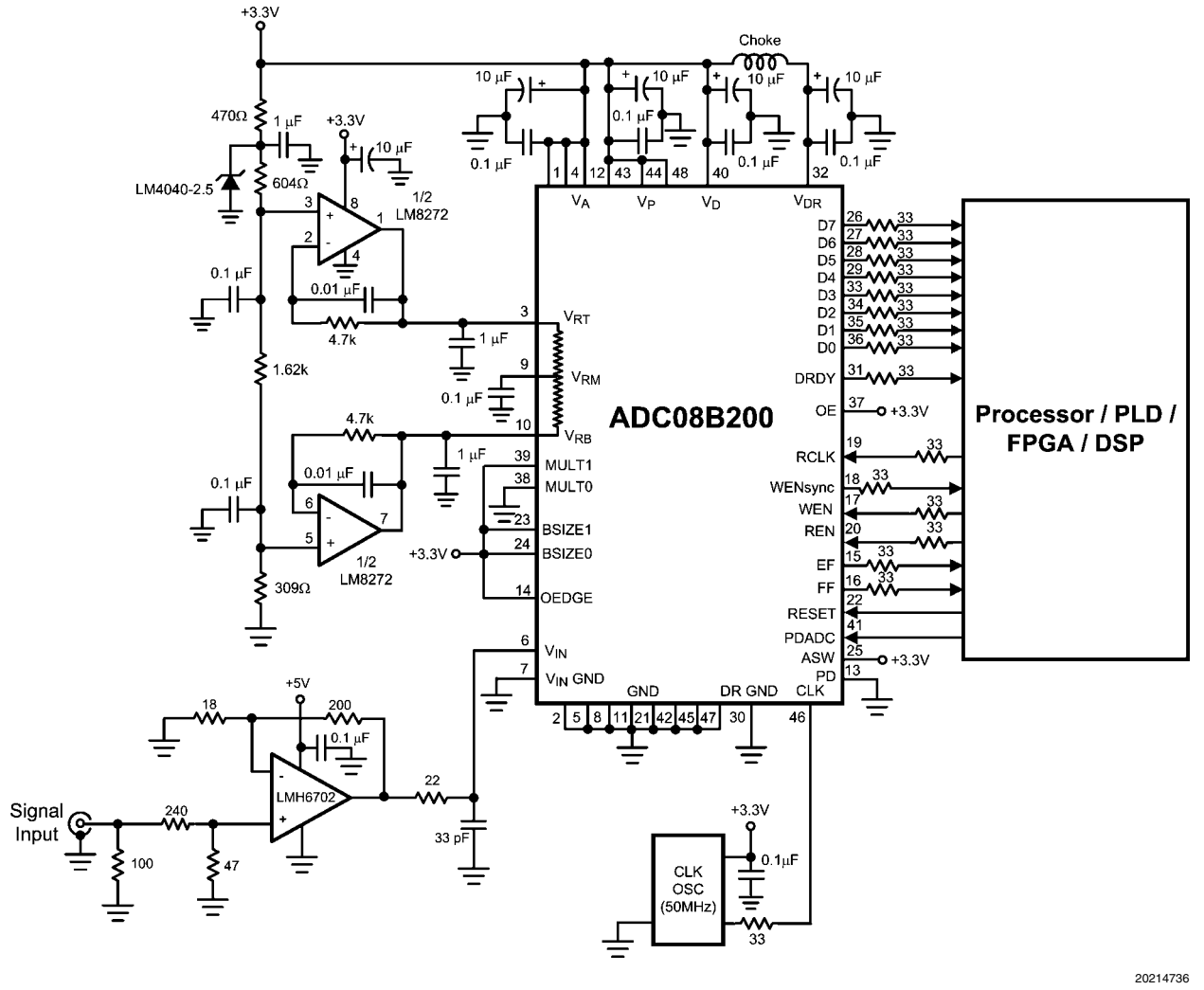


FIGURE 4. Example of a Typical Application.

The average power consumption of the ADC08B200 (assuming a new capture is taken as soon as the buffer contents is read) may be calculated by taking power consumed while capturing and writing to the buffer and multiplying it by the capture time divided by the throughput time (interval between the successive rises of the WEN signal), added to the power while reading the buffer with PDADC high (assuming the PDADC input is taken high whenever data is not being captured) multiplied by the time that PDADC is high (Buffer read time plus any idle time) divided by the throughput rate.

Assuming a Capture Power of 543 mW, a 200 Msps capture rate and a 66mW Read Power with PDADC high, a 50 MHz data read rate and no completely idle time, the average power consumption would be 161.4 mW.

12.0 POWER SUPPLY CONSIDERATIONS

It is important to note that capacitors have an equivalent series inductance associated with them such that, beyond a certain frequency, the capacitor behaves more like an inductance than a capacitance and adequate bypassing may be infective, resulting in the power distribution system having a high impedance, which could further result in excessive noise on the power supply. The frequency beyond which adequate bypassing may be effective depends primarily upon the chemistry of the capacitor dielectric, but can also vary a little from one manufacturer to another. Even so, this frequency is in the hundreds of Megahertz. Note, however, that a 200 MHz clock will have significant harmonic energy far beyond this. The result could be high frequency noise on the supply lines that could effect the SNR performance of the converter.

The use of adjacent power and ground planes will go a long way toward reducing the impedance of the power distribution system and is encouraged. Furthermore, we suggest placing the lowest value of bypass capacitor close to the supply pin on the same side of the board as the ADC and connect the ground end of the bypass capacitor to the ground plane with at least two through holes. The through holes have an inductance associated with them and using two or more such holes puts these inductances in parallel, lowering the effective inductance to ground.

12.1 Supply Voltages

The ADC8D200 will perform well with power supply voltages in the range specified in the Operating Ratings, just before the Electrical Table. Many individual devices may perform well down to supply voltages of 2.7V, but this should not be relied

upon because part of the product distribution, depending upon normal fabrication process tolerances, could result in the majority of some production runs not functioning well below 3.0V.

While all supplies may be of the same voltage, the digital supply (V_D), the PLL supply (V_P) and the output driver supply (V_{DR}) ADC08B200 should never be higher than 300 mV above the analog supply (V_A). Furthermore, the output driver supply, V_{DR} may be as low as 2.7V only when using the buffer and when the buffer read clock (RCLK) frequency is no higher than 50 MHz because the output slew rate decreases at low V_{DR} voltages and the output eye may not be open enough to allow reliable data capture.

13.0 LAYOUT AND GROUNDING

Proper grounding and proper routing of all signals are essential to ensure accurate conversion. A single, unified ground plane should be used. Do not split the ground plane.

Coupling between the typically noisy digital circuitry and the sensitive analog circuitry can lead to poor performance that may seem impossible to isolate and remedy. The solution is to keep all lines separated from each other by at least six times the height above the reference plane, and to keep the analog circuitry well separated from the digital circuitry.

The DR GND connection to the ground plane should not use the same through holes used by other ground connections. High power digital components should not be located near any analog components.

Generally, analog and digital lines should cross each other at 90° to avoid getting digital noise into the analog path. In high frequency systems, however, avoid crossing analog and digital lines altogether. Clock lines should be isolated from ALL other lines, analog AND digital. Even the generally accepted 90° crossing should be avoided as even a little coupling can cause problems at high frequencies. Best performance at high frequencies is obtained with a straight signal path.

The reference and analog inputs should be isolated from noisy signal traces to avoid coupling of spurious signals into the input. Any external component (e.g., a filter capacitor) connected between the converter's input and ground should be connected to a very clean point in the ground plane and preferably with 2 to 4 closely spaced through holes.

14.0 DYNAMIC PERFORMANCE

The ADC08B200 is a.c. tested and its dynamic performance is guaranteed. To meet the published specifications, the clock source driving the CLK input must exhibit as little jitter as possible. For best a.c. performance, each clock destination should be driven by a separate source, such as with a clock distribution chip or with a clock tree such as seen in *Figure 5*.

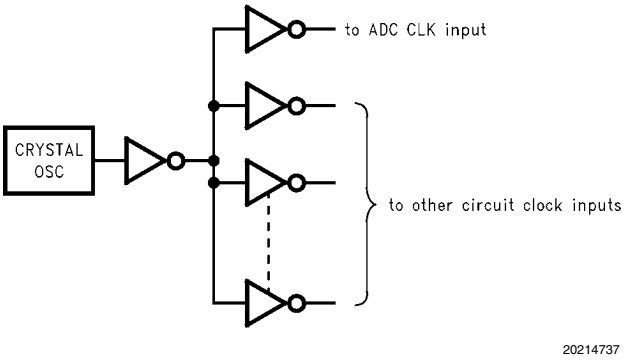


FIGURE 5. Isolating the ADC Clock from Digital Circuitry

It is good practice to keep the ADC clock line as short as possible and to keep it well away from other signals, which can introduce jitter into the clock signal. The clock signal can also introduce noise into a nearby signal path.

15.0 COMMON APPLICATION PITFALLS

Driving the inputs (analog or digital) beyond the power supply rails. For proper operation, all inputs should not go more than 300 mV below the ground pins or 300 mV above the supply pins. Exceeding these limits on even a transient basis may cause faulty or erratic operation. It is not uncommon for high speed digital circuits (e.g., 74F and 74AC devices) to exhibit undershoot that goes more than a volt below ground. A 47Ω resistor in series with the offending digital input, close to the driving source, will usually eliminate the problem.

Care should be taken not to overdrive the inputs of the ADC08B200. Such practice may lead to conversion inaccuracies and even to device damage.

Attempting to drive a high capacitance digital data bus. The more capacitance the output drivers must charge for each conversion, the more instantaneous digital current is required from V_{DR} and DR GND. These large charging current spikes can couple into the analog section, degrading dynamic performance. Buffering the digital data outputs may be necessary if the data bus capacitance exceeds 10 pF. Dynamic performance can also be improved by adding 12Ω to 27Ω series resistors at each digital output, reducing the energy coupled back into the converter input pins.

Using an inadequate amplifier to drive the analog input. As explained in *Section 2.0 THE ANALOG INPUT*, there are voltage spikes at the ADC analog input. These voltage spikes can cause instability in a feedback type amplifier used to drive the analog input. These spikes need not be filtered out, but should settle quickly. The amplifier should be fast enough to handle the frequencies presented to it, but not so fast that it would readily oscillate. A single-pole RC filter, as explained in *Section 2.0 THE ANALOG INPUT* will help ensure amplifier stability and accurate data capture.

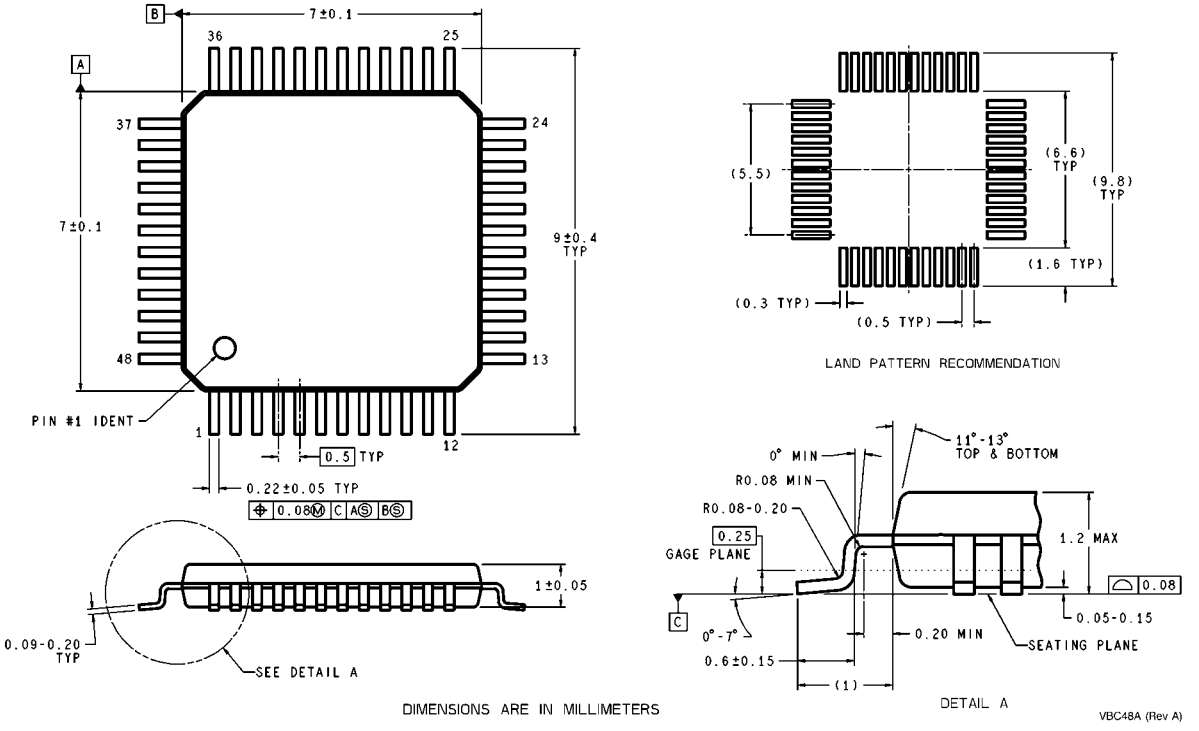
Driving the V_{RT} pin or the V_{RB} pin with devices that can not source or sink the current required by the ladder. As mentioned in *Section 1.0 REFERENCE INPUTS*, care should be taken to see that any driving devices can source sufficient current into the V_{RT} pin and sink sufficient current from the V_{RB} pin. If these pins are not driven with devices than can handle the required current, these reference pins will not be stable, resulting in a reduction of dynamic performance.

Using a clock source with excessive jitter, using an excessively long clock signal trace, or having other signals coupled to the clock signal trace. This will cause the sam-

pling interval to vary, causing excessive output noise and a reduction in SNR performance. The use of simple gates with RC timing is generally inadequate as a clock source.

Busing the data outputs. SNR performance of all ADCs, especially high speed ADCs, is sensitive to the amount of capacitance at the data outputs because the currents required of the ADC data outputs to charge and discharge these capacitances cause voltage spikes (noise) on the die. Minimizing the output capacitance will help maintain noise performance of the converter. Busing the outputs adds undesired capacitive loading to the ADC. Similarly, it is important to keep trace capacitance to a minimum by using short traces at the ADC outputs.

Physical Dimensions inches (millimeters) unless otherwise noted



NOTES: UNLESS OTHERWISE SPECIFIED

REFERENCE JEDEC REGISTRATION mo-153, VARIATION AD, DATED 7/93.

48-Lead Package BC
Order Number ADC08B200CIVS, ADC08B200QCIVS
NS Package Number VBC48A

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Switching Regulators	www.national.com/switchers	Distributors	www.national.com/contacts
LDOs	www.national.com/ldo	Quality and Reliability	www.national.com/quality
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