STV7710

Vaccum fluorescent display (VFD) driver

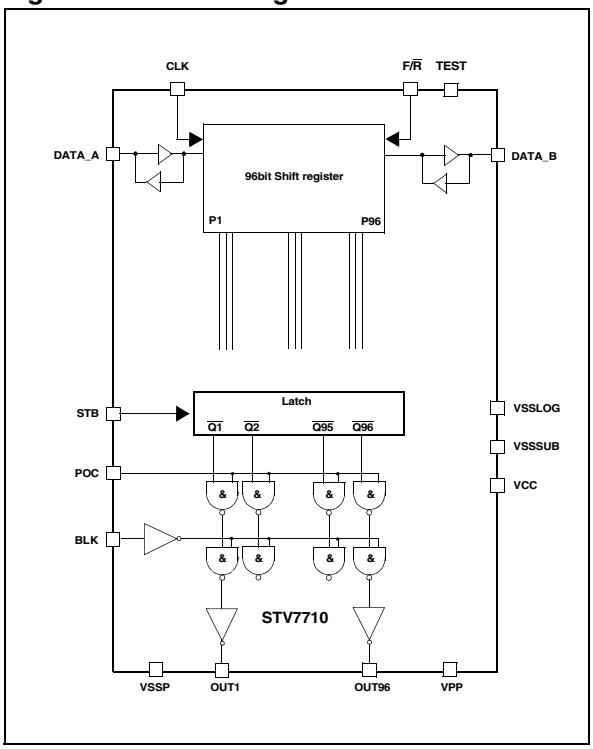
Features

- 96 outputs VFD driver
- 90 V absolute maximum supply
- 3.3V/5V compatible logic
- -40/30mA source/sink output MOS
- -50/50mA source/sink output diode
- 1-bit data bus (40 MHz)
- BCD process
- Packaging: die form

Description

STV7710 is a driver for vacuum fluorescent display (VFD) designed in the ST proprietary BCD high voltage technology. Using a 1 bit wide data bus, it can control 96 high current & high voltage outputs. The STV7710 is supplied with a separated 70V power output supply. All command inputs are CMOS and 3.3V logic levels compatible.

Figure 1. Block diagram



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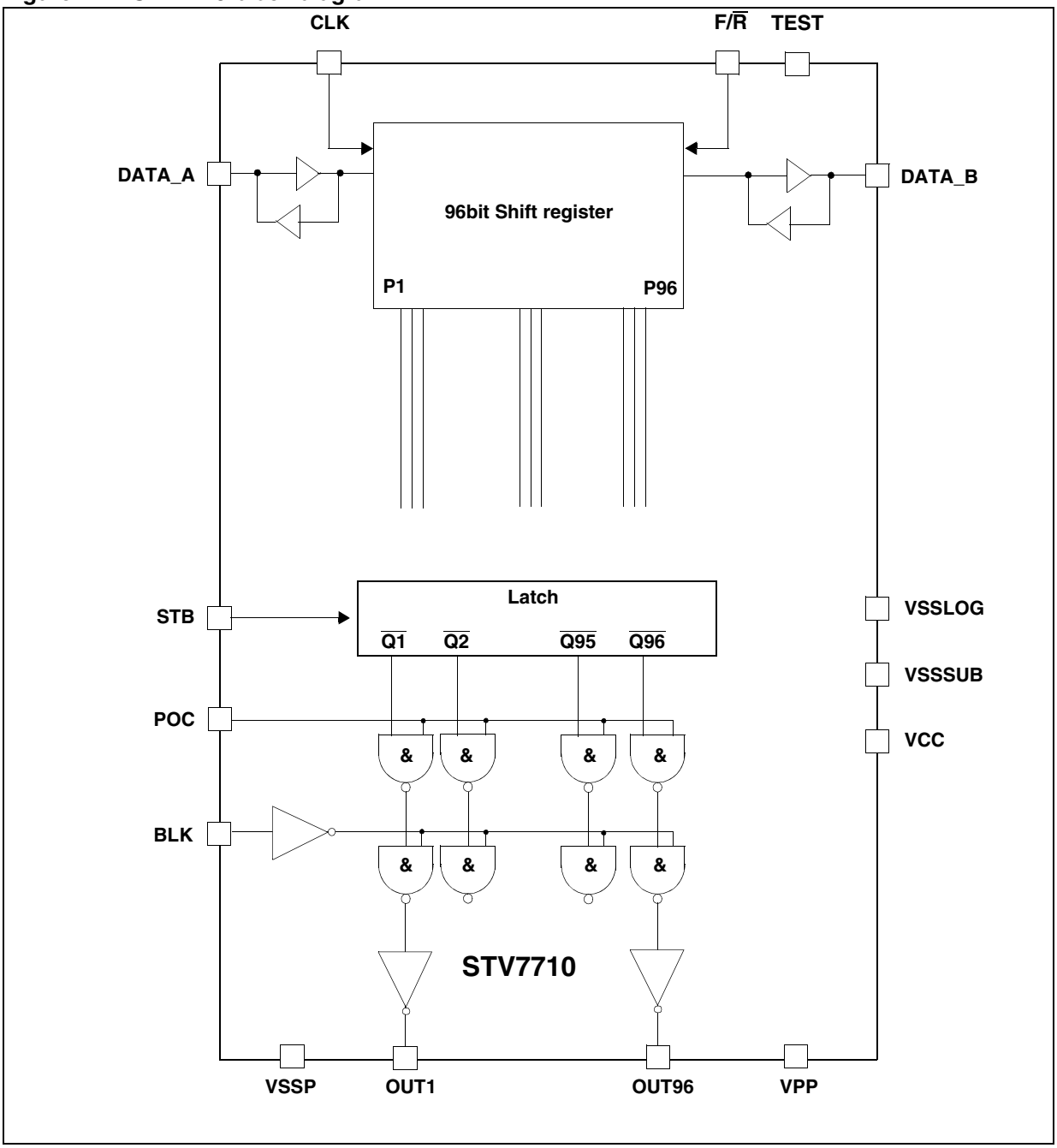
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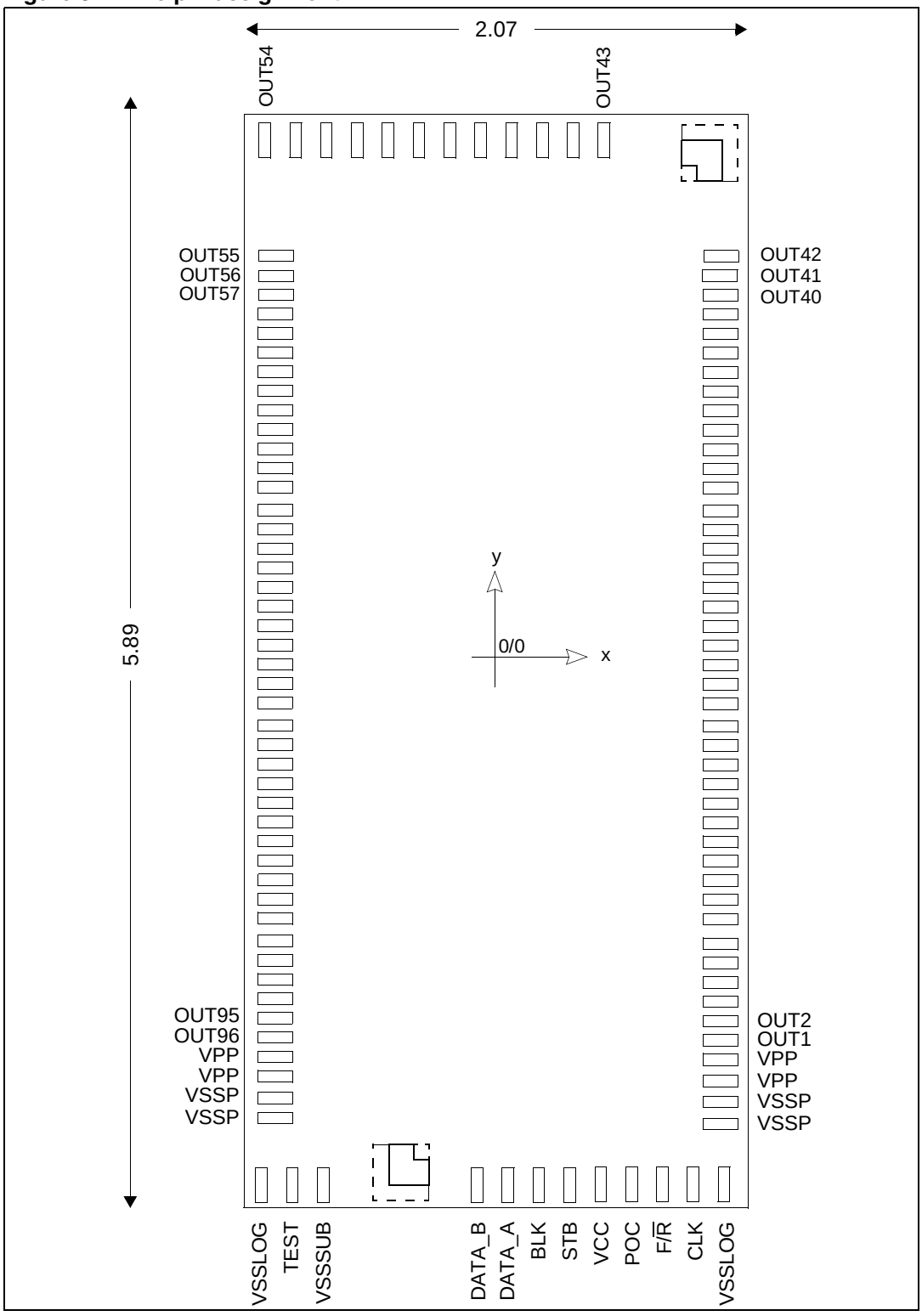
1 Block diagram

Figure 2. STV7710 block diagram



2 Die pin assignment

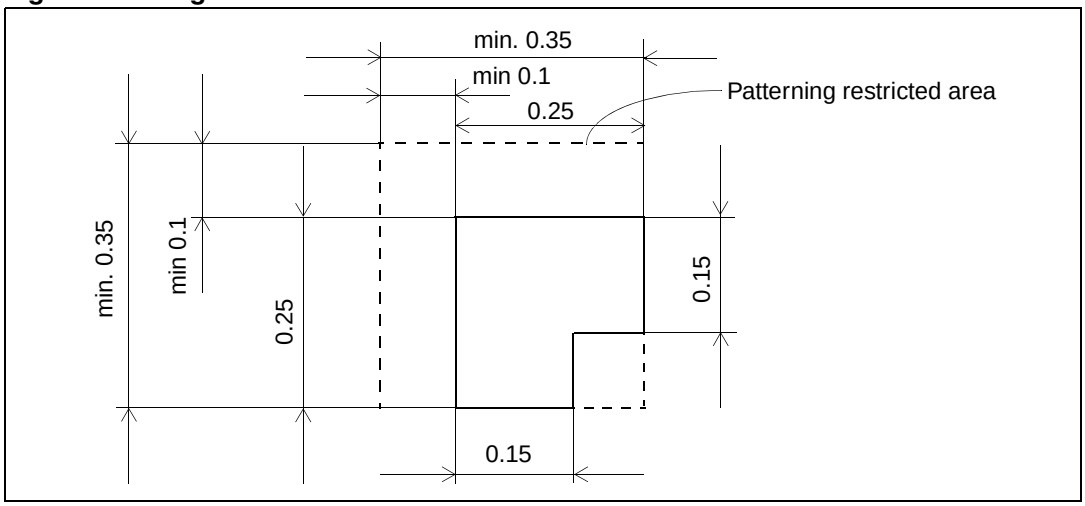
Figure 3. Die pin assignment



3 Mechanical specification

3.1 Alignment marks

Figure 4. Alignment marks



3.2 Pads specification

The reference is the centre of the die (x=0, y=0)

Table 1. Top side from left to right

Name	Centre: X	Centre: Y	Size: x	SIze: y
OUT54	-773.67	2796.11	76.00	92.00
OUT53	-670.48	2796.11	76.00	92.00
OUT52	-567.29	2796.11	76.00	92.00
OUT51	-464.1	2796.11	76.00	92.00
OUT50	-360.91	2796.11	76.00	92.00
OUT49	-257.72	2796.11	76.00	92.00
OUT48	-154.53	2796.11	76.00	92.00
OUT47	-51.34	2796.11	76.00	92.00
OUT46	51.85	2796.11	76.00	92.00
OUT45	155.04	2796.11	76.00	92.00
OUT44	258.23	2796.11	76.00	92.00
OUT43	361.42	2796.11	76.00	92.00

Table 2. Bottom side from right to left

Name	Centre: X	Centre: Y	Size: x	SIze: y
VSSLOG	771.63	-2802.23	76.00	92.00
CLK	669.54	-2802.23	76.00	92.00
F/$\overline{R}$	566.35	-2802.23	76.00	92.00
POC	463.16	-2802.23	76.00	92.00
VCC	359.97	-2802.23	76.00	92.00
STB	257.63	-2802.23	76.00	92.00
BLK	154.44	-2802.23	76.00	92.00
DATA_A	51.25	-2802.23	76.00	92.00
DATA_B	-119.85	-2802.23	76.00	92.00
VSSSUB	-567.88	-2802.23	76.00	92.00
TEST	-669.54	-2802.23	76.00	92.00
VSSLOG	-771.63	-2802.23	76.00	92.00

Table 3. Right side from top to bottom

Name	Centre: X	Centre: Y	Size: x	SIze: y
OUT42	887.61	2050.11	92.00	76.00
OUT41	887.61	1946.92	92.00	76.00
OUT40	887.61	1843.73	92.00	76.00
OUT39	887.61	1740.54	92.00	76.00
OUT38	887.61	1638.88	92.00	76.00
OUT37	887.61	1535.69	92.00	76.00
OUT36	887.61	1432.50	92.00	76.00
OUT35	887.61	1329.31	92.00	76.00
OUT34	887.61	1226.12	92.00	76.00
OUT33	887.61	1122.93	92.00	76.00
OUT32	887.61	1019.74	92.00	76.00
OUT31	887.61	916.55	92.00	76.00
OUT30	887.61	813.36	92.00	76.00
OUT29	887.61	710.17	92.00	76.00
OUT28	887.61	606.98	92.00	76.00
OUT27	887.61	503.79	92.00	76.00
OUT26	887.61	400.60	92.00	76.00
OUT25	887.61	297.41	92.00	76.00
OUT24	887.61	194.22	92.00	76.00
OUT23	887.61	91.03	92.00	76.00

Table 3. Right side from top to bottom (continued)

Name	Centre: X	Centre: Y	Size: x	SIze: y
OUT22	887.61	-12.15	92.00	76.00
OUT21	887.61	-115.34	92.00	76.00
OUT20	887.61	-218.53	92.00	76.00
OUT19	887.61	-321.72	92.00	76.00
OUT18	887.61	-424.91	92.00	76.00
OUT17	887.61	-528.10	92.00	76.00
OUT16	887.61	-631.29	92.00	76.00
OUT15	887.61	-734.48	92.00	76.00
OUT14	887.61	-837.67	92.00	76.00
OUT13	887.61	-940.86	92.00	76.00
OUT12	887.61	-1044.05	92.00	76.00
OUT11	887.61	-1147.24	92.00	76.00
OUT10	887.61	-1250.43	92.00	76.00
OUT9	887.61	-1353.62	92.00	76.00
OUT8	887.61	-1456.81	92.00	76.00
OUT7	887.61	-1560.00	92.00	76.00
OUT6	887.61	-1663.19	92.00	76.00
OUT5	887.61	-1766.38	92.00	76.00
OUT4	887.61	-1869.57	92.00	76.00
OUT3	887.61	-1972.76	92.00	76.00
OUT2	887.61	-2075.95	92.00	76.00
OUT1	887.61	-2179.14	92.00	76.00
VPP	887.61	-2282.16	92.00	76.00
VPP	887.61	-2385.35	92.00	76.00
VSSP	887.61	-2488.46	92.00	76.00
VSSP	887.61	-2591.65	92.00	76.00

Table 4. Left side from bottom to top

Name	Centre: X	Centre: Y	Size: x	SIze: y
VSSP	-887.61	-2591.65	92.00	76.00
VSSP	-887.61	-2488.46	92.00	76.00
VPP	-887.61	-2385.35	92.00	76.00
VPP	-887.61	-2282.16	92.00	76.00
OUT96	-887.61	-2179.14	92.00	76.00
OUT95	-887.61	-2075.95	92.00	76.00
OUT94	-887.61	-1972.76	92.00	76.00
OUT93	-887.61	-1869.57	92.00	76.00
OUT92	-887.61	-1766.38	92.00	76.00
OUT91	-887.61	-1663.19	92.00	76.00
OUT90	-887.61	-1560.00	92.00	76.00
OUT89	-887.61	-1456.81	92.00	76.00
OUT88	-887.61	-1353.62	92.00	76.00
OUT87	-887.61	-1250.43	92.00	76.00
OUT86	-887.61	-1147.24	92.00	76.00
OUT85	-887.61	-1044.05	92.00	76.00
OUT84	-887.61	-940.86	92.00	76.00
OUT83	-887.61	-837.67	92.00	76.00
OUT82	-887.61	-734.48	92.00	76.00
OUT81	-887.61	-631.29	92.00	76.00
OUT80	-887.61	-528.10	92.00	76.00
OUT79	-887.61	-424.91	92.00	76.00
OUT78	-887.61	-321.72	92.00	76.00
OUT77	-887.61	-218.53	92.00	76.00
OUT76	-887.61	-115.34	92.00	76.00
OUT75	-887.61	-12.15	92.00	76.00
OUT74	-887.61	91.03	92.00	76.00
OUT73	-887.61	194.22	92.00	76.00
OUT72	-887.61	297.41	92.00	76.00
OUT71	-887.61	400.60	92.00	76.00
OUT70	-887.61	503.79	92.00	76.00
OUT69	-887.61	606.98	92.00	76.00
OUT68	-887.61	710.17	92.00	76.00
OUT67	-887.61	813.36	92.00	76.00
OUT66	-887.61	916.55	92.00	76.00

Table 4. Left side from bottom to top (continued)

Name	Centre: X	Centre: Y	Size: x	SIze: y
OUT65	-887.61	1019.74	92.00	76.00
OUT64	-887.61	1122.93	92.00	76.00
OUT63	-887.61	1226.12	92.00	76.00
OUT62	-887.61	1329.31	92.00	76.00
OUT61	-887.61	1432.50	92.00	76.00
OUT60	-887.61	1535.69	92.00	76.00
OUT59	-887.61	1638.88	92.00	76.00
OUT58	-887.61	1740.54	92.00	76.00
OUT57	-887.61	1843.73	92.00	76.00
OUT56	-887.61	1946.92	92.00	76.00
OUT55	-887.61	2050.11	92.00	76.00

4 Circuit description

4.1 Pin description

Table 5. STV7710 pin description

Symbol	Function	Description
OUT(01-96)	Output	Power output
VSSP	Ground	Ground of power outputs
VPP	Supply	High voltage supply of power outputs
BLK	Input	Blanking input
POC	Input	Power output control input
F/$\overline{R}$	Input	Selection of shift direction
VCC	Supply	5V logic supply
VSSLOG	Ground	Logic ground
VSSSUB	Ground	Substrate ground
CLK	Input	Clock of data shift register
STB	Input	Latch of data to outputs
DATA_A	Input/output	Shift register input
DATA_B	Input/output	Shift register output
TEST	Input	Test input pin

4.2 Data bus configuration

Table 6. STV7710 data bus configuration

F/$\overline{R}$	Input	Data shift														Output	
		CLK	01	02	03	04	05	06	...	91	92	93	94	95	96		
H	DATA_A	Output	01	02	03	04	05	06		91	92	93	94	95	96	DATA_B	Forward shift
L	DATA_B	Output	96	95	94	93	92	91		06	05	04	03	02	01	DATA_A	Reverse shift

This table describes the position of the first data sampled by the first rising edge of the CLK signal.

4.3 Description

STV7710 includes all the logic and power circuits necessary to drive electrodes of a vacuum fluorescent display (VFD). Binary values of each pixel of the displayed line are loaded into the shift register DATA_A/B data bus. Data is shifted at each low to high transition of the *CLK* clock. After 96 shifts, the data is available at the output of the shift register. This output can be used to cascade several Ics to drive higher resolution displays.

The forward /reverse (F/$\overline{R}$) input is used to select the direction of the shift register. Data input/output status is set according to the selected direction (refer to *Table 6*).

The maximum frequency of the shift clock is 40MHz.

When the STB signal is high, data are transferred from the shift register to the latch and power output stages.

All the output data are kept memorized and held in the latch stage when the latch input STB is set at low level.

Vsssub and Vsslog must be connected as close as possible to the logical reference ground of the application. Also, make sure that TEST input pin is connected to ground (*Figure 8*).

STV7710 is supplied with a 5 V power supply. All the logic inputs can be driven either by 5 V CMOS logic, or by 3.3 V CMOS logic.

Table 7. Shift register truth table

Input		Data-in / data-out		Shift register function
F/$\overline{R}$	CLK	DATA_A	DATA_B	
H	↑	Data-in	Data-out	Forward shift
H	H or L	-	-	Steady
L	↑	Data-out	Data-in	Reverse shift
L	H or L	-	-	Steady

Table 8. Power output truth table

TEST	Qn	STB	BLK	POC	Driver output	Comments
L	X	X	H	X	all “Low”	Output at low level
L	X	X	L	L	all “High”	Output at high level
L	X	L	L	H	Qn	Data latched
L	L	H	L	H	L	Data transfered
L	H	H	L	H	H	Data transfered

5 Absolute maximum ratings

Table 9. Absolute maximum ratings

Symbol	Parameter	Value	Unit
V_{CC}	Logic supply range	-0.3, +7	V
V_{PP}	Driver supply range	-0.3, +90	V
V_{IN}	Logic input voltage range	-0.3, Vcc+0.3	V
I_{POUT}	Driver output current(1) (2)	-40 / +30	mA
Tjmax	Maximum junction temperature	125	°C
T_{STG}	Storage temperature range	-30, +150	°C
V_{OUT}	Output power voltage range	-0.3, +90	V

1. Through one power output.
2. Through one power output for all power outputs (see *Figure 6: Test configuration*) with Junction temperature lower than or equal to Tjmax

- ESD susceptibility
  - Human Body Model: 100 pF; 1.5 kΩ
  - All pins withstand ±2 kV except Data_A and Data_B: 1.2 kV

6 Electrical characteristics

(V_{CC} = 5 V, Vpp = 70 V, V_{SSP} = 0 V, Vss = 0 V, Tamb = 25 °C, f_{CLK} = 40 MHz, unless otherwise specified)

Table 10. Electrical characteristics

Symbol	Parameter	Min	Typ	Max	Unit
Supply					
V_{CC}	Logic supply voltage	4.50	5	5.5	V
I_{CC}	Logic supply current(1)	-	45	100	µA
I_{CCL}	Logic dynamic supply current (f_{CLK}=20 MHz)(2)	-	20	-	mA
I_{CC}	Logic supply current (V_{IH}=2.0V)		-	750	µA
V_{PP}	Power output supply voltage	15		70	V
I_{PPH}	Power output supply current (steady outputs)	-	-	10	µA
Output					
OUT1-OUT96 (*Figure 9*)					
V_{POUTH}	Power output high level (voltage drop versus V_{PP}) @I_{POUTH} = - 20 mA and V_{PP} = 70 V	-	7.5	14	V
V_{POUTL}	Power output low level @ I_{POUTL} = + 20 mA	-	5	11	V
V_{DOUTH}	Output diode voltage drop @ I_{DOUTH} = + 30 mA (3)	-	1	2	V
V_{DOUTL}	Output diode voltage drop @ I_{DOUTL} = - 30 mA(3)	-2	-1	-	V
DATA A, DATA B (*Figure 10*)					
V_{OH}	Logic output high level @I_{OH}=-1mA	4	4.8	-	V
V_{OL}	Logic output low level @I_{OL} = 1 mA	-	0.1	0.4	V
Input					
CLK, F/$\overline{R}$, STB, POC, BLK, DATA_A, DATA B (*Figure 8*)					
V_{IH}	Input high level	2.0	-	-	V
V_{IL}	Input low level	-	-	0.9	V
I_{IH}	High level input current (V_{IH} >=2.0V)	-	-	5	µA
I_{IL}	Low level input current (V_{IL} = 0v)	-	-	5	µA
C_{IN}	Input capacitance(4)			15	pF

1. Logic input levels compatible with 5V CMOS logic.
2. All data inputs are commuted at 10MHz
3. See *Figure 6: Test configuration*
4. This parameter is measured during ST's internal qualification which includes temperature characterization on standard and corner batches of the process. This parameter is not tested on the part.

7 AC timing requirements

V_{CC} = 4.5 V to 5.5 V, Tamb = -20 °C to +85 °C, input signals max leading edge & trailing edge (tr, tf) = 5 ns.

Table 11. AC timing requirements

Symbol	Parameter	Min	Typ	Max	Unit
t_{CLK}	Data clock period	25	-	-	ns
t_{WHCLK}	Duration of CLK pulse at high level	10	-	-	ns
t_{WLCLK}	Duration of CLK pulse at low level	10	-	-	ns
t_{SDAT}	Set-up time of data input before low to high clock transition	5	-	-	ns
t_{HDAT}	Hold-time of data input after low to high clock transition	5	-	-	ns
t_{HSTB}	Hold-time of STB after low to high clock transition	5	-	-	ns
t_{STB}	STB low level pulse duration	10	-	-	ns
t_{SSTB}	STB set-up time before CLK rise	5	-	-	ns

8 AC timing characteristics

V_{CC} = 5 V, V_{PP} = 70 V, V_{SSP} = 0 V, V_{SSSUB} = 0 V, Vsslog = 0 V, Tamb = 25°C, f_{CLK} = 40 MHz (V_{ILMAX} = 0.2 Vcc, V_{IHMIN} = 0.8 V_{CC})

Table 12. AC timing characteristics

Symbol	Parameter	Min	Typ	Max	Unit
t_{PHL1} t_{PLH1}	Delay of power output change after CLK transition - high to low - low to high	 - -	 35 30	 100 100	 ns ns
t_{PHL2} t_{PLH2}	Delay of power output change after STB transition - high to low - low to high	 -	 - -	 95 95	 ns ns
t_{PHL3} t_{PLH3}	Delay of power output change after BLK, POC transition - high to low - low to high	 -	 25 20	 90 90	 ns ns
$t_{R\ OUT}$	Power output rise time(1)	50	-	200	ns
$t_{F\ OUT}$	Power output fall time(1)	50	-	200	ns
t_S	Width of the falling edge smooth shape (not tested)(2)	-	30	-	ns
$t_{R\ DAT}$	Logic data output rise time (CL = 10pF)	-	9	20	ns
$t_{F\ DAT}$	Logic data output fall time (CL = 10pF)	-	5	12	ns
t_{PHL4} t_{PLH4}	Delay of logic data output change after CLK transition - high to low - low to high	 - -	 12 13	 25 25	 ns ns

1. One output among 96, loading capacitor CL = 50pF, other outputs at low level
2. See *Figure 7: Zoom for OUTn showing tS and tF OUT*

Figure 5. AC characteristics waveform

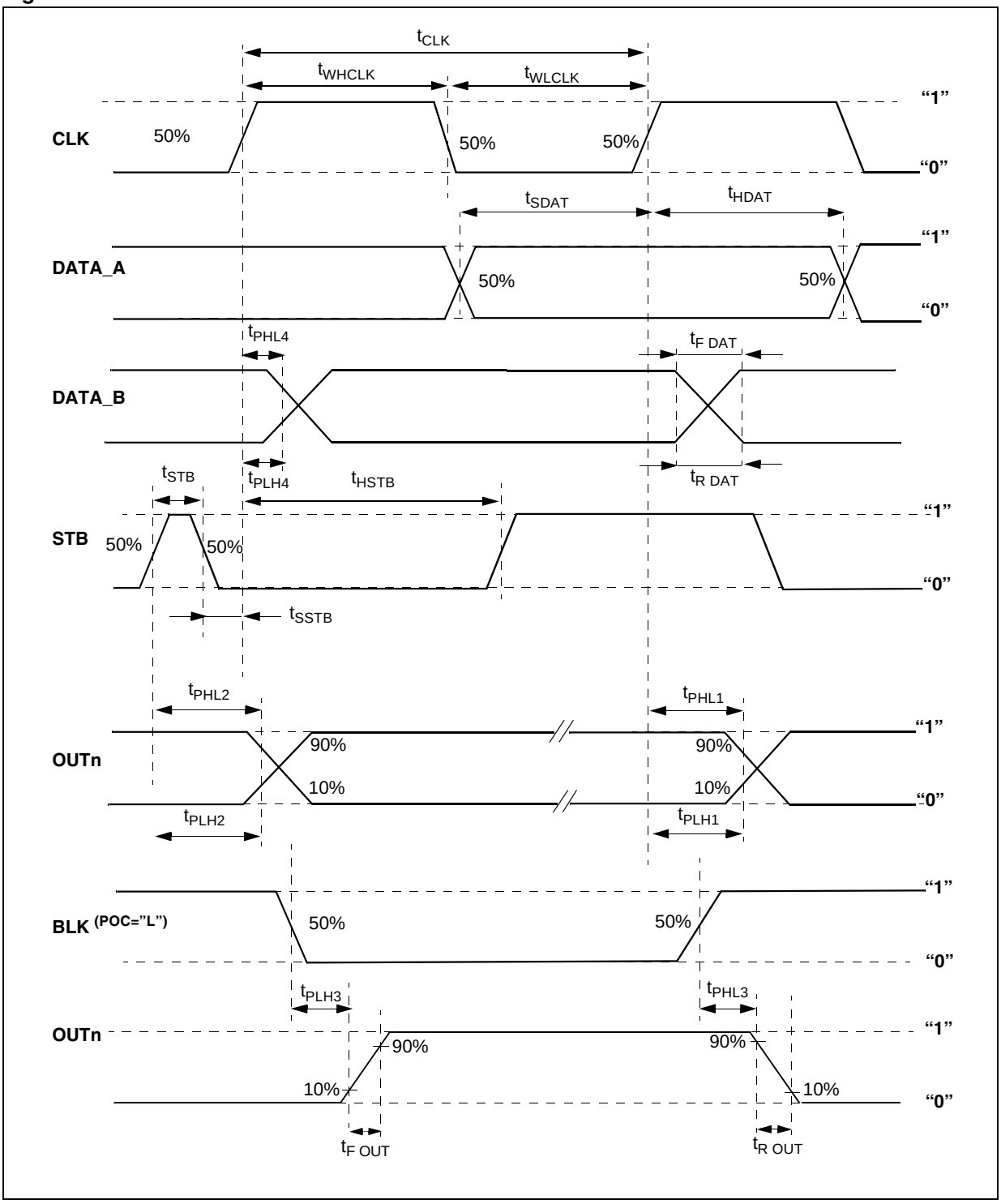
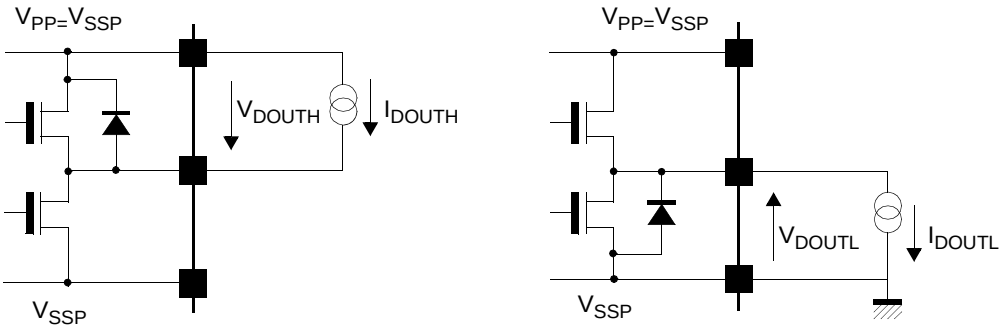
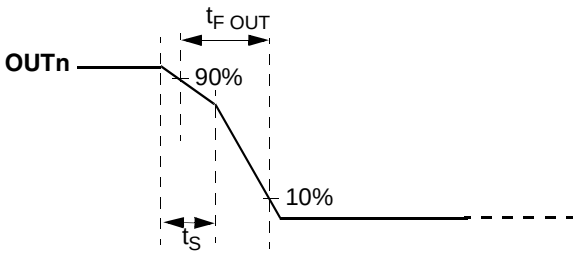


Figure 6. Test configuration



Output sinking current as positive value, sourcing current as negative value

Figure 7. Zoom for OUTn showing t_S and $t_{F\ OUT}$



9 Input/ouput schematics

Figure 8. CLK, STB, F/$\overline{R}$, POC, BLK inputs

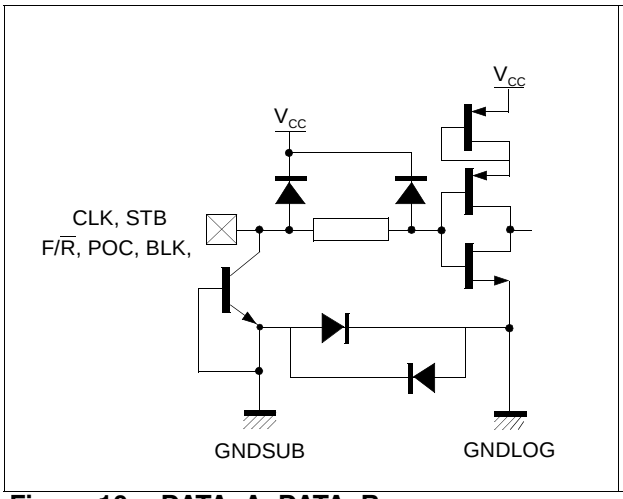


Figure 9. Test pin

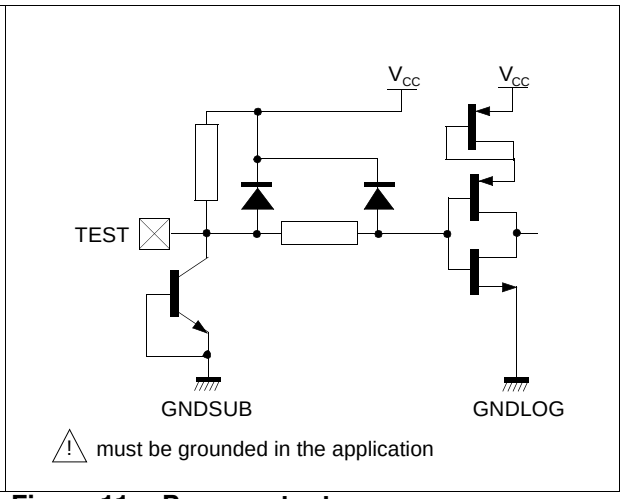


Figure 10. DATA_A, DATA_B

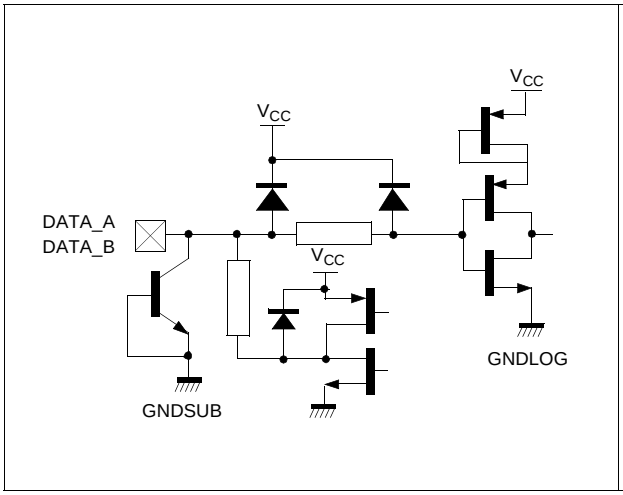
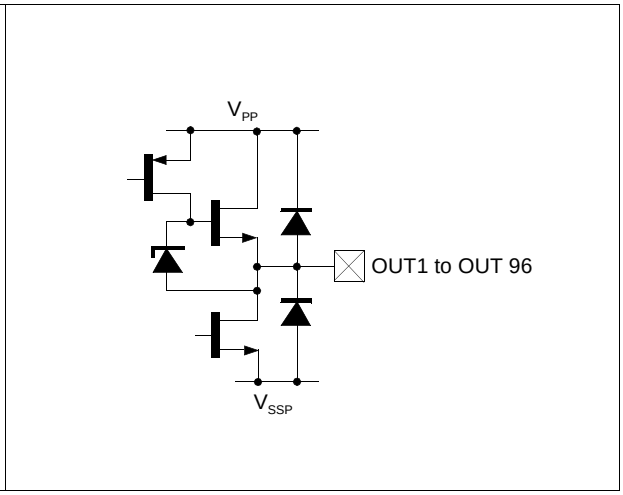


Figure 11. Power output

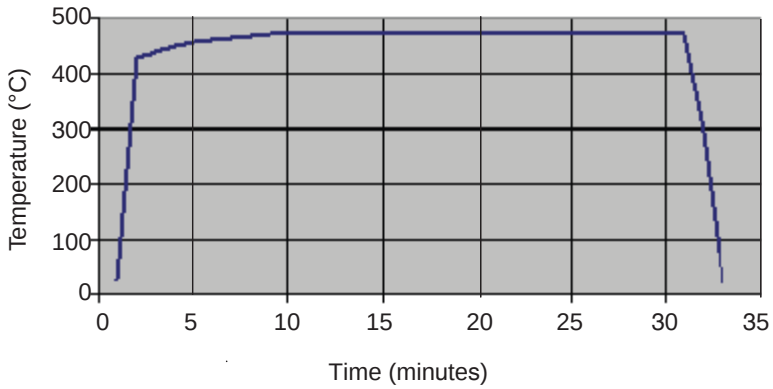


10 Thermal characteristics

STV7710 can be exposed to high temperatures during the manufacturing of the VFD module (display sealing).

STV7710 is qualified for a maximum storage temperature of 475°C during 30 minutes following the thermal profile described in *Figure 12*.

Figure 12. Thermal profile applied for internal qualification



11 Ordering information

Table 13. Order codes

Part number	Description
STV7710	Bare die
STV7710/BMP	Tested and usawn bump wafer (u=die)
STV7710/WAF	Unsawn wafer
STV7710/WP	Dice on cavity plate (unit=die)

12 Revision history

Table 14. Document revision history

Date	Revision	Changes
24-Mar-2004	1	Initial release.
30-Apr-2004	2	Renamed the document for STV7710/WAF order code.
11-Jul-2007	3	Added *Chapter 11: Ordering information* and *Chapter 12: Revision history*. Updated the document to cover all STV7710 order codes.

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