

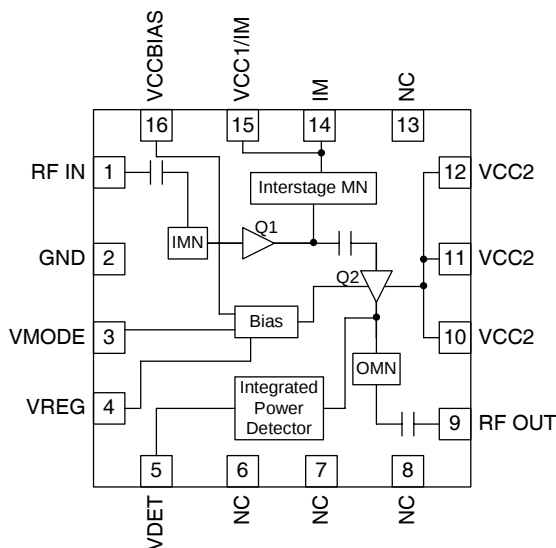


Features

- Input/Output Internally Matched@50Ω
- 27.5dBm Linear Output Power
- 42% Peak Linear Efficiency
- -41dBc ACLR @ ±5MHz
- Integrated Power Detector
- HSDPA Capable

Applications

- 3V W-CDMA Band 1 Handsets
- Multi-Mode W-CDMA 3G Handsets
- 3V TD-SCDMA Handsets
- Spread-Spectrum Systems



Functional Block Diagram

Product Description

The RF5198 is a high-power, high-efficiency linear amplifier module specifically designed for 3V handheld systems. The device is manufactured on an advanced third generation GaAs HBT process, and was designed for use as the final RF amplifier in 3V W-CDMA handheld digital cellular equipment, spread-spectrum systems, and other applications in the 1920MHz to 1980MHz band (Band 1). The RF5198 has a digital control pin for low power applications to lower quiescent current. This PA also includes a power detector circuit. The RF5198 is assembled in at 16-pin, 3mmx3mm, QFN package.

Ordering Information

RF5198	3V 1950MHz W-CDMA Linear Power Amplifier Module
RF5198PCBA-41X	Fully Assembled Evaluation Board

Optimum Technology Matching® Applied

- | | | | |
|--|--------------------------------------|-------------------------------------|-----------------------------------|
| ☒ GaAs HBT | ☐ SiGe BiCMOS | ☐ GaAs pHEMT | ☐ GaN HEMT |
| ☐ GaAs MESFET | ☐ Si BiCMOS | ☐ Si CMOS | |
| ☐ InGaP HBT | ☐ SiGe HBT | ☐ Si BJT | |

Absolute Maximum Ratings

Parameter	Rating	Unit
Supply Voltage (RF off)	+8.0	V
Supply Voltage ($P_{OUT} \leq 31$ dBm)	+5.2	V
Control Voltage (V_{REG})	+3.9	V
Input RF Power	+10	dBm
Mode Voltage (V_{MODE})	+3.9	V
Operating Temperature	-30 to +110	°C
Storage Temperature	-40 to +150	°C
Moisture Sensitivity Level (IPC/JEDEC J-STD-20)	MSL2@260	°C



Caution! ESD sensitive device.

Exceeding any one or a combination of the Absolute Maximum Rating conditions may cause permanent damage to the device. Extended application of Absolute Maximum Rating conditions to the device may reduce device reliability. Specified typical performance or functional operation of the device under Absolute Maximum Rating conditions is not implied.

RoHS status based on EUDirective2002/95/EC (at time of this document revision).

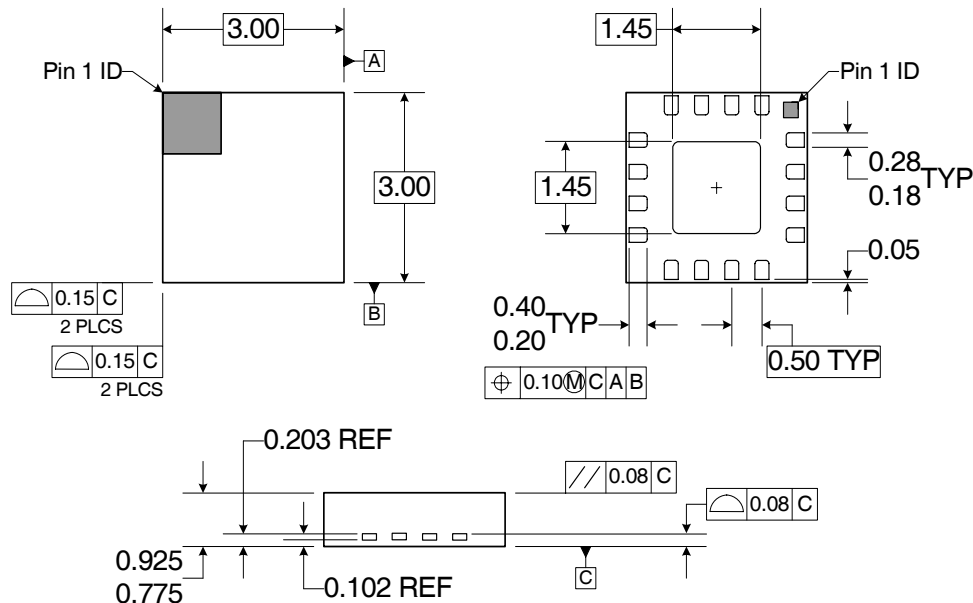
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Parameter	Specification			Unit	Condition
	Min.	Typ.	Max.		
High Power Mode (V_{MODE} Low)					$T = 25^\circ\text{C}$ Ambient, $V_{CC} = 3.4\text{V}$, $V_{CCBIAS} = 3.4\text{V}$, $V_{REG} = 2.8\text{V}$, $V_{MODE} = 0\text{V}$, and $P_{OUT} = 27.5\text{dBm}$ for all parameters (unless otherwise specified). Modulation is 3GPP 3.2 03-00 DPCCH + 1DPDCH.
Operating Frequency Range	1920		1980	MHz	
Linear Gain	26.0	28.5	32.0	dB	
Harmonics			-10	dBm	$f = 2f_0, 3f_0$
Maximum Linear Output	27.5			dBm	
Linear Efficiency	38	42	47	%	
Maximum I_{CC}	352	394	435	mA	
ACLR1 @ $\pm 5\text{MHz}$		-41	-37	dBc	
ACLR2 @ $\pm 10\text{MHz}$		-52	-48	dBc	
Input VSWR		2:1			
Output VSWR Stability			6:1		No oscillation > -70 dBc
Ruggedness			10:1		No damage
Noise Power		-154		dBm/Hz	$-50 \leq P_{OUT} \leq +27.5\text{dBm}$, RX = 925 MHz to 960 MHz (EGSM)
		-133		dBm/Hz	$-50 \leq P_{OUT} \leq +27.5\text{dBm}$, RX = 1805 MHz to 1880 MHz (DCS)
		-140		dBm/Hz	$-50 \leq P_{OUT} \leq +27.5\text{dBm}$, RX = 2110 MHz to 2170 MHz (W-CDMA), TX/RX Offset = 130 MHz
		-143		dBm/Hz	$-50 \leq P_{OUT} \leq +27.5\text{dBm}$, RX = 2110 MHz to 2170 MHz (W-CDMA), TX/RX Offset = 190 MHz
		-148		dBm/Hz	$-50 \leq P_{OUT} \leq +27.5\text{dBm}$, RX = 2400 MHz to 2480 MHz (Bluetooth)
		-107		dBm/Hz	$-50 \leq P_{OUT} \leq +27.5\text{dBm}$, TX = 1932.3 MHz to 1980 MHz, RX = 1893.5 MHz to 1919.6 MHz (PHS)
Reverse IM Products					
IM 5 MHz			-31	dBc	IF offset $f_0 + 5\text{MHz}$ with CW signal = -40 dBc
IM 10 MHz			-41	dBc	IF offset $f_0 + 10\text{MHz}$ with CW signal = -40 dBc

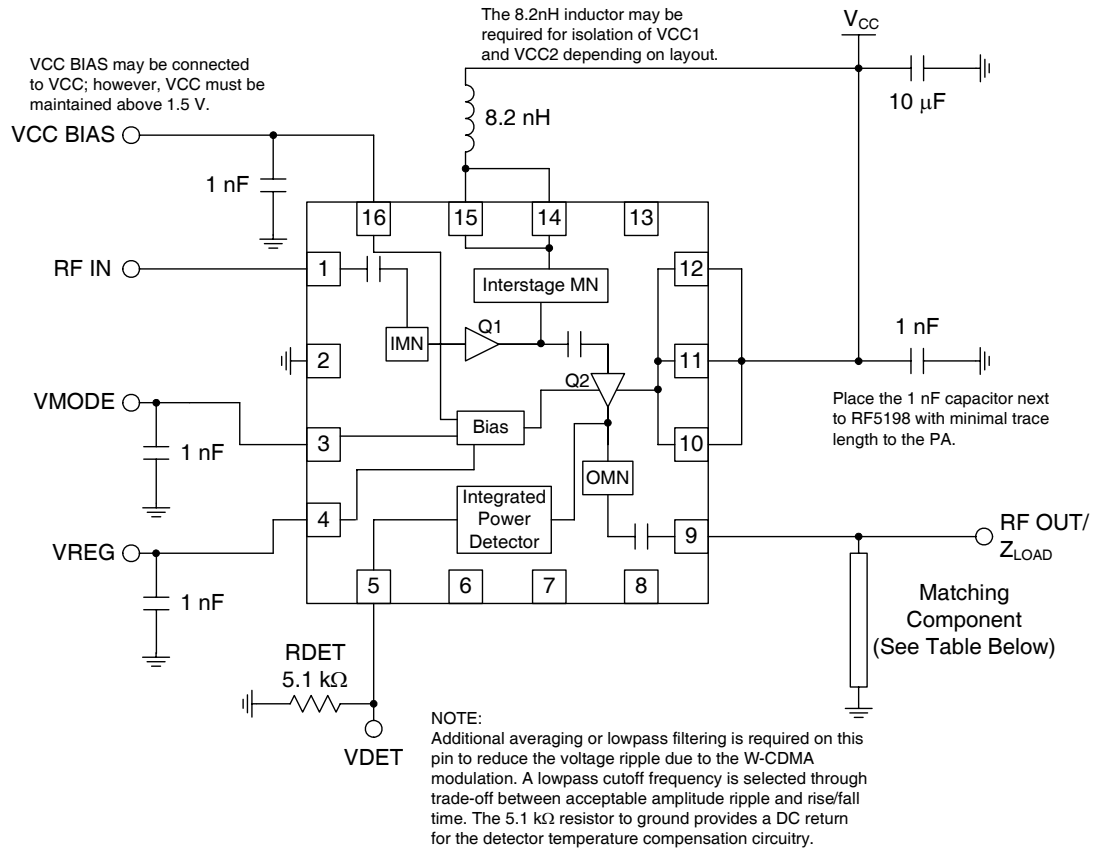
Parameter	Specification			Unit	Condition
	Min.	Typ.	Max.		
Low Power Mode (V_{MODE} High)					$T=25^{\circ}\text{C}$ Ambient, $V_{CC}=1.5\text{V}$, $V_{CCBIAS}=3.4\text{V}$, $V_{REG}=2.8\text{V}$, $V_{MODE}=2.8\text{V}$, and $P_{OUT}=16\text{dBm}$ for all parameters (unless otherwise specified). Modulation is 3GPP 3.2 03-00 DPCCH + 1DPDCH.
Operating Frequency Range	1920		1980	MHz	
Linear Gain	23	26	31	dB	$P_{OUT}=+16\text{dBm}$
Maximum Linear Output	16			dBm	
Linear Efficiency	18.3	21.0	25.3	%	$P_{OUT}=+16\text{dBm}$
ACLR @ $\pm 5\text{MHz}$		-41	-37	dBc	
ACLR @ $\pm 10\text{MHz}$		-54	-48	dBc	
Maximum I_{CC}	105	125	145	mA	$P_{OUT}=+16\text{dBm}$
Input VSWR		2:1			
Output VSWR Stability Ruggedness			6:1		No oscillation > -65dBc
			10:1		No damage
Reverse IM Products					
IM 5MHz			-31	dBc	IF offset $f_0 + 5\text{MHz}$ with CW signal = -40dBc
IM 10MHz			-41	dBc	IF offset $f_0 + 10\text{MHz}$ with CW signal = -40dBc
Power Supply					
Supply Voltage (V_{CC1} and V_{CC2})	3.2	3.4	4.3	V	
	0.6			V	Low power with DC to DC Converter
V_{CC} Bias	1.5		4.3	V	
High Power Idle Current ($I_{CC1}/I_{CC2}/I_{CCBIAS}$)	50	70	105	mA	$V_{MODE}=\text{low}$ and $V_{REG}=2.8\text{V}$
Low Power Idle Current ($I_{CC1}/I_{CC2}/I_{CCBIAS}$)	45	60	95	mA	$V_{MODE}=\text{high}$ and $V_{REG}=2.8\text{V}$
V_{REG} Current		2.4	5.0	mA	
V_{MODE} Current		150	300	μA	
RF Turn On/Off Time		1.2		μs	
DC Turn On/Off Time		2		μs	
Total Current (Power Down)		0.2	0.5	μA	
V_{REG} Low Voltage (Power Down)	0		0.5	V	
V_{REG} High Voltage (Recom- mended)	2.75	2.8	2.95	V	
V_{REG} High Voltage (Operational)	2.7		3.0	V	
V_{MODE} Voltage	0		0.5	V	High Power Mode
V_{MODE} Voltage	2.0		3.0	V	Low Power Mode
Peak Envelope Power Detector					$V_{CCBIAS}=3.4\text{V}$, $V_{REG}=2.8\text{V}$, $T=+25^{\circ}\text{C}$, $R_{DET}=5.1\text{k}\Omega$, $Z_{LOAD}=50\Omega$
Operating Frequency	1920		1980	MHz	
DC Output Voltage		0.3		V	$P_{OUT}=0\text{W}$
	0.65	0.70	0.78	V	$P_{OUT}=+16\text{dBm}$, $V_{CC1,2}=1.5\text{V}$, $V_{MODE}=2.5\text{V}$
	2.2	2.5	2.8	V	$P_{OUT}=+27.5\text{dBm}$, $V_{CC1,2}=3.4\text{V}$, $V_{MODE}=0.2\text{V}$

Pin	Function	Description	Interface Schematic
1	RF IN	RF input internally matched to 50Ω. This input is internally AC-coupled.	
2	GND	Ground connection.	
3	VMODE	For nominal operation (High Power mode), V _{MODE} is set LOW. When set HIGH, devices are biased lower to improve efficiency at lower output levels.	
4	VREG	Regulated voltage supply for amplifier bias circuit. In power down mode, both V _{REG} and V _{MODE} need to be LOW (<0.5V).	
5	VDET	An external load resistor (RDET) is required on this pin. A lowpass filter or averaging functionality is also required to reduce voltage ripple (due to modulation) to an acceptable amount. An isolator is required on the PA RF output for proper operation of PDET when the PA operates into a non-50Ω load impedance.	
6	NC	No connection. Do not connect this pin to any external circuit.	
7	NC	No connection. Do not connect this pin to any external circuit.	
8	NC	No connection. Do not connect this pin to any external circuit.	
9	RF OUT	RF output. Internally AC-coupled.	
10	VCC2	Output stage collector supply. Please see the schematic for required external components.	
11	VCC2	Same as pin 10.	
12	VCC2	Same as pin 10.	
13	NC	No connection. Do not connect this pin to any external circuit.	
14	IM	Interstage matching. Connect to pin 15.	
15	VCC1/IM	First stage collector supply and interstage matching.	
16	VCCBIAS	Power supply input for the DC bias circuitry.	
Pkg Base	GND	Ground connection. The backside of the package should be soldered to a top side ground pad which is connected to the ground plane with multiple vias. The pad should have a short thermal path to the ground plane.	

Package Drawing



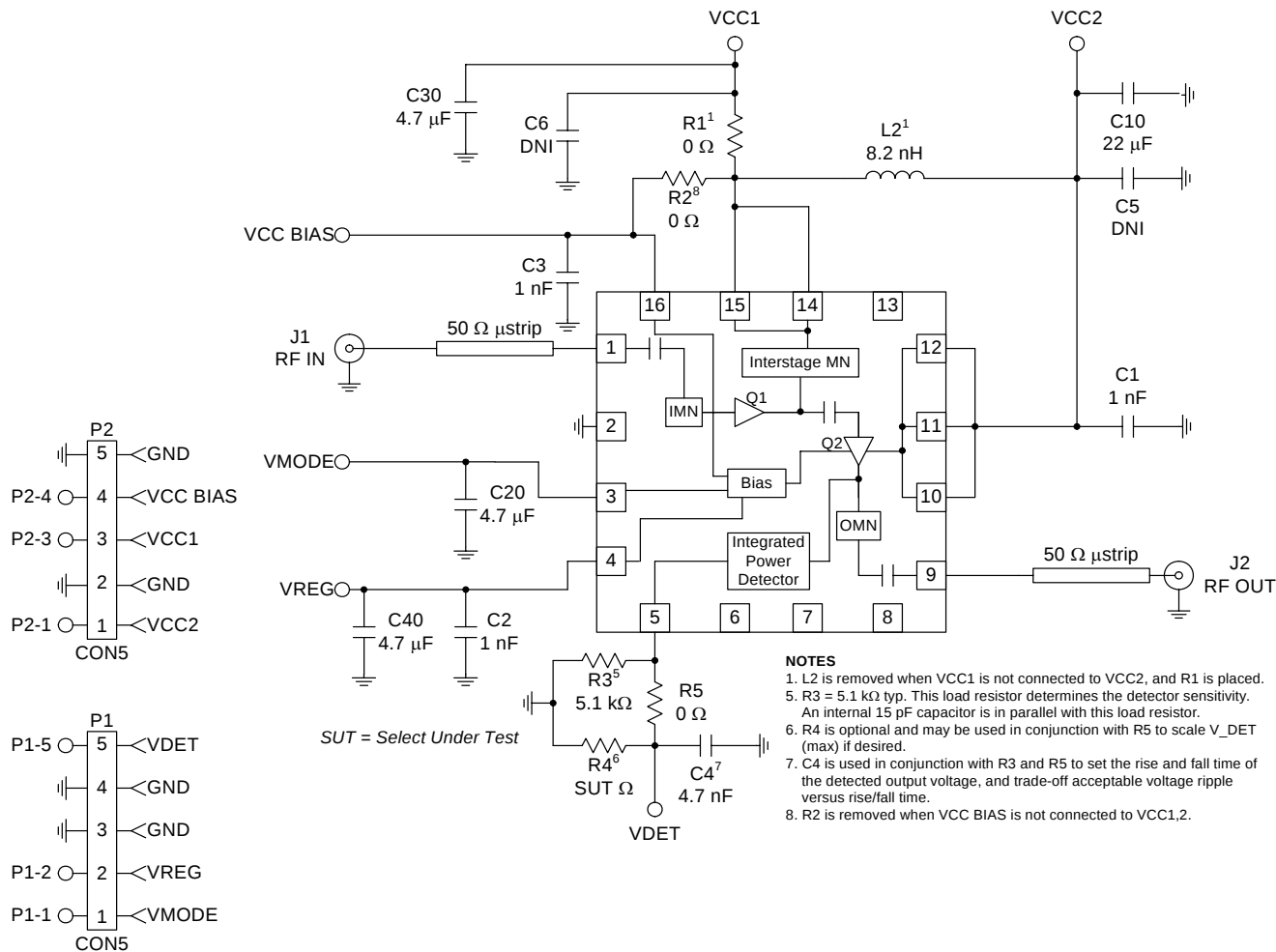
Application Schematic



Circuit Optimization for Various Output Power Requirements

Output Power (dBm)	Matching Component	Sample Part Number	Typical Efficiency (%)
28	12 nH	LQG15HN12NJ02D (Murata)	41
27.5	N/A		42
26.5	0.5 pF	GRM1555C1HR50BZ01E (Murata)	42
26	1.0 pF	GRM1555C1H1R0BZ01E (Murata)	42
25	1.5 pF	GRM1555C1H1R5BZ01E (Murata)	41

Evaluation Board Schematic



PCB Design Requirements

PCB Surface Finish

The PCB surface finish used for RFMD's qualification process is electroless nickel, immersion gold. Typical thickness is 3μinch to 8μinch gold over 180μinch nickel.

PCB Land Pattern Recommendation

PCB land patterns are based on IPC-SM-782 standards when possible. The pad pattern shown has been developed and tested for optimized assembly at RFMD; however, it may require some modifications to address company specific assembly processes. The PCB land pattern has been developed to accommodate lead and package tolerances.

PCB Metal Land Pattern

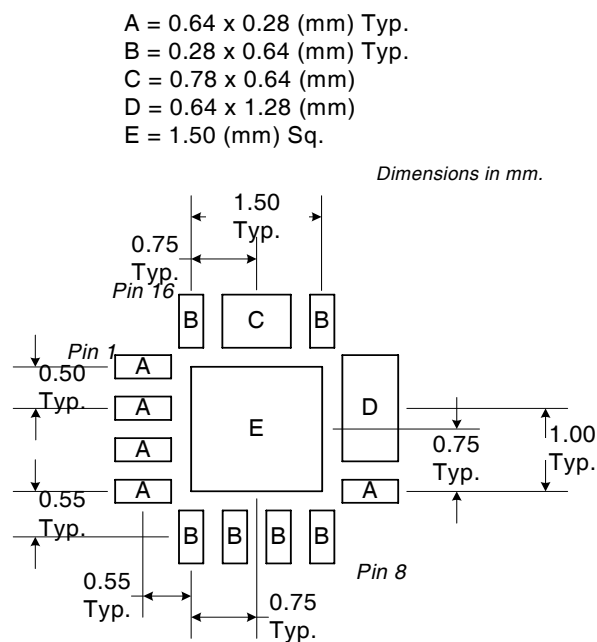


Figure 1. PCB Metal Land Pattern (Top View)

PCB Solder Mask Pattern

Liquid Photo-Imageable (LPI) solder mask is recommended. The solder mask footprint will match what is shown for the PCB metal land pattern with a 2mil to 3mil expansion to accommodate solder mask registration clearance around all pads. The center-grounding pad shall also have a solder mask clearance. Expansion of the pads to create solder mask clearance can be provided in the master data or requested from the PCB fabrication supplier.

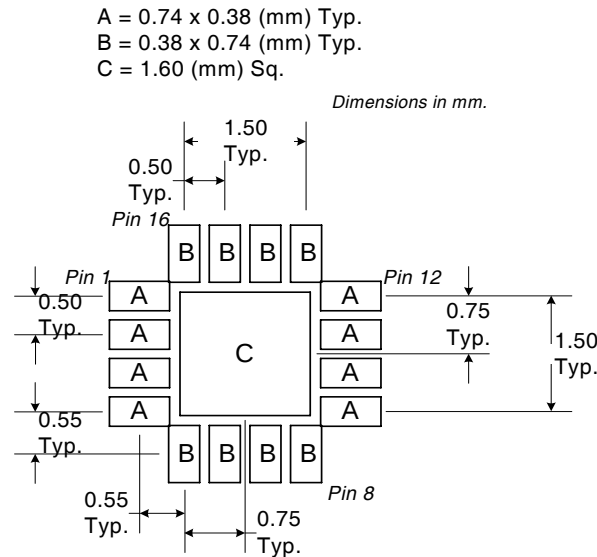


Figure 2. PCB Solder Mask Pattern (Top View)

Thermal Pad and Via Design

The PCB land pattern has been designed with a thermal pad that matches the die paddle size on the bottom of the device.

Thermal vias are required in the PCB layout to effectively conduct heat away from the package. The via pattern has been designed to address thermal, power dissipation and electrical requirements of the device as well as accommodating routing strategies.

The via pattern used for the RFMD qualification is based on thru-hole vias with 0.203mm to 0.330mm finished hole size on a 0.5mm to 1.2mm grid pattern with 0.025mm plating on via walls. If micro vias are used in a design, it is suggested that the quantity of vias be increased by a 4:1 ratio to achieve similar results.