

## Introduction

The Atmel® | SMART™ SAM C20 is a series of microcontrollers optimized for industrial automation, appliances and other 5V applications using the 32-bit ARM® Cortex®-M0+ processor, ranging from 32- to 64-pins with up to 256KB Flash and 32KB of SRAM and operate at a maximum frequency of 48MHz and reach 2.46 CoreMark®/MHz. The SAM C20 devices are designed for simple and intuitive migration with identical peripheral modules, hex compatible code, identical linear address map and pin compatible migration paths between all devices in the product series. All devices include intelligent and flexible peripherals, Atmel Event System for inter-peripheral signaling, and support for capacitive touch button, slider and wheel user interfaces.

SAM C20 devices are pin compatible to the SAM D and SAM C family of general purpose microcontrollers.

## Features

- Processor
  - ARM Cortex-M0+ CPU running at up to 48MHz
    - Single-cycle hardware multiplier
    - Micro Trace Buffer
    - Memory Protection Unit (MPU)
- Memories
  - 32/64/128/256KB in-system self-programmable Flash
  - 1/2/4/8KB independent self-programmable Flash for EEPROM emulation
  - 4/8/16/32KB SRAM Main Memory
- System
  - Power-on reset (POR) and brown-out detection (BOD)
  - Internal and external clock options with 48MHz to 96MHz Fractional Digital Phase Locked Loop (FDPLL96M)
  - External Interrupt Controller (EIC)
  - 16 external interrupts
  - One non-maskable interrupt

- Two-pin Serial Wire Debug (SWD) programming, test and debugging interface
- Low Power
  - Idle, standby, and off sleep modes
  - SleepWalking peripherals
- Peripherals
  - Hardware Divide and Square Root Accelerator (DIVAS)
  - 6-channel Direct Memory Access Controller (DMAC)
  - 6-channel Event System
  - Up to five 16-bit Timer/Counters (TC), configurable as either:
    - One 16-bit TC with compare/capture channels
    - One 8-bit TC with compare/capture channels
    - One 32-bit TC with compare/capture channels, by using two TCs
  - One 24-bit Timer/Counter for Control (TCC), with extended functions:
    - Up to four compare channels with optional complementary output
    - Generation of synchronized pulse width modulation (PWM) pattern across port pins
    - Deterministic fault protection, fast decay and configurable dead-time between complementary output
    - Dithering that increase resolution with up to 5 bit and reduce quantization error
  - Frequency Meter
  - 32-bit Real Time Counter (RTC) with clock/calendar function
  - Watchdog Timer (WDT)
  - CRC-32 generator
  - Up to four Serial Communication Interfaces (SERCOM), each configurable to operate as either:
    - USART with full-duplex and single-wire half-duplex configuration
    - I<sup>2</sup>C up to 3.4MHz
    - SPI
    - LIN master/slave
    - RS-485
  - One Configurable Custom Logic (CCL)
  - One 12-bit, 1Msps Analog-to-Digital Converter (ADC) with up to 12 channels
    - Differential and single-ended input
    - Automatic offset and gain error compensation
    - Oversampling and decimation in hardware to support 13-, 14-, 15- or 16-bit resolution
  - Two Analog Comparators (AC) with window compare function
  - Peripheral Touch Controller (PTC)
    - 256-Channel capacitive touch and proximity sensing
- I/O
  - Up to 52 programmable I/O pins
- Drop in compatible with SAM D20 and SAM D21
- Packages
  - 64-pin TQFP, QFN
  - 56-pin WLCSP
  - 48-pin TQFP, QFN

- 32-pin TQFP, QFN
- Operating Voltage
  - 2.7V – 5.5V

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## 1. Description

The Atmel SAM C20 devices provide the following features: In-system programmable Flash, six-channel direct memory access (DMA) controller, six-channel Event System, programmable interrupt controller, up to 52 programmable I/O pins, 32-bit real-time clock and calendar, up to five 16-bit Timer/Counters (TC) and three Timer/Counters for Control (TCC), where each TC can be configured to perform frequency and waveform generation, accurate program execution timing or input capture with time and frequency measurement of digital signals. The TCs can operate in 8- or 16-bit mode, selected TCs can be cascaded to form a 32-bit TC, and three timer/counters have extended functions optimized for motor, lighting and other control applications. Two TCC can operate in 24-bit mode, and the third TCC can operate in 16-bit mode. The series provide up to four Serial Communication Modules (SERCOM) that each can be configured to act as an USART, UART, SPI, I<sup>2</sup>C up to 3.4MHz, SMBus, RS-485 and LIN master/slave; one 12-bit, 1Msps ADC with up to 12-channels, two analog comparators with window mode, Peripheral Touch Controller supporting up to 256 buttons, sliders, wheels and proximity sensing; programmable Watchdog Timer, brown-out detector and power-on reset and two-pin Serial Wire Debug (SWD) program and debug interface.

All devices have accurate and low-power external and internal oscillators. All oscillators can be used as a source for the system clock. Different clock domains can be independently configured to run at different frequencies, enabling power saving by running each peripheral at its optimal clock frequency, and thus maintaining a high CPU frequency while reducing power consumption.

The SAM C20 devices have three software-selectable sleep modes, idle, standby and off. In idle mode the CPU is stopped while all other functions can be kept running. In standby all clocks and functions are stopped except those selected to continue running. In this mode all RAMs and logic contents are retained. The device supports SleepWalking. This feature allows the peripheral to wake up from sleep based on predefined conditions, and thus allows some internal operation like DMA transfer and/or the CPU to wake up only when needed, e.g. when a threshold is crossed or a result is ready. The Event System supports synchronous and asynchronous events, allowing peripherals to receive, react to and send events even in standby mode.

The Flash program memory can be reprogrammed in-system through the SWD interface. The same interface can be used for non-intrusive on-chip debug of application code. A boot loader running in the device can use any communication interface to download and upgrade the application program in the Flash memory.

The Atmel SAM C20 devices are supported with a full suite of program and system development tools, including C compilers, macro assemblers, program debugger/simulators, programmers and evaluation kits.

## 2. Configuration Summary

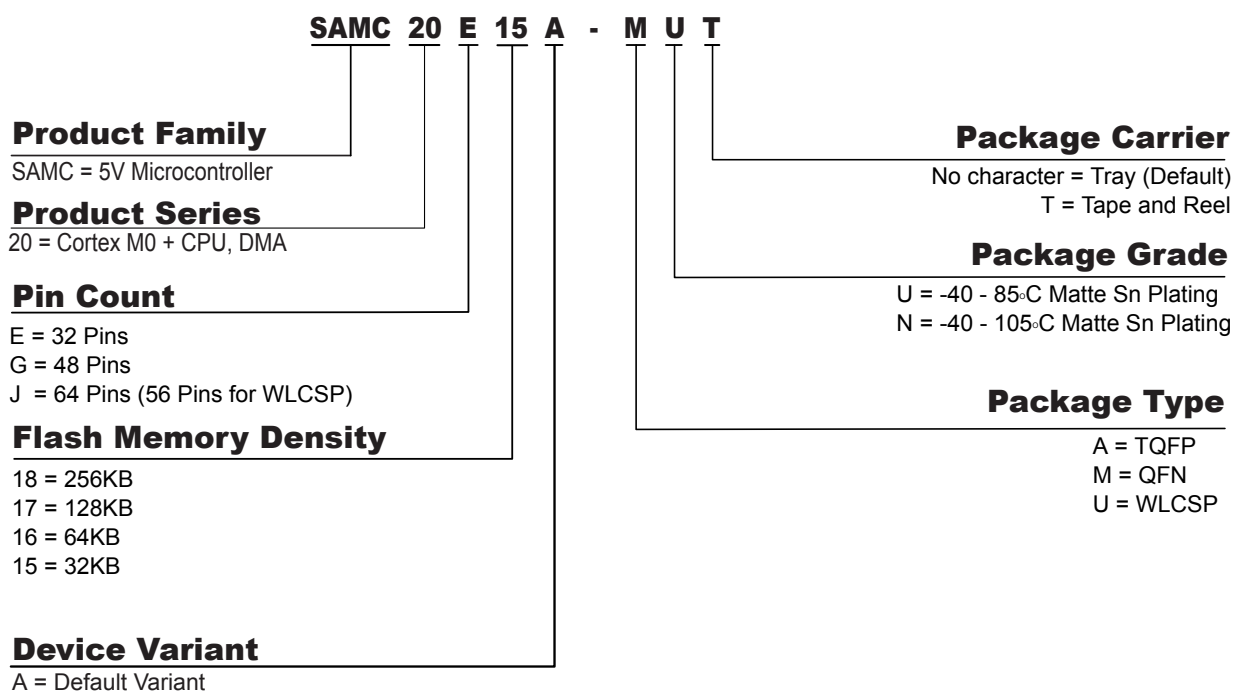
|                                                     | SAM C20J                              | SAM C20G                              | SAM C20E                              |
|-----------------------------------------------------|---------------------------------------|---------------------------------------|---------------------------------------|
| Pins                                                | 64 (56 for WLCSP)                     | 48                                    | 32                                    |
| General Purpose I/O-pins (GPIOs)                    | 52                                    | 38                                    | 26                                    |
| Flash                                               | 256/128/64/32KB                       | 256/128/64/32KB                       | 256/128/64/32KB                       |
| Flash RWW section                                   | 8/4/2/1KB                             | 8/4/2/1KB                             | 8/4/2/1KB                             |
| System SRAM                                         | 32/16/8/4KB                           | 32/16/8/4KB                           | 32/16/8/4KB                           |
| Timer Counter (TC) instances                        | 5                                     | 5                                     | 5                                     |
| Waveform output channels per TC instance            | 2                                     | 2                                     | 2                                     |
| Timer Counter for Control (TCC) instances           | 1                                     | 1                                     | 1                                     |
| Waveform output channels per TCC                    | 8                                     | 8                                     | 6                                     |
| DMA channels                                        | 6                                     | 6                                     | 6                                     |
| Configurable Custom Logic (CCL) (LUTs)              | 4                                     | 4                                     | 4                                     |
| Serial Communication Interface (SERCOM) instances   | 4                                     | 4                                     | 4                                     |
| Analog-to-Digital Converter (ADC) channels          | 12                                    | 12                                    | 10                                    |
| Analog Comparators (AC)                             | 2                                     | 2                                     | 2                                     |
| Real-Time Counter (RTC)                             | Yes                                   | Yes                                   | Yes                                   |
| RTC alarms                                          | 1                                     | 1                                     | 1                                     |
| RTC compare values                                  | One 32-bit value or two 16-bit values | One 32-bit value or two 16-bit values | One 32-bit value or two 16-bit values |
| External Interrupt lines                            | 16                                    | 16                                    | 16                                    |
| Peripheral Touch Controller (PTC)                   | 32                                    | 22                                    | 16                                    |
| Number of self-capacitance channels (Y-lines)       |                                       |                                       |                                       |
| Peripheral Touch Controller (PTC)                   | 256 (16x16)                           | 121 (11x11)                           | 64 (8x8)                              |
| Number of mutual-capacitance channels (X x Y lines) |                                       |                                       |                                       |
| Maximum CPU frequency                               | 48MHz                                 |                                       |                                       |
| Packages                                            | QFN<br>TQFP<br>WLCSP                  | QFN<br>TQFP                           | QFN<br>TQFP                           |

|                       | SAM C20J                                                                                                                                                                                                                                                                                       | SAM C20G | SAM C20E |
|-----------------------|------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|----------|----------|
| Oscillators           | 32.768kHz crystal oscillator (XOSC32K)<br>0.4-32MHz crystal oscillator (XOSC)<br>32.768kHz internal oscillator (OSC32K)<br>32KHz ultra-low-power internal oscillator (OSCULP32K)<br>48MHz high-accuracy internal oscillator (OSC48M)<br>96MHz Fractional Digital Phased Locked Loop (FDPLL96M) |          |          |
| Event System channels | 6                                                                                                                                                                                                                                                                                              | 6        | 6        |
| SW Debug Interface    | Yes                                                                                                                                                                                                                                                                                            | Yes      | Yes      |
| Watchdog Timer (WDT)  | Yes                                                                                                                                                                                                                                                                                            | Yes      | Yes      |

#### Related Links

[I/O Multiplexing and Considerations](#) on page 21

### 3. Ordering Information



#### 3.1. SAM C20E

Table 3-1. SAM C20E15A Ordering Codes

| Ordering Code     | FLASH (bytes) | SRAM (bytes) | Package | Carrier Type | Temp  |
|-------------------|---------------|--------------|---------|--------------|-------|
| ATSAM C20E15A-AUT | 32K           | 4K           | TQFP32  | Tape & Reel  | 85°C  |
| ATSAM C20E15A-ANT | 32K           | 4K           | TQFP32  | Tape & Reel  | 105°C |
| ATSAM C20E15A-MUT | 32K           | 4K           | QFN32   | Tape & Reel  | 85°C  |
| ATSAM C20E15A-MNT | 32K           | 4K           | QFN32   | Tape & Reel  | 105°C |

Table 3-2. SAM C20E16A Ordering Codes

| Ordering Code     | FLASH (bytes) | SRAM (bytes) | Package | Carrier Type | Temp  |
|-------------------|---------------|--------------|---------|--------------|-------|
| ATSAM C20E16A-AUT | 64K           | 8K           | TQFP32  | Tape & Reel  | 85°C  |
| ATSAM C20E16A-ANT | 64K           | 8K           | TQFP32  | Tape & Reel  | 105°C |
| ATSAM C20E16A-MUT | 64K           | 8K           | QFN32   | Tape & Reel  | 85°C  |
| ATSAM C20E16A-MNT | 64K           | 8K           | QFN32   | Tape & Reel  | 105°C |

**Table 3-3. SAM C20E17A Ordering Codes**

| Ordering Code     | FLASH (bytes) | SRAM (bytes) | Package | Carrier Type | Temp  |
|-------------------|---------------|--------------|---------|--------------|-------|
| ATSAM C20E17A-AUT | 128K          | 16K          | TQFP32  | Tape & Reel  | 85°C  |
| ATSAM C20E17A-ANT | 128K          | 16K          | TQFP32  | Tape & Reel  | 105°C |
| ATSAM C20E17A-MUT | 128K          | 16K          | QFN32   | Tape & Reel  | 85°C  |
| ATSAM C20E17A-MNT | 128K          | 16K          | QFN32   | Tape & Reel  | 105°C |

**Table 3-4. SAM C20E18A Ordering Codes**

| Ordering Code     | FLASH (bytes) | SRAM (bytes) | Package | Carrier Type | Temp  |
|-------------------|---------------|--------------|---------|--------------|-------|
| ATSAM C20E18A-AUT | 256K          | 32K          | TQFP32  | Tape & Reel  | 85°C  |
| ATSAM C20E18A-ANT | 256K          | 32K          | TQFP32  | Tape & Reel  | 105°C |
| ATSAM C20E18A-MUT | 256K          | 32K          | QFN32   | Tape & Reel  | 85°C  |
| ATSAM C20E18A-MNT | 256K          | 32K          | QFN32   | Tape & Reel  | 105°C |

## 3.2. SAM C20G

**Table 3-5. SAM C20G15A Ordering Codes**

| Ordering Code     | FLASH (bytes) | SRAM (bytes) | Package | Carrier Type | Temp  |
|-------------------|---------------|--------------|---------|--------------|-------|
| ATSAM C20G15A-AUT | 32K           | 4K           | TQFP48  | Tape & Reel  | 85°C  |
| ATSAM C20G15A-ANT | 32K           | 4K           | TQFP48  | Tape & Reel  | 105°C |
| ATSAM C20G15A-MUT | 32K           | 4K           | QFN48   | Tape & Reel  | 85°C  |
| ATSAM C20G15A-MNT | 32K           | 4K           | QFN48   | Tape & Reel  | 105°C |

**Table 3-6. SAM C20G16A Ordering Codes**

| Ordering Code     | FLASH (bytes) | SRAM (bytes) | Package | Carrier Type | Temp  |
|-------------------|---------------|--------------|---------|--------------|-------|
| ATSAM C20G16A-AUT | 64K           | 8K           | TQFP48  | Tape & Reel  | 85°C  |
| ATSAM C20G16A-ANT | 64K           | 8K           | TQFP48  | Tape & Reel  | 105°C |
| ATSAM C20G16A-MUT | 64K           | 8K           | QFN48   | Tape & Reel  | 85°C  |
| ATSAM C20G16A-MNT | 64K           | 8K           | QFN48   | Tape & Reel  | 105°C |

**Table 3-7. SAM C20G17A Ordering Codes**

| Ordering Code     | FLASH (bytes) | SRAM (bytes) | Package | Carrier Type | Temp  |
|-------------------|---------------|--------------|---------|--------------|-------|
| ATSAM C20G17A-AUT | 128K          | 16K          | TQFP48  | Tape & Reel  | 85°C  |
| ATSAM C20G17A-ANT | 128K          | 16K          | TQFP48  | Tape & Reel  | 105°C |
| ATSAM C20G17A-MUT | 128K          | 16K          | QFN48   | Tape & Reel  | 85°C  |
| ATSAM C20G17A-MNT | 128K          | 16K          | QFN48   | Tape & Reel  | 105°C |

**Table 3-8. SAM C20G18A Ordering Codes**

| Ordering Code     | FLASH (bytes) | SRAM (bytes) | Package | Carrier Type | Temp  |
|-------------------|---------------|--------------|---------|--------------|-------|
| ATSAM C20G18A-AUT | 256K          | 32K          | TQFP48  | Tape & Reel  | 85°C  |
| ATSAM C20G18A-ANT | 256K          | 32K          | TQFP48  | Tape & Reel  | 105°C |
| ATSAM C20G18A-MUT | 256K          | 32K          | QFN48   | Tape & Reel  | 85°C  |
| ATSAM C20G18A-MNT | 256K          | 32K          | QFN48   | Tape & Reel  | 105°C |

### 3.3. SAM C20J

**Table 3-9. SAM C20J15A Ordering Codes**

| Ordering Code     | FLASH (bytes) | SRAM (bytes) | Package | Carrier Type | Temp  |
|-------------------|---------------|--------------|---------|--------------|-------|
| ATSAM C20J15A-AUT | 32K           | 4K           | TQFP64  | Tape & Reel  | 85°C  |
| ATSAM C20J15A-ANT | 32K           | 4K           | TQFP64  | Tape & Reel  | 105°C |
| ATSAM C20J15A-MUT | 32K           | 4K           | QFN64   | Tape & Reel  | 85°C  |
| ATSAM C20J15A-MNT | 32K           | 4K           | QFN64   | Tape & Reel  | 105°C |

**Table 3-10. SAM C20J16A Ordering Codes**

| Ordering Code     | FLASH (bytes) | SRAM (bytes) | Package | Carrier Type | Temp  |
|-------------------|---------------|--------------|---------|--------------|-------|
| ATSAM C20J16A-AUT | 64K           | 8K           | TQFP64  | Tape & Reel  | 85°C  |
| ATSAM C20J16A-ANT | 64K           | 8K           | TQFP64  | Tape & Reel  | 105°C |
| ATSAM C20J16A-MUT | 64K           | 8K           | QFN64   | Tape & Reel  | 85°C  |
| ATSAM C20J16A-MNT | 64K           | 8K           | QFN64   | Tape & Reel  | 105°C |

**Table 3-11. SAM C20J17A Ordering Codes**

| Ordering Code                    | FLASH (bytes) | SRAM (bytes) | Package | Carrier Type | Temp  |
|----------------------------------|---------------|--------------|---------|--------------|-------|
| ATSAM C20J17A-AUT                | 128K          | 16K          | TQFP64  | Tape & Reel  | 85°C  |
| ATSAM C20J17A-ANT                | 128K          | 16K          | TQFP64  | Tape & Reel  | 105°C |
| ATSAM C20J17A-MUT                | 128K          | 16K          | QFN64   | Tape & Reel  | 85°C  |
| ATSAM C20J17A-MNT                | 128K          | 16K          | QFN64   | Tape & Reel  | 105°C |
| ATSAM C20J17A-UUT <sup>(1)</sup> | 128K          | 16K          | WLCSP56 | Tape & Reel  | 85°C  |

1. Contact your local Microchip sales representative for availability.

**Table 3-12. SAM C20J18A Ordering Codes**

| Ordering Code                    | FLASH (bytes) | SRAM (bytes) | Package | Carrier Type | Temp  |
|----------------------------------|---------------|--------------|---------|--------------|-------|
| ATSAM C20J18A-AUT                | 256K          | 32K          | TQFP64  | Tape & Reel  | 85°C  |
| ATSAM C20J18A-ANT                | 256K          | 32K          | TQFP64  | Tape & Reel  | 105°C |
| ATSAM C20J18A-MUT                | 256K          | 32K          | QFN64   | Tape & Reel  | 85°C  |
| ATSAM C20J18A-MNT                | 256K          | 32K          | QFN64   | Tape & Reel  | 105°C |
| ATSAM C20J18A-UUT <sup>(1)</sup> | 256K          | 32K          | WLCSP56 | Tape & Reel  | 85°C  |

1. Contact your local Microchip sales representative for availability.

### 3.4. Device Identification

The DSU - Device Service Unit peripheral provides the Device Selection bits in the Device Identification register (DID.DEVSEL) in order to identify the device by software. The SAM C20 variants have a reset value of DID=0x1101drxx, with the LSB identifying the die number ('d'), the die revision ('r') and the device selection ('xx').

**Table 3-13. SAM C20 Device Identification Values**

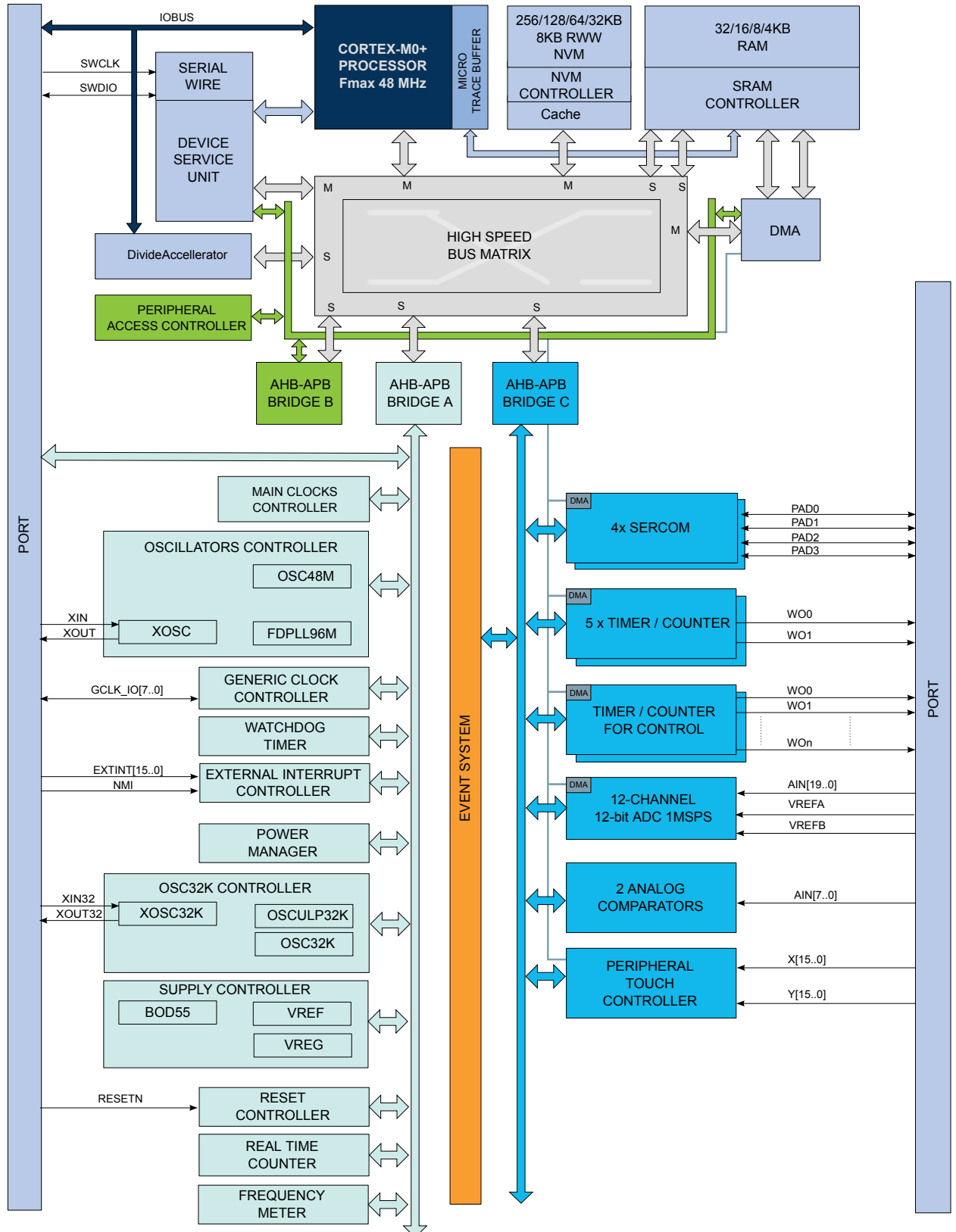
| DEVSEL (DID[7:0]) | Device      |
|-------------------|-------------|
| 0x00              | SAM C20J18A |
| 0x01              | SAM C20J17A |
| 0x02              | SAM C20J16A |
| 0x03              | SAM C20J15A |
| 0x04              | Reserved    |
| 0x05              | SAM C20G18A |
| 0x06              | SAM C20G17A |
| 0x07              | SAM C20G16A |
| 0x08              | SAM C20G15A |

| DEVSEL (DID[7:0]) | Device      |
|-------------------|-------------|
| 0x09              | Reserved    |
| 0x0A              | SAM C20E18A |
| 0x0B              | SAM C20E17A |
| 0x0C              | SAM C20E16A |
| 0x0D              | SAM C20E15A |
| 0x0E-0xFF         | Reserved    |

**Note:** The device variant (last letter of the ordering number) is independent of the die revision (DSU.DID.REVISION): The device variant denotes functional differences, whereas the die revision marks evolution of the die.

## 4. Block Diagram

Figure 4-1. System Block Diagram for SAM C20E/G/J



**Note:**

1. Some products have different number of SERCOM instances, Timer/Counter instances, PTC signals and ADC signals.
2. The three TCC instances have different configurations, including the number of Waveform Output (WO) lines.

**Related Links**

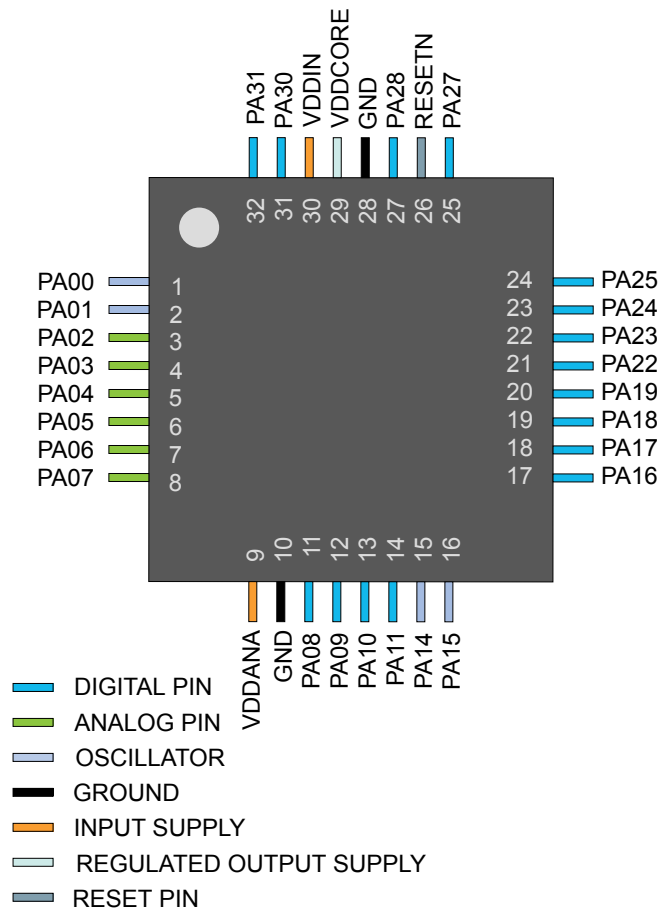
[TCC Configurations](#) on page 24

[Multiplexed Signals](#) on page 21

## 5. Pinout

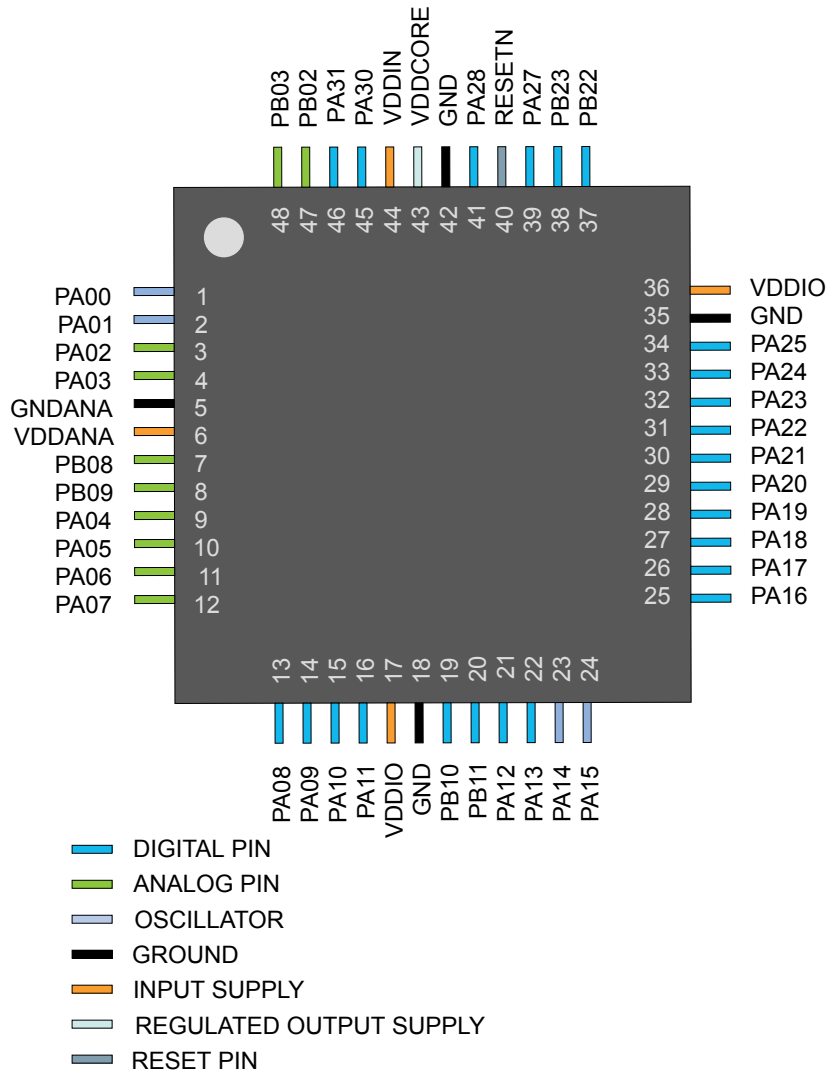
### 5.1. SAM C20E

#### 5.1.1. QFN32 / TQFP32



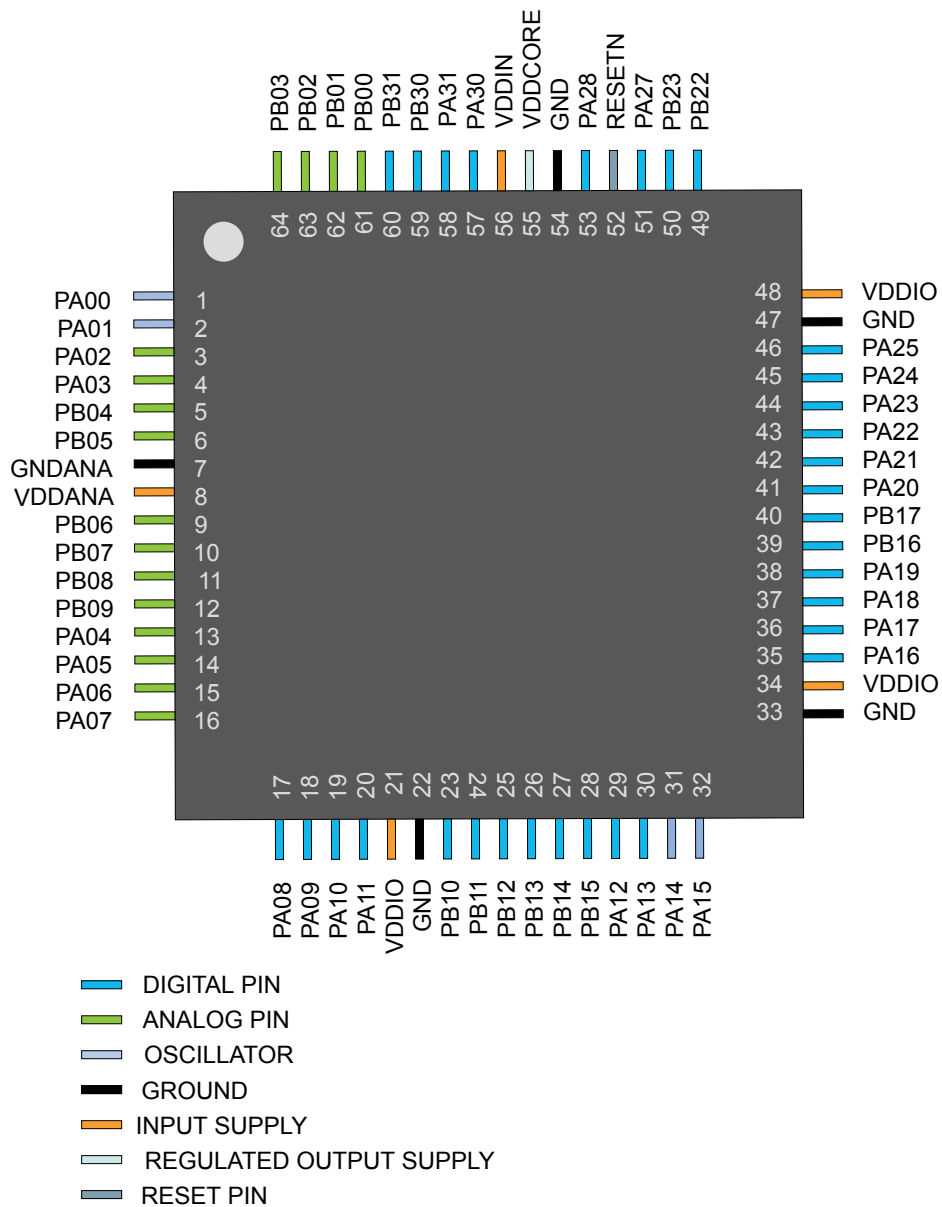
## 5.2. SAM C20G

### 5.2.1. QFN48 / TQFP48

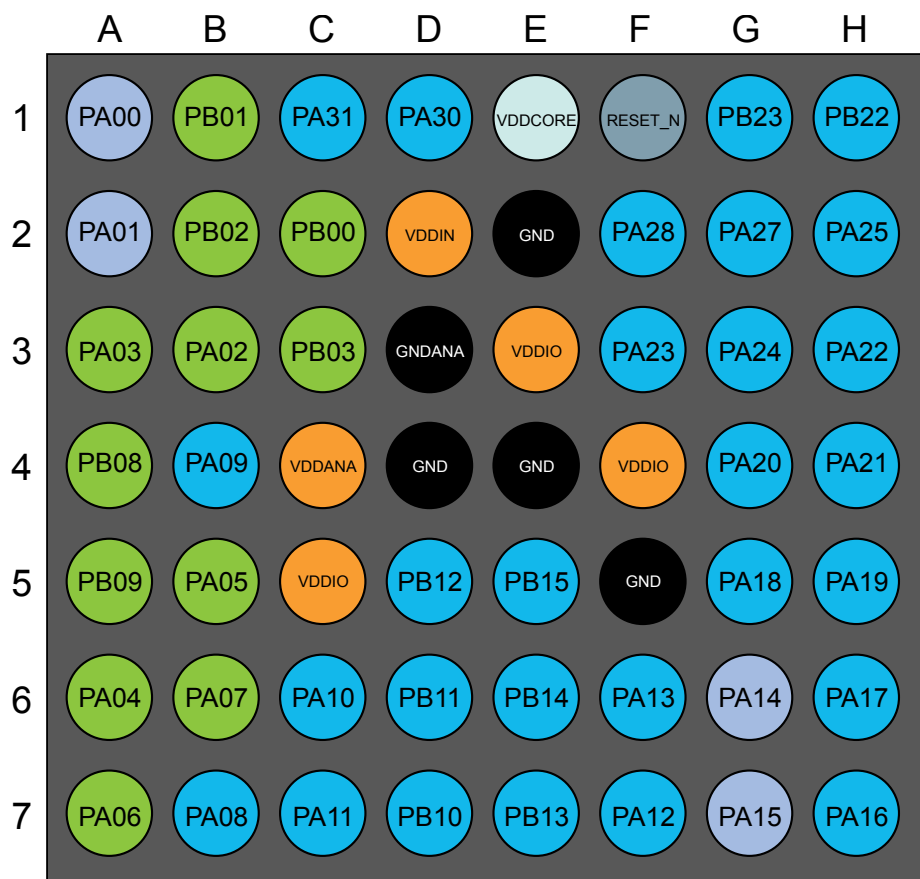


### 5.3. SAM C20J

#### 5.3.1. QFN64 / TQFP64



### 5.3.2. WLCSP56



- DIGITAL PIN
- ANALOG PIN
- OSCILLATOR
- GROUND
- INPUT SUPPLY
- REGULATED OUTPUT SUPPLY
- RESET PIN

## 6. Signal Descriptions List

The following table gives details on signal names classified by peripheral.

**Table 6-1. Signal Descriptions List**

| Signal Name                                     | Function                                                              | Type           | Active Level |
|-------------------------------------------------|-----------------------------------------------------------------------|----------------|--------------|
| <b>Analog Comparators - AC</b>                  |                                                                       |                |              |
| AIN[7:0]                                        | AC Analog Inputs                                                      | Analog         |              |
| CMP[2:0]                                        | AC Comparator Outputs                                                 | Digital        |              |
| <b>Analog Digital Converter - ADCx</b>          |                                                                       |                |              |
| AIN[11:0]                                       | ADC Analog Inputs                                                     | Analog         |              |
| VREFA                                           | ADC Voltage External Reference A                                      | Analog         |              |
| <b>External Interrupt Controller - EIC</b>      |                                                                       |                |              |
| EXTINT[15:0]                                    | External Interrupts inputs                                            | Digital        |              |
| NMI                                             | External Non-Maskable Interrupt input                                 | Digital        |              |
| <b>Generic Clock Generator - GCLK</b>           |                                                                       |                |              |
| GCLK_IO[7:0]                                    | Generic Clock (source clock inputs or generic clock generator output) | Digital        |              |
| <b>Custom Control Logic - CCL</b>               |                                                                       |                |              |
| IN[11:0]                                        | Logic Inputs                                                          | Digital        |              |
| OUT[3:0]                                        | Logic Outputs                                                         | Digital        |              |
| <b>Power Manager - PM</b>                       |                                                                       |                |              |
| RESETN                                          | Reset input                                                           | Digital        | Low          |
| <b>Serial Communication Interface - SERCOMx</b> |                                                                       |                |              |
| PAD[3:0]                                        | SERCOM Inputs/Outputs Pads                                            | Digital        |              |
| <b>Oscillators Control - OSCCTRL</b>            |                                                                       |                |              |
| XIN                                             | Crystal or external clock Input                                       | Analog/Digital |              |
| XOUT                                            | Crystal Output                                                        | Analog         |              |
| <b>32KHz Oscillators Control - OSC32CTRL</b>    |                                                                       |                |              |
| XIN32                                           | 32KHz Crystal or external clock Input                                 | Analog/Digital |              |
| XOUT32                                          | 32KHz Crystal Output                                                  | Analog         |              |
| <b>Timer Counter - TCx</b>                      |                                                                       |                |              |
| WO[1:0]                                         | Waveform Outputs                                                      | Digital        |              |
| <b>Timer Counter - TCCx</b>                     |                                                                       |                |              |
| WO[1:0]                                         | Waveform Outputs                                                      | Digital        |              |
| <b>Peripheral Touch Controller - PTC</b>        |                                                                       |                |              |
| X[15:0]                                         | PTC Input                                                             | Analog         |              |
| Y[15:0]                                         | PTC Input                                                             | Analog         |              |
| <b>General Purpose I/O - PORT</b>               |                                                                       |                |              |
| PA25 - PA00                                     | Parallel I/O Controller I/O Port A                                    | Digital        |              |

| Signal Name | Function                           | Type    | Active Level |
|-------------|------------------------------------|---------|--------------|
| PA28 - PA27 | Parallel I/O Controller I/O Port A | Digital |              |
| PA31 - PA30 | Parallel I/O Controller I/O Port A | Digital |              |
| PB17 - PB00 | Parallel I/O Controller I/O Port B | Digital |              |
| PB23 - PB22 | Parallel I/O Controller I/O Port B | Digital |              |
| PB31 - PB30 | Parallel I/O Controller I/O Port B | Digital |              |

## 7. I/O Multiplexing and Considerations

### 7.1. Multiplexed Signals

Each pin is by default controlled by the PORT as a general purpose I/O and alternatively it can be assigned to one of the peripheral functions A, B, C, D, E, F, G, H or I. To enable a peripheral function on a pin, the Peripheral Multiplexer Enable bit in the Pin Configuration register corresponding to that pin (PINCFGn.PMUXEN, n = 0-31) in the PORT must be written to one. The selection of peripheral function A to H is done by writing to the Peripheral Multiplexing Odd and Even bits in the Peripheral Multiplexing register (PMUXn.PMUXE/O) in the PORT.

**Table 7-1. PORT Function Multiplexing**

|          | Pin <sup>(1)</sup> |          | I/O Pin | Supply | A          |           |         | B <sup>(2)(3)</sup> |             | C                        | D                  | E          | F              | G   | H          | I               |
|----------|--------------------|----------|---------|--------|------------|-----------|---------|---------------------|-------------|--------------------------|--------------------|------------|----------------|-----|------------|-----------------|
| SAM C20E | SAM C20G           | SAM C20J |         |        | EIC        | REF       | ADC0    | AC                  | PTC         | SERCOM <sup>(2)(3)</sup> | SERCOM-ALT         | TC<br>TCC  | TCC            | COM | AC/GCLK    | CCL             |
| 1        | 1                  | 1        | PA00    | VDDANA | EXTINT[0]  |           |         |                     |             |                          | SERCOM1/<br>PAD[0] |            |                |     | CMP[2]     |                 |
| 2        | 2                  | 2        | PA01    | VDDANA | EXTINT[1]  |           |         |                     |             |                          | SERCOM1/<br>PAD[1] |            |                |     | CMP[3]     |                 |
| 3        | 3                  | 3        | PA02    | VDDANA | EXTINT[2]  |           | AIN[0]  | AIN[4]              | Y[0]        |                          |                    |            |                |     |            |                 |
| 4        | 4                  | 4        | PA03    | VDDANA | EXTINT[3]  | ADC/VREFA | AIN[1]  | AIN[5]              | Y[1]        |                          |                    |            |                |     |            |                 |
|          |                    | 5        | PB04    | VDDANA | EXTINT[4]  |           |         |                     | Y[10]       |                          |                    |            |                |     |            |                 |
|          |                    | 6        | PB05    | VDDANA | EXTINT[5]  |           |         | AIN[6]              | Y[11]       |                          |                    |            |                |     |            |                 |
|          |                    | 9        | PB06    | VDDANA | EXTINT[6]  |           |         | AIN[7]              | Y[12]       |                          |                    |            |                |     |            | CCL2/<br>IN[6]  |
|          |                    | 10       | PB07    | VDDANA | EXTINT[7]  |           |         |                     | Y[13]       |                          |                    |            |                |     |            | CCL2/<br>IN[7]  |
|          | 7                  | 11       | PB08    | VDDANA | EXTINT[8]  |           | AIN[2]  |                     | Y[14]       |                          |                    | TC0/WO[0]  |                |     |            | CCL2/<br>IN[8]  |
|          | 8                  | 12       | PB09    | VDDANA | EXTINT[9]  |           | AIN[3]  |                     | Y[15]       |                          |                    | TC0WO[1]   |                |     |            | CCL2/<br>OUT[2] |
| 5        | 9                  | 13       | PA04    | VDDANA | EXTINT[4]  |           | AIN[4]  | AIN[0]              | Y[2]        |                          | SERCOM0/<br>PAD[0] | TCC0/WO[0] |                |     |            | CCL0/<br>IN[0]  |
| 6        | 10                 | 14       | PA05    | VDDANA | EXTINT[5]  |           | AIN[5]  | AIN[1]              | Y[3]        |                          | SERCOM0/<br>PAD[1] | TCC0/WO[1] |                |     |            | CCL0/<br>IN[1]  |
| 7        | 11                 | 15       | PA06    | VDDANA | EXTINT[6]  |           | AIN[6]  | AIN[2]              | Y[4]        |                          | SERCOM0/<br>PAD[2] |            |                |     |            | CCL0/<br>IN[2]  |
| 8        | 12                 | 16       | PA07    | VDDANA | EXTINT[7]  |           | AIN[7]  | AIN[3]              | Y[5]        |                          | SERCOM0/<br>PAD[3] |            |                |     |            | CCL0/<br>OUT[0] |
| 11       | 13                 | 17       | PA08    | VDDIO  | NMI        |           | AIN[8]  |                     | X[0]/Y[16]  | SERCOM0/<br>PAD[0]       | SERCOM2/<br>PAD[0] | TCC0/WO[0] |                |     |            | CCL1/<br>IN[3]  |
| 12       | 14                 | 18       | PA09    | VDDIO  | EXTINT[9]  |           | AIN[9]  |                     | X[1]/Y[17]  | SERCOM0/<br>PAD[1]       | SERCOM2/<br>PAD[1] | TCC0/WO[1] |                |     |            | CCL1/<br>IN[4]  |
| 13       | 15                 | 19       | PA10    | VDDIO  | EXTINT[10] |           | AIN[10] |                     | X[2]/Y[18]  | SERCOM0/<br>PAD[2]       | SERCOM2/<br>PAD[2] |            | TCC0/<br>WO[2] |     | GCLK_IO[4] | CCL1/<br>IN[5]  |
| 14       | 16                 | 20       | PA11    | VDDIO  | EXTINT[11] |           | AIN[11] |                     | X[3]/Y[19]  | SERCOM0/<br>PAD[3]       | SERCOM2/<br>PAD[3] |            | TCC0/<br>WO[3] |     | GCLK_IO[5] | CCL1/<br>OUT[1] |
|          | 19                 | 23       | PB10    | VDDIO  | EXTINT[10] |           |         |                     |             |                          |                    | TC1/WO[0]  | TCC0/<br>WO[4] |     | GCLK_IO[4] | CCL1/<br>IN[5]  |
|          | 20                 | 24       | PB11    | VDDIO  | EXTINT[11] |           |         |                     |             |                          |                    | TC1/WO[1]  | TCC0/<br>WO[5] |     | GCLK_IO[5] | CCL1/<br>OUT[1] |
|          |                    | 25       | PB12    | VDDIO  | EXTINT[12] |           |         |                     | X[12]/Y[28] |                          |                    | TC0/WO[0]  | TCC0/<br>WO[6] |     | GCLK_IO[6] |                 |
|          |                    | 26       | PB13    | VDDIO  | EXTINT[13] |           |         |                     | X[13]/Y[29] |                          |                    | TC0/WO[1]  | TCC0/<br>WO[7] |     | GCLK_IO[7] |                 |
|          |                    | 27       | PB14    | VDDIO  | EXTINT[14] |           |         |                     | X[14]/Y[30] |                          |                    | TC1/WO[0]  |                |     | GCLK_IO[0] | CCL3/<br>IN[9]  |
|          |                    | 28       | PB15    | VDDIO  | EXTINT[15] |           |         |                     | X[15]/Y[31] |                          |                    | TC1/WO[1]  |                |     | GCLK_IO[1] | CCL3/<br>IN[10] |
|          | 21                 | 29       | PA12    | VDDIO  | EXTINT[12] |           |         |                     |             | SERCOM2/<br>PAD[0]       |                    |            | TCC0/<br>WO[6] |     | AC/CMP[0]  |                 |
|          | 22                 | 30       | PA13    | VDDIO  | EXTINT[13] |           |         |                     |             | SERCOM2/<br>PAD[1]       |                    |            | TCC0/<br>WO[7] |     | AC/CMP[1]  |                 |
| 15       | 23                 | 31       | PA14    | VDDIO  | EXTINT[14] |           |         |                     |             | SERCOM2/<br>PAD[2]       |                    | TC4/WO[0]  | TCC0/<br>WO[4] |     | GCLK_IO[0] |                 |
| 16       | 24                 | 32       | PA15    | VDDIO  | EXTINT[15] |           |         |                     |             | SERCOM2/<br>PAD[3]       |                    | TC4/WO[1]  | TCC0/<br>WO[5] |     | GCLK_IO[1] |                 |
| 17       | 25                 | 35       | PA16    | VDDIO  | EXTINT[0]  |           |         |                     | X[4]/Y[20]  | SERCOM1/<br>PAD[0]       | SERCOM3/<br>PAD[0] |            | TCC0/<br>WO[6] |     | GCLK_IO[2] | CCL0/<br>IN[0]  |

| SAM C20E | Pin <sup>(1)</sup><br>SAM C20G | SAM C20J | I/O Pin | Supply | A<br>EIC   | REF | ADC0 | B <sup>(2)(3)</sup><br>AC | PTC         | C<br>SERCOM <sup>(2)(3)</sup> | D<br>SERCOM-ALT    | E<br>TC<br>TCC | F<br>TCC       | G<br>COM             | H<br>AC/GCLK | I<br>CCL        |
|----------|--------------------------------|----------|---------|--------|------------|-----|------|---------------------------|-------------|-------------------------------|--------------------|----------------|----------------|----------------------|--------------|-----------------|
| 18       | 26                             | 36       | PA17    | VDDIO  | EXTINT[1]  |     |      |                           | X[5]/Y[21]  | SERCOM1/<br>PAD[1]            | SERCOM3/<br>PAD[1] |                | TCC0/<br>WO[7] |                      | GCLK_IO[3]   | CCL0/<br>IN[1]  |
| 19       | 27                             | 37       | PA18    | VDDIO  | EXTINT[2]  |     |      |                           | X[6]/Y[22]  | SERCOM1/<br>PAD[2]            | SERCOM3/<br>PAD[2] | TC4/WO[0]      | TCC0/<br>WO[2] |                      | AC/CMP[0]    | CCL0/<br>IN[2]  |
| 20       | 28                             | 38       | PA19    | VDDIO  | EXTINT[3]  |     |      |                           | X[7]/Y[23]  | SERCOM1/<br>PAD[3]            | SERCOM3/<br>PAD[3] | TC4/WO[1]      | TCC0/<br>WO[3] |                      | AC/CMP[1]    | CCL0/<br>OUT[0] |
|          |                                | 39       | PB16    | VDDIO  | EXTINT[0]  |     |      |                           |             |                               |                    | TC2/WO[0]      | TCC0/<br>WO[4] |                      | GCLK_IO[2]   | CCL3/<br>IN[11] |
|          |                                | 40       | PB17    | VDDIO  | EXTINT[1]  |     |      |                           |             |                               |                    | TC2/WO[1]      | TCC0/<br>WO[5] |                      | GCLK_IO[3]   | CCL3/<br>OUT[3] |
|          | 29                             | 41       | PA20    | VDDIO  | EXTINT[4]  |     |      |                           | X[8]/Y[24]  |                               | SERCOM3/<br>PAD[2] | TC3/WO[0]      | TCC0/<br>WO[6] |                      | GCLK_IO[4]   |                 |
|          | 30                             | 42       | PA21    | VDDIO  | EXTINT[5]  |     |      |                           | X[9]/Y[25]  |                               | SERCOM3/<br>PAD[3] | TC3/WO[1]      | TCC0/<br>WO[7] |                      | GCLK_IO[5]   |                 |
| 21       | 31                             | 43       | PA22    | VDDIO  | EXTINT[6]  |     |      |                           | X[10]/Y[26] | SERCOM3/<br>PAD[0]            |                    | TC0/WO[0]      | TCC0/<br>WO[4] |                      | GCLK_IO[6]   | CCL2/<br>IN[6]  |
| 22       | 32                             | 44       | PA23    | VDDIO  | EXTINT[7]  |     |      |                           | X[11]/Y[27] | SERCOM3/<br>PAD[1]            |                    | TC0/WO[1]      | TCC0/<br>WO[5] |                      | GCLK_IO[7]   | CCL2/<br>IN[7]  |
| 23       | 33                             | 45       | PA24    | VDDIO  | EXTINT[12] |     |      |                           |             | SERCOM3/<br>PAD[2]            |                    | TC1/WO[0]      |                |                      | AC/CMP[2]    | CCL2/<br>IN[8]  |
| 24       | 34                             | 46       | PA25    | VDDIO  | EXTINT[13] |     |      |                           |             | SERCOM3/<br>PAD[3]            |                    | TC1/WO[1]      |                |                      | AC/CMP[3]    | CCL2/<br>OUT[2] |
|          | 37                             | 49       | PB22    | VDDIN  | EXTINT[6]  |     |      |                           |             |                               |                    | TC3/WO[0]      |                |                      | GCLK_IO[0]   | CCL0/<br>IN[0]  |
|          | 38                             | 50       | PB23    | VDDIN  | EXTINT[7]  |     |      |                           |             |                               |                    | TC3/WO[1]      |                |                      | GCLK_IO[1]   | CCL0/<br>OUT[0] |
| 25       | 39                             | 51       | PA27    | VDDIN  | EXTINT[15] |     |      |                           |             |                               |                    |                |                | BRK                  | GCLK_IO[0]   |                 |
| 27       | 41                             | 53       | PA28    | VDDIN  | EXTINT[8]  |     |      |                           |             |                               |                    |                |                |                      | GCLK_IO[0]   |                 |
| 31       | 45                             | 57       | PA30    | VDDIN  | EXTINT[10] |     |      |                           |             |                               | SERCOM1/<br>PAD[2] |                |                | CORTEX_M0P/<br>SWCLK | GCLK_IO[0]   | CCL1/<br>IN[3]  |
| 32       | 46                             | 58       | PA31    | VDDIN  | EXTINT[11] |     |      |                           |             |                               | SERCOM1/<br>PAD[3] |                |                | CORTEX_M0P/<br>SWDIO |              | CCL1/<br>OUT[1] |
|          |                                | 59       | PB30    | VDDIN  | EXTINT[14] |     |      |                           |             |                               |                    | TC0/WO[0]      |                |                      | AC/CMP[2]    |                 |
|          |                                | 60       | PB31    | VDDIN  | EXTINT[15] |     |      |                           |             |                               |                    | TC0/WO[1]      |                |                      | AC/CMP[3]    |                 |
|          |                                | 61       | PB00    | VDDANA | EXTINT[0]  |     |      |                           | Y[6]        |                               |                    | TC3/WO[0]      |                |                      |              | CCL0/<br>IN[1]  |
|          |                                | 62       | PB01    | VDDANA | EXTINT[1]  |     |      |                           | Y[7]        |                               |                    | TC3/WO[1]      |                |                      |              | CCL0/<br>IN[2]  |
|          | 47                             | 63       | PB02    | VDDANA | EXTINT[2]  |     |      |                           | Y[8]        |                               |                    | TC2/WO[0]      |                |                      |              | CCL0/<br>OUT[0] |
|          | 48                             | 64       | PB03    | VDDANA | EXTINT[3]  |     |      |                           | Y[9]        |                               |                    | TC2/WO[1]      |                |                      |              |                 |

1. Use the SAM C21J pinout muxing for the WLCSP56 package.
2. All analog pin functions are on peripheral function B. Peripheral function B must be selected to disable the digital control of the pin.
3. Only some pins can be used in SERCOM I2C mode. Refer to [SERCOM I2C Pins](#).

#### Related Links

[SERCOM I2C Pins](#) on page 23

## 7.2. Other Functions

### 7.2.1. Oscillator Pinout

The oscillators are not mapped to the normal PORT functions and their multiplexing are controlled by registers in the Oscillators Controller (OSCCTRL) and in the 32K Oscillators Controller (OSC32KCTRL).

**Table 7-2. Oscillator Pinout**

| Oscillator | Supply | Signal | I/O pin |
|------------|--------|--------|---------|
| XOSC       | VDDIO  | XIN    | PA14    |
|            |        | XOUT   | PA15    |

| Oscillator | Supply | Signal | I/O pin |
|------------|--------|--------|---------|
| XOSC32K    | VDDANA | XIN32  | PA00    |
|            |        | XOUT32 | PA01    |

### 7.2.2. Serial Wire Debug Interface Pinout

Only the SWCLK pin is mapped to the normal PORT functions. A debugger cold-plugging or hot-plugging detection will automatically switch the SWDIO port to the SWDIO function.

**Table 7-3. Serial Wire Debug Interface Pinout**

| Signal | Supply | I/O pin |
|--------|--------|---------|
| SWCLK  | VDDIN  | PA30    |
| SWDIO  | VDDIN  | PA31    |

### 7.2.3. SERCOM I<sup>2</sup>C Pins

**Table 7-4. SERCOM Pins Supporting I<sup>2</sup>C**

| Device   | Pins Supporting I <sup>2</sup> C Hs mode                                                                   |
|----------|------------------------------------------------------------------------------------------------------------|
| SAM C20E | PA08, PA09, PA10, PA11, PA16, PA17, PA22, PA23                                                             |
| SAM C20G | PA08, PA09, PA10, PA11, PA12, PA13, PA16, PA17, PA22, PA23, PB10, PB11                                     |
| SAM C20J | PA08, PA09, PA10, PA11, PA12, PA13, PA16, PA17, PA22, PA23, PB10, PB11, PB12, PB13, PB16, PB17, PB30, PB31 |

### 7.2.4. GPIO Clusters

**Table 7-5. GPIO Clusters**

| Package | Cluster | GPIO                                                                                            | Supplies Pin connected to the cluster |             |
|---------|---------|-------------------------------------------------------------------------------------------------|---------------------------------------|-------------|
| 64 pins | 1       | PB31 PB30 PA31 PA30 PA28 PA27                                                                   | VDDIN (56)                            | GND (54)    |
|         | 2       | PB23 PB22                                                                                       | VDDIO (48)                            | GND (54+47) |
|         | 3       | PA25 PA24 PA23 PA22 PA21 PA20 PB17<br>PB16 PA19 PA18 PA17 PA16                                  | VDDIO (48+34)                         | GND (47+33) |
|         | 4       | PA15 PA14 PA13 PA12 PB15 PB14 PB13<br>PB12 PB11 PB10                                            | VDDIO (34+21)                         | GND (33+22) |
|         | 5       | PA11 PA10 PA08 PA09                                                                             | VDDIO (21)                            | GND (22)    |
|         | 6       | PA07 PA06 PA05 PA04 PB09 PB08 PB07<br>PB06 PB05 PB04 PA03 PA02 PA01 PA00<br>PB03 PB02 PB01 PB00 | VDDANA (8)                            | GNDANA (7)  |

| Package | Cluster | GPIO                                                                                  | Supplies Pin connected to the cluster |             |
|---------|---------|---------------------------------------------------------------------------------------|---------------------------------------|-------------|
| 48 pins | 1       | PA31 PA30 PA28 PA27                                                                   | VDDIN (44)                            | GND (42)    |
|         | 2       | PB23 PB22                                                                             | VDDIO (36)                            | GND (42+35) |
|         | 3       | PA25 PA24 PA23 PA22 PA21 PA20 PA19<br>PA18 PA17 PA16 PA15 PA14 PA13 PA12<br>PB11 PB10 | VDDIO (36+17)                         | GND (35+18) |
|         | 4       | PA11 PA10 PA08 PA09                                                                   | VDDIO (17)                            | GND (18)    |
|         | 5       | PA07 PA06 PA05 PA04 PB09 PB08 PA03<br>PA02 PA01 PA00 PB03 PB02                        | VDDANA (6)                            | GNDANA (5)  |
| 32 pins | 1       | PA31 PA30 PA28 PA27                                                                   | VDDIN (30)                            | GND (28)    |
|         | 2       | PA25 PA24 PA23 PA22 PA19 PA18 PA17<br>PA16 PA15 PA14 PA11 PA10 PA08 PA09              | VDDIO (9)                             | GND (28+10) |
|         | 3       | PA07 PA06 PA05 PA04 PA03 PA02 PA01<br>PA00                                            | VDDANA (9)                            | GND (28+10) |

### 7.2.5. TCC Configurations

The SAM C20 has one instance of the Timer/Counter for Control applications (TCC) peripheral, . The following table lists the features for each TCC instance.

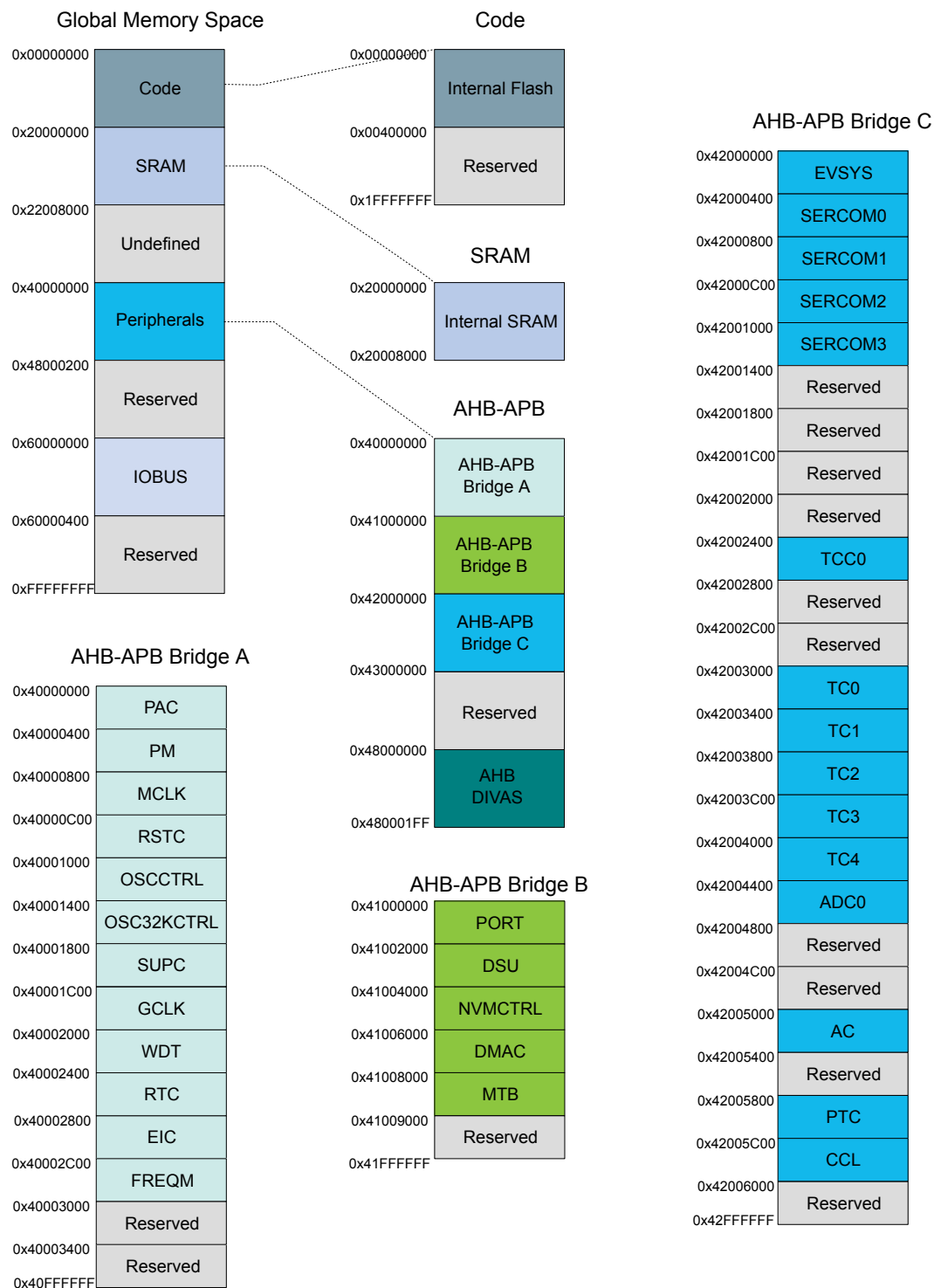
**Table 7-6. TCC Configuration Summary**

| TCC# | Channels (CC_NUM) | Waveform Output (WO_NUM) | Counter size | Fault | Dithering | Output matrix | Dead Time Insertion (DTI) | SWAP | Pattern generation |
|------|-------------------|--------------------------|--------------|-------|-----------|---------------|---------------------------|------|--------------------|
| 0    | 4                 | 8                        | 24-bit       | Yes   | Yes       | Yes           | Yes                       | Yes  | Yes                |

**Note:** The number of CC registers (CC\_NUM) for each TCC corresponds to the number of compare/capture channels, so that a TCC can have more Waveform Outputs (WO\_NUM) than CC registers.

## 8. Product Mapping

Figure 8-1. SAM C20 Product Mapping



## 9. Processor and Architecture

### 9.1. Cortex M0+ Processor

The Atmel SAM C20 implements the ARM® Cortex™-M0+ processor, based on the ARMv6 Architecture and Thumb®-2 ISA. The Cortex M0+ is 100% instruction set compatible with its predecessor, the Cortex-M0 core, and upward compatible to Cortex-M3 and M4 cores. The implemented ARM Cortex-M0+ is revision r0p1. For more information refer to <http://www.arm.com>.

#### 9.1.1. Cortex M0+ Configuration

**Table 9-1. Cortex M0+ Configuration**

| Features                         | Cortex-M0+ options           | SAM C20 configuration |
|----------------------------------|------------------------------|-----------------------|
| Interrupts                       | External interrupts 0-32     | 32                    |
| Data endianness                  | Little-endian or big-endian  | Little-endian         |
| SysTick timer                    | Present or absent            | Present               |
| Number of watchpoint comparators | 0, 1, 2                      | 2                     |
| Number of breakpoint comparators | 0, 1, 2, 3, 4                | 4                     |
| Halting debug support            | Present or absent            | Present               |
| Multiplier                       | Fast or small                | Fast (single cycle)   |
| Single-cycle I/O port            | Present or absent            | Present               |
| Wake-up interrupt controller     | Supported or not supported   | Not supported         |
| Vector Table Offset Register     | Present or absent            | Present               |
| Unprivileged/Privileged support  | Present or absent            | Present               |
| Memory Protection Unit           | Not present or 8-region      | 8-region              |
| Reset all registers              | Present or absent            | Absent                |
| Instruction fetch width          | 16-bit only or mostly 32-bit | 32-bit                |

The ARM Cortex-M0+ core has two bus interfaces:

- Single 32-bit AMBA-3 AHB-Lite system interface that provides connections to peripherals and all system memory, which includes flash and RAM.
- Single 32-bit I/O port bus interfacing to the PORT and DIVAS with 1-cycle loads and stores.

#### 9.1.2. Cortex-M0+ Peripherals

- System Control Space (SCS)
  - The processor provides debug through registers in the SCS. Refer to the Cortex-M0+ Technical Reference Manual for details (<http://www.arm.com>).
- Nested Vectored Interrupt Controller (NVIC)
  - External interrupt signals connect to the NVIC, and the NVIC prioritizes the interrupts. Software can set the priority of each interrupt. The NVIC and the Cortex-M0+ processor core are closely coupled, providing low latency interrupt processing and efficient processing of late

arriving interrupts. Refer to [Nested Vector Interrupt Controller](#) and the Cortex-M0+ Technical Reference Manual for details (<http://www.arm.com>).

- System Timer (SysTick)
  - The System Timer is a 24-bit timer clocked by CLK\_CPU that extends the functionality of both the processor and the NVIC. Refer to the Cortex-M0+ Technical Reference Manual for details (<http://www.arm.com>).
- System Control Block (SCB)
  - The System Control Block provides system implementation information, and system control. This includes configuration, control, and reporting of the system exceptions. Refer to the Cortex-M0+ Devices Generic User Guide for details (<http://www.arm.com>).
- Micro Trace Buffer (MTB)
  - The CoreSight MTB-M0+ (MTB) provides a simple execution trace capability to the Cortex-M0+ processor. Refer to section [Micro Trace Buffer](#) and the CoreSight MTB-M0+ Technical Reference Manual for details (<http://www.arm.com>).
- Memory Protection Unit (MPU)
  - The Memory Protection Unit divides the memory map into a number of regions, and defines the location, size, access permissions and memory attributes of each region. Refer to the Cortex-M0+ Devices Generic User Guide for details (<http://www.arm.com>).

### 9.1.3. Cortex-M0+ Address Map

Table 9-2. Cortex-M0+ Address Map

| Address    | Peripheral                                  |
|------------|---------------------------------------------|
| 0xE000E000 | System Control Space (SCS)                  |
| 0xE000E010 | System Timer (SysTick)                      |
| 0xE000E100 | Nested Vectored Interrupt Controller (NVIC) |
| 0xE000ED00 | System Control Block (SCB)                  |
| 0x41008000 | Micro Trace Buffer (MTB)                    |

#### Related Links

[Product Mapping](#) on page 25

### 9.1.4. I/O Interface

#### 9.1.4.1. Overview

Because accesses to the AMBA® AHB-Lite™ and the single cycle I/O interface can be made concurrently, the Cortex-M0+ processor can fetch the next instructions while accessing the I/Os. This enables single cycle I/O accesses to be sustained for as long as needed.

#### 9.1.4.2. Description

Direct access to PORT registers and DIVAS registers.

## 9.2. Nested Vector Interrupt Controller

### 9.2.1. Overview

The Nested Vectored Interrupt Controller (NVIC) in the SAM C20 supports 32 interrupt lines with four different priority levels. For more details, refer to the Cortex-M0+ Technical Reference Manual (<http://www.arm.com>).

### 9.2.2. Interrupt Line Mapping

Each of the interrupt lines is connected to one peripheral instance, as shown in the table below. Each peripheral can have one or more interrupt flags, located in the peripheral's Interrupt Flag Status and Clear (INTFLAG) register.

The interrupt flag is set when the interrupt condition occurs. Each interrupt in the peripheral can be individually enabled by writing a one to the corresponding bit in the peripheral's Interrupt Enable Set (INTENSET) register, and disabled by writing a one to the corresponding bit in the peripheral's Interrupt Enable Clear (INTENCLR) register.

An interrupt request is generated from the peripheral when the interrupt flag is set and the corresponding interrupt is enabled.

The interrupt requests for one peripheral are ORed together on system level, generating one interrupt request for each peripheral. An interrupt request will set the corresponding interrupt pending bit in the NVIC interrupt pending registers (SETPEND/CLRPEND bits in ISPR/ICPR).

For the NVIC to activate the interrupt, it must be enabled in the NVIC interrupt enable register (SETENA/CLRENA bits in ISER/ICER). The NVIC interrupt priority registers IPR0-IPR7 provide a priority field for each interrupt.

**Table 9-3. Interrupt Line Mapping**

| Peripheral Source                                                                                                                                                                          | NVIC Line |
|--------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|-----------|
| EIC NMI – External Interrupt Controller                                                                                                                                                    | NMI       |
| PM – Power Manager<br>MCLK - Main Clock<br>OSCCTRL - Oscillators Controller<br>OSC32KCTRL - 32kHz Oscillators Controller<br>SUPC - Supply Controller<br>PAC - Protection Access Controller | 0         |
| WDT – Watchdog Timer                                                                                                                                                                       | 1         |
| RTC – Real Time Clock                                                                                                                                                                      | 2         |
| EIC – External Interrupt Controller                                                                                                                                                        | 3         |
| FREQM – Frequency Meter                                                                                                                                                                    | 4         |
| Reserved                                                                                                                                                                                   | 5         |
| NVMCTRL – Non-Volatile Memory Controller                                                                                                                                                   | 6         |
| DMAC - Direct Memory Access Controller                                                                                                                                                     | 7         |
| EVSYS – Event System                                                                                                                                                                       | 8         |
| SERCOM0 – Serial Communication Controller 0                                                                                                                                                | 9         |
| SERCOM1 – Serial Communication Controller 1                                                                                                                                                | 10        |
| SERCOM2 – Serial Communication Controller 2                                                                                                                                                | 11        |
| SERCOM3 – Serial Communication Controller 3                                                                                                                                                | 12        |

| Peripheral Source                    | NVIC Line |
|--------------------------------------|-----------|
| Reserved                             | 13        |
| Reserved                             | 14        |
| Reserved                             | 15        |
| Reserved                             | 16        |
| TCC0 – Timer Counter for Control 0   | 17        |
| Reserved                             | 18        |
| Reserved                             | 19        |
| TC0 – Timer Counter 0                | 20        |
| TC1 – Timer Counter 1                | 21        |
| TC2 – Timer Counter 2                | 22        |
|                                      | 23        |
|                                      | 24        |
| ADC0 – Analog-to-Digital Converter 0 | 25        |
| Reserved                             | 26        |
| AC – Analog Comparator               | 27        |
| Reserved                             | 28        |
| Reserved                             | 29        |
| PTC – Peripheral Touch Controller    | 30        |
| Reserved                             | 31        |

## 9.3. Micro Trace Buffer

### 9.3.1. Features

- Program flow tracing for the Cortex-M0+ processor
- MTB SRAM can be used for both trace and general purpose storage by the processor
- The position and size of the trace buffer in SRAM is configurable by software
- CoreSight compliant

### 9.3.2. Overview

When enabled, the MTB records changes in program flow, reported by the Cortex-M0+ processor over the execution trace interface shared between the Cortex-M0+ processor and the CoreSight MTB-M0+. This information is stored as trace packets in the SRAM by the MTB. An off-chip debugger can extract the trace information using the Debug Access Port to read the trace information from the SRAM. The debugger can then reconstruct the program flow from this information.

The MTB simultaneously stores trace information into the SRAM, and gives the processor access to the SRAM. The MTB ensures that trace write accesses have priority over processor accesses.

The execution trace packet consists of a pair of 32-bit words that the MTB generates when it detects the processor PC value changes non-sequentially. A non-sequential PC change can occur during branch instructions or during exception entry. See the CoreSight MTB-M0+ Technical Reference Manual for more details on the MTB execution trace packet format.

Tracing is enabled when the MASTER.EN bit in the Master Trace Control Register is 1. There are various ways to set the bit to 1 to start tracing, or to 0 to stop tracing. See the CoreSight Cortex-M0+ Technical Reference Manual for more details on the Trace start and stop and for a detailed description of the MTB's MASTER register. The MTB can be programmed to stop tracing automatically when the memory fills to a specified watermark level or to start or stop tracing by writing directly to the MASTER.EN bit. If the watermark mechanism is not being used and the trace buffer overflows, then the buffer wraps around overwriting previous trace packets.

The base address of the MTB registers is 0x41008000; this address is also written in the CoreSight ROM Table. The offset of each register from the base address is fixed and as defined by the CoreSight MTB-M0+ Technical Reference Manual. The MTB has 4 programmable registers to control the behavior of the trace features:

- POSITION: Contains the trace write pointer and the wrap bit,
- MASTER: Contains the main trace enable bit and other trace control fields,
- FLOW: Contains the WATERMARK address and the AUTOSTOP and AUTOHALT control bits,
- BASE: Indicates where the SRAM is located in the processor memory map. This register is provided to enable auto discovery of the MTB SRAM location, by a debug agent.

See the CoreSight MTB-M0+ Technical Reference Manual for a detailed description of these registers.

## 9.4. High-Speed Bus System

### 9.4.1. Features

High-Speed Bus Matrix has the following features:

- Symmetric crossbar bus switch implementation
- Allows concurrent accesses from different masters to different slaves
- 32-bit data bus
- Operation at a 1-to-1 clock frequency with the bus masters

## 9.4.2. Configuration

Figure 9-1. Master-Slave Relation High-Speed Bus Matrix

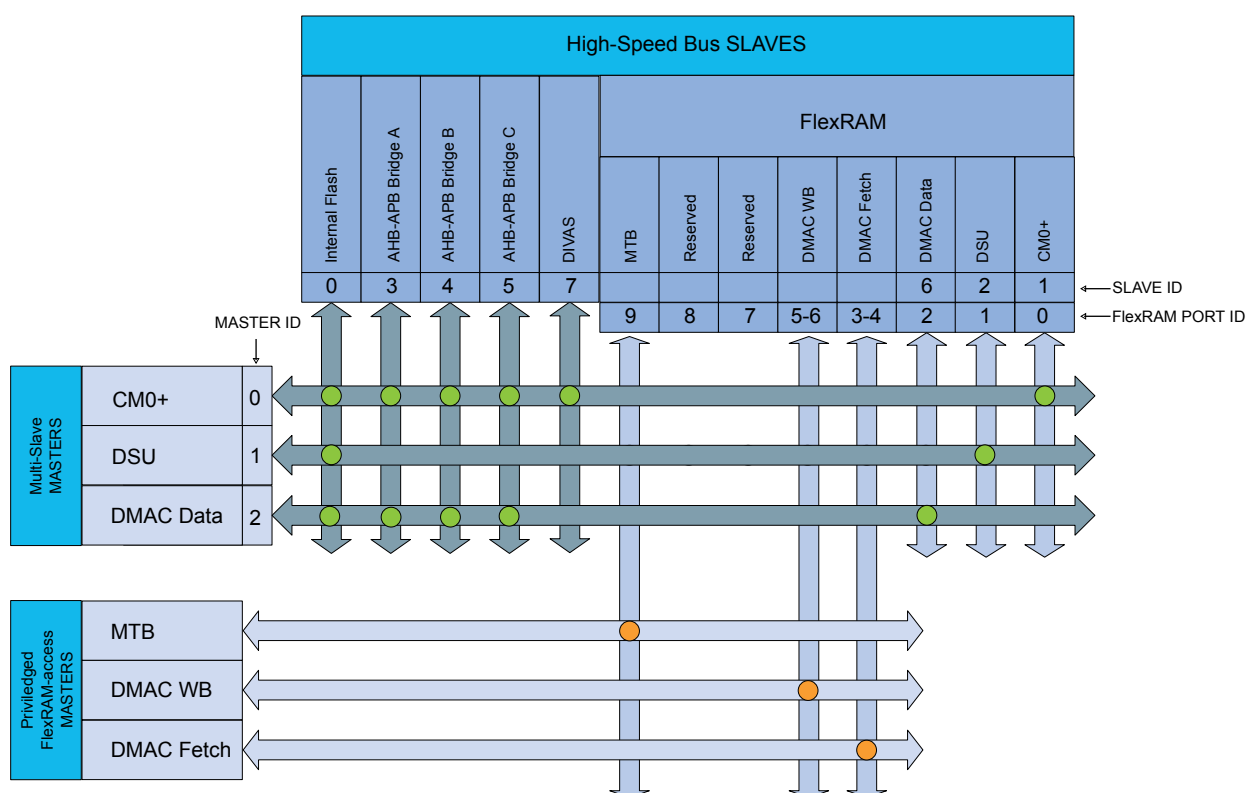


Table 9-4. Bus Matrix Masters

| Bus Matrix Masters                                   | Master ID |
|------------------------------------------------------|-----------|
| CM0+ - Cortex M0+ Processor                          | 0         |
| DSU - Device Service Unit                            | 1         |
| DMAC - Direct Memory Access Controller / Data Access | 2         |

Table 9-5. Bus Matrix Slaves

| Bus Matrix Slaves              | Slave ID |
|--------------------------------|----------|
| Internal Flash Memory          | 0        |
| SRAM Port 4 - CM0+ Access      | 1        |
| SRAM Port 6 - DSU Access       | 2        |
| AHB-APB Bridge A               | 3        |
| AHB-APB Bridge B               | 4        |
| AHB-APB Bridge C               | 5        |
| SRAM Port 5 - DMAC Data Access | 6        |
| DIVAS - Divide Accelerator     | 7        |

**Table 9-6. SRAM Port Connections**

| SRAM Port Connection                                         | Port ID | Connection Type |
|--------------------------------------------------------------|---------|-----------------|
| CM0+ - Cortex M0+ Processor                                  | 0       | Bus Matrix      |
| DSU - Device Service Unit                                    | 1       | Bus Matrix      |
| DMAC - Direct Memory Access Controller - Data Access         | 2       | Bus Matrix      |
| DMAC - Direct Memory Access Controller - Fetch Access 0      | 3       | Direct          |
| DMAC - Direct Memory Access Controller - Fetch Access 1      | 4       | Direct          |
| DMAC - Direct Memory Access Controller - Write-Back Access 0 | 5       | Direct          |
| DMAC - Direct Memory Access Controller - Write-Back Access 1 | 6       | Direct          |
| Reserved                                                     | 7       | Direct          |
| Reserved                                                     | 8       | Direct          |
| MTB - Micro Trace Buffer                                     | 9       | Direct          |

#### 9.4.3. SRAM Quality of Service

To ensure that masters with latency requirements get sufficient priority when accessing RAM, the different masters can be configured to have a given priority for different type of access.

The Quality of Service (QoS) level is independently selected for each master accessing the RAM. For any access to the RAM the RAM also receives the QoS level. The QoS levels and their corresponding bit values for the QoS level configuration is shown in below.

**Table 9-7. Quality of Service Level Configuration**

| Value | Name    | Description                         |
|-------|---------|-------------------------------------|
| 0x0   | DISABLE | Background (no sensitive operation) |
| 0x1   | LOW     | Sensitive Bandwidth                 |
| 0x2   | MEDIUM  | Sensitive Latency                   |
| 0x3   | HIGH    | Critical Latency                    |

If a master is configured with QoS level DISABLE (0x0) or LOW (0x1) there will be minimum latency of one cycle for the RAM access.

The priority order for concurrent accesses are decided by two factors. First, the QoS level for the master and second, a static priority given by [Table 9-6](#). The lowest port ID has the highest static priority.

The MTB has fixed QoS level HIGH (0x3) and the DSU has fixed QoS level LOW (0x1).

The CPU QoS level can be written/read at address 0x41007110, bits [1:0]. Its reset value is 0x0.

Refer to different master QOSCTRL registers for configuring QoS for the other masters (DMAC).

## 10. Packaging Information

### 10.1. Thermal Considerations

#### 10.1.1. Thermal Resistance Data

The following table summarizes the thermal resistance data depending on the package.

**Table 10-1. Thermal Resistance Data**

| Package Type  | $\theta_{JA}$ | $\theta_{JC}$ |
|---------------|---------------|---------------|
| 32-pin TQFP   | 68°C/W        | 25.8°C/W      |
| 48-pin TQFP   | 78.8°C/W      | 12.3°C/W      |
| 64-pin TQFP   | 66.7°C/W      | 11.9°C/W      |
| 32-pin QFN    | 37.2°C/W      | 3.1°C/W       |
| 48-pin QFN    | 31.6°C/W      | 10.3°C/W      |
| 64-pin QFN    | 32.2°C/W      | 10.1°C/W      |
| 56-ball WLCSP | 37.5°C/W      | 5.48°C/W      |

#### 10.1.2. Junction Temperature

The average chip-junction temperature,  $T_J$ , in °C can be obtained from the following:

1.  $T_J = T_A + (P_D \times \theta_{JA})$
2.  $T_J = T_A + (P_D \times (\theta_{HEATSINK} + \theta_{JC}))$

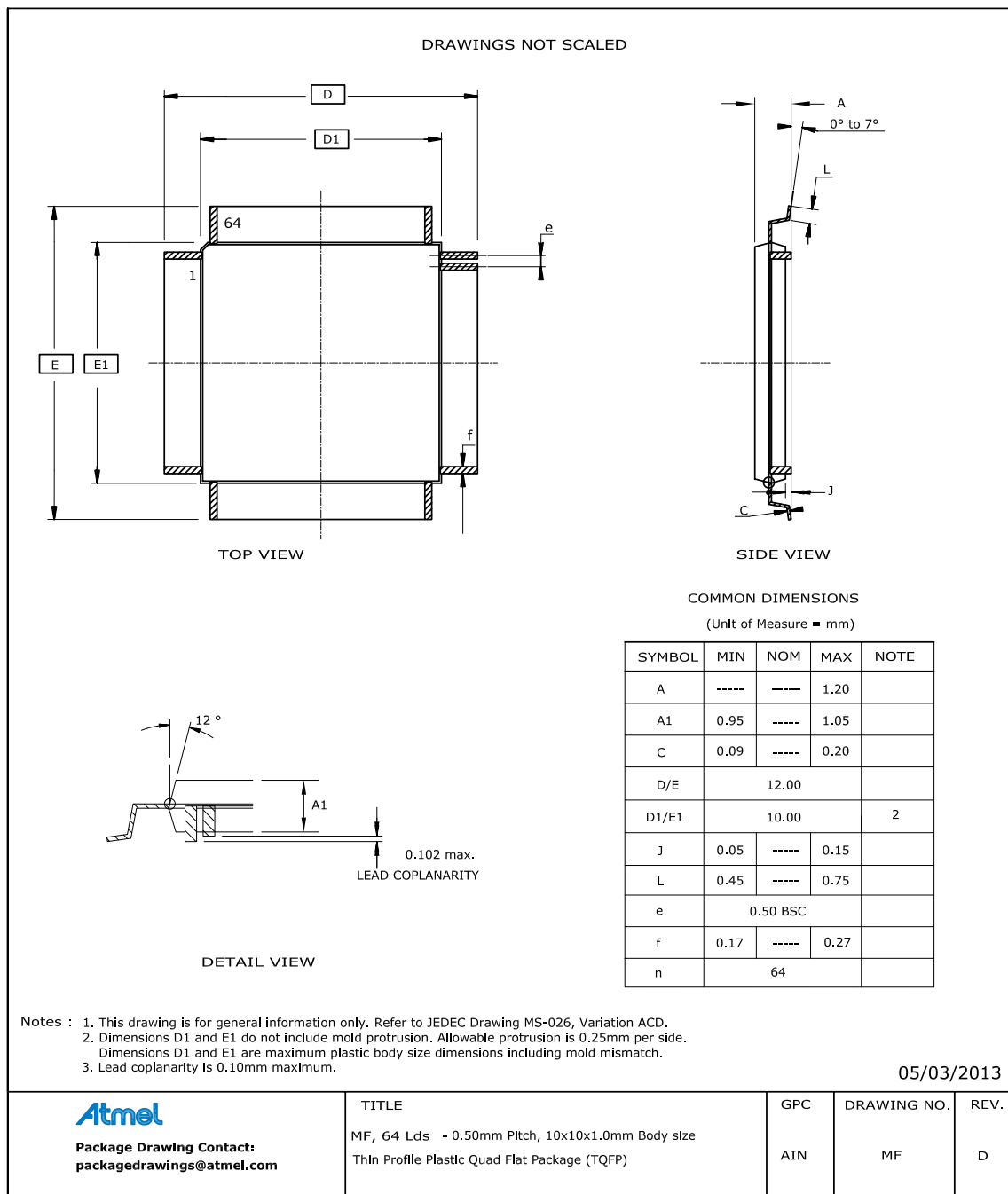
where:

- $\theta_{JA}$  = Package thermal resistance, Junction-to-ambient (°C/W), see Thermal Resistance Data
- $\theta_{JC}$  = Package thermal resistance, Junction-to-case thermal resistance (°C/W), see Thermal Resistance Data
- $\theta_{HEATSINK}$  = Thermal resistance (°C/W) specification of the external cooling device
- $P_D$  = Device power consumption (W)
- $T_A$  = Ambient temperature (°C)

From the first equation, the user can derive the estimated lifetime of the chip and decide if a cooling device is necessary or not. If a cooling device is to be fitted on the chip, the second equation should be used to compute the resulting average chip-junction temperature  $T_J$  in °C.

## 10.2. Package Drawings

### 10.2.1. 64 pin TQFP



**Table 10-2. Device and Package Maximum Weight**

|     |    |
|-----|----|
| 300 | mg |
|-----|----|

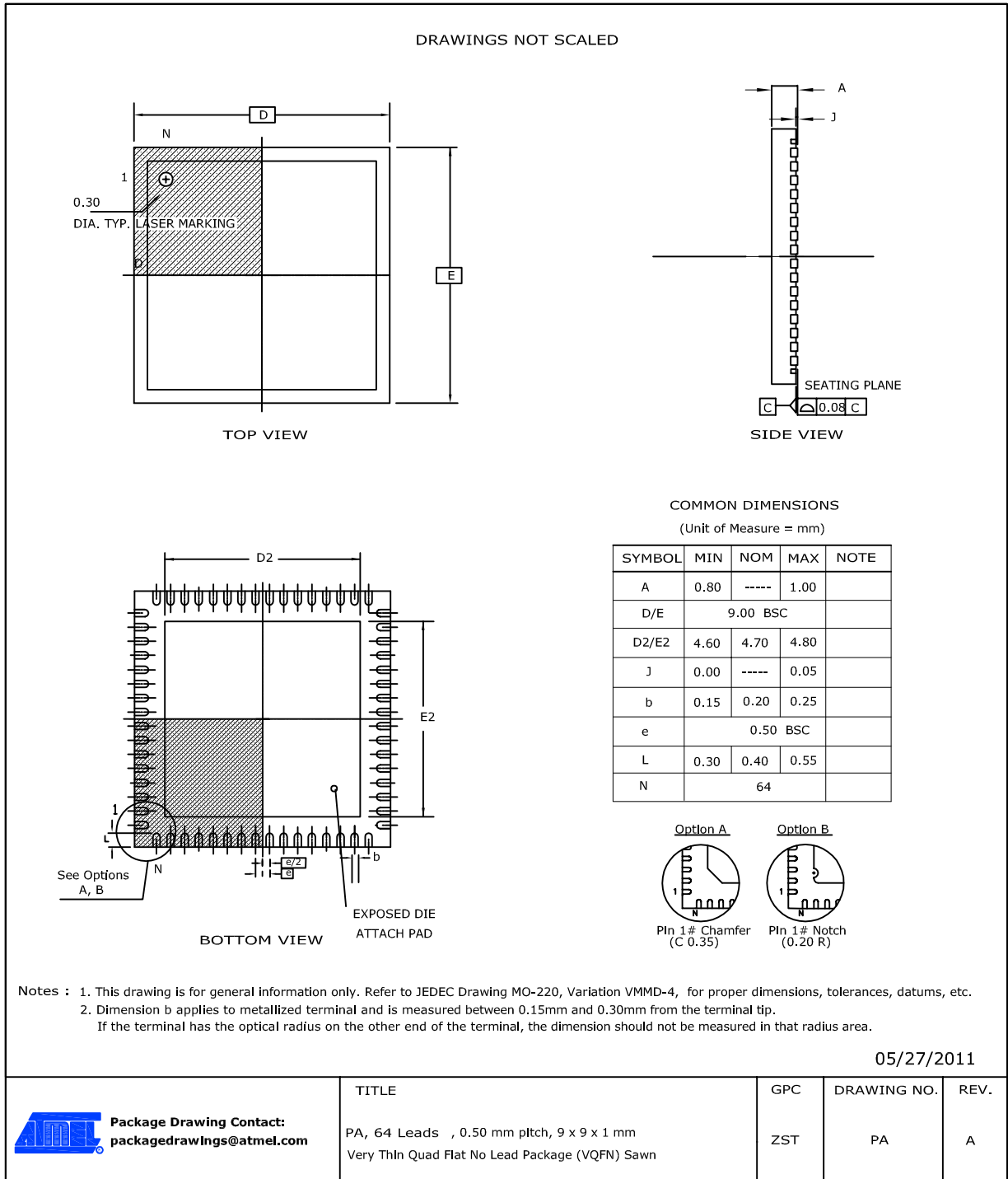
**Table 10-3. Package Characteristics**

|                            |      |
|----------------------------|------|
| Moisture Sensitivity Level | MSL3 |
|----------------------------|------|

**Table 10-4. Package Reference**

|                         |        |
|-------------------------|--------|
| JEDEC Drawing Reference | MS-026 |
| JESD97 Classification   | E3     |

## 10.2.2. 64 pin QFN



**Note:** The exposed die attach pad is not connected electrically inside the device.

**Table 10-5. Device and Package Maximum Weight**

|     |    |
|-----|----|
| 200 | mg |
|-----|----|

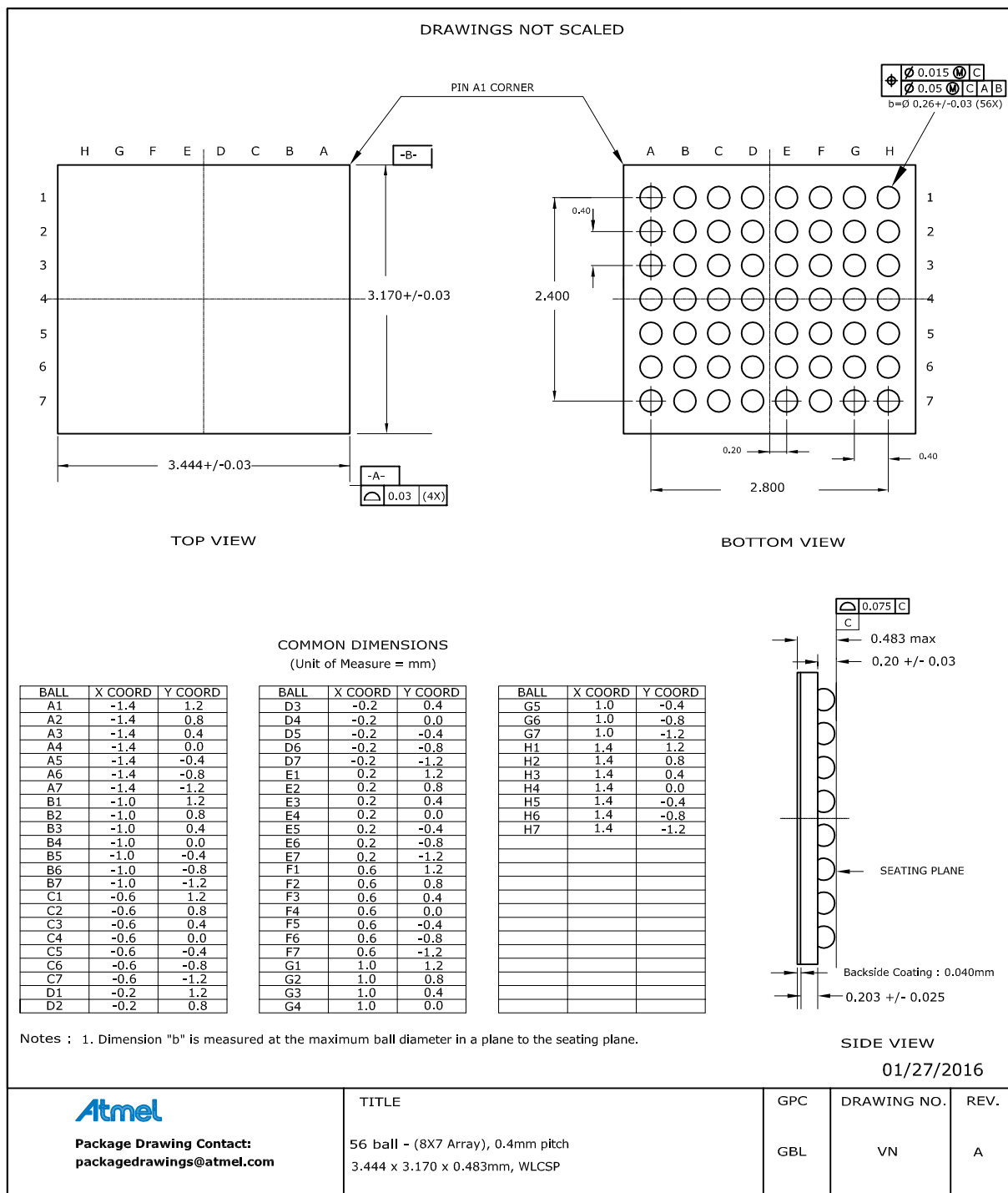
**Table 10-6. Package Characteristics**

|                            |      |
|----------------------------|------|
| Moisture Sensitivity Level | MSL3 |
|----------------------------|------|

**Table 10-7. Package Reference**

|                         |        |
|-------------------------|--------|
| JEDEC Drawing Reference | MO-220 |
| JESD97 Classification   | E3     |

### 10.2.3. 56-Ball WLCSP



**Table 10-8. Device and Package Maximum Weight**

|      |    |
|------|----|
| 9.63 | mg |
|------|----|

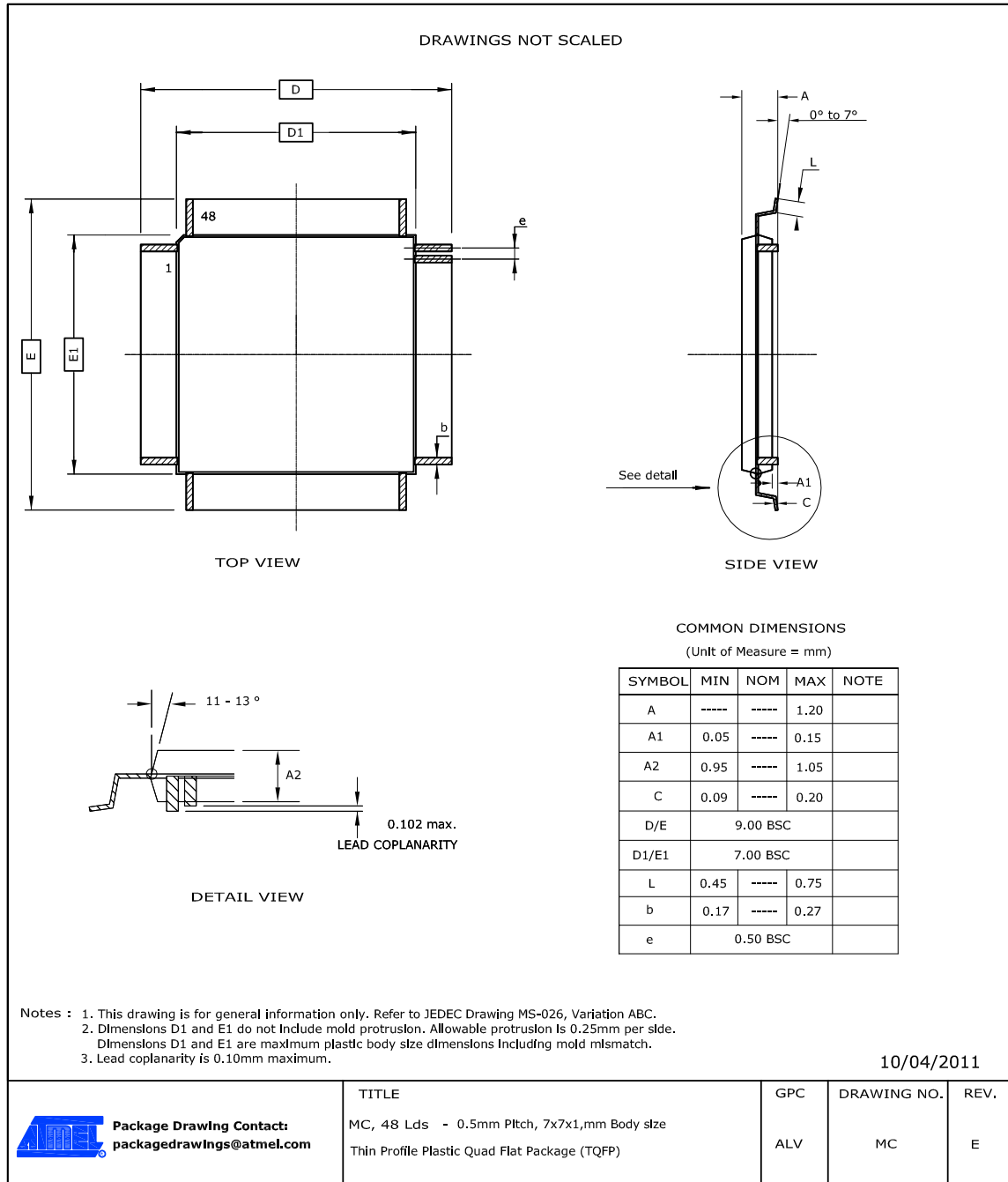
**Table 10-9. Package Characteristics**

|                            |      |
|----------------------------|------|
| Moisture Sensitivity Level | MSL1 |
|----------------------------|------|

**Table 10-10. Package Reference**

|                         |     |
|-------------------------|-----|
| JEDEC Drawing Reference | N/A |
| JESD97 Classification   | e1  |

#### 10.2.4. 48 pin TQFP



**Table 10-11. Device and Package Maximum Weight**

|     |    |
|-----|----|
| 140 | mg |
|-----|----|

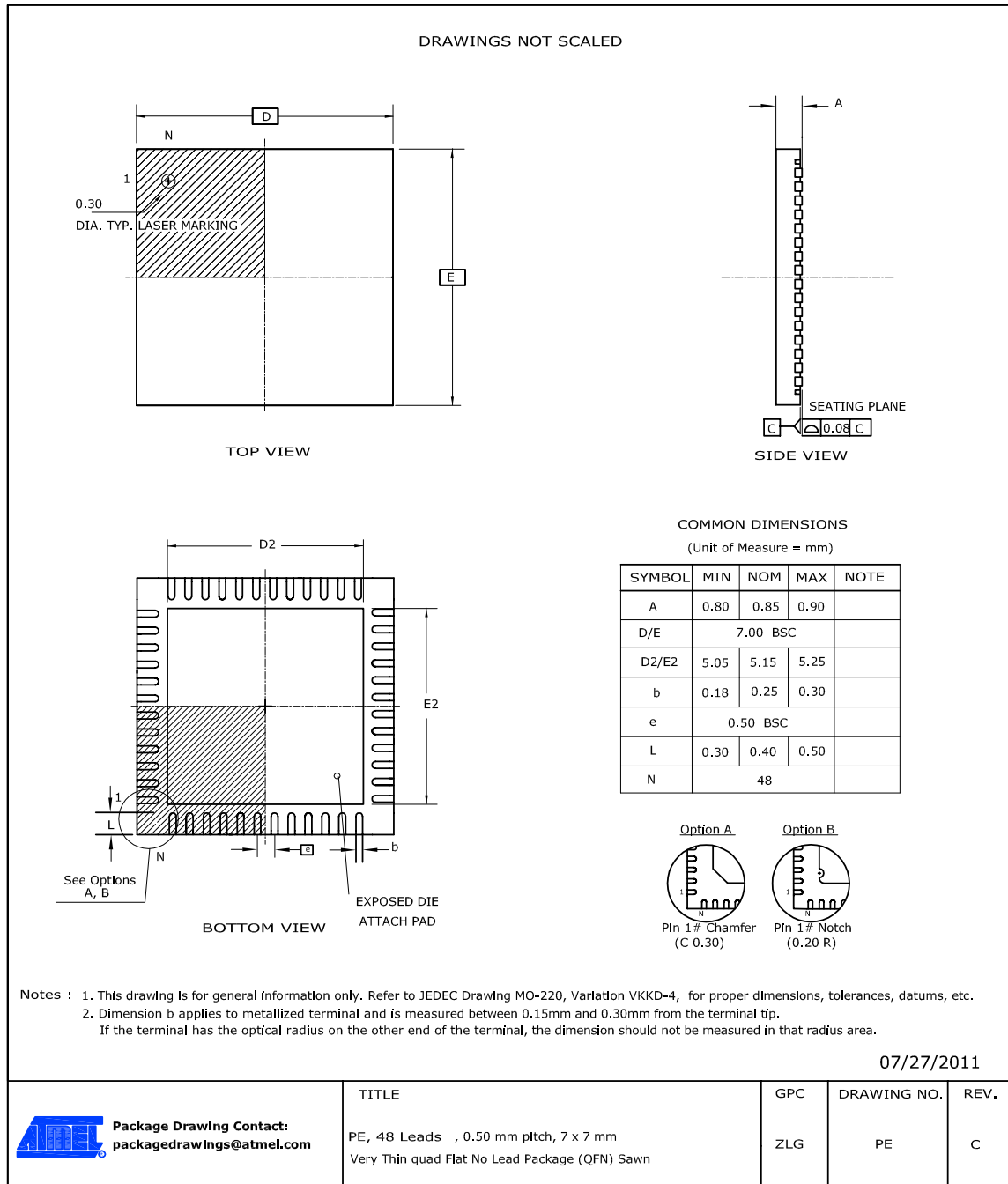
**Table 10-12. Package Characteristics**

|                            |      |
|----------------------------|------|
| Moisture Sensitivity Level | MSL3 |
|----------------------------|------|

**Table 10-13. Package Reference**

|                         |        |
|-------------------------|--------|
| JEDEC Drawing Reference | MS-026 |
| JESD97 Classification   | E3     |

### 10.2.5. 48 pin QFN



**Note:** The exposed die attach pad is not connected electrically inside the device.

**Table 10-14. Device and Package Maximum Weight**

|     |    |
|-----|----|
| 140 | mg |
|-----|----|

**Table 10-15. Package Characteristics**

|                            |      |
|----------------------------|------|
| Moisture Sensitivity Level | MSL3 |
|----------------------------|------|

**Table 10-16. Package Reference**

|                         |        |
|-------------------------|--------|
| JEDEC Drawing Reference | MO-220 |
| JESD97 Classification   | E3     |

10.2.6. 32 pin TQFP

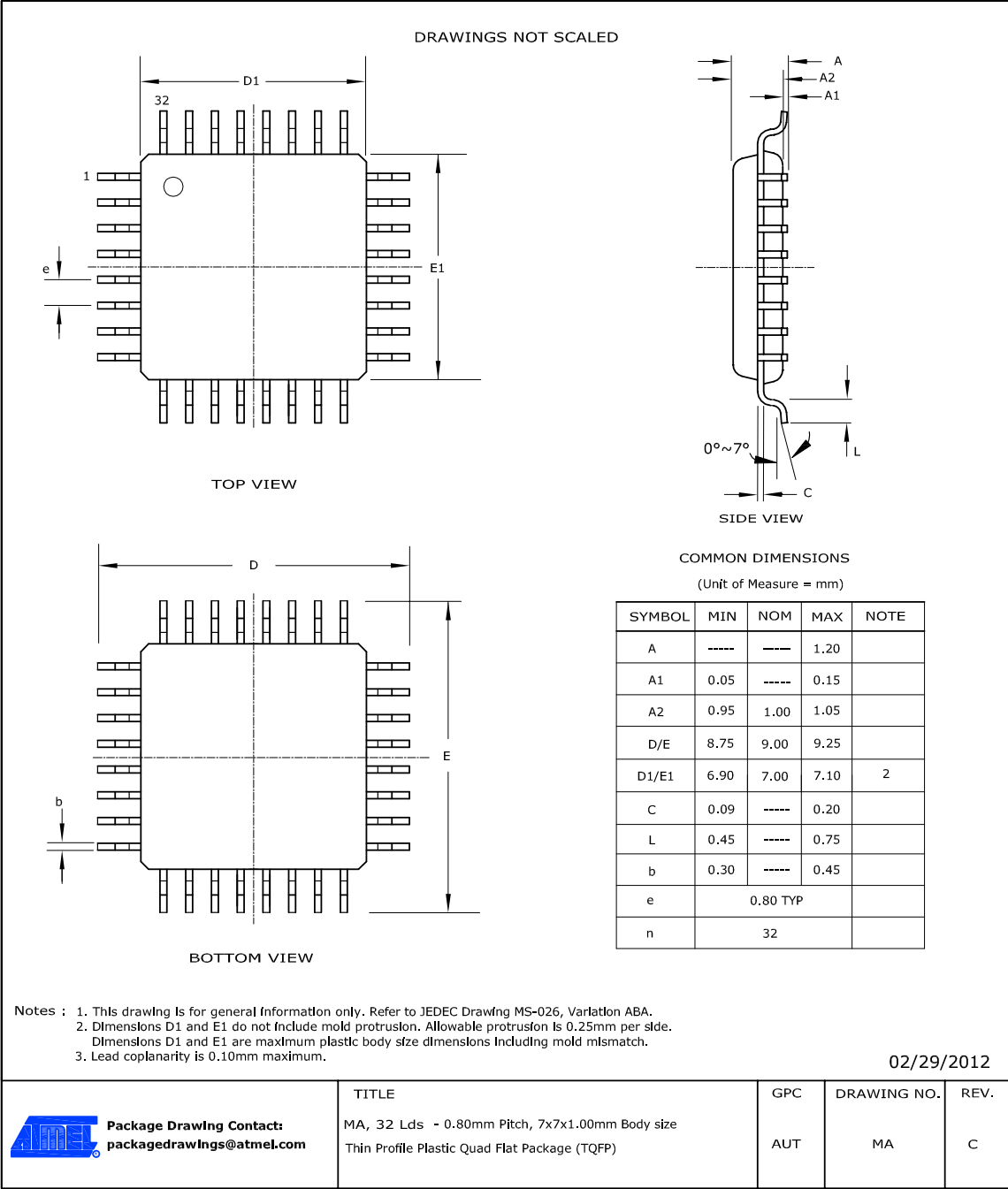


Table 10-17. Device and Package Maximum Weight

|     |    |
|-----|----|
| 100 | mg |
|-----|----|

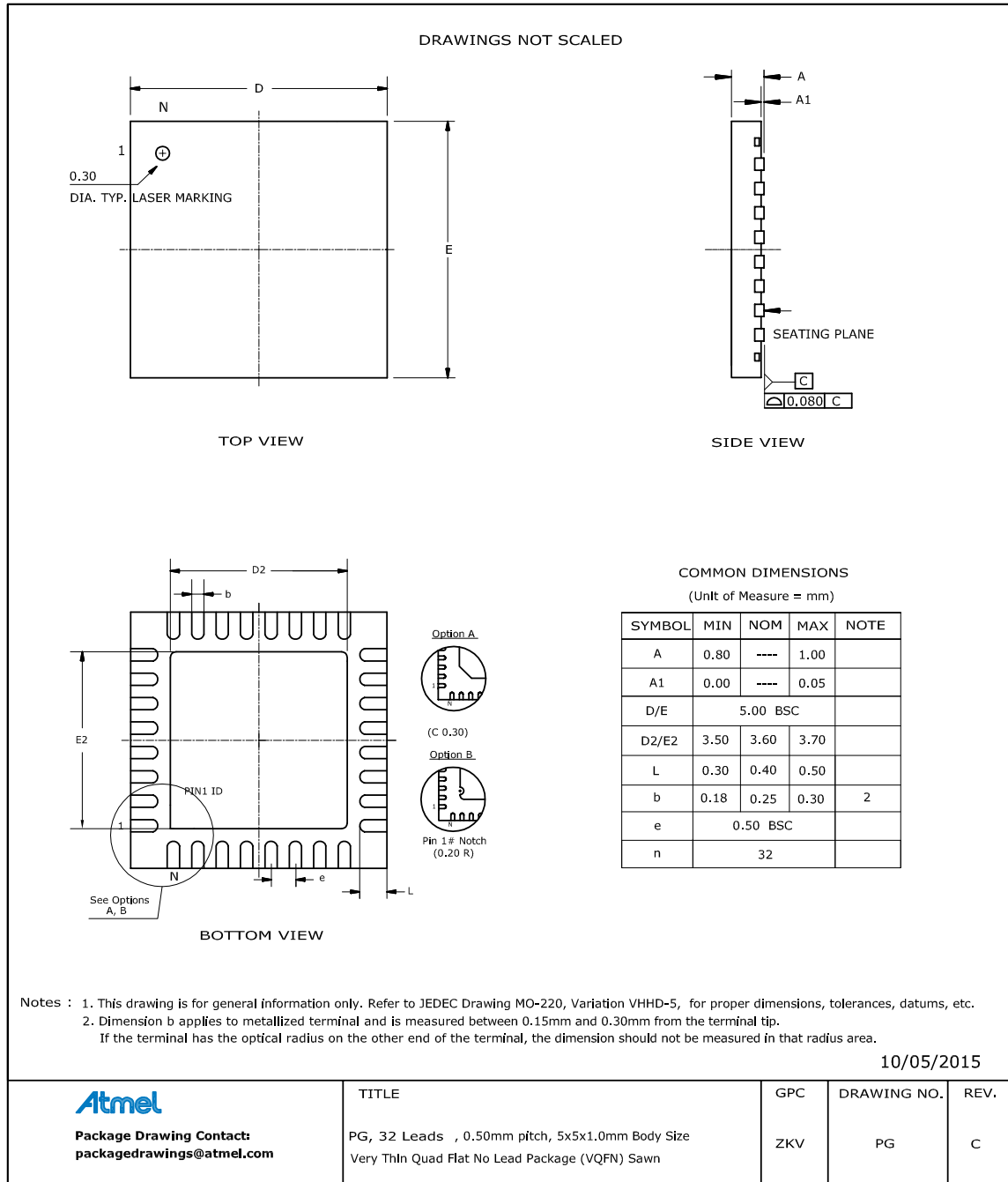
Table 10-18. Package Characteristics

|                            |      |
|----------------------------|------|
| Moisture Sensitivity Level | MSL3 |
|----------------------------|------|

**Table 10-19. Package Reference**

|                         |        |
|-------------------------|--------|
| JEDEC Drawing Reference | MS-026 |
| JESD97 Classification   | E3     |

### 10.2.7. 32 pin QFN



**Note:** The exposed die attach pad is connected inside the device to GND and GNDANA.

**Table 10-20. Device and Package Maximum Weight**

|    |    |
|----|----|
| 90 | mg |
|----|----|

**Table 10-21. Package Characteristics**

|                            |      |
|----------------------------|------|
| Moisture Sensitivity Level | MSL3 |
|----------------------------|------|

**Table 10-22. Package Reference**

|                         |        |
|-------------------------|--------|
| JEDEC Drawing Reference | MO-220 |
| JESD97 Classification   | E3     |

### 10.3. Soldering Profile

The following table gives the recommended soldering profile from J-STD-20.

**Table 10-23.**

| Profile Feature                            | Green Package  |
|--------------------------------------------|----------------|
| Average Ramp-up Rate (217°C to peak)       | 3°C/s max.     |
| Preheat Temperature 175°C ±25°C            | 150-200°C      |
| Time Maintained Above 217°C                | 60-150s        |
| Time within 5°C of Actual Peak Temperature | 30s            |
| Peak Temperature Range                     | 260°C          |
| Ramp-down Rate                             | 6°C/s max.     |
| Time 25°C to Peak Temperature              | 8 minutes max. |

A maximum of three reflow passes is allowed per component.



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