

# DATA SHEET

## **NE56605-42**

System reset with built-in watchdog timer

Product data  
Supersedes data of 2001 Apr 24  
File under Integrated Circuits, Standard Analog

2001 Aug 22

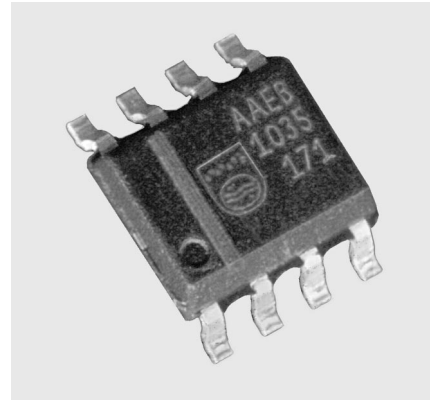
# System reset with built-in watchdog timer

# NE56605-42

## GENERAL DESCRIPTION

The NE56605-42 is designed to generate a reset signal, at a threshold voltage of 4.2 V, for a variety of microprocessor and logic systems. Accurate reset signals are generated during momentary power interruptions, or whenever power supply voltages sag to intolerable levels. The NE56605-42 has a built-in Watchdog Timer to monitor the microprocessor and ensure it is operating properly. Any abnormal system operations due to microprocessor malfunctions are terminated by the watchdog's generating a system reset. The NE56605-42 has a watchdog monitoring time of 10 ms (typical).

The NE56605-42 is offered in the SO8 surface mount package.



## FEATURES

- Both positive and negative logic reset output signals are available
- Accurate threshold detection
- Internal power-on reset delay
- Internal watchdog timer programmable with external capacitor
- Watchdog monitoring time of 10 ms
- Reset assertion with  $V_{CC}$  down to  $0.8 V_{DC}$  (typical)
- Few external components required.

## APPLICATIONS

- Microcomputer systems
- Logic systems.

## SIMPLIFIED SYSTEM DIAGRAM

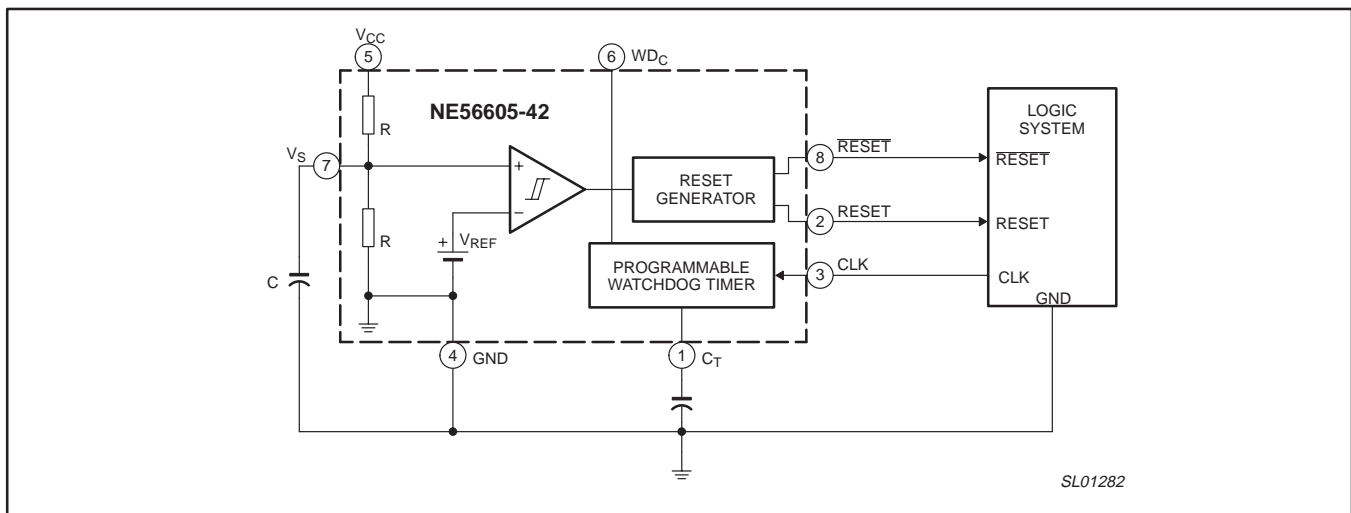


Figure 1. Simplified system diagram.

## ORDERING INFORMATION

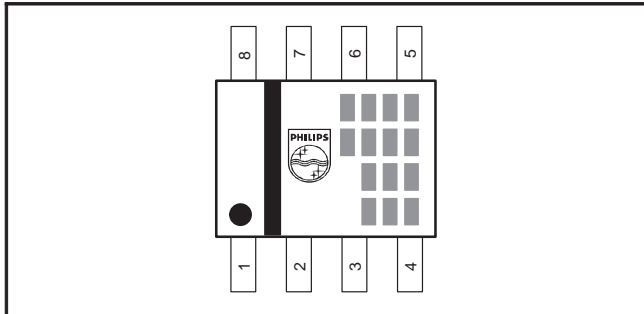
TYPE NUMBER	PACKAGE		TEMPERATURE RANGE
	NAME	DESCRIPTION	
NE56605-42D	SO8	plastic small outline package; 8 leads; body width 3.9 mm	-20 to +70 °C

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## Part number marking

The package is marked with a four letter code in the first line to the right of the logo. The first three letters designate the product. The fourth letter, represented by 'x', is a date tracking code. The remaining two or three lines of characters are internal manufacturing codes.



Part number	Marking
NE56605-42	AAE x

## PIN CONFIGURATION

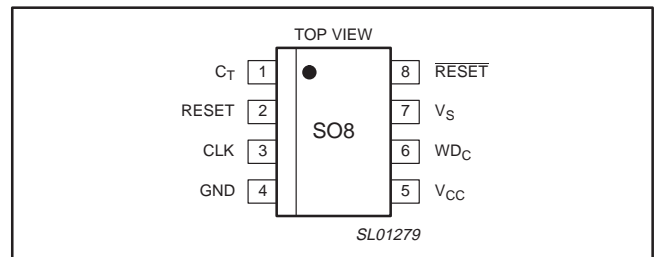


Figure 2. Pin configuration.

## PIN DESCRIPTION

PIN	SYMBOL	DESCRIPTION
1	C <sub>T</sub>	t <sub>WDM</sub> , t <sub>WDR</sub> , t <sub>PR</sub> adjustment pin. t <sub>WDM</sub> , t <sub>WDR</sub> , t <sub>PR</sub> times are dependent on the value of external C <sub>T</sub> capacitor used. See Figure 18 (Timing Diagram) for definition of t <sub>WDM</sub> , t <sub>WDR</sub> , t <sub>PR</sub> times.
2	RESET	Reset HIGH output pin.
3	CLK	Clock input pin from logic system for watchdog timer.
4	GND	Circuit ground.
5	V <sub>CC</sub>	Power supply pin for circuit.
6	W <sub>D</sub> C	Watchdog timer control pin. The watchdog timer is enabled when this pin is unconnected, and disabled when this pin is connected to ground.
7	V <sub>S</sub>	Detection threshold adjustment pin. The detection threshold can be increased by connecting this pin to V <sub>CC</sub> with a pull-up resistor. The detection threshold can be decreased by connecting this pin to ground with a pull-down resistor.
8	RESET	Reset LOW output pin.

## MAXIMUM RATINGS

SYMBOL	PARAMETER	MIN.	MAX.	UNIT
V <sub>CC</sub>	Power supply voltage	-0.3	10	V
V <sub>S</sub>	V <sub>S</sub> pin voltage	-0.3	10	V
V <sub>CLK</sub>	CLK pin voltage	-0.3	10	V
V <sub>OH</sub>	RESET and RESET pin voltage	-0.3	10	V
T <sub>oper</sub>	Operating temperature	-20	70	°C
T <sub>stg</sub>	Storage temperature	-40	125	°C
P	Power dissipation	-	250	mW

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**DC ELECTRICAL CHARACTERISTICS**

Characteristics measured with  $V_{CC} = 5.0\text{ V}$ , and  $T_{amb} = 25\text{ °C}$ , unless otherwise specified.  
See Figure 23 (Test circuit 1) for test configuration used for DC parameters.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
$I_{CC}$	Supply current during watchdog timer operation		–	0.7	1.0	mA
$V_{SL}$	Reset detection threshold	$V_S = \text{open}; V_{CC} = \text{falling}$	4.05	4.20	4.35	V
$V_{SH}$	Reset detection threshold	$V_S = \text{open}; V_{CC} = \text{rising}$	4.15	4.30	4.45	V
$\Delta V_S / \Delta T_{amb}$	Temperature coefficient of reset threshold	$-20\text{ °C} \leq T_{amb} \leq 70\text{ °C}$	–	$\pm 0.01$	–	%/°C
$V_{hys}$	Reset threshold hysteresis	$V_{HYS} = V_{SH} (\text{rising } V_{CC}) - V_{SL} (\text{falling } V_{CC})$	50	100	150	mV
$V_{TH}$	CLK input threshold		0.8	1.2	2.0	V
$I_{IH}$	CLK input current, HIGH-level	$V_{CLK} = 5.0\text{ V}$	–	0	1.0	$\mu\text{A}$
$I_{IL}$	CLK input current, LOW-level	$V_{CLK} = 0\text{ V}$	–20	–10	–3.0	$\mu\text{A}$
$V_{OH1}$	Output voltage, HIGH-level	$\overline{I_{RESET}} = -5.0\text{ }\mu\text{A}; V_S = \text{open}$	4.5	4.8	–	V
$V_{OH2}$		$\overline{I_{RESET}} \text{ current} = -5.0\text{ mA}; V_S = 0\text{ V}$	4.5	4.8	–	V
$V_{OL1}$	Output voltage, LOW-level	$\overline{I_{RESET}} = 3.0\text{ mA}; V_S = 0\text{ V}$	–	0.2	0.4	V
$V_{OL2}$		$\overline{I_{RESET}} = 10\text{ mA}; V_S = 0\text{ V}$	–	0.3	0.5	V
$V_{OL3}$		$\overline{I_{RESET}} = 0.5\text{ mA}; V_S = \text{open}$	–	0.2	0.4	V
$V_{OL4}$		$\overline{I_{RESET}} = 1.0\text{ mA}; V_S = \text{open}$	–	0.3	0.5	V
$I_{OL1}$	Output sink current	$\overline{V_{RESET}} = 1.0\text{ V}; V_S = 0\text{ V}$	10	16	–	mA
$I_{OL2}$		$\overline{V_{RESET}} = 1.0\text{ V}; V_S = \text{open}$	1.0	2.0	–	mA
$I_{CT1}$	$C_T$ charge current	$V_{CT} = 1.0\text{ V}; \overline{WD_C} = \text{open during watchdog operation}$	–8	–12	–24	$\mu\text{A}$
$I_{CT2}$		$V_{CT} = 1.0\text{ V};$ during power-on reset operation	–0.8	–1.2	–2.4	$\mu\text{A}$
$V_{CCL1}$	Supply voltage to assert reset operation	$\overline{V_{RESET}} = 0.4\text{ V};$ $\overline{RESET} \text{ current} = 0.2\text{ mA}$	–	0.8	1.0	V
$V_{CCL2}$		$V_{RESET} = V_{CC} - 0.1\text{ V};$ 1 M $\Omega$ resistor (pin 2 to GND)	–	0.8	1.0	V

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**AC ELECTRICAL CHARACTERISTICS**

Characteristics measured with  $V_{CC} = 5.0\text{ V}$ , and  $T_{amb} = 25\text{ }^{\circ}\text{C}$ , unless otherwise specified.  
See Figure 24 (Test circuit 2) for test configuration used for AC parameters.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
$t_{P1}$	Minimum power supply pulse width for detection	$4.0\text{ V} \leq \text{negative-going } V_{CC} \text{ pulse} \leq 5.0\text{ V}$	8.0	–	–	$\mu\text{s}$
$t_{CLKW}$	Clock input pulse width		3.0	–	–	$\mu\text{s}$
$t_{CLK}$	Clock input cycle		20	–	–	$\mu\text{s}$
$t_{WDM}$	Watchdog monitoring time (Notes 1, 6)	$C_T = 0.1\text{ }\mu\text{F}$ ; $R_{CT} = \text{open}$	5.0	10	15	ms
$t_{WDR}$	Watchdog reset time (Notes 2, 6)	$C_T = 0.1\text{ }\mu\text{F}$	1.0	2.0	3.0	ms
$t_{PR}$	Power-on reset delay time (Notes 3, 6)	$V_{CC} = \text{rising from } 0\text{ V}$ ; $C_T = 0.1\text{ }\mu\text{F}$	50	100	150	ms
$t_{PD1}$	RESET, $\overline{\text{RESET}}$ propagation delay time (Note 4)	RESET: $R_{L1} = 2.2\text{ k}\Omega$ ; $C_{L1} = 100\text{ pF}$	–	2.0	10	$\mu\text{s}$
$t_{PD2}$		RESET: $R_{L2} = 10\text{ k}\Omega$ ; $C_{L2} = 20\text{ pF}$	–	3.0	10	$\mu\text{s}$
$t_{R1}$	RESET, $\overline{\text{RESET}}$ rise time (Note 5)	RESET: $R_{L1} = 2.2\text{ k}\Omega$ ; $C_{L1} = 100\text{ pF}$	–	1.0	1.5	$\mu\text{s}$
$t_{R2}$		RESET: $R_{L2} = 10\text{ k}\Omega$ ; $C_{L2} = 20\text{ pF}$	–	1.0	1.5	$\mu\text{s}$
$t_{F1}$	RESET, $\overline{\text{RESET}}$ fall time (Note 5)	RESET: $R_{L1} = 2.2\text{ k}\Omega$ ; $C_{L1} = 100\text{ pF}$	–	0.1	0.5	$\mu\text{s}$
$t_{F2}$		RESET: $R_{L2} = 10\text{ k}\Omega$ ; $C_{L2} = 20\text{ pF}$	–	0.5	1.0	$\mu\text{s}$

**NOTES:**

- 'Watchdog monitoring time' is the duration from the last pulse (negative-going edge) of the timer clear clock pulse until reset output pulse occurs (see Figure 18). A reset signal is output if a clock pulse is not input during this time.
- 'Watchdog reset time' is the reset pulse width (see Figure 18).
- 'Power-on reset delay time' is the duration measured from the time  $V_{CC}$  exceeds the upper detection threshold ( $V_{SH}$ ) and power-on reset release is experienced (RESET output HIGH;  $\overline{\text{RESET}}$  output LOW).
- 'RESET,  $\overline{\text{RESET}}$  propagation delay time' is the duration from when the supply voltage sags below the lower detection threshold ( $V_{SL}$ ) and reset occurs ( $\overline{\text{RESET}}$  output LOW, RESET output HIGH).
- RESET,  $\overline{\text{RESET}}$  rise and fall times are measured at 10% and 90% output levels.
- Watchdog monitoring time ( $t_{WDM}$ ), watchdog reset time ( $t_{WDR}$ ), and power-on reset delay time ( $t_{PR}$ ) during power-on can be modified by varying the  $C_T$  capacitance. The times can be approximated by applying the following formula. The recommended range for  $C_T$  is  $0.001\text{ }\mu\text{F}$  to  $10\text{ }\mu\text{F}$ .

**Formula 1.** Calculation for approximate  $t_{PR}$ ,  $t_{WDM}$ , and  $t_{WDR}$  values:

$$\begin{aligned} t_{PR} (\text{ms}) &\approx 1000 \times C_T (\mu\text{F}) \\ t_{WDM} (\text{ms}) &\approx 100 \times C_T (\mu\text{F}) \\ t_{WDR} (\text{ms}) &\approx 20 \times C_T (\mu\text{F}) \end{aligned}$$

Example: When  $C_T = 0.1\text{ }\mu\text{F}$  and  $WD_C = \text{open}$ :

$$\begin{aligned} t_{PR} &\approx 100\text{ ms} \\ t_{WDM} &\approx 10\text{ ms} \\ t_{WDR} &\approx 2.0\text{ ms} \end{aligned}$$

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## TYPICAL PERFORMANCE CURVES

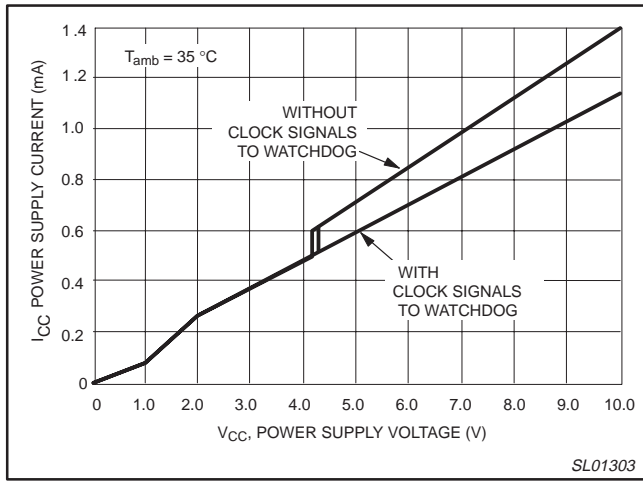


Figure 3. Power supply current versus voltage.

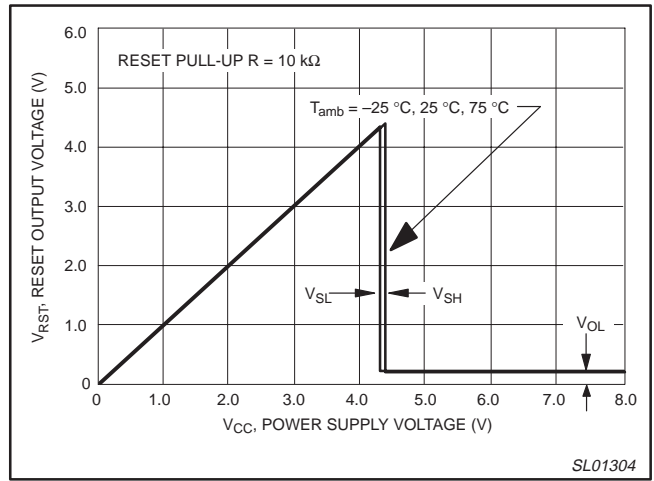


Figure 4. RESET output voltage versus supply voltage.

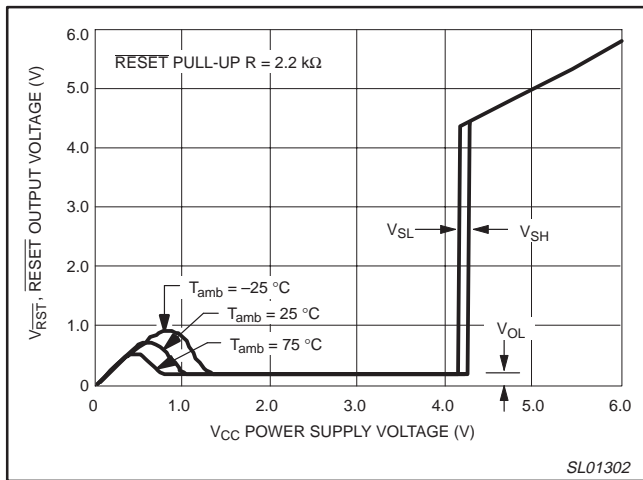


Figure 5. RESET output voltage versus supply voltage.

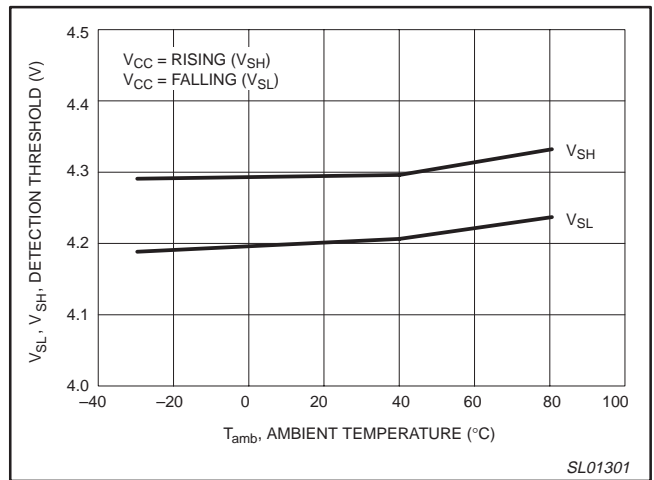


Figure 6. Detection threshold versus temperature.

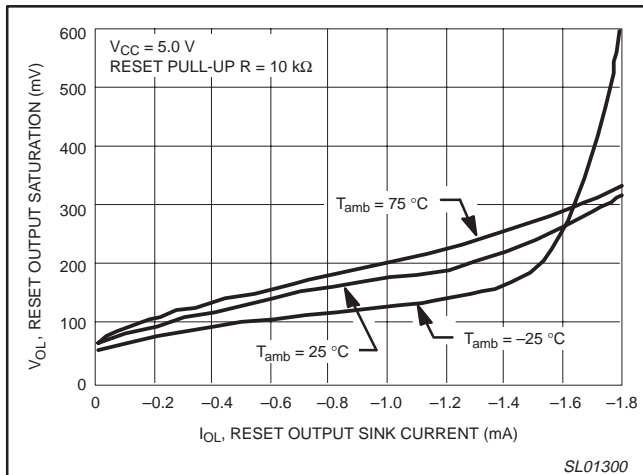


Figure 7. RESET saturation versus sink current.

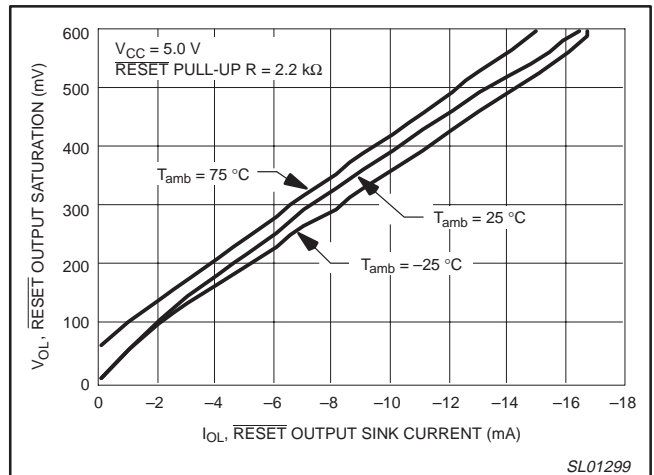


Figure 8. RESET saturation versus sink current.

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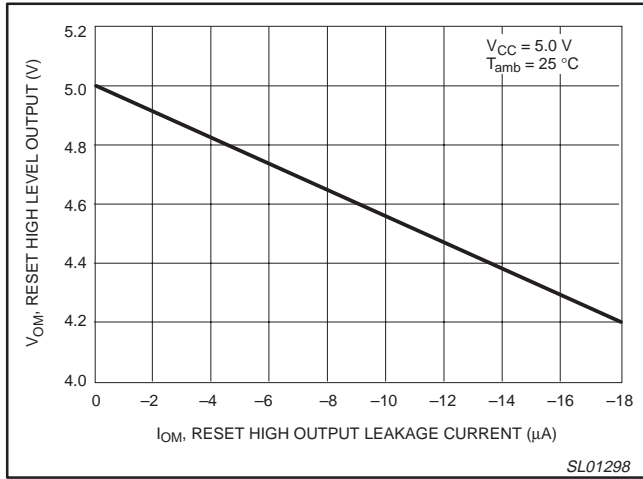


Figure 9. RESET HIGH-level voltage versus current.

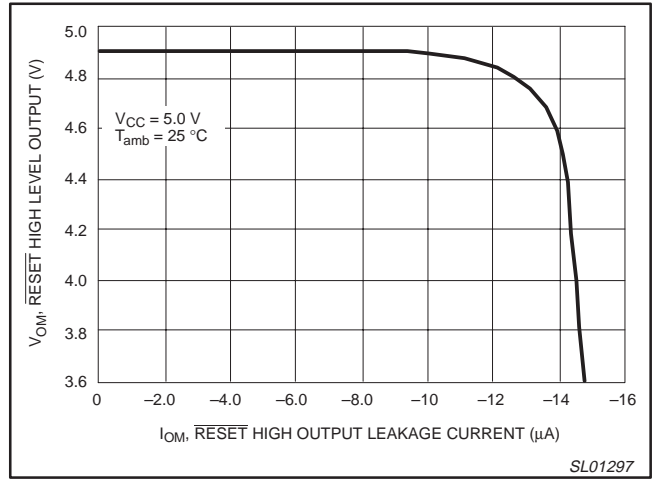


Figure 10. RESET HIGH-level voltage versus current.

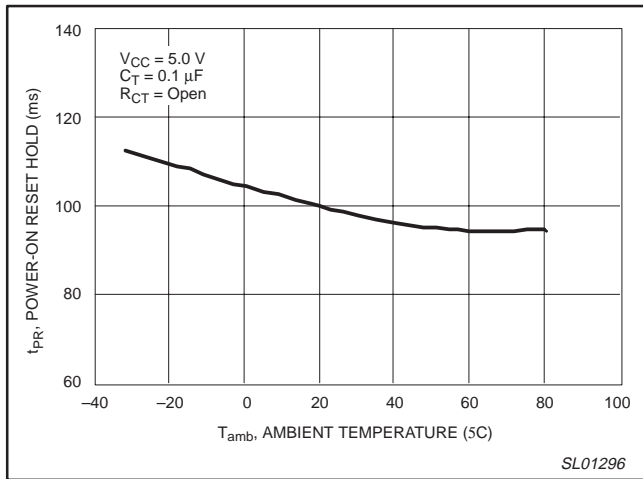


Figure 11. Power-on reset hold time versus temperature.

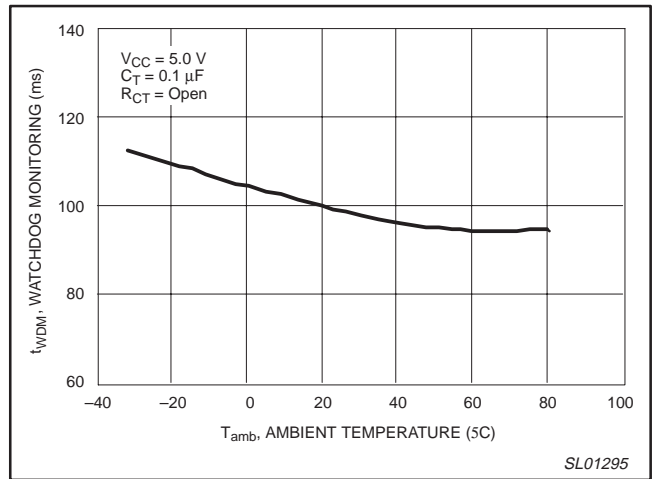


Figure 12. Watchdog monitoring time versus temperature.

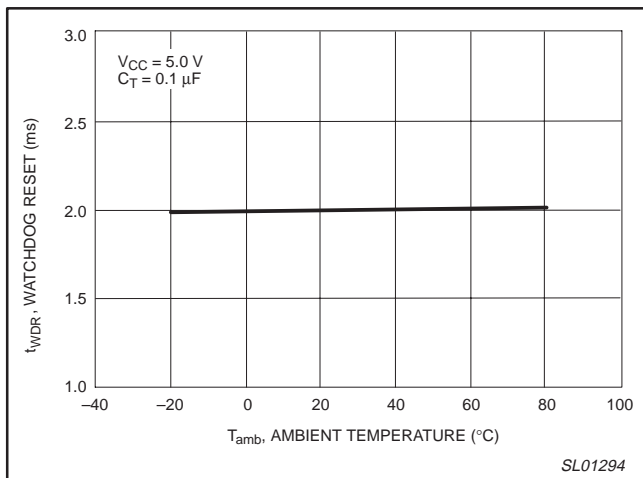


Figure 13. Watchdog reset time versus temperature.

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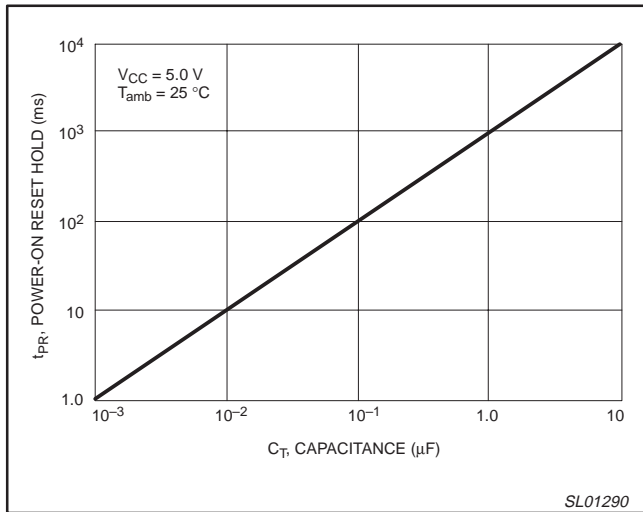


Figure 14. Power-on reset hold time versus  $C_T$ .

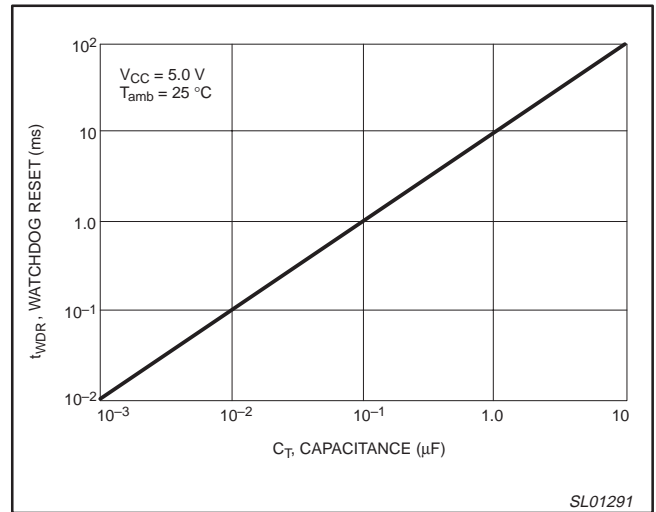


Figure 15. Watchdog reset time versus  $C_T$ .

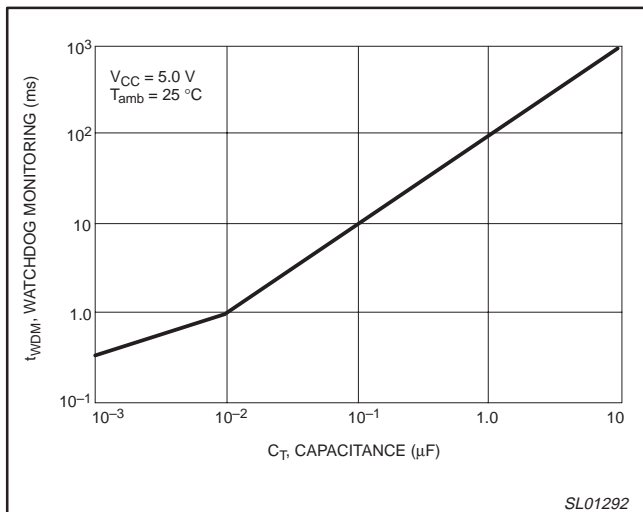


Figure 16. Watchdog reset time versus  $C_T$ .



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## TECHNICAL DESCRIPTION

### General discussion

The NE56605-42 combines a watchdog timer and an undervoltage reset function in a single SO8 surface mount package. This provides a space-saving solution for maintaining proper operation of typical 5.0 volt microprocessor-based logic systems. Either function, or both, can force the microprocessor into a reset.

While the watchdog monitors the microprocessor operation, the undervoltage reset monitors the supply voltage to the microprocessor. If the microprocessor clock signal ceases or becomes erratic, the NE56605-42 outputs a reset signal to the microprocessor. If the microprocessor supply voltage sags to 4.2 volts or less, the NE56605-42 outputs a reset signal for the duration of the supply voltage deficiency. The undervoltage reset signal allows the microprocessor to shut down in an orderly manner to avoid system corruption. In addition to a single reset output, the NE56605-42 has complementary  $\overline{\text{RESET}}$  and  $\text{RESET}$  outputs for system use. The undervoltage detection threshold incorporates hysteresis to prevent generating erratic resets.

The watchdog timer requires a pulse input. Normally this signal comes from the system microprocessor's clock. For operation, an

external capacitor ( $C_T$ ) must be connected from Pin 1 to ground. Normally a 0.1  $\mu\text{F}$  capacitor is used for  $C_T$ . The  $C_T$  capacitor and a fixed internal resistance establish the required minimum frequency of watchdog input signal for the device to **not** output a reset signal. In the absence of a watchdog input pulse, the  $C_T$  capacitor charges to the 0.2 volt threshold of the internal comparator, causing a reset signal to be output. If microprocessor clock signals are received within the required interval, no watchdog reset signal will be output. Grounding the watchdog control pin ( $\text{WD}_C$ , Pin 6) disables the watchdog function. Removing the ground from Pin 6, allowing it to float, enables the watchdog function. Enabling or disabling the watchdog function has no effect on the undervoltage detection function.

Although the temperature coefficient of detection threshold is specified over a temperature of  $-20\text{ }^\circ\text{C}$  to  $+70\text{ }^\circ\text{C}$ , the device will support operation in excess of this temperature range. See the supporting curves for performance over the full temperature range of  $-30\text{ }^\circ\text{C}$  to  $+85\text{ }^\circ\text{C}$ . Some degradation in performance will be experienced at the temperature extremes and the system designer should take this into account.

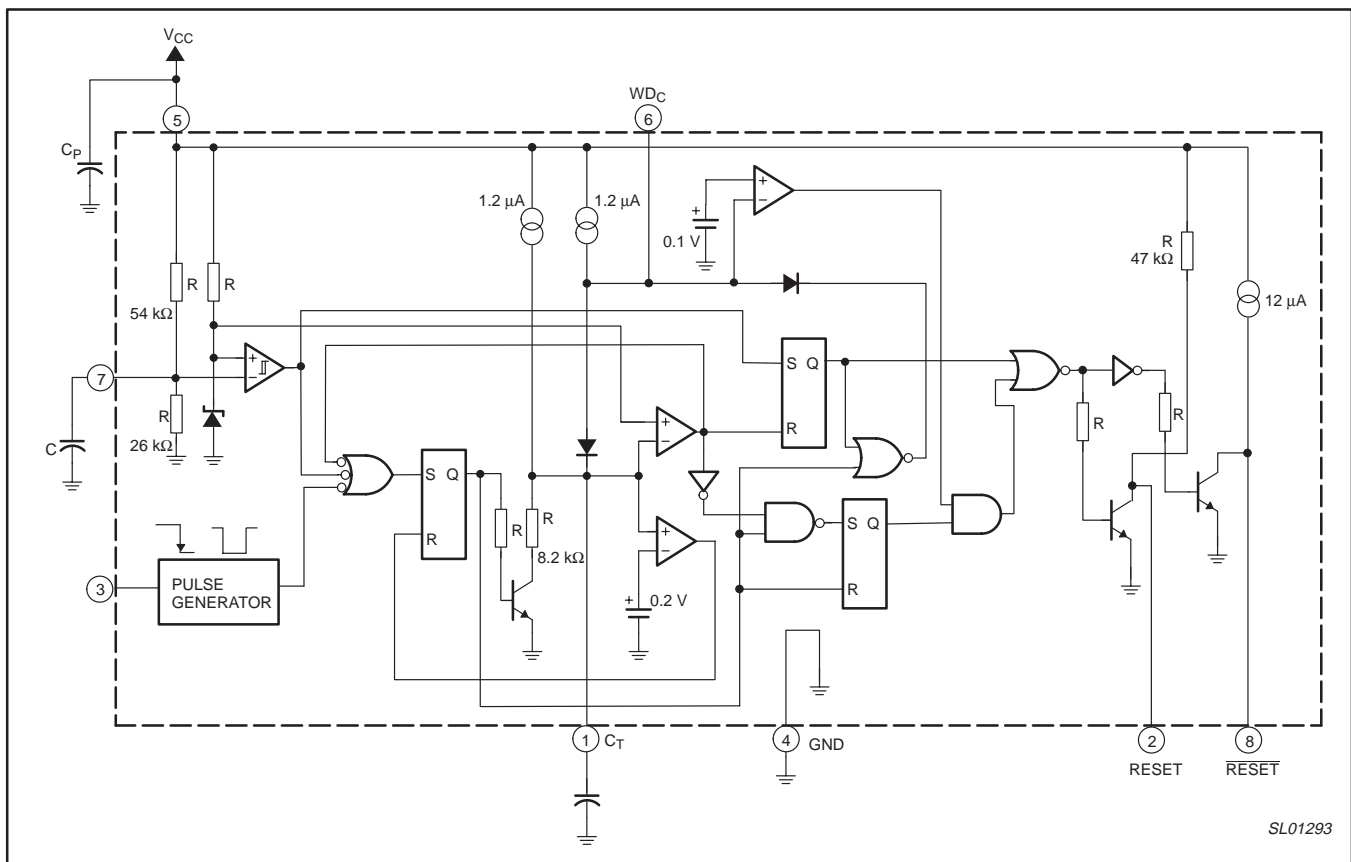


Figure 17. Functional diagram.

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## Timing diagram

The timing diagram shown in Figure 18 depicts the operation of the device. Letters indicate events on the TIME axis.

**A:** At start-up 'A', the  $V_{CC}$  and RESET voltages begin to rise. Also the RESET voltage initially rises, but then abruptly returns to a LOW state. This is due to  $V_{CC}$  reaching the level (approximately 0.8 V) that activates the internal bias circuitry, asserting RESET.

**B:** Just before 'B', the  $C_T$  voltage starts to ramp up. This is caused by, and coincident to,  $V_{CC}$  reaching the threshold level of  $V_{SH}$ . At this level the device is in full operation. The RESET output continues to rise as  $V_{CC}$  rises above  $V_{SH}$ . This is normal.

**C:** At 'C',  $V_{CC}$  is above the undervoltage detect threshold, and  $C_T$  has ramped up to its upper detect level. At this point, the device removes the hold on the resets.  $\overline{RESET}$  goes HIGH while RESET goes LOW. Also, an internal ramp discharge transistor activates, discharging  $C_T$ .

In a microprocessor-based system these events remove the reset from the microprocessor, allowing it to function normally. The system must send clock signals to the Watchdog Timer often enough to prevent  $C_T$  from ramping up to the  $C_T$  threshold, to prevent reset signals from being generated. Each clock signal discharges  $C_T$ .

**C-D:** Midway between 'C' and 'D', the CLK signals cease allowing the  $C_T$  voltage to ramp up to its upper threshold at 'D'. At this time, reset signals are generated (RESET goes LOW; RESET goes HIGH). The device attempts to come out of reset as the  $C_T$  voltage is discharged and finally does come out of reset when CLK signals are re-established after two attempts of  $C_T$ .

**E-F:** Immediately before 'E', falling  $V_{CC}$  causes the  $\overline{RESET}$  signal to sag. CLK signals are still being received,  $C_T$  is within normal operating range, and reset signals are not output.  $V_{CC}$  continues to sag until the  $V_{SL}$  undervoltage threshold is reached. At that time, reset signals are generated (RESET goes LOW; RESET goes HIGH).

At 'E',  $V_{CC}$  starts to rise, and the Reset voltage rises with  $V_{CC}$ . However,  $C_T$  voltage does not start to ramp up until 'F' when  $V_{CC}$  reaches the  $V_{SH}$  upper threshold.

**G:** The reset outputs are released at 'G' when  $C_T$  reaches the upper threshold level again. After 'G', normal CLK signals are received, but at a lower frequency than those following event 'C'. The frequency is above the minimum frequency required to keep the device from outputting reset signals.

**G-H:** At 'H',  $V_{CC}$  is normal, CLK signals are being received, and no reset signals are output. At event 'H', the  $V_{CC}$  starts falling, causing RESET to also fall.

**J:** At event 'J',  $V_{CC}$  sags to the point where the  $V_{SL}$  undervoltage threshold point is reached, and at that level reset signals are output (RESET to a LOW state, and RESET to a HIGH state). As the  $V_{CC}$  voltage falls lower, the Reset voltage falls lower.

**K:** At event 'K', the  $V_{CC}$  voltage has deteriorated to a level where normal internal circuit bias is no longer able to maintain a RESET, and as a result may exhibit a slight rise to something less than 0.8 V. As  $V_{CC}$  decays even further, RESET also decreases to zero.

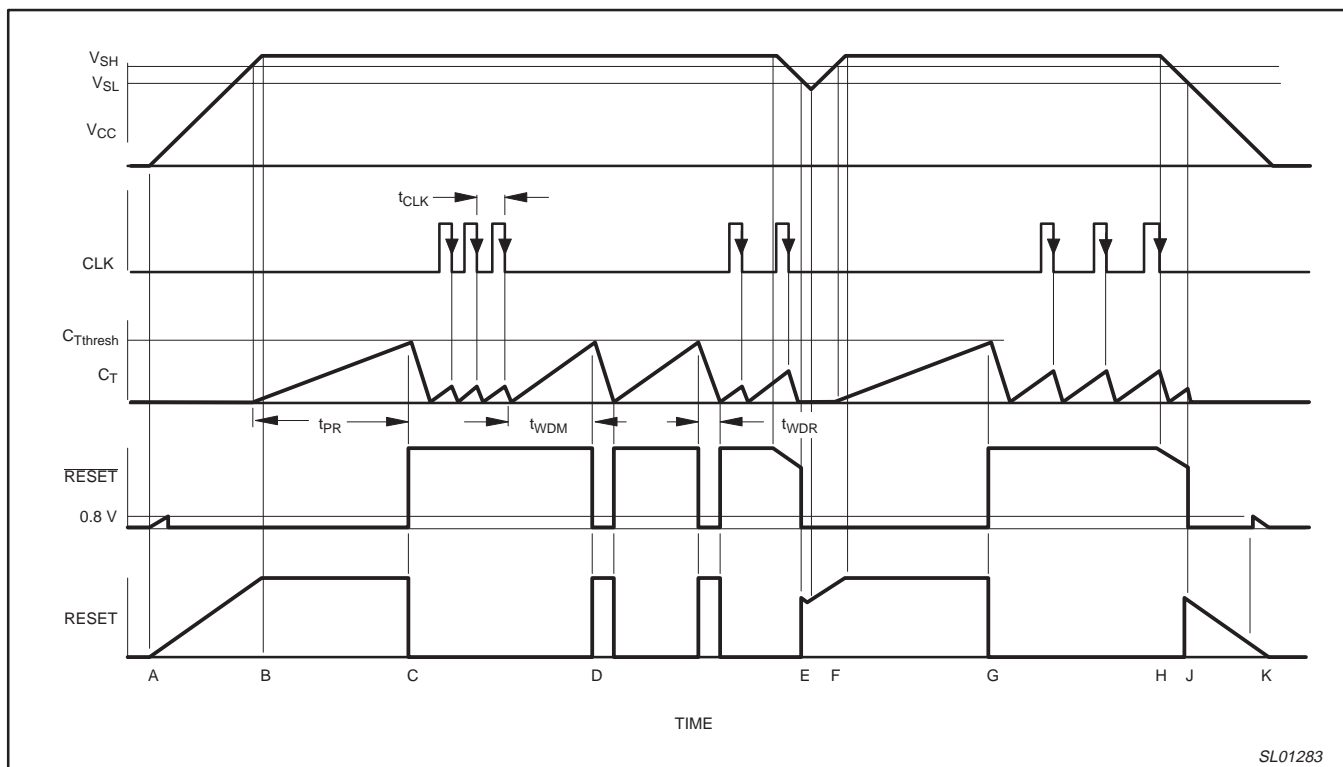


Figure 18. Timing diagram.

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### Application information

The detection threshold voltage can be adjusted by externally influencing the internal divider reference voltage. Figures 19 and 21 show a method to lower and raise the threshold voltage. Figures 20 and 22 show the influence of the pull-down and pull-up resistors on the threshold voltage. The use of a capacitor (1000 pF or larger) from Pin 7 to ground is recommended to filter out noise from being imposed on the threshold voltages.

The Reset Detection Threshold can be decreased by connecting an external resistor  $R_1$  from Pin 7 to  $V_{CC}$ , as shown in Figure 19. See Figure 20 to determine the approximate value of  $R_1$  to use.

The Reset Detection Threshold can be increased by connecting an external resistor  $R_2$  from Pin 7 to ground, as shown in Figure 21. See Figure 22 to determine the approximate value of  $R_2$  to use.

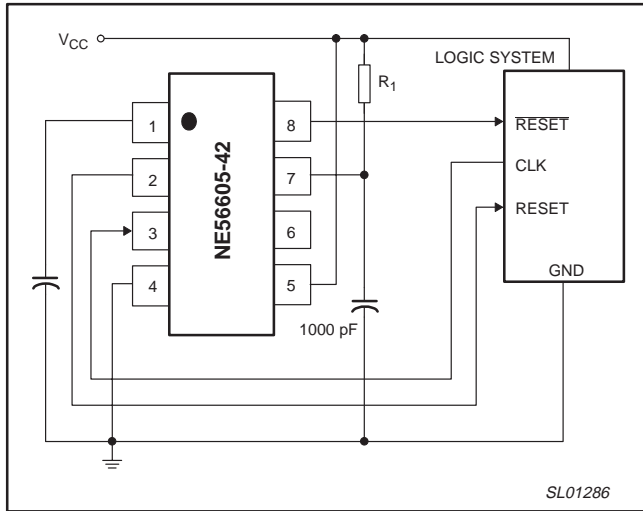


Figure 19. Circuit to lower detection threshold.

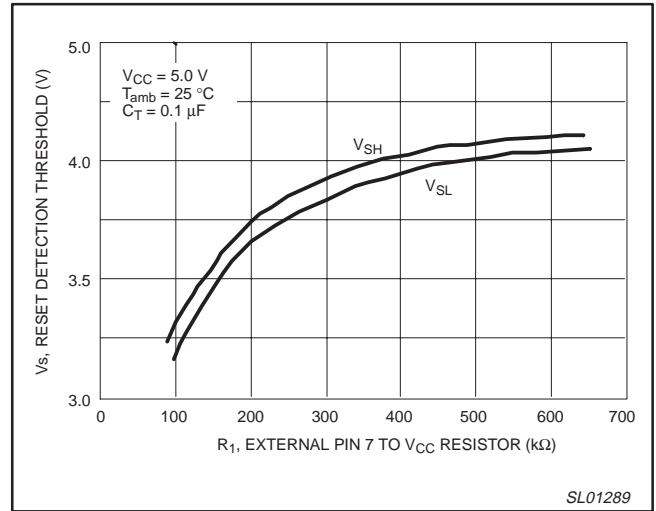


Figure 20. Reset detection threshold versus external  $R_1$ .

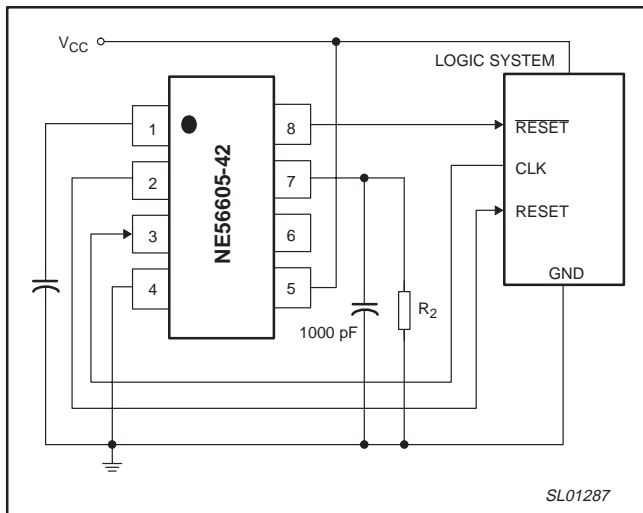


Figure 21. Circuit to raise detection threshold.

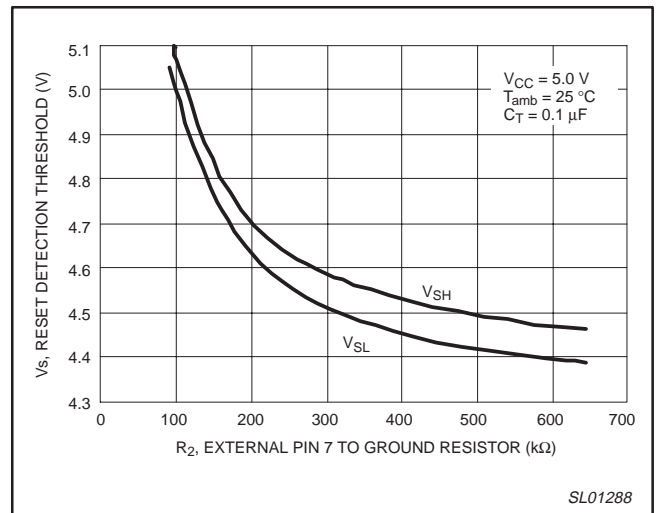


Figure 22. Reset detection threshold versus external  $R_2$ .

# System reset with built-in watchdog timer

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## Parametric testing

DC and AC Characteristics can be tested using the circuits shown in Figures 23 and 24. Associated switch and power supply settings are shown in Table 1 and Table 2, respectively.

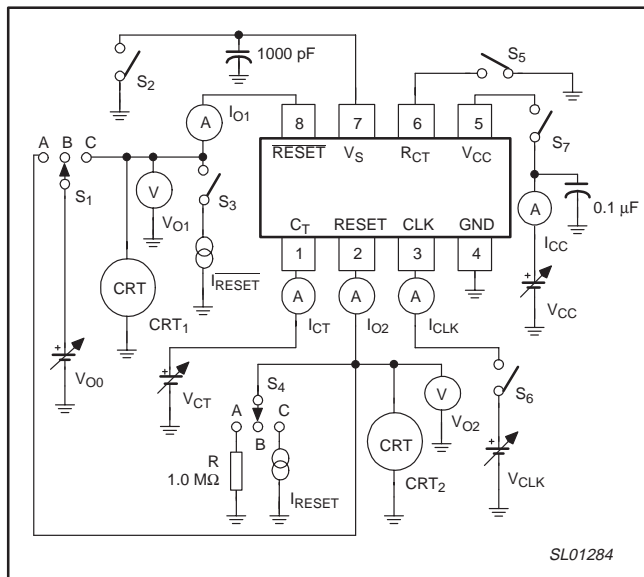


Figure 23. Test Circuit 1 (DC parameters).

Table 1. DC characteristics Test Circuit 1 switch and power supply settings

Parameter	Symbol	S <sub>1</sub>	S <sub>2</sub>	S <sub>3</sub>	S <sub>4</sub>	S <sub>5</sub>	S <sub>6</sub>	S <sub>7</sub>	V <sub>CC</sub>	V <sub>CLK</sub>	V <sub>CT</sub>	I <sub>RESET</sub>	I <sub>RESET</sub>	Read
Power supply current	I <sub>CC</sub>	B	OFF	OFF	B	OFF	ON	ON	5.0 V	5.0 V	0 V	-	-	I <sub>CC</sub>
Reset threshold (LOW) (Note 1)	V <sub>SL</sub>	B	OFF	OFF	B	ON	ON	ON	5.0 to 4.0 V	3.0 V	3.0 V	-	-	V <sub>O1</sub> , CRT <sub>1</sub>
Reset threshold (HIGH) (Note 2)	V <sub>SH</sub>	B	OFF	OFF	B	ON	ON	ON	4.0 to 5.0 V	3.0 V	3.0 V	-	-	V <sub>O1</sub> , CRT <sub>1</sub>
Clock input threshold (Note 3)	V <sub>TH</sub>	B	OFF	OFF	B	OFF	ON	ON	5.0 V	0 to 3.0 V	1.0V	-	-	I <sub>CLK</sub>
Clock input current (HIGH)	I <sub>TH</sub>	B	OFF	OFF	B	OFF	ON	ON	5.0 V	5.0 V	0 V	-	-	I <sub>CLK</sub>
Clock input current (LOW)	I <sub>TL</sub>	B	OFF	OFF	B	OFF	ON	ON	5.0 V	0 V	0 V	-	-	I <sub>CLK</sub>
Reset output voltage (HIGH)	V <sub>OH1</sub>	B	OFF	ON	B	ON	ON	ON	5.0 V	5.0 V	3.0 V	-5.0 μA	-	V <sub>O1</sub>
	V <sub>OH2</sub>	B	ON	OFF	C	ON	ON	ON	5.0 V	5.0 V	3.0 V	-	-5.0 μA	V <sub>O2</sub>
Reset output voltage (LOW)	V <sub>OL1</sub>	B	ON	ON	B	ON	ON	ON	5.0 V	5.0 V	3.0 V	3.0 mA	-	V <sub>O1</sub>
	V <sub>OL2</sub>	B	ON	ON	B	ON	ON	ON	5.0 V	5.0 V	3.0 V	10 mA	-	V <sub>O1</sub>
	V <sub>OL3</sub>	B	OFF	OFF	C	ON	ON	ON	5.0 V	5.0 V	3.0 V	-	0.5 mA	V <sub>O2</sub>
	V <sub>OL4</sub>	B	OFF	OFF	C	ON	ON	ON	5.0 V	5.0 V	3.0 V	-	1.0 mA	V <sub>O2</sub>
Reset output sink current (Note 4)	I <sub>OL1</sub>	C	ON	OFF	B	ON	ON	ON	5.0 V	5.0 V	3.0 V	-	-	I <sub>O1</sub>
	I <sub>OL2</sub>	A	OFF	OFF	B	ON	ON	ON	5.0 V	5.0 V	3.0 V	-	-	I <sub>O2</sub>
C <sub>T</sub> charge current 1	I <sub>CT1</sub>	B	OFF	OFF	B	OFF	OFF	ON	5.0 V	-	1.0 V	-	-	I <sub>CT</sub>
C <sub>T</sub> charge current 2	I <sub>CT2</sub>	B	OFF	OFF	B	ON	OFF	ON	5.0 V	-	1.0 V	-	-	I <sub>CT</sub>
Minimum power supply for RESET (Note 5)	V <sub>CCL1</sub>	B	OFF	ON	B	ON	ON	ON	0 to 2.0 V	0 V	0 V	-	-	V <sub>O1</sub> , V <sub>CC</sub>
Minimum power supply for RESET (Note 6)	V <sub>CCL2</sub>	B	ON	OFF	A	ON	ON	ON	0 to 2.0 V	0 V	0 V	-	-	V <sub>O2</sub> , V <sub>CC</sub>

**NOTES:**

1. Decrease V<sub>CC</sub> from 5.0 V to 4.0 V and note the V<sub>CC</sub> value when V<sub>O1</sub> (observed on CRT<sub>1</sub>) transitions to an abrupt LOW state.
2. Increase V<sub>CC</sub> from 4.0 V to 5.0 V and note the V<sub>CC</sub> value when V<sub>O1</sub> (observed on CRT<sub>1</sub>) transitions to an abrupt HIGH state.
3. Increase the Clock voltage (V<sub>CLK</sub>) from 0 V to 3.0 V and observe the value of V<sub>CLK</sub> when I<sub>CLK</sub> transitions to an abrupt increase.
4. Measured with V<sub>O0</sub> = 1.0 V.
5. Increase V<sub>CC</sub> from 0 V to 2.0 V and note the V<sub>CC</sub> value when V<sub>O1</sub> (observed on CRT<sub>1</sub>) transitions to an abrupt LOW state. The V<sub>O1</sub> value will initially track the V<sub>CC</sub> voltage increase until the internal circuit bias becomes active, at which time the V<sub>O1</sub> value will return to a LOW state.
6. Increase V<sub>CC</sub> from 0 V to 2.0 V and note the V<sub>CC</sub> value when V<sub>O2</sub> (observed on CRT<sub>2</sub>) starts to track the V<sub>CC</sub> voltage.

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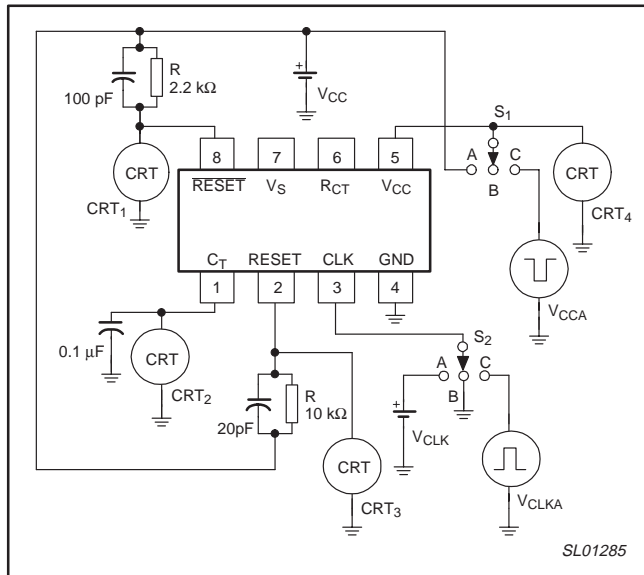


Figure 24. Test Circuit 2 (AC parameters).

Table 2. Switch and power supply settings, AC parameters

Parameter	Symbol	S <sub>1</sub>	S <sub>2</sub>	V <sub>CCA</sub>	V <sub>CC</sub>	V <sub>CLKA</sub>	V <sub>CLK</sub>	CRT
V <sub>CC</sub> pulse width for detection (Note 1)	t <sub>P1</sub>	C	C	5.0 V 4.0 V	—	1.4 V 0 V	—	1, 2, 3
Clock input pulse width (Note 2)	t <sub>CLKW</sub>	A	C	—	5.0 V	1.4 V 0 V	—	1, 2, 3
Clock input cycle (Note 3)	t <sub>CLK</sub>	A	C	—	5.0 V	1.4 V 0 V	—	1, 2, 3
Watchdog monitoring time	t <sub>WDM</sub>	A	A	—	5.0 V	—	5.0 V	1, 2, 3
Watchdog reset time	t <sub>WDR</sub>	A	A	—	5.0 V	—	5.0 V	1, 2, 3
Power-on reset delay time	t <sub>PR</sub>	B to A	A	—	5.0 V	—	5.0 V	1, 2, 3
RESET, $\overline{\text{RESET}}$ propagation delay time	t <sub>PD1</sub>	C	B	5.0 V 4.0 V	—	—	0 V	1, 2
	t <sub>PD2</sub>	C	B	5.0 V 4.0 V	—	—	0 V	2, 3
RESET, $\overline{\text{RESET}}$ rise time	t <sub>R1</sub>	A	A	—	5.0 V	—	5.0 V	1
	t <sub>R2</sub>	A	A	—	5.0 V	—	5.0 V	3
RESET, $\overline{\text{RESET}}$ fall time	t <sub>F1</sub>	A	A	—	5.0 V	—	5.0 V	1
	t <sub>F2</sub>	A	A	—	5.0 V	—	5.0 V	3

**NOTES:**

1. t<sub>1</sub> = 8.0 μs.
2. t<sub>2</sub> = 3.0 μs.
3. t<sub>3</sub> = 20 μs.

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## PACKING METHOD

The NE56605-42 is packed in reels, as shown in Figure 25.

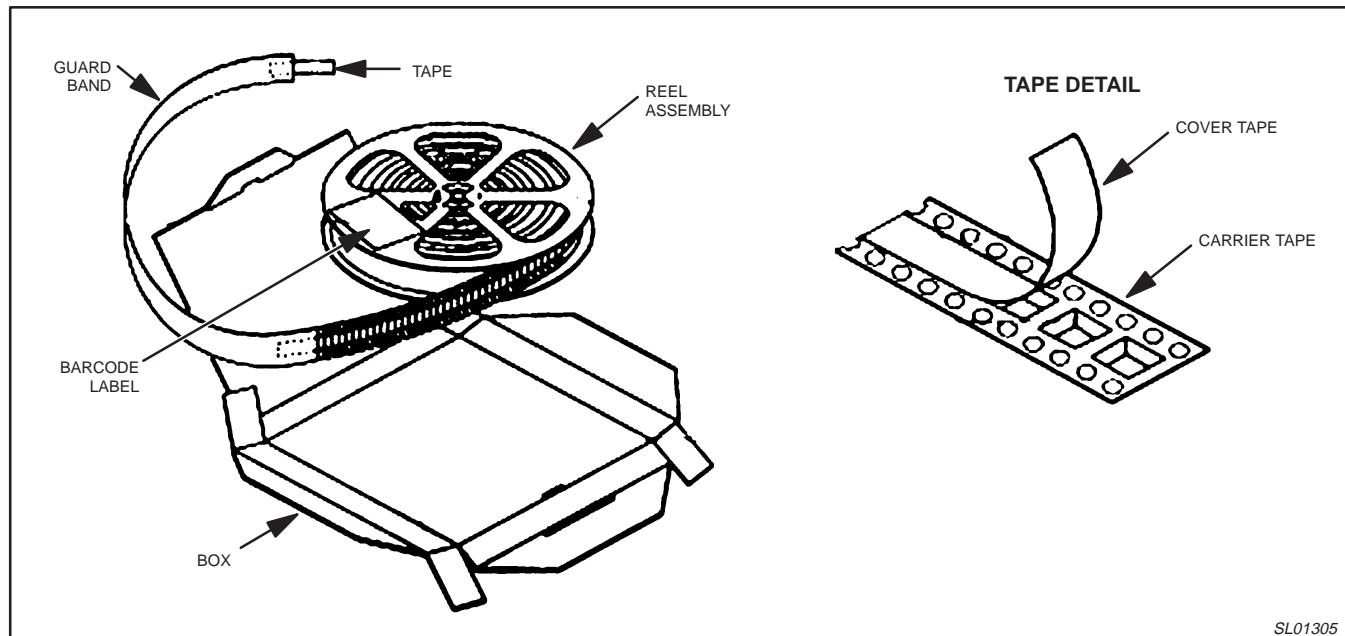
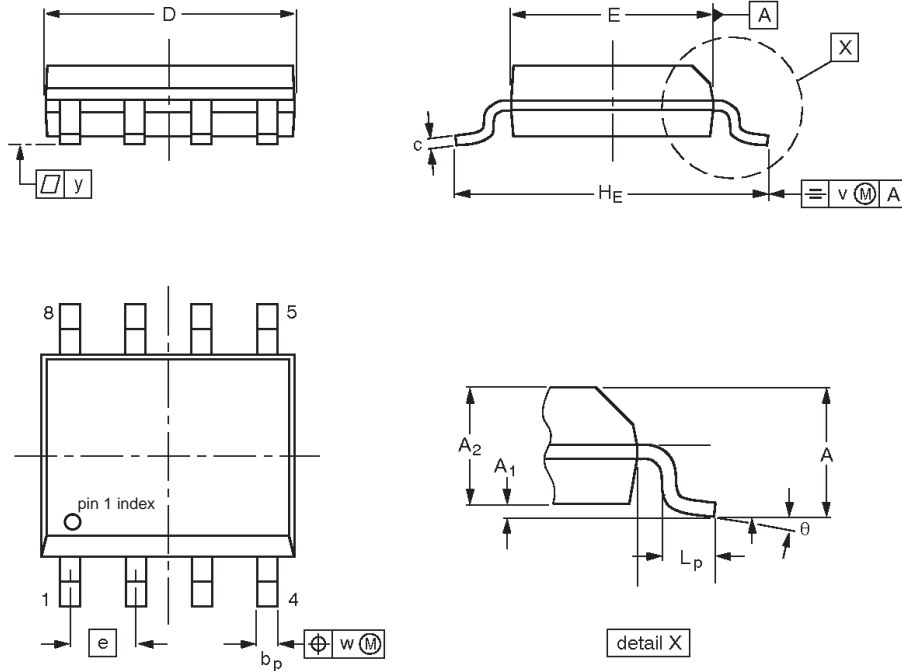


Figure 25. Tape and reel packing method

# System reset with built-in watchdog timer

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**SO8: plastic small outline package; 8 leads; body width 3.9 mm**



**DIMENSIONS (inch dimensions are derived from the original mm dimensions)**

UNIT	A max.	A <sub>1</sub>	A <sub>2</sub>	B <sub>2</sub>	b <sub>p</sub>	c	D <sup>(1)</sup>	E <sup>(2)</sup>	e	H <sub>E</sub>	L <sub>p</sub>	y	θ
mm	1.73 0.10	0.25 1.25	1.45 4.80	4.95 8.80	0.51 0.33	0.25 0.19	4.95 4.80	4.0 3.8	1.27	6.2 5.8	1.27 0.38	0.076	8° 0°
inches	0.068 0.004	0.010 0.049	0.057 0.195	0.189 0.195	0.013 0.020	0.0100 0.0075	0.20 0.19	0.16 0.15	0.050	0.244 0.228	0.050 0.015	0.003	

**Notes**

1. Plastic or metal protrusions of 0.15 mm maximum per side are not included.
2. Plastic or metal protrusions of 0.25 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES		
	IEC	JEDEC	EIAJ
SO8	076E03	MS-012	

## System reset with built-in watchdog timer

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## Data sheet status

Data sheet status <sup>[1]</sup>	Product status <sup>[2]</sup>	Definitions
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Date of release: 10-01

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