11/14/03

Errata Document for CY7C1312V18 & CY7C1314V18

This document describes errata for the CY7C1312V18 and CY7C1314V18. Details include errata trigger conditions, available workarounds, and silicon revision applicability. This document should be used as a suplement to the existing datasheet.

Please contact your local Cypress Sales Representative if you have further questions.

Part Numbers Affected

Part Number	Architecture	Confguration	Clock Frequency
CY7C1312V18-133BZC	QDR-II Burst of 2	1 M x 18	133 MHz
CY7C1312V18-167BZC	QDR-II Burst of 2	1 M x 18	167 MHz
CY7C1314V18-133BZC	QDR-II Burst of 2	512 K x 36	133 MHz
CY7C1314V18-167BZC	QDR-II Burst of 2	512 K x 36	167 MHz

CY7C1312V18 & CY7C1314V18 Qualification Status

These parts are currently available as Engineering Samples.

The reliability report is available on our website, www.cypress.com, QTP# 032105

CY7C1312V18 & CY7C1314V18 Errata Summary

The following table defines the errata applicability to the CY7C1312V18 and CY7C1314V18.

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Items	CY7C1312V18	CY7C1314V18	Fix Status
1. Address 7C Errata	X	X	Cypress plans to fix this errata with changes to the silicon.
2. First Clock Cycle Errata	X	X	Cypress does not plan to fix this errata. Contact your local Cypress sales office for additional information.

1. ADDRESS 7C ERRATA

- **PROBLEM DEFINITION**

  In a given clock cycle:

  - The read address is provided on the rising edge of K
  - The write address is provided on the rising edge of K#
  - If the read and write address are the same, data is forwarded from the input port to the output port and the data from the memory array is ignored. This feature is called the data forwarding feature and it ensures that the most current data is always output from the device.

  In the event that address 7C is the only address that changes between the read address, and the write address in a given clock cycle, and if address 7C is changing from "1" to "0", then the data forwarding may be erroneously activated. The data from the memory array may be ignored and the data from the input bus may be improperly forwarded.

- **PARAMETERS AFFECTED**

  This errata impacts the integrity of the data. It does not impact any timing or operating parameters.

- **TRIGGER CONDITION(S)**

  This errata can occur across all datasheet operating conditions.

- **SCOPE OF IMPACT**

  This issue only applies to the burst of 2 arhcitecture only. QDR-II. Burst of 4 devices are NOT affected by this issue. This errata affects the output of the data from the device. It does not affect the data integrity in the memory array.

  The impact this has in an application has two components. First, it is dependent on how often the failing condition occurs. Second, it is dependent on the system's ability to recover from the occurance of incorrect data.

  In applications with truly random access of the memory, it will occur at a rate of 2 PPM for the CY7C1312V18 and 4 PPM for the CY7C1314V18. However, it will occur more frequently in applications where the failing conditions occur more frequently.

- **WORKAROUND**

  Prohibit the failing conditions in the SRAM controller's software.

- **FIX STATUS**

  Cypress has identified a change to the silicon that will eliminate this errata.

2. FIRST CLOCK CYCLE ERRATA

- **PROBLEM DEFINITION**

  In the first clock cylce seen by the device, it is possible for data to be written into the memory array incorrectly. Specificlly, the first word may be written to the second burst address and the second word may be written to the first burst address. This can only occur in the first clock cycle seen by the device and will not occur in subsequent clock cycles.

  To date, Cypress is unaware of any applications that have experienced this issue.

- **PARAMETERS AFFECTED**

  This errata impacts the integrity of the data. It does not impact any timing or operating parameters.

- **TRIGGER CONDITION(S)**

  This errata will only occur during the first clock cycle seen by the device. It will not occur after the second rising edges of the K and K# clocks. Therefore, if the device sees any clock cycles during power up, this errata will not occur.

  This errata occurs under the following conditions:

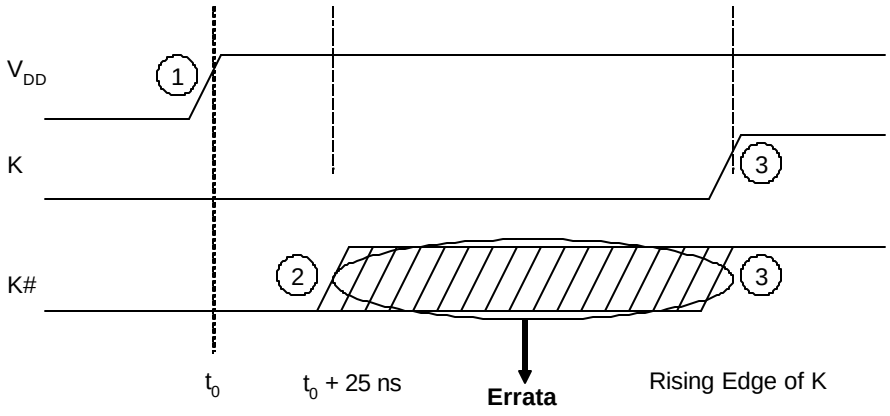
  (1) V_{DD} reaches 1.7 V at t_0,

  (2) K# rises from low to high after t_0 + 25 ns,

  (3) K# rises from low to high before the first rising edge of K.

  A timing diagram for these trigger conditions is shown below:

Timing Diagram For First Clock Cycle Errata Trigger Conditions



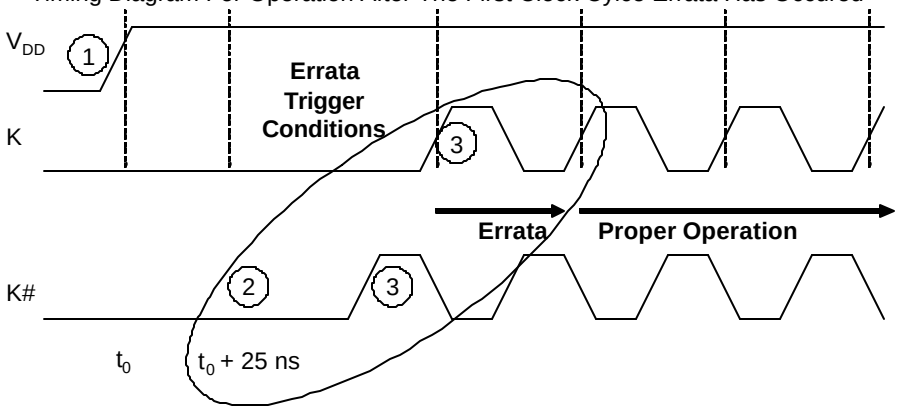
- **SCOPE OF IMPACT**

  This errata only impacts the data integrity of data written during the first clock cycle seen by the device. All subsequent writes will be written correctly.

  To date, none of our customers have reported seeing this failure mechanism in an application.

  A timing diagram describing device operation after the first clock cycle errata is triggered is shown below.

Timing Diagram For Operation After The First Clock Cylce Errata Has Occured

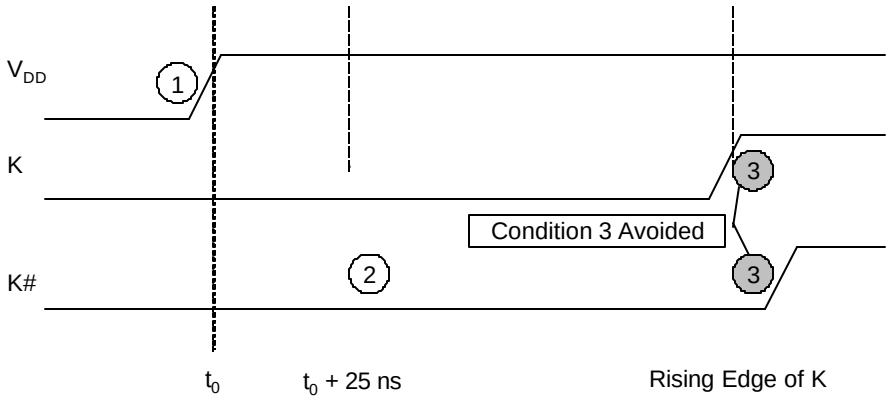


- **WORKAROUND**

  There are numerous available workarounds to this errata. These include the following:

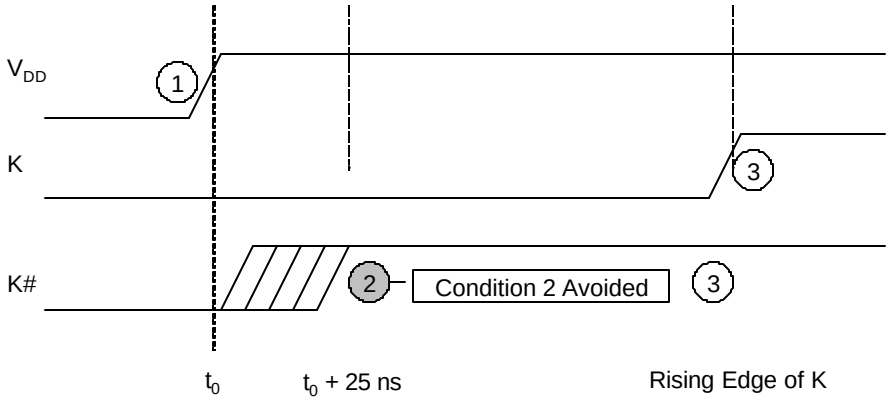
  1. Wait until after the first clock cycle to write to the device.
  2. Ensure that K rises high before K# (Shown Below)

Timing Diagram For Ensuring K Rises Before K#



3. Bring K# input high prior to t_0 + 25 ns.

Timing Diagram For Bringing K# High Prior to t_0 + 25 ns



- **FIX STATUS**
  Cypress does not have a plan to correct this errata. If your application cannot accommodate the suggested workarounds, please contact your Cypress FAE.

References

[1] Document # 38-05180,CY7C1310V18/CY7C1312V18/CY7C1314V18: 18-Mb QDR(TM)-II SRAM Two-word Burst Architecture (Preliminary)

Document History Page

Document Title: CY7C1312V18 & CY7C1314V18 Errata Document Number: 38-17005				
REV.	**ECN NO.**	**Issue Date**	**Orig. of Change**	**Description of Change**
**	131284	11/14/03	RCS	1. New Document