



512K X 16 BIT LOW POWER CMOS SRAM

FEATURES

- Process Technology : 0.15 μ m Full CMOS
- Organization : 512K x 16 bit
- Power Supply Voltage : 2.7V ~ 3.6V
- Low Data Retention Voltage : 1.5V(Min.)
- Three state output and TTL Compatible
- Package Type : 48-FPBGA, 44-TSOP2

GENERAL DESCRIPTION

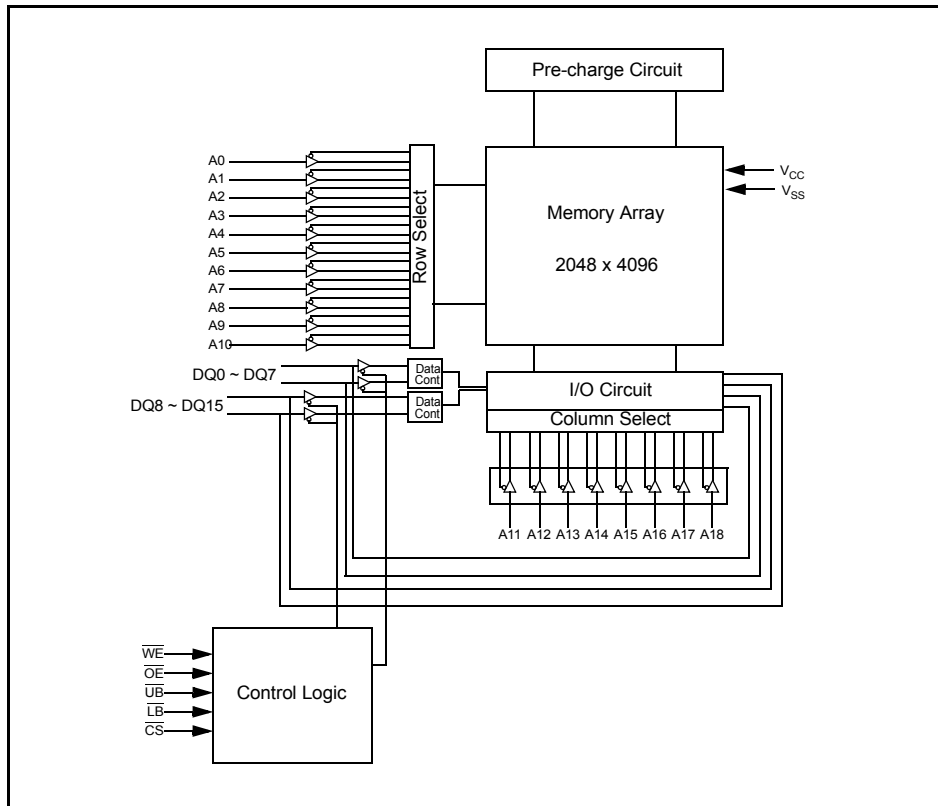
The AS6C8016A is fabricated by Alliance 's advanced full CMOS process technology. The families support industrial temperature range and Chip Scale Package for user flexibility of system design. The families also support low data retention voltage for battery back-up operation with low data retention current.

PRODUCT FAMILY

| | Operating Temperature | Vcc Range | Speed | Power Dissipation | | PKG Type |
|-----------------|-------------------------|-------------|-------|-----------------------------------|------------------------------------|----------|
| | | | | Standby (I _{SB1} , Typ.) | Operating (I _{CC1} -Max.) | |
| AS6C8016A | Industrial (-40 ~ 85°C) | 2.7 ~ 3.6 V | 55 ns | 2 μ A ¹⁾ | 4 mA | KGD |
| AS6C8016A-55BIN | | | | | | 48-FPBGA |
| AS6C8016A-55ZIN | | | | | | 44-TSOP2 |

1. Typical values are measured at Vcc=3.3V, T_A=25°C and not 100% tested.

FUNCTIONAL BLOCK DIAGRAM





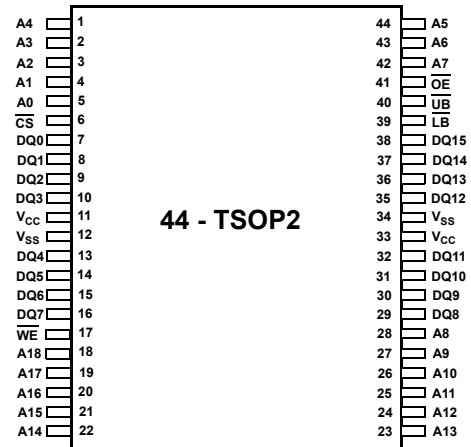
512K X 16 BIT LOW POWER CMOS SRAM

PIN CONFIGURATIONS

FPBGA-48 : Top view(ball down)

| | 1 | 2 | 3 | 4 | 5 | 6 |
|---|------------------------|------------------------|-----|-----|------------------------|-----------------|
| A | $\overline{\text{LB}}$ | $\overline{\text{OE}}$ | A0 | A1 | A2 | NC |
| B | DQ8 | $\overline{\text{UB}}$ | A3 | A4 | $\overline{\text{CS}}$ | DQ0 |
| C | DQ9 | DQ10 | A5 | A6 | DQ1 | DQ2 |
| D | V _{SS} | DQ11 | A17 | A7 | DQ3 | V _{CC} |
| E | V _{CC} | DQ12 | NC | A16 | DQ4 | V _{SS} |
| F | DQ14 | DQ13 | A14 | A15 | DQ5 | DQ6 |
| G | DQ15 | NC | A12 | A13 | $\overline{\text{WE}}$ | DQ7 |
| H | A18 | A8 | A9 | A10 | A11 | NC |

44 - TSOP2 : Top view



PIN DESCRIPTION

| | Function | Name | Function |
|------------------------|---------------------|------------------------|-----------------------|
| $\overline{\text{CS}}$ | Chip Select input | V _{CC} | Power Supply |
| $\overline{\text{OE}}$ | Output Enable input | V _{SS} | Ground |
| $\overline{\text{WE}}$ | Write Enable input | $\overline{\text{UB}}$ | Upper Byte (DQ8~DQ15) |
| A0~A18 | Address inputs | $\overline{\text{LB}}$ | Lower Byte (DQ0~DQ7) |
| DQ0~DQ15 | Data inputs/outputs | NC | No Connection |



512K X 16 BIT LOW POWER CMOS SRAM

ABSOLUTE MAXIMUM RATINGS¹⁾

| | Symbol | Ratings | Unit |
|---|------------------------------------|-------------|------|
| Voltage on Any Pin Relative to V _{SS} | V _{IN} , V _{OUT} | -0.2 to 4.0 | V |
| Voltage on V _{CC} supply relative to V _{SS} | V _{CC} | -0.2 to 4.0 | V |
| Power Dissipation | P _D | 1.0 | W |
| Operating Temperature | T _A | -40 to 85 | °C |

1. Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. Functional operation should be restricted to recommended operating condition. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

FUNCTIONAL DESCRIPTION

| $\overline{\text{CS}}$ | $\overline{\text{OE}}$ | $\overline{\text{WE}}$ | $\overline{\text{LB}}$ | $\overline{\text{UB}}$ | DQ0~7 | DQ8~15 | Mode | Power |
|------------------------|------------------------|------------------------|------------------------|------------------------|----------|----------|------------------|----------|
| H | X | X | X | X | High-Z | High-Z | Deselected | Stand by |
| X | X | X | H | H | High-Z | High-Z | Deselected | Stand by |
| L | H | H | L | X | High-Z | High-Z | Output Disabled | Active |
| L | H | H | X | L | High-Z | High-Z | Output Disabled | Active |
| L | L | H | L | H | Data Out | High-Z | Lower Byte Read | Active |
| L | L | H | H | L | High-Z | Data Out | Upper Byte Read | Active |
| L | L | H | L | L | Data Out | Data Out | Word Read | Active |
| L | X | L | L | H | Data In | High-Z | Lower Byte Write | Active |
| L | X | L | H | L | High-Z | Data In | Upper Byte Write | Active |
| L | X | L | L | L | Data In | Data In | Word Write | Active |

NOTE : X means don't care. (Must be low or high state)



512K X 16 BIT LOW POWER CMOS SRAM

RECOMMENDED DC OPERATING CONDITIONS ¹⁾

| | Symbol | Min | Typ | Max | Unit |
|--------------------|----------|-------------|-----|---------------------|------|
| Supply voltage | V_{CC} | 2.7 | 3.3 | 3.6 | V |
| Ground | V_{SS} | 0 | 0 | 0 | V |
| Input high voltage | V_{IH} | 2.2 | - | $V_{CC} + 0.2^{2)}$ | V |
| Input low voltage | V_{IL} | $-0.2^{3)}$ | - | 0.6 | V |

1. $T_A = -40$ to 85°C , otherwise specified
2. Overshoot: $V_{CC} + 2.0$ V in case of pulse width ≤ 20 ns
3. Undershoot: -2.0 V in case of pulse width ≤ 20 ns
4. Overshoot and undershoot are sampled, not 100% tested.

CAPACITANCE ¹⁾ ($f = 1\text{MHz}$, $T_A = 25^\circ\text{C}$)

| Item | Symbol | Test Condition | Min | Max | Unit |
|--------------------------|----------|----------------------|-----|-----|------|
| Input capacitance | C_{IN} | $V_{IN} = 0\text{V}$ | - | 8 | pF |
| Input/Output capacitance | C_{IO} | $V_{IO} = 0\text{V}$ | - | 10 | pF |

1. Capacitance is sampled, not 100% tested

DC AND OPERATING CHARACTERISTICS

| Parameter | Symbol | Test Conditions | Min | Typ | Max | Unit |
|---------------------------|-----------|--|------|-----|----------|---------------------|
| Input leakage current | I_{LI} | $V_{IN} = V_{SS}$ to V_{CC} | -1 | - | 1 | μA |
| Output leakage current | I_{LO} | $\overline{CS} = V_{IH}$ or $\overline{OE} = V_{IH}$ or $\overline{WE} = V_{IL}$ or $\overline{LB} = \overline{UB} = V_{IH}$ $V_{IO} = V_{SS}$ to V_{CC} | -1 | - | 1 | μA |
| Operating power supply | I_{CC} | $I_{IO} = 0\text{mA}$, $\overline{CS} = V_{IL}$, $\overline{WE} = V_{IH}$, $V_{IN} = V_{IH}$ or V_{IL} | - | - | 2 | mA |
| Average operating current | I_{CC1} | Cycle time = $1\mu\text{s}$, 100% duty, $I_{IO} = 0\text{mA}$, $\overline{CS} \leq 0.2\text{V}$, $\overline{LB} \leq 0.2\text{V}$ or/and $\overline{UB} \leq 0.2\text{V}$, $V_{IN} \leq 0.2\text{V}$ or $V_{IN} \geq V_{CC} - 0.2\text{V}$ | - | - | 4 | mA |
| | I_{CC2} | Cycle time = Min, $I_{IO} = 0\text{mA}$, 100% duty, $\overline{CS} = V_{IL}$, $\overline{LB} = V_{IL}$ or/and $\overline{UB} = V_{IL}$, $V_{IN} = V_{IL}$ or V_{IH} | 55ns | - | 35 | mA |
| Output low voltage | V_{OL} | $I_{OL} = 2.1\text{mA}$ | - | - | 0.4 | V |
| Output high voltage | V_{OH} | $I_{OH} = -1.0\text{mA}$ | 2.4 | - | - | V |
| Standby Current (TTL) | I_{SB} | $\overline{CS} = V_{IH}$, Other inputs = V_{IH} or V_{IL} | - | - | 0.5 | mA |
| Standby Current (CMOS) | I_{SB1} | $\overline{CS} \geq V_{CC} - 0.2\text{V}$, Other inputs = $0 \sim V_{CC}$ (Typ. condition : $V_{CC} = 3.3\text{V}$ @ 25°C) (Max. condition : $V_{CC} = 3.6\text{V}$ @ 85°C) | LF | - | $2^{1)}$ | 15 μA |

1. Typical values are measured at $V_{CC} = 3.3\text{V}$, $T_A = 25^\circ\text{C}$ and not 100% tested.



512K X 16 BIT LOW POWER CMOS SRAM

AC OPERATING CONDITIONS

Test Conditions (Test Load and Test Input/Output Reference)

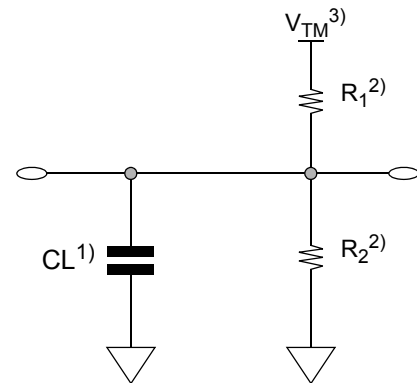
Input Pulse Level : 0.4 to 2.4V

Input Rise and Fall Time : 5ns

Input and Output reference Voltage : 1.5V

Output Load (See right) : $CL^{(1)} = 100\text{pF} + 1 \text{ TTL}(70\text{nsec})$ $CL^{(1)} = 30\text{pF} + 1 \text{ TTL}(45\text{ns}/55\text{ns})$

1. Including scope and Jig capacitance

2. $R_1=3070\Omega$, $R_2=3150\Omega$ 3. $V_{TM}=2.8\text{V}$ 4. $CL = 5\text{pF} + 1 \text{ TTL}$ (measurement with t_{LZ} , t_{HZ} , t_{OLZ} , t_{OHZ} , t_{WHZ})READ CYCLE ($V_{CC}=2.7$ to 3.6V , $Gnd = 0\text{V}$, $T_A = -40^\circ\text{C}$ to $+85^\circ\text{C}$)

| | Symbol | 55ns | | Unit |
|---|-----------|------|-----|------|
| | | Min | Max | |
| Read cycle time | t_{RC} | 55 | - | ns |
| Address access time | t_{AA} | - | 55 | ns |
| Chip select to output | t_{CO} | - | 55 | ns |
| Output enable to valid output | t_{OE} | - | 35 | ns |
| \overline{UB} , \overline{LB} access time | t_{BA} | | 45 | ns |
| Chip select to low-Z output | t_{LZ} | 5 | - | ns |
| \overline{UB} , \overline{LB} enable to low-Z output | t_{BLZ} | 5 | - | ns |
| Output enable to low-Z output | t_{OLZ} | 5 | - | ns |
| Chip disable to high-Z output | t_{HZ} | 0 | 20 | ns |
| \overline{UB} , \overline{LB} disable to how-Z output | t_{BHZ} | 0 | 20 | ns |
| Output disable to high-Z output | t_{OHZ} | 0 | 20 | ns |
| Output hold from address change | t_{OH} | 10 | - | ns |

WRITE CYCLE ($V_{CC}=2.7$ to 3.6V , $Gnd = 0\text{V}$, $T_A = -40^\circ\text{C}$ to $+85^\circ\text{C}$)

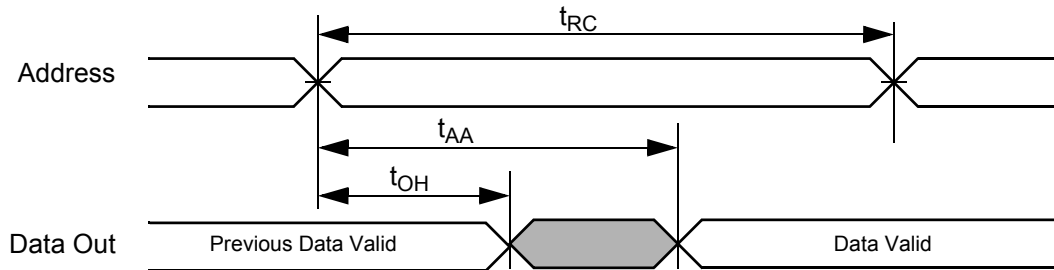
| Parameter | Symbol | 55ns | | Unit |
|---|-----------|------|-----|------|
| | | Min | Max | |
| Write cycle time | t_{WC} | 55 | - | ns |
| Chip select to end of write | t_{CW} | 45 | - | ns |
| Address setup time | t_{AS} | 0 | - | ns |
| Address valid to end of write | t_{AW} | 45 | - | ns |
| \overline{UB} , \overline{LB} valid to end of write | t_{BW} | 45 | - | ns |
| Write pulse width | t_{WP} | 45 | - | ns |
| Write recovery time | t_{WR} | 0 | - | ns |
| Write to output high-Z | t_{WHZ} | 0 | 20 | ns |
| Data to write time overlap | t_{DW} | 25 | | ns |
| Data hold from write time | t_{DH} | 0 | - | ns |
| End write to output low-Z | t_{OW} | 5 | - | ns |



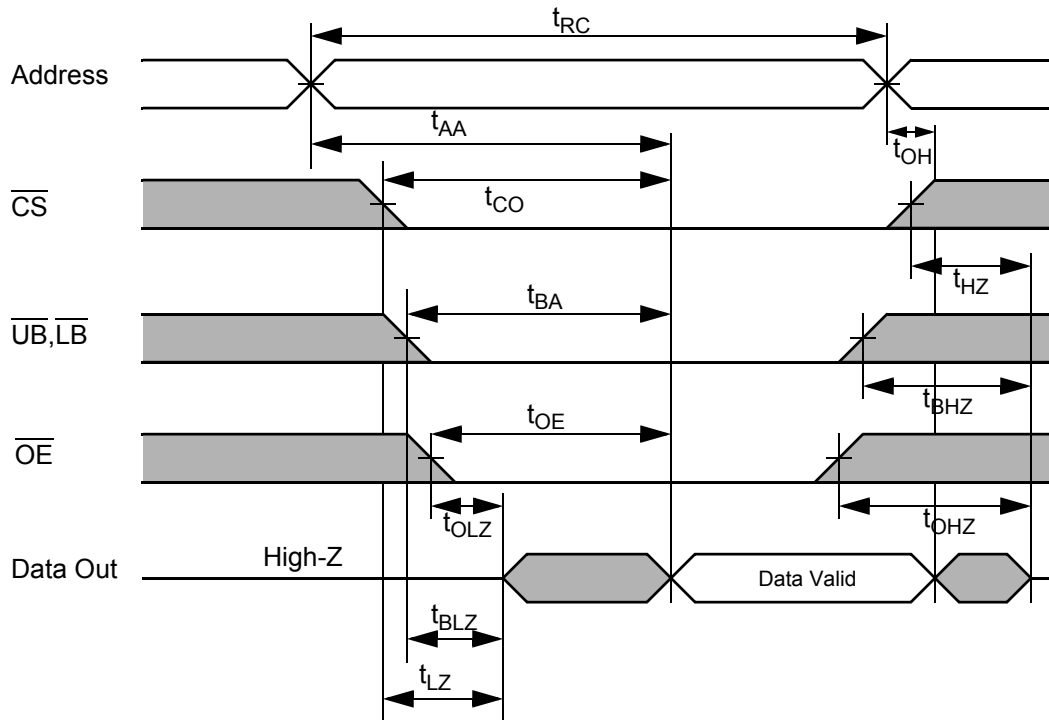
512K X 16 BIT LOW POWER CMOS SRAM

TIMING DIAGRAMS

TIMING WAVEFORM OF READ CYCLE(1) (Address Controlled, $\overline{CS}=\overline{OE}=V_{IL}$, $\overline{WE}=V_{IH}$, \overline{UB} or/and $\overline{LB}=V_{IL}$)



TIMING WAVEFORM OF READ CYCLE(2) ($\overline{WE} = V_{IH}$)



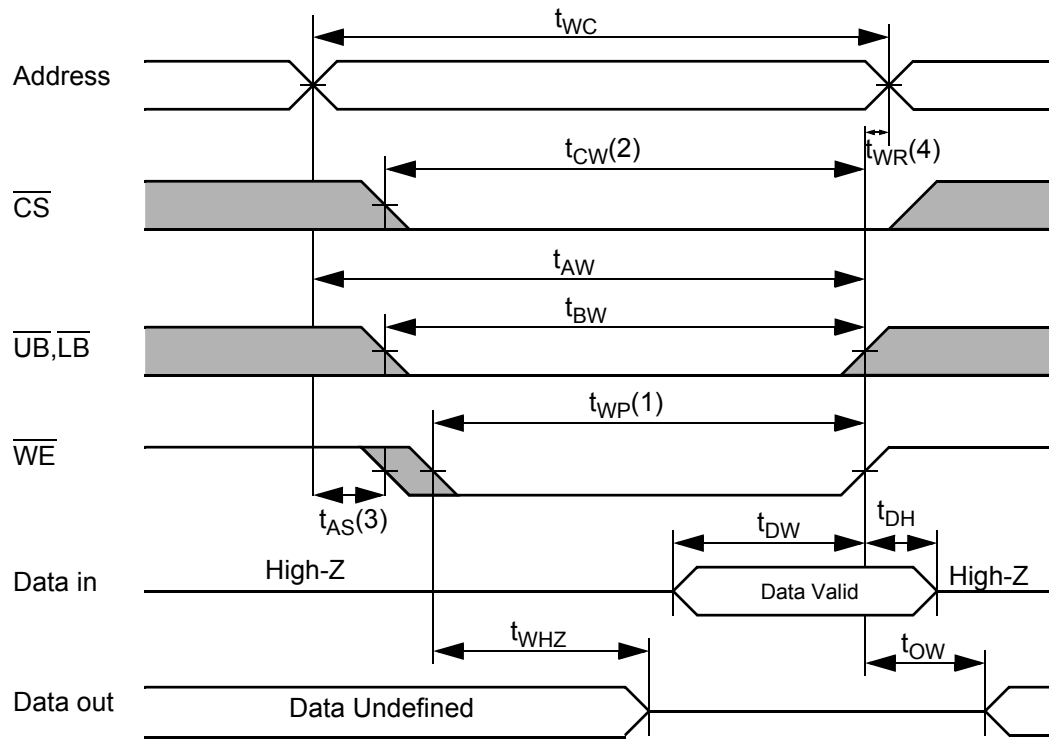
NOTES (READ CYCLE)

1. t_{HZ} and t_{OHZ} are defined as the outputs achieve the open circuit conditions and are not referenced to output voltage levels.
2. At any given temperature and voltage condition, $t_{HZ}(\text{Max.})$ is less than $t_{LZ}(\text{Min.})$ both for a given device and from device to device interconnection.

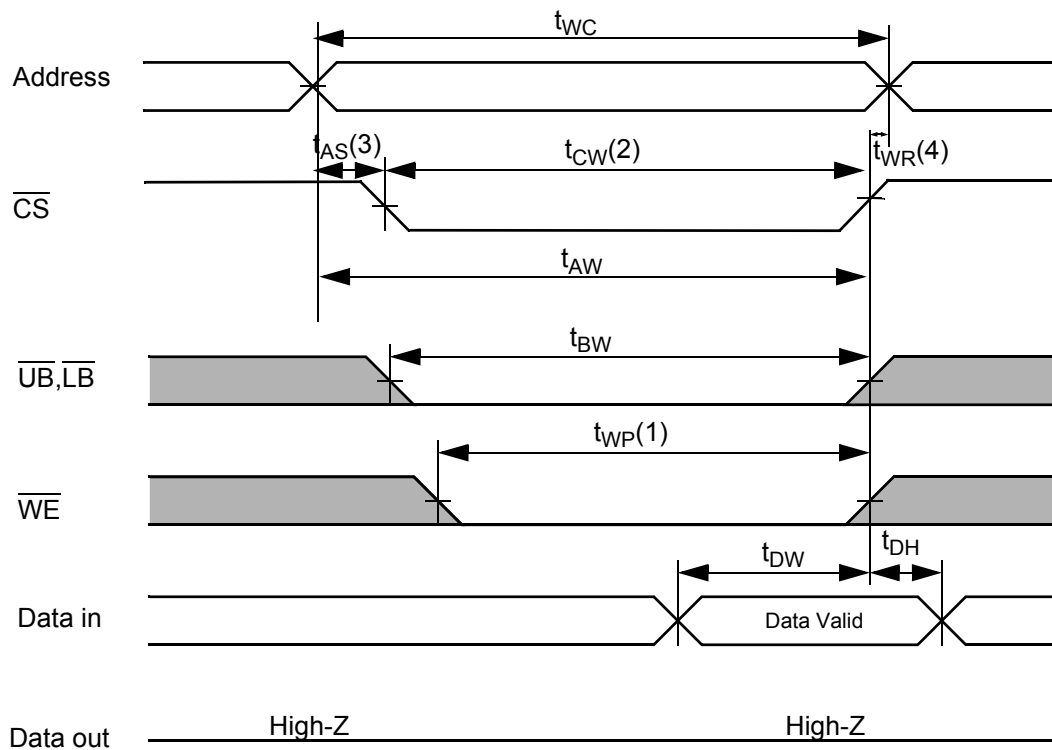


512K X 16 BIT LOW POWER CMOS SRAM

TIMING WAVEFORM OF WRITE CYCLE(1) (\overline{WE} Controlled)

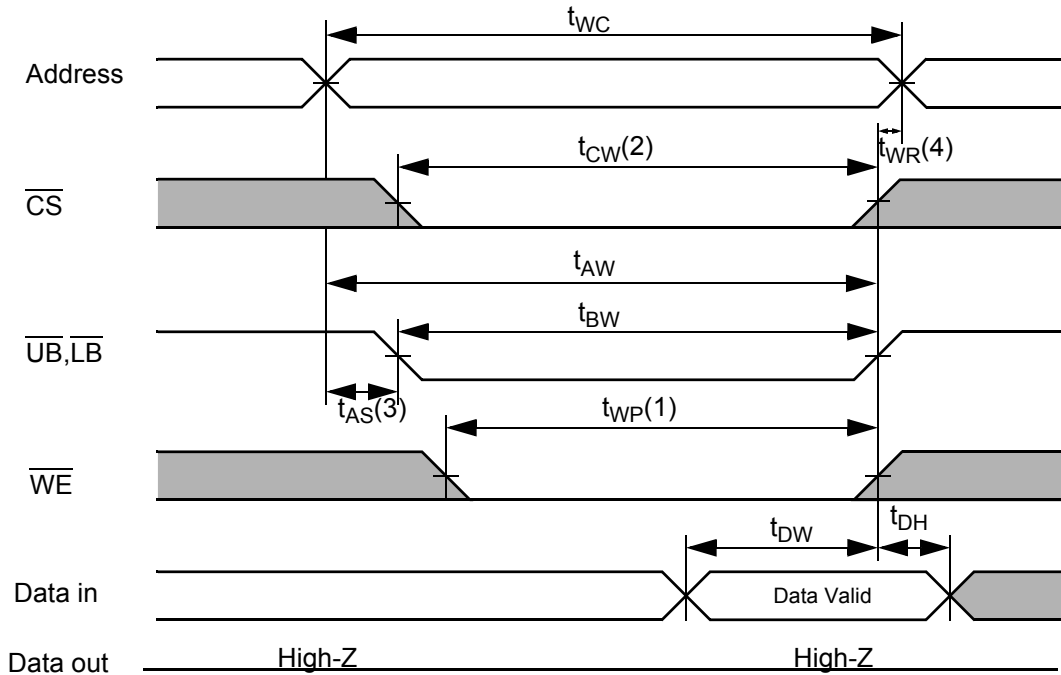


TIMING WAVEFORM OF WRITE CYCLE(2) (\overline{CS} Controlled)





512K X 16 BIT LOW POWER CMOS SRAM

TIMING WAVEFORM OF WRITE CYCLE(3) (\overline{UB} , \overline{LB} Controlled)**NOTES (WRITE CYCLE)**

1. A write occurs during the overlap (t_{WP}) of low \overline{CS} and low \overline{WE} . A write begins when \overline{CS} goes low and \overline{WE} goes low with asserting \overline{UB} or \overline{LB} for single byte operation or simultaneously asserting \overline{UB} and \overline{LB} for double byte operation. A write ends at the earliest transition when \overline{CS} goes high and \overline{WE} goes high. The t_{WP} is measured from the beginning of write to the end of write.
2. t_{CW} is measured from the \overline{CS} going low to end of write.
3. t_{AS} is measured from the address valid to the beginning of write.
4. t_{WR} is measured from the end of write to the address change. t_{WR} applied in case a write ends as \overline{CS} or \overline{WE} going high.



512K X 16 BIT LOW POWER CMOS SRAM

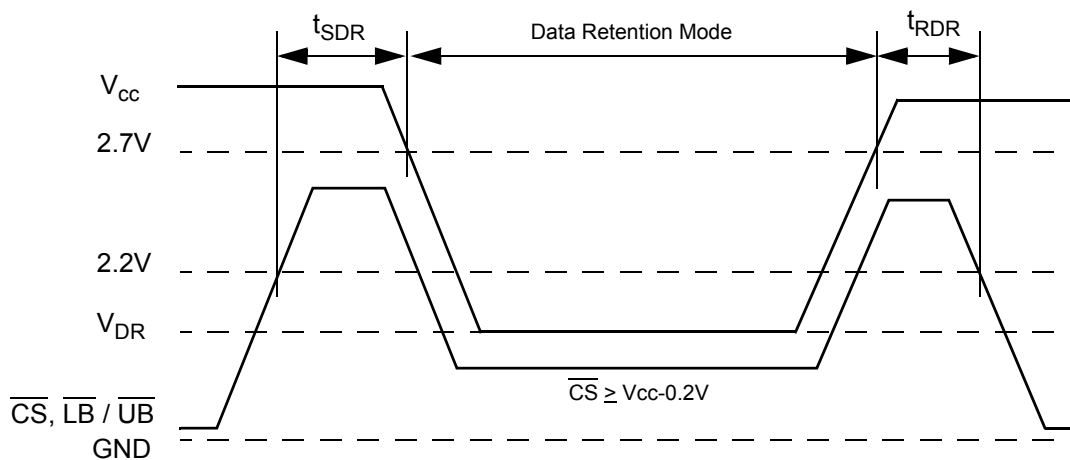
DATA RETENTION CHARACTERISTICS

| | Symbol | Test Condition | Min | Typ | Max | Unit |
|--------------------------------------|-----------|--|----------|-----|-----|---------|
| V_{CC} for Data Retention | V_{DR} | I_{SB1} Test Condition (Chip Disabled) ¹⁾ | 1.5 | - | 3.6 | V |
| Data Retention Current | I_{DR} | $V_{CC}=1.5V$, I_{SB1} Test Condition (Chip Disabled) ¹⁾ | - | - | 4 | μA |
| Chip Deselect to Data Retention Time | t_{SDR} | See data retention wave form | 0 | - | - | ns |
| Operation Recovery Time | t_{RDR} | | t_{RC} | - | - | |

NOTES

1. See the I_{SB1} measurement condition of datasheet page 4.

DATA RETENTION WAVE FORM





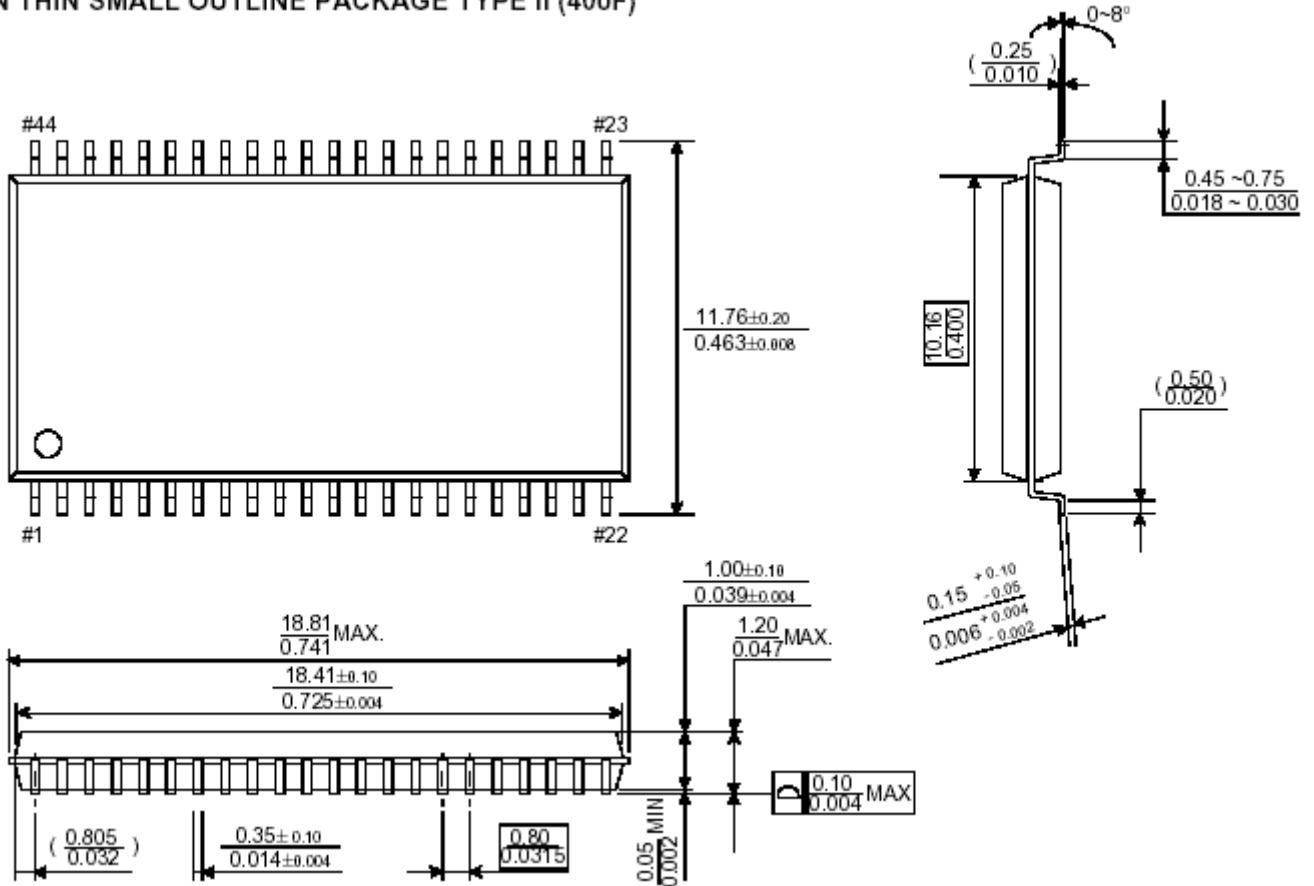
512K X 16 BIT LOW POWER CMOS SRAM

PACKAGE DIMENSION

44 - TSOP2 (0.8mm pin pitch)

Unit : millimeters / inches

44 PIN THIN SMALL OUTLINE PACKAGE TYPE II (400F)

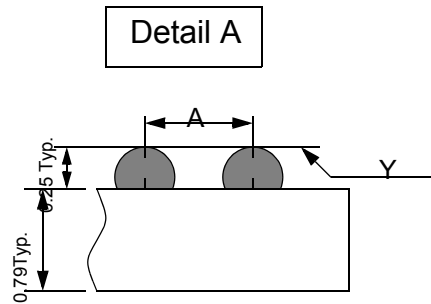
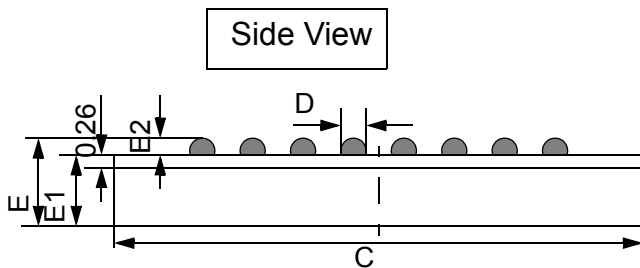
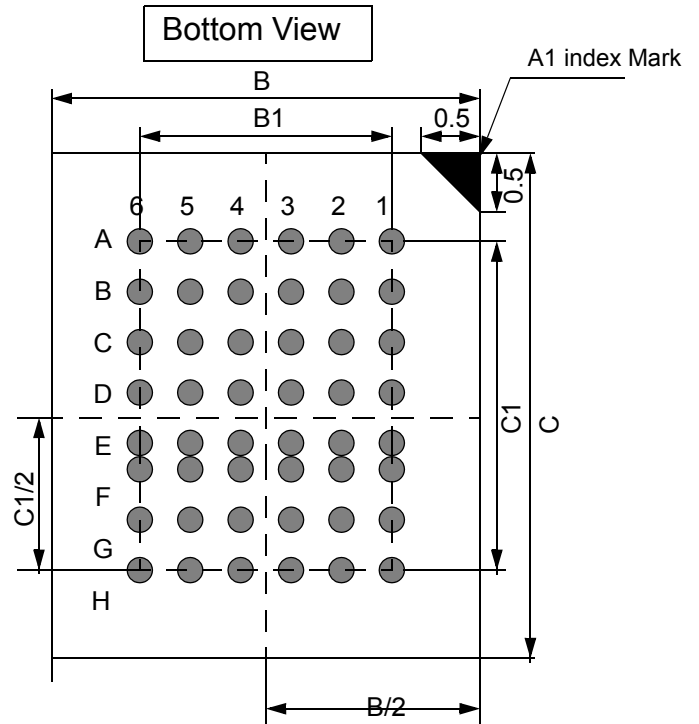
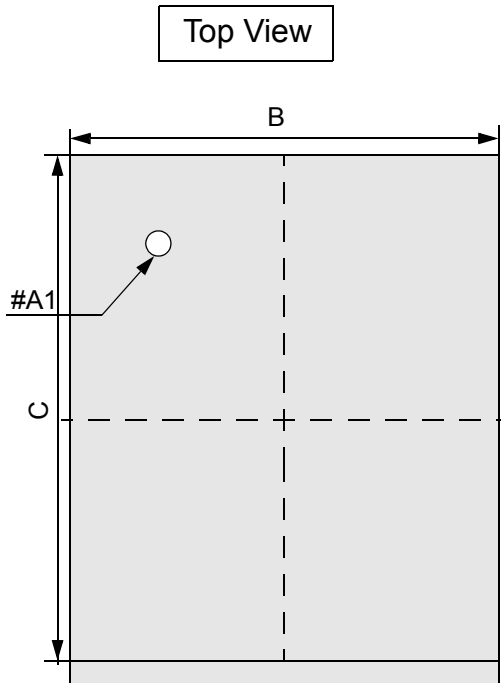




512K X 16 BIT LOW POWER CMOS SRAM

48 Ball Fine Pitch BGA (0.75mm ball pitch)

Unit: millimeters



| | Min | Typ | Max |
|----|------|-------|-------|
| A | - | 0.75 | - |
| B | 7.95 | 8.00 | 8.05 |
| B1 | - | 3.75 | - |
| C | 9.95 | 10.00 | 10.05 |
| C1 | - | 5.25 | - |
| D | 0.30 | 0.35 | 0.40 |
| E | - | - | 1.00 |
| E1 | - | - | 0.70 |
| E2 | 0.20 | 0.25 | 0.30 |
| Y | - | - | 0.08 |

NOTES.

1. Bump counts : 48(8row x 6column)
2. Bump pitch : (x,y)=(0.75x0.75) (typ.)
3. All tolerance are +/-0.050 unless otherwise specified.
4. Typ : Typical
5. Y is coplanarity : 0.08(Max)



512K X 16 BIT LOW POWER CMOS SRAM

ORDERING INFORMATION

| Alliance | Organization | VCC Range | Package | Operating Temp | Speed ns |
|------------------|--------------|------------|---------------|---------------------------|----------|
| AS6C8016A -55ZIN | 512K x 16 | 2.7 - 3.6V | 44pin TSOP II | Industrial ~ -40 C - 85 C | 55 |
| AS6C8016A -55BIN | 512K x 16 | 2.7 - 3.6V | 48ball FBGA | Industrial ~ -40 C - 85 C | 55 |

PART NUMBERING SYSTEM

| AS6C | 8016 | -55 | X | X | N |
|-----------------------|--------------------------------------|-------------|---|--|-----------------------------------|
| Low power SRAM prefix | Device Number 80 = 8M 16 = x16 | Access Time | Package Option Z - 44pin TSOP B = 48ball FBGA | Temperature Range I = Industrial (-40 to + 85 C) | N = Lead Free RoHS compliant part |



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